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Fault Tolerant Operation of CHB Multilevel Inverters Based on the SVM Technique Using an Auxiliary Unit

B. Hemanth Kumar[†], Makarand M. Lokhande[*], Raghavendra Reddy Karasani[**], and Vijay B. Borghate[*]

[†,*]Depatrment of Electrical Engineering, Visvesvaraya National Institute of Technology (VNIT), Nagpur, India
[**]Sagi RamaKrishnam Raju (SRKR) Engineering College, Bhimavaram, India

Abstract

In this paper, an improved Space Vector Modulation (SVM) based fault tolerant operation on a nine-level Cascaded H-Bridge (CHB) inverter with an additional backup circuit is proposed. Any type of fault in a power converter may result in a power interruption and productivity loss. Three different faults on H-bridge modules in all three phases based on the SVM approach are investigated with diagrams. Any fault in an inverter phase creates an unbalanced output voltage, which can lead to instability in the system. An additional auxiliary unit is connected in series to the three phase cascaded H-bridge circuit. With the help of this and the redundant switching states in SVM, the CHB inverter produces a balanced output with low harmonic distortion. This ensures high DC bus utilization under numerous fault conditions in three phases, which improves the system reliability. Simulation results are presented on three phase nine-level inverter with the automatic fault detection algorithm in the MATLAB/SIMULINK software tool, and experimental results are presented with DSP on five-level inverter to validate the practicality of the proposed SVM fault tolerance strategy on a CHB inverter with an auxiliary circuit.

Key words: Auxiliary circuit, Cascaded H-Bridge (CHB) inverter, Fault tolerance, Reliability, Space Vector Modulation (SVM)

I. INTRODUCTION

The utilization of Multilevel Inverters (MLIs) has been drastically increasing in medium voltage and high power industrial applications [1] in recent years. The basic role of multilevel converter is to obtain a high power by the series link of switching devices through lower DC voltage sources. The advantages of multilevel converters are their high DC bus utilization, superior efficiency, lower harmonic distortion and common mode voltage [2]. However, the number of semiconductor devices required is increased for higher voltage levels, which causes a reduction in system reliability and an increase in system cost. The reliability of the MLIs is very crucial in high power industrial applications. It necessitates continual operation even under faulty cases. For example, induction motor drives are mostly used for process control. If a fault occurs on the inverter side, a fuse or circuit breaker operates to isolate the power supply to protect the system. As a result, the induction motor stops working, which stops the production in industry. On the other hand, during a fault condition, an inverter may produce unbalanced output voltages, which may damage the motor if the motor runs continuously for a long time. Thus, fault tolerant techniques are very useful to improve the reliability of inverters under fault conditions.

The well known classical MLIs topologies are the flying capacitor [3], diode clamped [4] and cascaded H-bridge inverters [5], [6]. When compared to the other clamping structures, the cascaded H-bridge is suitable for industrial applications because the CHB has a modular structure and cell redundancy which improves the reliability of the inverter during fault conditions. In addition, the CHB inverter does not require any extra components like diodes or capacitors as in the other clamping structures. In addition, separate dc source inverter topologies are widely used for renewable energy applications [7], [8] like wind, fuel cell and photovoltaic systems. To control inverters, various modulation techniques have been reported. The Space Vector Pulse Width Modulation

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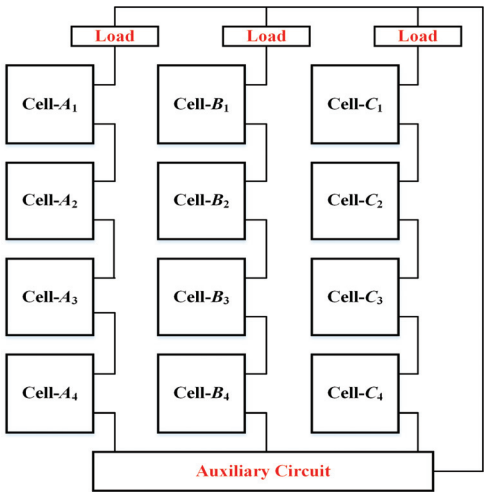
[†]Corresponding Author: hemub09@gmail.com
Tel: +91-9766031642, Visvesvaraya Nat'l Inst. of Tech. (VNIT)
[*]Dept. of Electrical Eng., Visvesvaraya Nat'l Inst. of Tech. (VNIT), India
[**]Sagi RamaKrishnam Raju (SRKR) Engineering College, India

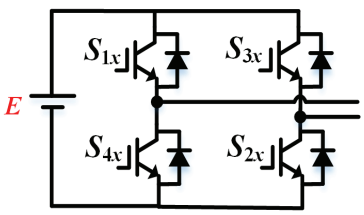
(SVPWM) technique [9] is a very promising method due to its good characteristics such as lower harmonic distortion, lower switching loss, and high DC bus utilization. SVPWM for MLIs has an increased number of redundant switching states. Suppose, a cascaded H-bridge inverter has damaged cells. Then, by using the redundancy switching states [10], the balance in the line to line voltages of the inverter can be restored.

Detection and identification of fault type is also important in MLIs, which need a separate fault detection unit. The functions that need to be accomplished for any fault tolerance control are fault detection, and determining the location and type of fault, followed by restoring suitable operation. For MLIs, several fault detection techniques have been presented in [11], [12]. For example, short circuit faults can be detected by di/dt feedback or desaturation with the help of logic gate circuits. Meanwhile, open circuit faults can be detected by waveform analysis. By using those methods, it is easy to find the location and type of fault in less time. The objective of a fault tolerant system is to maintain operation even under fault conditions. Many fault tolerant techniques are presented in [13], [14] for power electronic converters. These methods for CHB inverters can be achieved either by modifying the inverter control strategy or by connecting an additional circuit in series to an inverter. In all of these methods, faulty bridge is bypassed [15], [16] with the addition of contractors or SCRs at the load terminals of the inverter. Some methods make the use of the other leg of an H-bridge by giving suitable signals to the complementary switches [17], [18] so that the faulty leg is bypassed. If a switch fault is a short type, a control signal makes it so that the complementary switch should be OFF; and if switch fault is an open type, a control signal makes it so that the complementary switch should be ON.

In [19], by using carrier based PWM, balance in the line-to-line voltages is achieved by modifying the phase angle between the reference phase voltage under the fault condition in a CHB inverter. In [20], the SVM based fault tolerant control strategy is presented, where the faulty cell is bypassed and replaced with an additional SCR. In addition, by using the redundancy switching states, balanced voltage is produced. On the other hand, the maximum voltage obtained during the fault condition is reduced. In [21], the effect of different H-bridge faults in a space vector diagram and the maximum voltage achieved for different faults are presented for a seven level CHB inverter. Based on the injection of zero sequence voltage and DC voltage optimization, a fault tolerant control on a three phase seven level CHB inverter is presented in [22]. With some additional backup H-bridge cells, one cell in each phase is used to achieve the maximum voltage during fault conditions. This is achieved when a single cell fault occurs in different phases. In [23], an additional circuit compensates faults only one phase at a time. If two similar faults occur in two phases at the same



(a)



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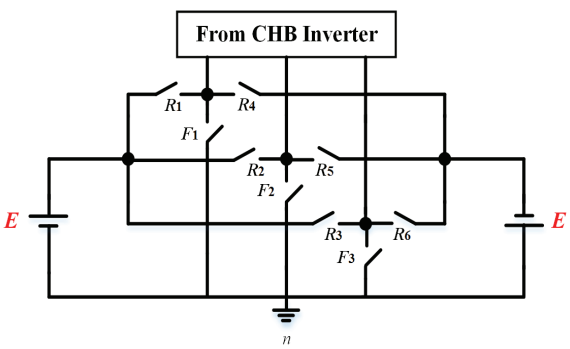
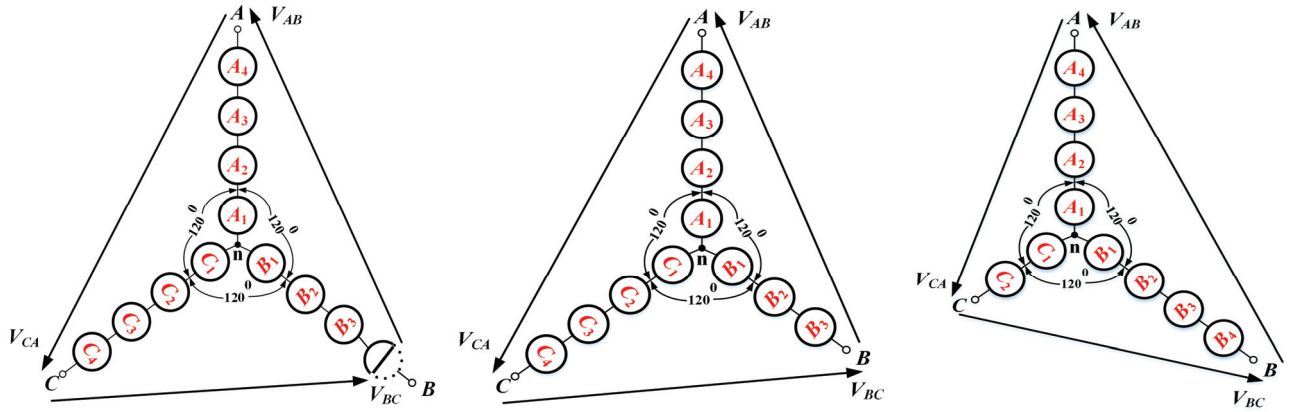


(c)

Fig. 1. Structure of: (a) a three phase nine-level CHB inverter; (b) an internal H-bridge cell; (c) the proposed auxiliary circuit.

time, it produces an unbalanced output voltage. In [24], an additional circuit is employed for a CHB inverter based SVM approach on a five level inverter. However, the additional circuit is unable to produce negative peak voltage during a cell fault in all three phases. Thus, the maximum output voltage achieved is lower under fault conditions..

The main goal of this paper is to acquire the necessary action subsequent to a fault. An improved SVPWM based fault tolerance is presented on a nine-level CHB inverter with a simple automatic fault detection algorithm. By taking the advantage of the modularity in CHB inverters and the redundancy of switching states in SVM, faulty operation on a MLI with the help of an auxiliary circuit is presented. Three



(a) (b) (c)

Fig. 2. Output voltage obtainable for 4 cells per phase with: (a) a Type-1 or Type-2 fault in one cell of phase-b; (b) a Type-3 fault in one cell of phase-b; (c) a Type-3 fault in two cells of phase-c.

different kinds of faults are considered for analysis in a single H-bridge cell and their effects on space vectors are presented. By this method, high DC bus utilization is achieved subsequent to the occurrence of a fault for different types of faults.

II. NINE-LEVEL CASCADED H-BRIDGE INVERTER

The structures of a three phase nine level CHB inverter made up of a series connection of 4-H-bridge cells per phase, an H-bridge cell and the proposed auxiliary circuit are shown in Fig. 1. In Fig. 1(c), F_1, F_2 and F_3 are the fuses in three different phases, E is the cell DC voltage source, and R_1, R_2, R_3, R_4, R_5 and R_6 are relays. Each cell produces three different voltage levels of $+E$, 0 and $-E$. To produce a $+E$ output level, S_{1x} and S_{2x} should be ON; to produce a $-E$ output level, S_{3x} and S_{4x} should be ON; and for 0 (zero) level, either S_{1x} and S_{3x} should be ON or S_{2x} and S_{4x} should be ON. In each H-bridge cell, two switches in the same leg are complimentary, which means that S_{1x} and S_{4x} are complementary switches in the first leg, and S_{2x} and S_{3x} are complementary switches in the second leg.

Open circuit and short circuit are the common faults in switches. In an H-bridge cell, if an open circuit switch failure occurs in any leg, the cell cannot produce all three output levels, which may lead to an unbalanced output voltage.

If a short circuit switch failure occurs in any leg, this may cause a short circuit across the DC source. When an open circuit (short circuit) failure occurs, its complementary switch in the leg must be ON (OFF). In this work three different kinds of faults are considered in each H-bridge cell for explaining fault tolerance operation.

1. Type 1 fault: when switch S_{1x} or S_{2x} is open circuited or S_{3x} or S_{4x} is short circuited, the highest positive level is missing.
2. Type 2 fault: when switch S_{3x} or S_{4x} is open circuited or S_{1x} or S_{2x} is short circuited, the highest negative level is missing.
3. Type 3 fault: when both of the switches S_{1x} and S_{3x} or S_{2x} and S_{4x} are open circuited or S_{2x} and S_{4x} or S_{1x} and S_{3x} are short circuited, both the highest positive and negative levels are missing.

The balanced output voltage for four cells in a phase, the unbalanced output voltage when a Type-3 faults occurs for one cell in phase-b and two cells in phase-c are shown in Fig. 2 (a), Fig. 2(b) and Fig. 2(c), respectively. The maximum possible peak value of the inverter output voltage obtained for single cell faults in different phases are given in Table I.

III. SPACE VECTOR MODULATION (SVM) CONTROL STRATEGY

When the inverter level increases, SVM has a large number of redundant switching states for each Space Vector (SV) to obtain a desired reference voltage (V_{ref}). Initially, a three phase balanced (a-b-c) system is converted in to a two phase (d-q) system by using Park's transformation. From (2) and (3), the desired reference voltage (V_{ref}) and phase angle with reference to the q-axis are obtained.

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} 2/3 & -1/3 & -1/3 \\ 0 & -1/\sqrt{3} & -1/\sqrt{3} \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (1)$$

Where V_a, V_b and V_c are phase variables.

$$\overline{V}_{ref} = \overline{V}_d + \mathrm{j}\overline{V}_q \quad (2)$$

$$\theta = \tan^{-1}(V_q / V_d) \quad (3)$$

Now, the components along the m-n axis are calculated by using the following expressions for a N-level inverter.

TABLE I
MAXIMUM POSSIBLE OUTPUT VOLTAGES FOR DIFFERENT FAULTS

Fault case	Phase-A	Phase-B	Phase-B	Maximum output Voltage
1	0	0	0	$4\sqrt{3}$
2	Type-1	0	0	$3.5\sqrt{3}$
3	0	Type-2	0	$3.5\sqrt{3}$
4	0	0	Type-3	$3.5\sqrt{3}$
5	Type-1	Type-1	0	$3.5\sqrt{3}$
6	0	Type-2	Type-2	$3.5\sqrt{3}$
7	Type-3	0	Type-3	$3\sqrt{3}$
8	Type-1	Type-2	0	$3.5\sqrt{3}$
9	0	Type-2	Type-3	$3\sqrt{3}$
10	Type-1	0	Type-3	$3\sqrt{3}$
11	Type-1	Type-1	Type-3	$3.5\sqrt{3}$
12	Type-1	Type-1	Type-2	$3\sqrt{3}$
13	Type-2	Type-2	Type-3	$3\sqrt{3}$
14	Type-2	Type-2	Type-1	$3.5\sqrt{3}$
15	Type-3	Type-3	Type-1	$3\sqrt{3}$
16	Type-3	Type-3	Type-2	$3\sqrt{3}$
17	Type-1	Type-1	Type-1	$3.5\sqrt{3}$
18	Type-2	Type-2	Type-2	$3.5\sqrt{3}$
19	Type-3	Type-3	Type-3	$3\sqrt{3}$
20	Type-1	Type-2	Type-3	$3\sqrt{3}$

$$V_m = \frac{2(N-1)V_{ref}}{\sqrt{3}E}\sin(60-\theta)$$
$$V_n = \frac{2(N-1)V_{ref}}{\sqrt{3}E}\sin(\theta) \quad (4)$$

The angle between the *m*-axis and the *n*-axis is 60°.

Consider the lowest bound integer values of V_m and V_n to be *m* and *n*, respectively.

$$m = floor\,(V_m) \quad (5)$$
$$n = floor\,(V_n) \quad (6)$$

Now, all of the space vectors are changed to numeral values. The Three Nearest Space Vectors (TNSV) can be found as follows:

$$\text{when}\,(V_m + V_n) \le (m+n+1)\,\text{then TNSVs are}$$
$$(m_1, n_1) = (m, n)$$
$$(m_2, n_2) = (m, n+1)$$
$$(m_3, n_3) = (m+1, n) \quad (7)$$

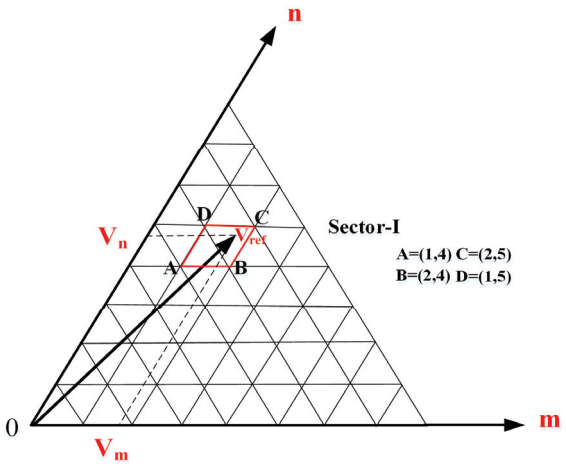


Fig. 3. Decomposing of V_{ref} in the *m*-*n* axis system.

$$\text{when}\,(V_m + V_n) > (m+n+1)\,\text{then TNSVs are}$$
$$(m_1, n_1) = (m, n+1)$$
$$(m_2, n_2) = (m+1, n)$$
$$(m_3, n_3) = (m+1, n+1) \quad (8)$$

Fig. 3 shows the decomposition of V_{ref} in the *m*-*n* system with the nearest Space Vectors (SVs), where A, B, C and D are space vectors. For the TNSVs, the dwell times are t_1, t_2 and t_3, respectively. The values of t_1, t_2 and t_3 are obtained by solving the following three sets of equations.

$$m_1 t_1 + m_2 t_2 + m_3 t_3 = V_m T_s$$
$$n_1 t_1 + n_2 t_2 + n_3 t_3 = V_n T_s \quad (9)$$
$$t_1 + t_2 + t_3 = T_s$$

where T_s is the sampling time:

For any SV (m, n), the number of possible switching instants are obtained as follows:

$$N_{sw} = N - (m+n) \quad (10)$$

For phase-a, all of the inverter switching instants are as follows:

$$S_a = \begin{cases} (m+n)-((N-1)/2) \\ (m+n)-((N-1)/2)+1 \\ (m+n)-((N-1)/2)+2 \\ \vdots \\ (N-1)/2 \end{cases} \quad (11)$$

Similarly, for phase-b and phase c, all of the inverter switching states are as follows:

$$S_b = S_a - m$$
$$S_c = S_b - n = S_a - (m+n) \quad (12)$$

The number of distinct switching inverter states increases with an increase in the inverter level. The selection of a particular switching state for the three phases depends on the values of *m* and *n*, which are shown in Table II.

TABLE II
SELECTION OF SWITCHING STATES BASED ON M AND N VALUES

(m+n) value	S_a	S_b	S_c
Even	(m+n)/2	(n-m)/2	-(m+n)/2
Odd & n is odd value	(m+n-1)/2	(n-m-1)/2	- (m+n-1)/2
Odd & m is odd value	(m+n+1)/2	(n-m+1)/2	-(m+n+1)/2

TABLE III
CORRELATION BETWEEN SWITCHING STATES IN DIFFERENT SECTORS

Sector no.	Phase A	Phase B	Phase C
I	S_a	S_b	S_c
II	- S_b	- S_c	- S_a
III	S_c	S_a	S_b
IV	- S_a	- S_b	- S_c
V	S_b	S_c	S_a
VI	- S_c	- S_a	- S_b

The seven segment switching sequences are applied with dwell times obtained from (9). They are the same as those in the conventional SVPWM method to synthesize V_{ref}. The switching sequence arrangement is determined based on the objective of the switching arrangement. The objective is to minimize both the switching losses and the harmonic distortion. Depending on the above criteria, one particular switching state is chosen from different switching instants based on m and n values. Based on the relationship between the switching instants in the six sectors shown in Table III, for different sectors, the switching states are chosen accordingly.

IV. PROPOSED SVPWM BASED FAULT TOLERANCE STRATEGY

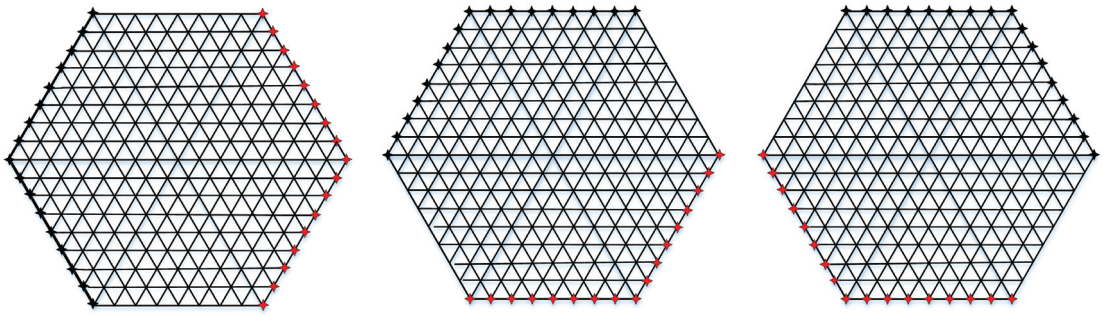
A. Effect of Space Vectors (SV) Under Faulty Conditions

The main goal of this paper is to acquire the necessary action subsequent to a fault. When a single fault occurs in one phase, that phase is unable to produce a nine level output voltage and the remaining healthy two phases produce a nine level output voltage. This causes uneven stress on the switches of the same leg due to the DC offset current in the inverter phases. It also degrades the inverter load performance. During faults, some of the SVs with their respective switching states are disabled. However, the reduced balanced line to line voltage can be produced based on the availability of SVs.

The peak value of the inverter output voltage depends on the radius of the circle placed within the largest healthy hexagon. Fig. 4(a) shows a Space Vector Diagram (SVD) when Type-1 (colored red), Type-2 (colored black) and Type-3 (both colors) faults occur in a single cell in Phase-a. Similarly, for Phase-b and Phase-c, SVDs for different faults are in a single cell are shown in Figs. 4b and 4c, respectively. Fig. 5 shows a SVD when a single cell has a common fault in all three phases. Fig. 6 (a) shows a SVD when a single cell has a Type-3 fault in Phase-a and Phase-b, and a Type-2 fault in Phase-c. Fig. 6(b) shows a SVD when a single cell has a Type-3 fault in Phase-a and a Type-2 fault in Phase-b and Phase-c. Fig. 6(c) shows a SVD when a single cell has a Type-3 fault in Phase-a, and a Type-1 fault in Phase-b and Phase-c. Fig. 7(a) shows a SVD when two cells have a Type-3 fault in Phase-a, a Type-1 fault in a single cell of Phase-b, and a Type-2 fault in a single cell of Phase-c. A SVD for two cells with a Type-3 fault in Phase-a, a Type-3 fault in a single cell of Phase-b, and a Type-3 fault in a single cell of Phase-c is shown in Fig. 7(b). Fig. 7(c) shows a SVD for three cells with a Type-3 fault in Phase-a, two cells with a Type-3 fault in Phase-a, and one cell with a Type-3 fault in Phase-c. In all of the figures from Fig. 4 to Fig. 7, a star mark indicates invalid space vectors.

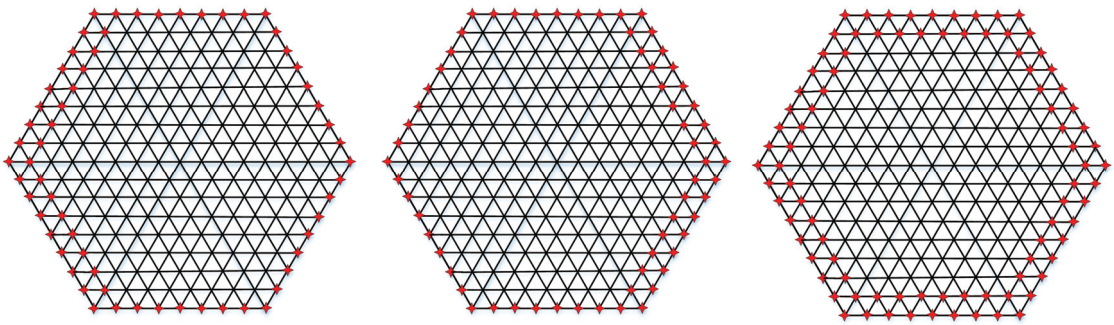
B. Rearrangement of the Modulation Technique and Hardware Topology

To undertake suitable action for an inverter during a faulty situation, appropriate switching instants have to be selected. Under fault conditions, the number of switching instants diminishes in an inverter SVD. The selection of appropriate switching instants is necessary because some of the space vectors are invalid during fault conditions. Therefore, a modulation strategy has to be modified to produce a balanced voltage. If a single cell Type-1 fault occurs in phase-a, the faulty phase can produce -9E to +8E output voltage levels and phase-b and phase-c can produce -9E to +9E output voltage levels, so that the number of healthy layers in the SVD is reduced. With the help of an auxiliary circuit, it is possible to produce -9E to +9E output voltage levels in a faulty phase. In this case, the relay R_1 in the auxiliary circuit has to be ON. Then the respective faulty phase fuse blows out and the required voltage is added to the faulty phase. In addition, if a single cell Type-2 fault occurs in phase-b, the faulty phase can produce -8E to +9E output voltage levels and phase-a and phase-c can produce -9E to +9E output voltage levels, so that the number of healthy layers in the SVD is reduced. With the help of an auxiliary circuit, it is possible to produce -9E to +9E output voltage levels in a faulty phase. In this case, the relay R_5 in the auxiliary circuit has to be ON. With the help of the proposed auxiliary circuit, it is possible to produce an inverter output



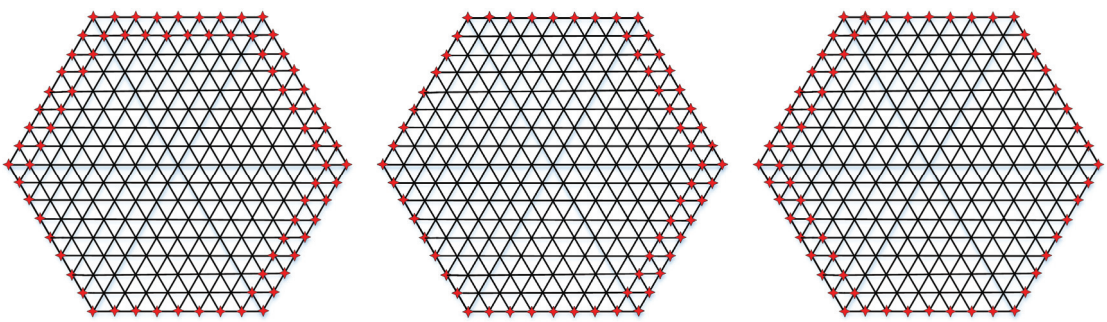
(a) (b) (c)

Fig. 4. Space Vector Diagrams with Type-1 (red), Type-2 (black) and Type-3 (red & black) faults in: (a) Phase-a; (b) Phase-b; (c)Phase-c.



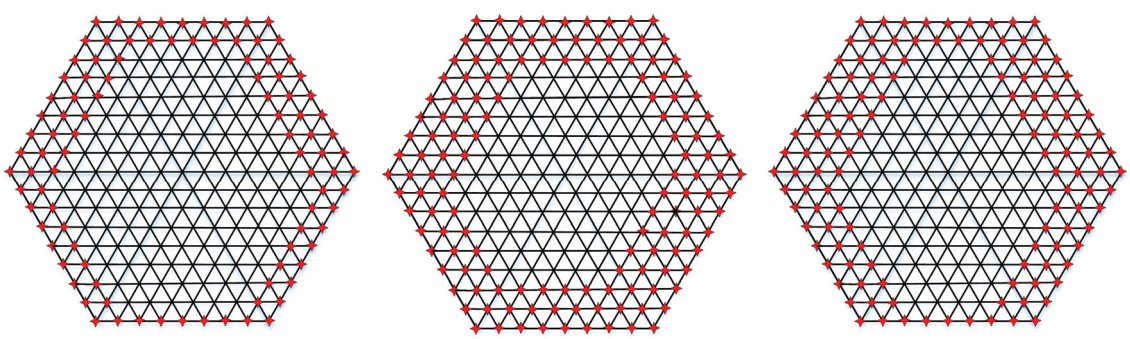
(a) (b) (c)

Fig. 5. Space Vector Diagrams with a single fault in three phases: (a) Type-1; (b) Type-2; (c) Type-3.



(a) (b) (c)

Fig. 6. Space Vector Diagrams with different faults in three phases: (a) Type-3 in Phase-a and Phase-b, Type-2 in Phase-c; (b) Type-3 in Phase-a, Type-2 fault in Phase-b and Phase-c; (c) Type-3 in Phase-a, Type-1 fault in Phase-b and Phase-c.



(a) (b) (c)

Fig. 7. Space Vector Diagrams with different faults in three phases: (a) Two cells have Type-3 in Phase-a, Type-1 in Phase-b and Type-2 in Phase-c; (b) Two cells have Type-3 in Phase-a, Type-3 in Phase-b and Type-3 in Phase-c; (c) Three cells have Type-3 in Phase-a, Type-1 in Phase-b and Type-2 in Phase-c.

voltage that is the same as that during healthy conditions for single cell faults in all three phases and for double cell faults in all three phases, while the maximum balanced output voltage is obtained.

Suppose a Type-3 fault occurs in phase-c, and its phase voltage is reduced by two voltage levels, i.e., -9E and +9E voltage levels. To produce -9E voltage level, the relay R_6 is ON and to produce a +9E voltage level, the relay R_3 is ON and its respective fuse F_3 is blown. By changing the SVM strategy, the proposed circuit is able to generate an output voltage during faulty conditions that is the same as that during healthy condition for single cell fault per phase.

V. Fault Detection Technique

The variables used for the fault detection techniques in an inverter are mainly: the input DC current, the output current and the output voltage [25]. Among these different variables, the output voltage is chosen as a fault discovery variable, because the output voltage is independent of the load, whereas the current varies with respect to the load variation, which may result in false detection of a fault as the load varies. Therefore, current sensing is not preferable over voltage sensing for fault detection. In this method, the MLI output voltage is sensed to detect faults. From the sensed output voltage, the RMS and mean voltages can be extracted for analysis. The occurrence of a fault in an inverter is reflected in the output voltage, such as a reduction in the RMS value, the addition of a DC offset value and an increased in the THD value of the output voltage.

In this technique, the inverter phase voltages and bridge voltages are required to detect the type of fault and its location. Initially, all of the bridge RMS voltages for different fault cases and three phase voltages under normal operation are calculated. The procedure used to detect the type of fault and its location is shown below.

1. Read all of the phase voltages RMS voltages.
2. Calculate error = $V_{reference}$ - $V_{measured}$.
3. If error > maximum allowable error, then there is a fault in the phase (the maximum allowable error is preferably 2V), else there is no fault in the phase.
4. Repeat steps 2 and 3 for the remaining phases to find whether the phase is faulty or not.
5. After finding the faulty phase, the faulty bridge has to be found. For that, read all of the H-bridge RMS and mean voltages in the faulty phase.
6. If obtained H-bridge RMS voltage $V_{obt} < V_{ref}$, then there is a fault in the bridge, else there is no fault in the bridge.
7. Repeat step 6, for the remaining H-bridges in the faulty phase.

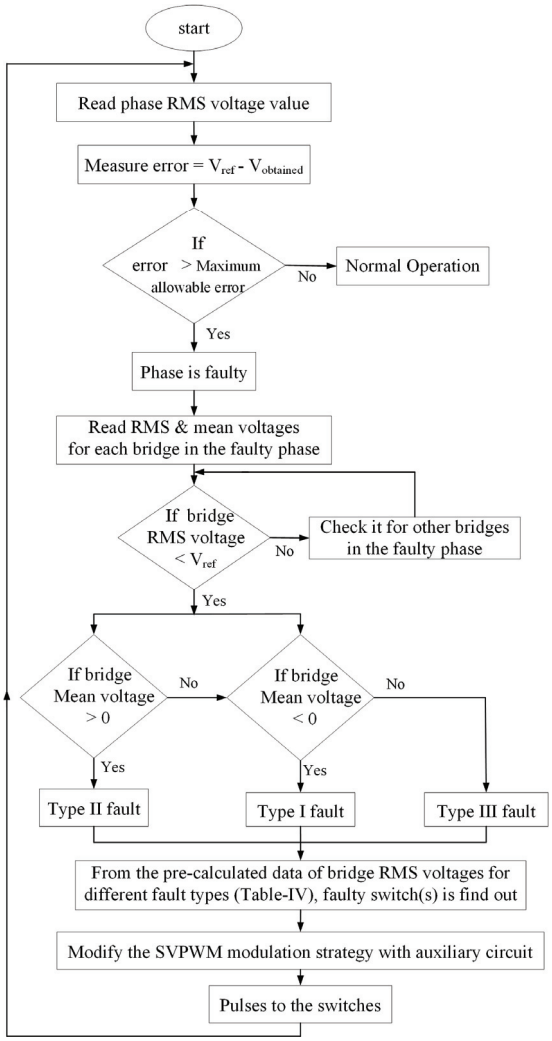


Fig. 8. Flow chart for the fault detection algorithm.

8. To determine the type of fault in the H-bridge in the faulty phase: Check
   a. If the obtained bridge mean voltage < 0 in the faulty phase (has negative DC offset), then a Type-1 fault occurred in the H-bridge.
   b. If the obtained bridge mean voltage > 0 in the faulty phase (has positive DC offset), then a Type-2 fault occurred in the H-bridge.
   c. If the obtained bridge mean voltage = 0 in a faulty phase, then a Type-3 fault occurs in the H-bridge.
9. To find the location of a fault i.e, faulty switch(s) in a faulty h-bridge: check, which faulty case bridge RMS voltage matches the measured bridge RMS voltage during the fault.
10. Then modify the SVPWM control strategy with the use of an auxiliary circuit.
11. Pulses to the switches.

A flow chart for the automatic fault detection technique per phase is shown in Fig. 8.

TABLE IV
BRIDGE (A1) RMS VOLTAGE UNDER DIFFERENT OPERATING CONDITIONS FOR A NINE LEVEL INVERTER

Operating condition		Bridge RMS voltage (V)
No fault		74.62
Type-1 fault	Switch S_1 is open	37.31
	Switch S_2 is open	29.21
Type-2 fault	Switch S_3 is open	28.69
	Switch S_4 is open	35.78
Type-3 fault	Switches S_1 & S_3 are open	7.15
	Switches S_2 & S_4 are open	11.35

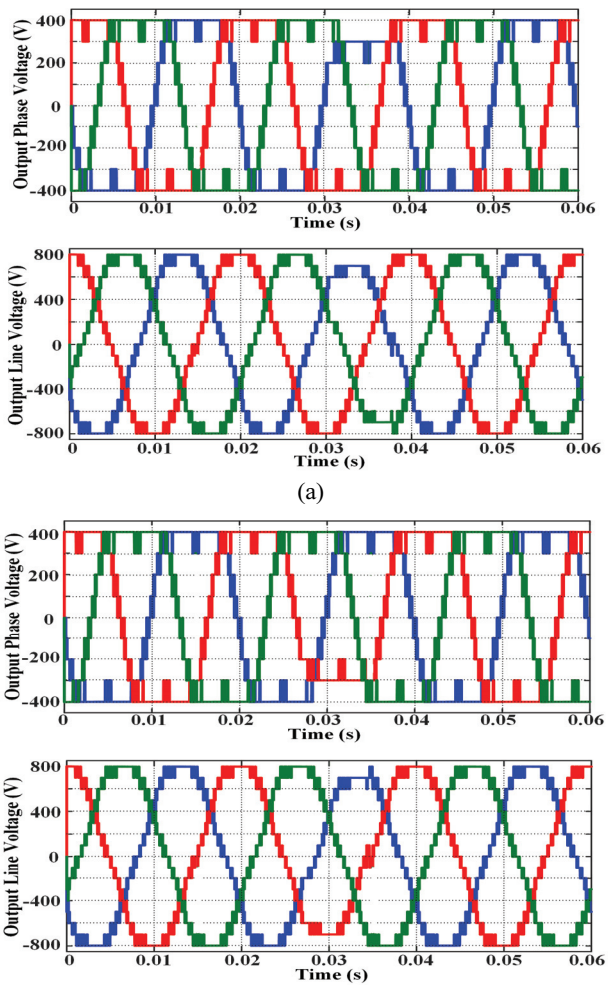


Fig. 9. Nine-level inverter output voltage waveforms. (a) Three phase and line voltages when one cell has a Type-1 fault in phase-b. (b) Three phase and line voltages when one cell has a Type-2 fault in phase-a.

In the above fault detection procedure, step 9 is explained clearly as follows:

After finding the faulty bridge and fault type, then it is necessary to find the faulty switch. Precalculated data of one bridge-A_1 RMS voltages for different fault conditions is shown in Table IV. Consider that a Type-1 fault is found out in a bridge based on the fault detection algorithm in step 8. Now it is necessary to find whether the switch S_1 is open or the switch S_2 is open. To find the particular switch, check which condition bridge RMS voltage from Table IV matches the measured bridge RMS voltage. Among the two conditions under a Type-I fault, one condition definitely matches. Then, depending on the faulty switch, step 10 in the procedure is executed. The same procedure is used for other types of faults in any bridges in the three phases. For a N-level CHB inverter, the number of sensors required for fault detection is $2(N\text{-}1)$ per phase. Meanwhile, the presented fault detection scheme requires $(N+1)/2$ sensors per phase.

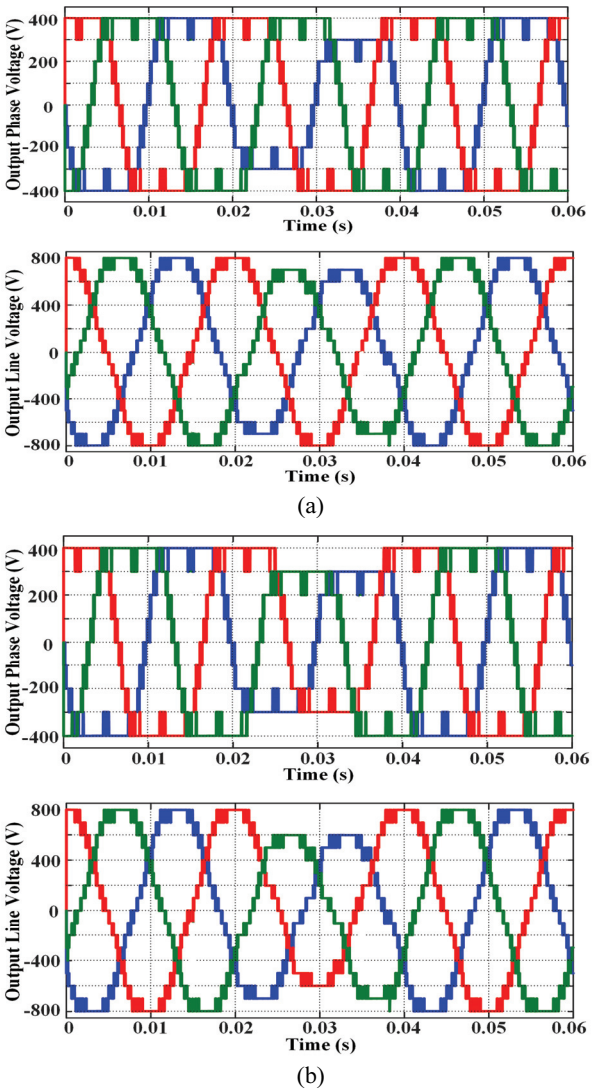


Fig. 10. Nine-level inverter output voltage waveforms. (a) Three phase and line voltages when one cell has a Type-3 fault in phase-b. (b) Three phase and line voltages when one cell has a Type-2 fault in phase-a, a Type-1 fault in phase-b and a Type-3 fault in phase-c.

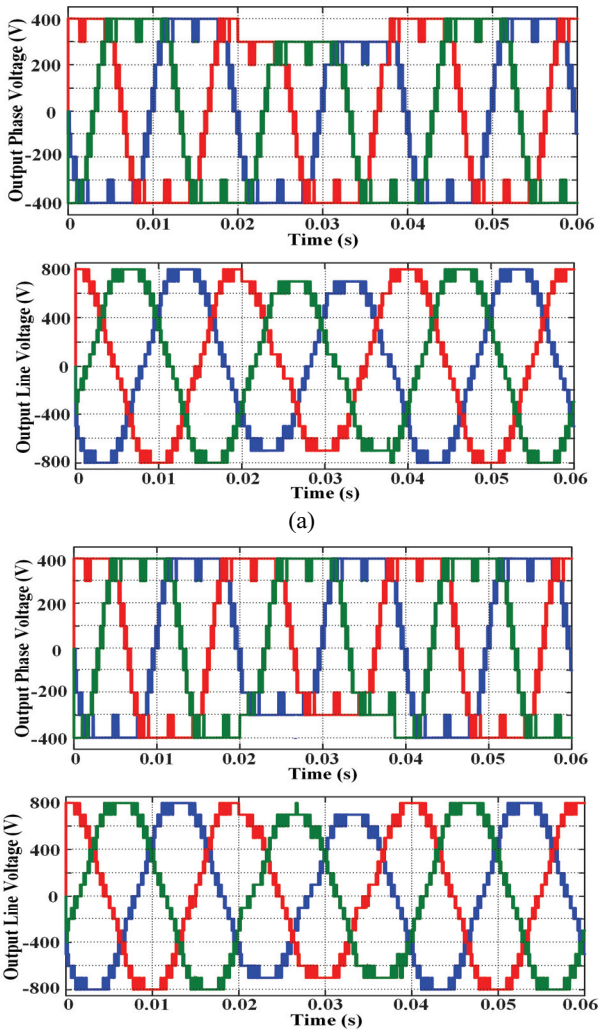


Fig. 11. Nine-level inverter output voltage waveforms. (a) phase and line voltages when one cell has a Type-1 fault in all three phases. (b) Three phase and line voltages when one cell has a Type-2 fault in all three phases.

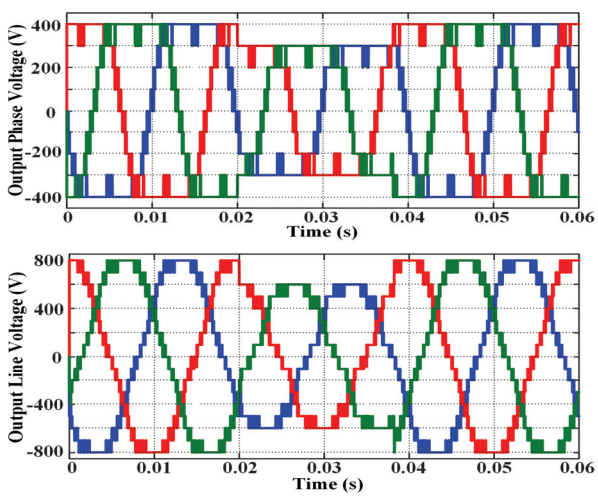


Fig. 12. Nine-level inverter output voltage waveforms: Three phase and line voltages when one cell has a Type-3 fault in all three phases.

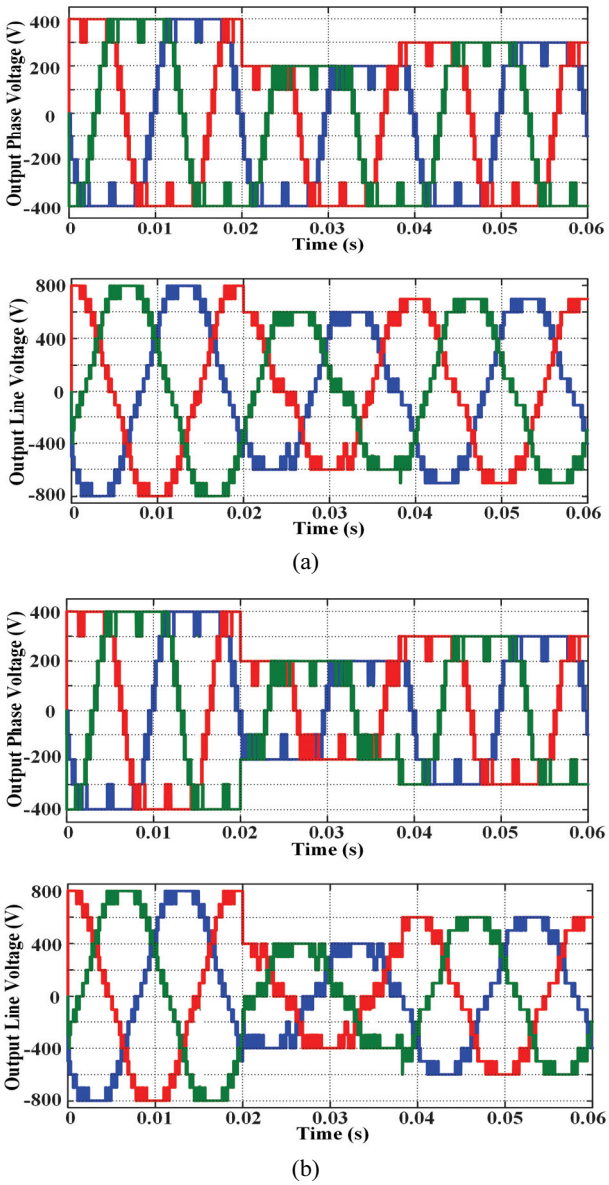


Fig. 13. Nine-level inverter output voltage waveforms. (a) Three phase and line voltages when two cells have a Type-1 fault in all three phases. (b) Three phase and line voltages when two cells have a Type-3 fault in all three phases.

VI. Investigation of the Fault Tolerant Technique

A. Simulation Results

Simulations have been carried out in the three phase cascaded H-bridge nine-level inverter by MATLAB/ SIMULINK tool to verify the presented fault tolerance strategy. Three different faults in different phases in one cell and two cells per phase have been carried out in a nine-level CHB inverter with a simple automatic fault detection algorithm by taking the output voltage as a fault detection parameter. In the simulation, a Type-1 fault is introduced in the bridge circuit

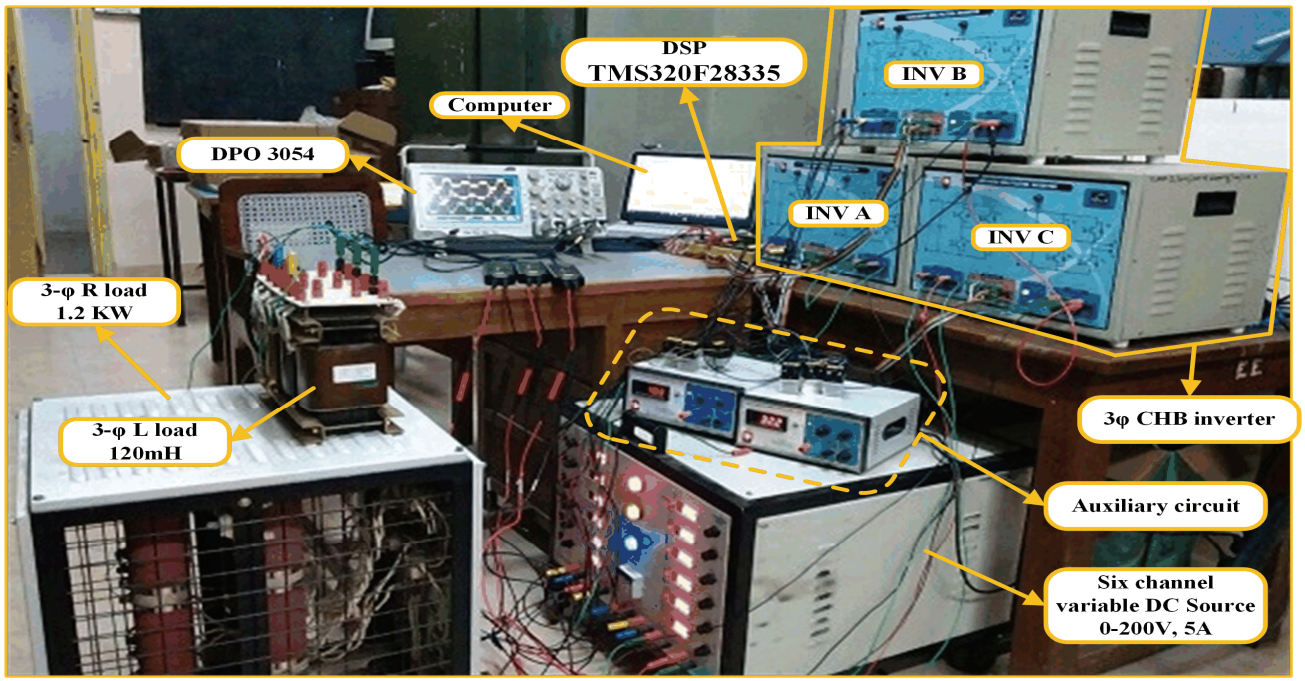


Fig. 14. Experimental set up for a three phase five-level CHB inverter with an auxiliary circuit.

by removing the firing pulse to the switch S_{1X}, a Type-2 fault is introduced in the bridge circuit by removing the firing pulse to the switch S_{3X} and a Type-3 fault is introduced in the bridge circuit by removing the firing pulse to the switches S_{1X} and S_{3X} at t=0.02sec. All of the faults are detected in less than one cycle using the fault detection algorithm, as shown in Fig. 8. For each cell, the DC supply voltage (E) is 100V and the sampling frequency for the SVPWM modulation technique is 2.1 KHz. Fig. 9(a) shows the three phase and line voltages, when a single cell has a Type-1 fault in phase-b. Here, the positive peak level is missing in phase-b, which is compensated by using the relay R_2 with the help of an auxiliary circuit. Fig. 9(b) shows the three phase and line voltages, when a single cell has a Type-2 fault in phase-a. Here, the negative peak level in phase-a is compensated by using the relay R_4 in an auxiliary circuit.

The three phase and line voltages when a single cell Type-3 fault occurs in phase-b, are shown in Fig. 10(a). In this case, both the positive and negative peak levels are compensated by using relays R_2 and R_5 in an auxiliary circuit.

The three phase and line voltages when a single cell Type-2 fault in phase-a, a single cell Type-1 fault in phase-b and a single cell Type-3 fault in phase-c are shown in Fig. 10(b). Here, the balanced output voltage is obtained by modifying the control strategy with the help of an auxiliary circuit. The three phase and line voltages when a single cell Type-1 fault occurs in all three phases are shown in Fig. 11 (a). Here, the positive peak voltage level is missing in all the three phases, which can be compensated by using relays R_1, R_2 and R_3 in phase-a, phase-b and phase-c, respectively.

The three phase and line voltages when a single cell Type-2 fault occurs in all three phases are shown in Fig. 11(b). Here, the positive peak voltage level is missing in all three phases, which can be compensated by using auxiliary circuit, with relays R_4, R_5 and R_3 in phase-a, phase-b and phase-c, respectively. The three phase and line voltages when a single cell Type-3 fault occurs in all three phases are shown in Fig. 12. Here, the balanced output voltage is obtained by modifying the control strategy with the help of an auxiliary circuit. The three phase and line voltages when two cells have a Type-1 fault in all three phases are shown in Fig. 13(a). The three phase and line voltages when two cells have a Type-3 fault in all the three phases are shown in Fig. 13(b). In all of the above cases, the fault is introduced at t=0.02sec and it is detected within one power cycle i.e., t=0.038sec. Hence, for single cell faults in all three phases, the proposed fault tolerant method produces output voltage during fault condition that is same as that in the normal condition.

B. Hardware Results

To validate the practicality of the proposed fault tolerant method, a hardware prototype of a five-level CHB inverter is presented, which is shown in Fig. 14. Each H-bridge cell has a DC source (E) of 110V. A three phase R-L load is connected to the CHB inverter, whose values are 110Ω and 120mH per phase. The SVPWM algorithm is implemented with a TMS-28335 digital signal processor. The presumed fault duration is considered for two cycles in the hardware results.

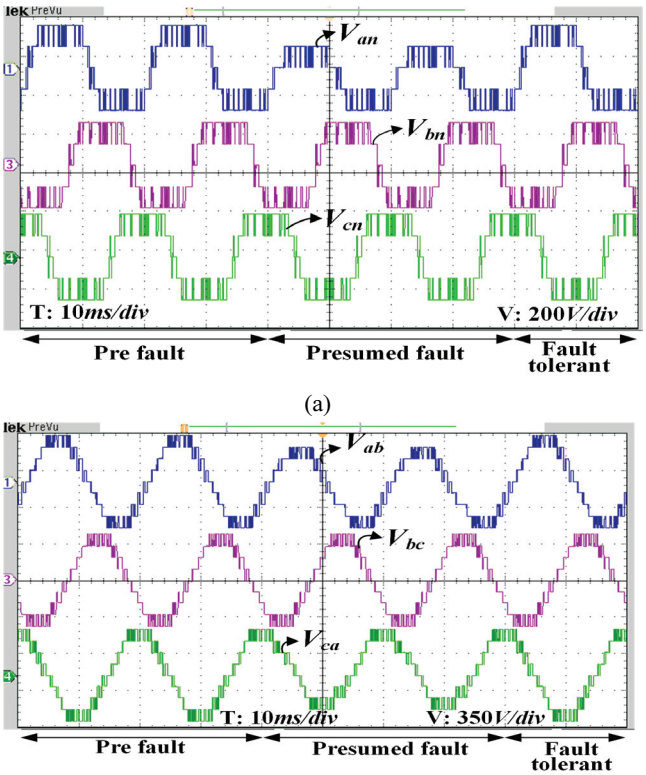


Fig. 15. Five-level inverter output voltage waveforms: Three phase and line voltages when a single cell has a Type-1 fault in phases-a.

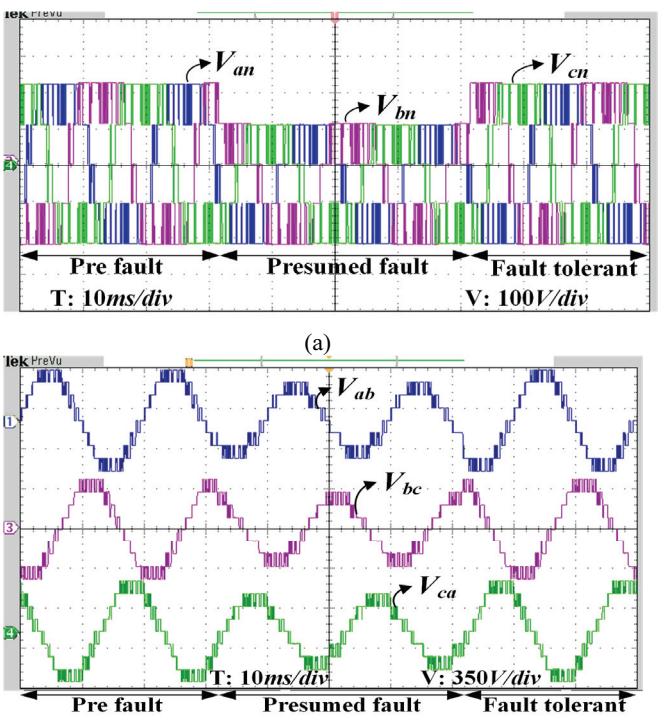


Fig. 16. Five-level inverter output voltage waveforms: Three phase and line voltages when a single cell has a Type-1 fault in all three phases.

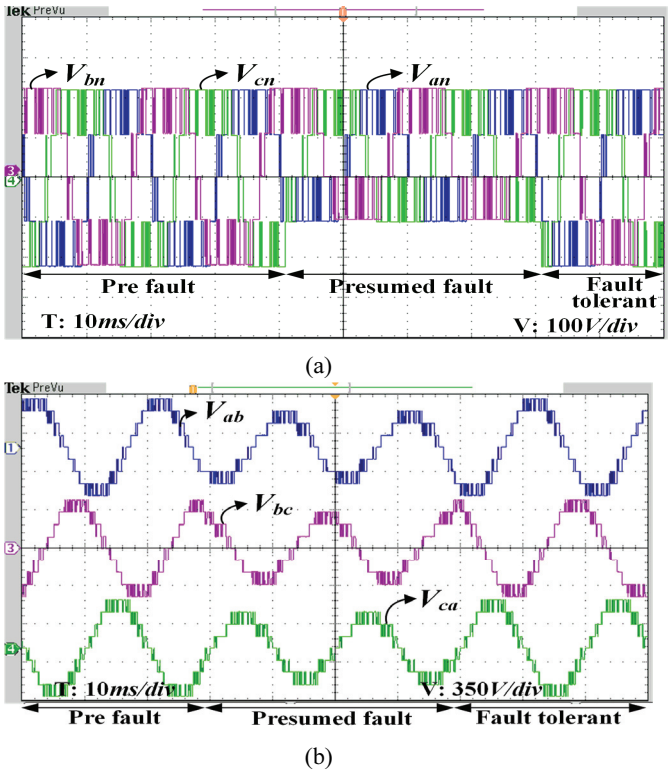


Fig. 17. Five-level inverter output voltage waveforms: Three phase and line voltages when a single cell has a Type-2 fault occurs in all three phases.

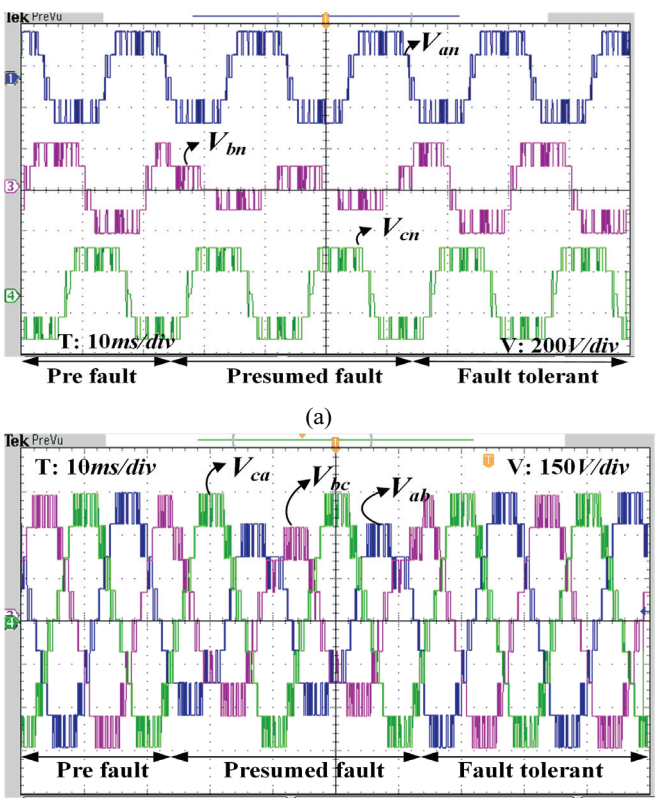
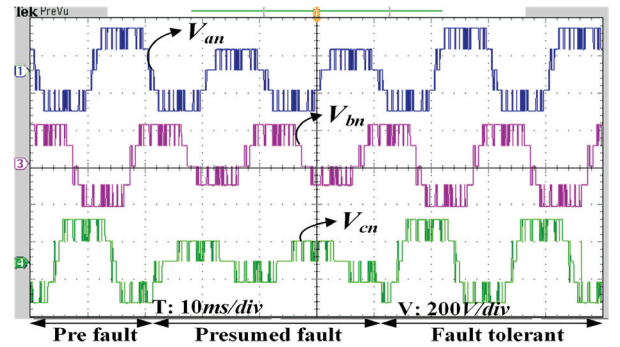
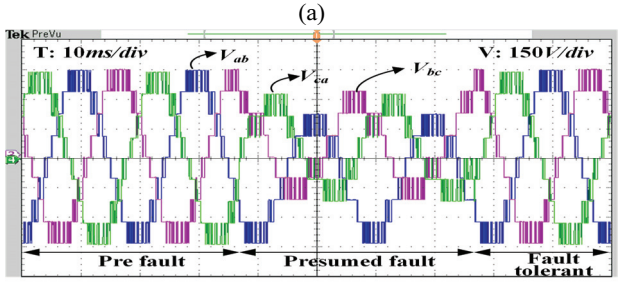


Fig. 18. Five-level inverter output voltage waveforms: Three phase voltage when a single cell has a Type-3 fault in phase-b.

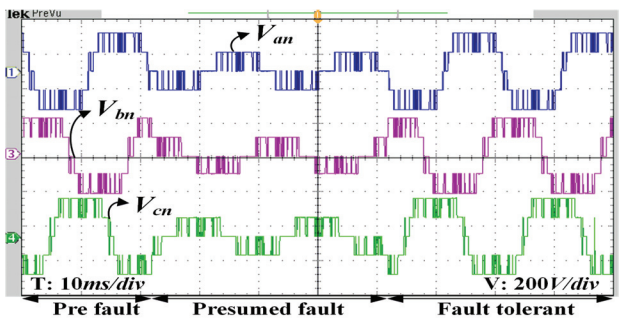


(a)

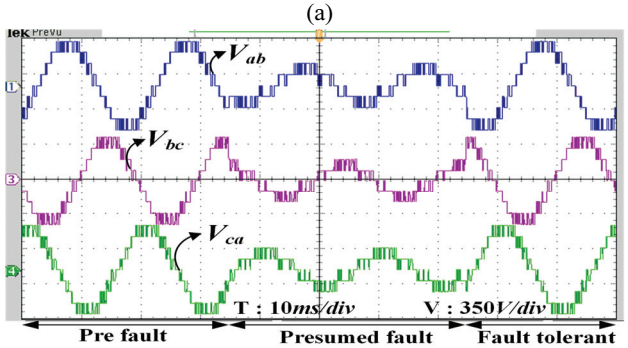


(b)

Fig. 19. Five-level inverter output voltage waveforms: Three phase and line voltages when one cell has a Type-1 fault in phase-a, a Type-2 fault in phase-b and a Type-3 fault in phase-c.



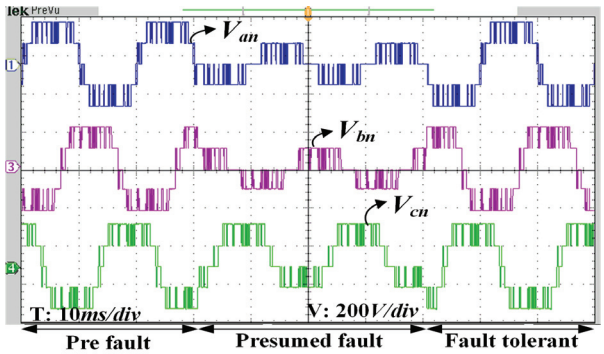
(a)



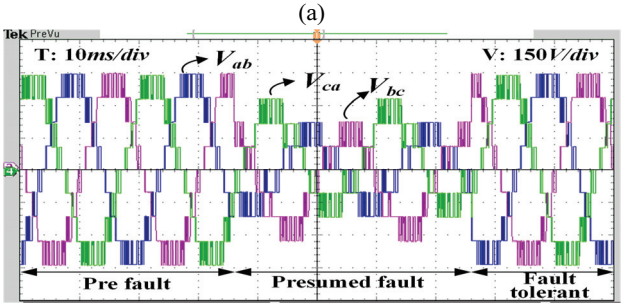
(b)

Fig. 20. Five-level inverter output voltage waveforms: Phase and line voltages when a single cell has a Type-3 fault in all three phases.

Figs. 15 (a) and (b) show the five level three phase and line voltages when a single cell has a Type-1 fault in phase-a. Figs. 16 (a) and (b) show the three phase and line voltages when a single cell has a Type-1 fault in all three phases. In this faulty

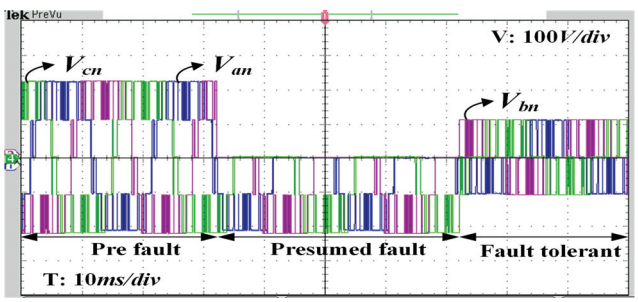


(a)

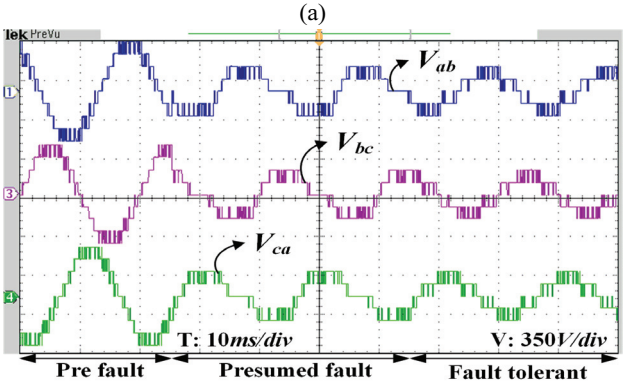


(b)

Fig. 21. Five-level inverter output voltage waveforms: Three phase and line voltages when a single cell has a Type-3 fault in phase-a and phase-b and a Type-2 fault in phase-c.



(a)



(b)

Fig. 22. Five-level inverter output voltage waveforms: Three phase and line voltages when two cells have a Type-1 fault in all three phases.

case, the positive peak voltage level is missing in all three phases. This can be achieved by modifying the control strategy with the use of an auxiliary circuit.

The five-level three phase and line voltages when single cell has a Type-2 fault in all three phases are shown in Figs. 17 (a) and (b). Figs. 18 (a) and (b) show the five-level three phase and line voltages when a single cell has a Type-3 fault in phase-b. The five-level three phase and line voltages when a single cell has a Type-1 fault in phase-a, a Type-2 fault in phase-b and a Type-3 fault in phase-c are shown in Figs. 19 (a) and (b). Figs. 20 (a) and (b) show the five-level three phase and line voltages when a single cell has a Type-3 fault in all three phases.

Figs. 21(a) and (b) show the five-level three phase and line voltages when a single cell has a Type-3 fault in phase-a and phase-b and a Type-2 fault in phase-c. Figs. 22 (a) and (b) show the three phase and line voltages when two cells have a Type-1 fault in all three phases. In this faulty case, two positive voltage levels are missing in all three phases, which is achieved by modifying the control strategy with the use of an auxiliary circuit. In all of the hardware results, the presumed fault duration is shown for two cycles.

VII. CONCLUSION

In this paper, an improved SVM based fault tolerant operation on a nine-level CHB inverter with an auxiliary circuit is investigated. The main goal of this work is to take the necessary action subsequent to fault analysis. A simple automatic fault detection algorithm is presented by taking the output voltage as a fault detection parameter. Three different faults are considered in a single cell for analysis. By using the proposed fault tolerant scheme, an inverter is able to produce an output voltage that is the same as that produced in normal condition for single cell faults in all three phases. If any fault occurs in more than one cell per phase, balanced three phase line to line voltage can be produced by modifying the SVM control strategy with the use of an auxiliary circuit. Furthermore, the maximum achievable line voltage is obtained in fault tolerant operation, independent of any fault type and location. Thus, CHB inverter reliability is enhanced. The proposed fault tolerant strategy was implemented on a nine-level CHB inverter in MATLAB/SIMULINK with an automatic fault detection algorithm. It has also been verified on a five-level CHB inverter with the presumed fault in a hardware prototype. The proposed strategy is general and can be applied to any higher inverter voltage levels.

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B. Hemanth Kumar received his B.Tech degree in Electrical and Electronics Engineering from Narayana Engineering College (NRNG), Gudur, India, in 2012; and his M.Tech degree in Instrumentation and Control Systems from Sri Venkateswara University University (SVU), Tirupathi, India, in 2015. He is presently working towards his Ph.D. degree at the Visvesvaraya National Institute of Technology (VNIT), Nagpur, India. His current research interests include pulse width modulation techniques, space vector modulation, power electronic converters, and electrical drives and control.

Makarand M. Lokhande received his B.E. degree in Electrical Engineering from Nagpur University, Nagpur, India, in 2001; his M.E. degree in Power Systems from the University of Pune, Pune, India, in 2003; and his Ph.D. degree from the Indian Institute of Technology Bombay (IITB), Powai, India, in 2010. He worked as an Assistant Professor in the Department of Electrical Engineering of the Pandit Deendayal Petroleum University (PDPU), Gandhinagar, India, from 2009 to 2013; and at the Sardar Vallabhbhai National Institute of Technology (SVNIT), Surat, India, from 2013 to 2015. He has been working as an Assistant Professor in the Department of Electrical Engineering at the Visvesvaraya National Institute of Technology (VNIT), Nagpur, India, since 2015. His current research interests include photovoltaic systems, electric vehicles and pulse width modulation techniques.

Raghavendra Reddy Karasani received his B.Tech degree in Electrical and Electronics Engineering from the Sri Chundi Ranganayakulu Engineering College (SCREC), Guntur, India, in 2003; his M.Tech in Power Control and Drives from the National Institute of Technology (NIT), Rourkela, India, in 2008; and his Ph.D. degree from the Visvesvaraya National Institute of Technology (VNIT), Nagpur, India, in 2017. He worked as an Assistant Professor in the Department of Electrical and Electronics Engineering, EVM College of Engineering and Technology, Narasaraopet, India, from 2008 to 2012; and at the Sir C R Reddy College of Engineering, Eluru, India, from 2012 to 2014. He is presently working as a faculty member in the Department of Electrical Engineering at Sagi Ramakrishnam Raju (SRKR) Engineering College, Bhimavaram, India. His current research interests include power electronic converters, electrical drives, FACTS and renewable energy systems.

Vijay B. Borghate was born in 1960. He received his B.E. degree in Electrical Engineering, his M.Tech. degree in Integrated Power Systems, and his Ph.D. degree from the Visvesvaraya National Institute of Technology (VNIT), Nagpur, India, in 1982, 1984 and 2007, respectively. He worked as an Engineer for the Maharashtra State Electricity Board, Mumbai, India, from 1985 to 1985. He became a Lecturer at VNIT (then VRCE) in 1985, where he is presently working as Professor in the Department of Electrical Engineering. His current research interests includes resonant converters and multilevel converters.