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New Strategy for Eliminating Zero-sequence Circulating Current between Parallel Operating Three-level NPC Voltage Source Inverters

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Abstract

A novel strategy based on a zero common mode voltage pulse-width modulation (ZCMV-PWM) technique and zero-sequence circulating current (ZSCC) feedback control is proposed in this study to eliminate ZSCCs between three-level neutral point clamped (NPC) voltage source inverters, with common AC and DC buses, that are operating in parallel. First, an equivalent model of ZSCC in a three-phase three-level NPC inverter paralleled system is developed. Second, on the basis of the analysis of the excitation source of ZSCCs, i.e., the difference in common mode voltages (CMVs) between paralleled inverters, the ZCMV-PWM method is presented to reduce CMVs, and a simple electric circuit is adopted to control ZSCCs and neutral point potential. Finally, simulation and experiment are conducted to illustrate effectiveness of the proposed strategy. Results show that ZSCCs between paralleled inverters can be eliminated effectively under steady and dynamic states. Moreover, the proposed strategy exhibits the advantage of not requiring carrier synchronization. It can be utilized in inverters with different types of filter.

Key words: Common mode voltage, Neutral point clamped, Neural point potential, Voltage source inverter, Zero sequence circulating current

I. INTRODUCTION

Modular design for power electronics is highly attractive in many applications, particularly in microgrids. If modular designed inverters can be optionally combined by users, then the integration of additional energy sources, the extension of system power capacity, and the improvement of system redundancy will become easy [1], [2].

To achieve this objective, modularized inverters must exhibit an autonomous characteristic [3]. As shown in Fig. 1, a fundamental requirement is that inverters can be operated under different modes (rectify or inverter modes) and can be paralleled with one another with different types of filters. Furthermore, paralleled inverters should be operated independently without any data exchange and interconnection.

When inverters are connected to common AC and DC buses, zero-sequence circulating currents (ZSCCs) are generated due to mismatches of control parameters, circuit parameters and the small total zero-sequence impedance within paralleled inverters. ZSCCs cause many problems, such as unbalanced output currents, output current distortion, system loss increase, and system protection shutdown [4]. Thus, one of the challenges in the application of modularized inverters is attributed to ZSCCs.

To eliminate ZSCCs, many studies on different methods have been conducted in the past few years. The high impedance method [5] and the synchronized control method [6] were adopted to eliminate ZSCCs between paralleled inverters with common AC and DC buses. For the high impedance approach, however, the reactor provides high impedance only at medium and high frequencies. It cannot prevent the low-frequency component in ZSCCs. The synchronized control approach is

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unsuitable for the modularized inverter design. When an increasing number of inverters are operating in parallel, the system becomes highly complicated to design and control. The ZSCC feedback control method was first investigated in 2002 [7]. A small signal model of ZSCC between paralleled operating inverters and the excitation source of ZSCCs, i.e., the difference in common mode voltages (CMVs), were analyzed. Then, various hybrid methods have been developed as follows. Advance control methods [8]-[10], such as deadbeat control, proportional resonant, and other bandwidth expansion methods, are used to achieve high performance in ZSCC elimination, increasing impedance reducing CMV [11]-[13]. In [11], the common mode choking coil was used to increase the loop impedance of ZSCCs. The discontinuous pulse-width modulation (DPWM) method was utilized to reduce CMV. Interleaving inductance and DPWM methods were used in [12], [13]. However, choking coil and interleaving inductance cannot prevent the DC component and low-frequency ZSCCs. Moreover, these methods are open-loop, which may lead to poor dynamic performance. Reduced CMV and ZSCC feedback control [14]-[17], such as active zero-state PWM (AZPWM), remote-state PWM (RSPWM), and selective harmonic elimination PWM (SHEPWM), were used to reduce the amplitude or frequency of CMV fluctuations. However, CMV-reduced PWM will result in unacceptable harmonic distortion in the phase current and cause eddy-current loss in the filter. The aforementioned methods are focused on two-level inverters. Furthermore, carrier synchronization is essential and critical in existing methods. If the carrier synchronization bus is disabled, then ZSCCs will increase significantly and lead to a high total harmonic distortion (THD) for the phase current.

For three-level inverters, a modified inductor–capacitor–inductor filter was proposed to eliminate the high-frequency components in ZSCCs, and a ZSCC feedback control loop was utilized to suppress low-frequency components [18], [19]. Moreover, a modified modulation method, with a modulation wave that is similar to that of the two-level space vector PWM (SVPWM), was used to reduce the high-frequency components of ZSCCs. This approach can effectively eliminate ZSCCs in three-level inverters. However, it can only be used in inverters with same types of filter.

To suppress ZSCCs in parallel operating three-level neutral point clamped (NPC) inverters with common AC and DC buses, the zero common mode voltage PWM (ZCMV-PWM) and ZSCC feedback methods were preliminarily investigated in [20]. The ZCMV-PWM method, which can keep CMV at zero, was proposed to eliminate high-frequency components, whereas the ZSCC feedback-based neutral point potential (NPP) control was used to suppress low-frequency components. The excitation sources of ZSCCs, the ZCMV-PWM method, the ZSCC feedback control strategy, and the parameter design are fully analyzed in the current study. The proposed scheme is

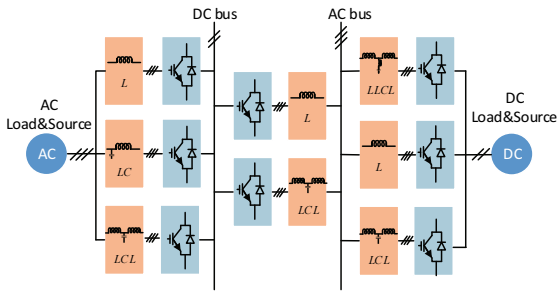


Fig. 1. Modularized inverters in a hybrid AC and DC system.

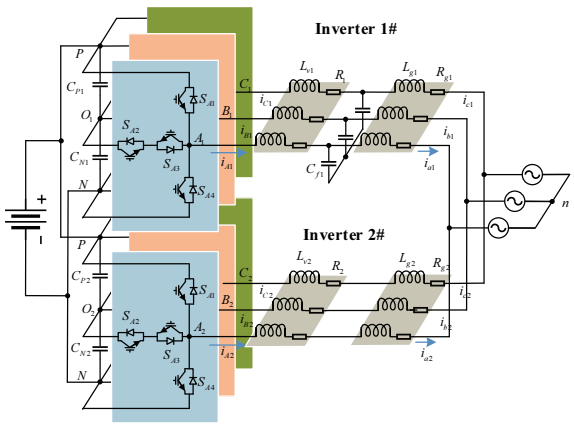


Fig. 2. Structure of the proposed parallel system.

verified via simulation and experiment. The results show the effectiveness of the proposed method in eliminating ZSCCs and its good performance in the steady and dynamic states. Compared with existing strategies, the proposed strategy exhibits the advantage of not requiring carrier synchronization. It can be utilized in inverters with different types of filter.

The remainder of this article is organized as follows. The equivalent model of ZSCC is developed in Section II. The excitation sources of ZSCCs are analyzed in Section III. On the basis of the analysis, a combined ZCMV-PWM and ZSCC feedback method for eliminating ZSCCs is proposed in Section IV. In Sections V and VI, the effectiveness of the proposed scheme is verified via simulation and experiment. Section VII summarizes the conclusions and contributions of this study.

II. Modeling of ZSCC

This study considers two three-phase three-level T-type NPC inverters that are paralleled with each other. As illustrated in Fig. 2, the two inverters, which have the same structure but different filters, are connected with a common DC and AC power supply. C_P and C_N denote the DC bus capacitors. L_{v1} and L_{v2} are the inverter-side filter inductances. L_{g1} and L_{g2} are the grid-side filter inductances. R_1, R_2, R_{g1}, and R_{g2} are the equivalent series resistances (ESRs) of the three-phase inductances L_1, L_2, L_{g1}, and L_{g2}, respectively. C_f denotes the filter capacitor. O_1 and O_2 denote the neural points of inverters $1^{\#}$ and $2^{\#}$, respectively. n denotes the

potential of the star point of the utility grid.

To simplify the explanation, the inductor currents and the DC bus voltage are assumed constant in a switching cycle. In accordance with Kirchhoff's voltage law (KVL), the following equation can be obtained:

$$\begin{aligned} &U_{m1N}-L_{v1}\frac{di_{m1}}{dt}-R_1 i_{m1}-L_{g1}\frac{di_{n1}}{dt}-R_{g1}i_{n1}= \\ &U_{m2N}-L_{v2}\frac{di_{m2}}{dt}-R_2 i_{m2}-L_{g2}\frac{di_{n2}}{dt}-R_{g2}i_{n2} \end{aligned}, \tag{1}$$

where i_{mj} (m = A, B, C; j = 1, 2) is the inverter-side phase current of the jth inverter, i_{kj} (k = a, b, c) is the grid-side phase current of the jth inverter, and U_{mjN} is the voltage of the phase leg mj to the negative DC bus N.

U_{mjN} can be obtained by the following equation:

$$U_{mjN}=\frac{U_{dc}}{2}(S_{mj}+1)+\frac{\Delta U_j}{2}(|S_{mj}|-1), \tag{2}$$

where S_{mj} is defined as the switching state of the m phase of the jth inverter. S_{mj} = 1, 0, –1 indicates that the corresponding phase voltages to the neural points are positive, zero, and negative, respectively. The voltage difference of DC capacitors ΔU_j is defined as $U_{Pj} - U_{Nj}$.

From the definition of ZSCC in [7], the ZSCC of the parallel system can be obtained as follows:

$$\begin{aligned} &i_{01}=(i_{A1}+i_{B1}+i_{C1})=(i_{a1}+i_{b1}+i_{c1}) \\ &=-i_{02}=-(i_{A2}+i_{B2}+i_{C2})=-(i_{a2}+i_{b2}+i_{c2}) \end{aligned}, \tag{3}$$

where i_{0j} denotes the ZSCC of inverter $j^{\#}$.

The following ZSCC equation can be obtained by adding the three-phase equations in Eq. (1) and substituting with Eq. (3):

$$U_Z=\sum_{m=A,B,C}(U_{m1N}-U_{m2N})=L_\Sigma\frac{di_{01}}{dt}+R_\Sigma i_{01}, \tag{4}$$

where U_Z is the excitation voltage of ZSCC; L_Σ is the sum of L_{v1}, L_{v2}, L_{g1}, and L_{g2}; and R_Σ is the sum of R_{v1}, R_{v2}, R_{g1}, and R_{g2}.

The definition of CMV depends on the reference point. In this study, the CMV of inverter $j^{\#}$ is defined as follows:

$$U_{CMVj}=\frac{1}{3}\times\sum_{m=A,B,C}\left(U_{mjN}-\frac{U_{dc}}{2}\right), \tag{5}$$

where U_{CMVj} is the CMV of inverter $j^{\#}$, and $U_{mjN}-U_{dc}/2$ is the voltage of phase leg mj to the potential neutral point of the DC bus.

From Eqs. (2), (4), and (5), the following equation can be obtained:

$$\begin{aligned} U_Z=3\times(U_{CMV1}-U_{CMV2})=&\underbrace{\frac{U_{dc}}{2}\times\sum_{m=A,B,C}(S_{m1}-S_{m2})}_{Part\_I} \\ &\underbrace{+\frac{\Delta U_2}{2}\times(3-\sum_{m=A,B,C}|S_{m1}|)-\frac{\Delta U_1}{2}\times(3-\sum_{m=A,B,C}|S_{m2}|)}_{Part\_II} \end{aligned}. \tag{6}$$

Thus, Eq. (4) can be rewritten as follows:

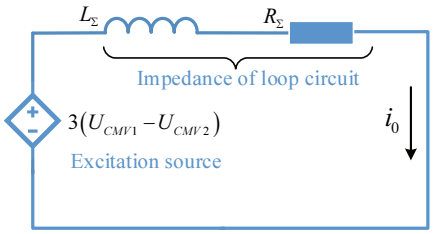


Fig. 3. Equivalent circuit of the ZSCC loop.

$$3\times(U_{CMV1}-U_{CMV2})=L_\Sigma\frac{di_{01}}{dt}+R_\Sigma i_{01}. \tag{7}$$

Eq. (7) is the equivalent model of the ZSCC between the paralleled inverters. The equivalent circuit of the ZSCC is illustrated in Fig. 3.

The following conclusions can be drawn from the preceding analysis:

1) ZSCC is related to the impedance of the loop circuit and the excitation source.
2) The ESR of the inductance is too small and the inductance of the loop circuit can only provide high impedance in high frequencies; thus, the impedance characteristic of ZSCC can be regarded as a low-pass filter.
3) The difference between the CMVs of the parallel inverters is the excitation source of ZSCC.
4) ZSCC can be eliminated by increasing the impedance of the loop circuit and decreasing the excitation source.

However, increasing the impedance of the loop circuit is costly and results in a bulky system. Thus, this study investigates the approach in which the excitation source is decreased.

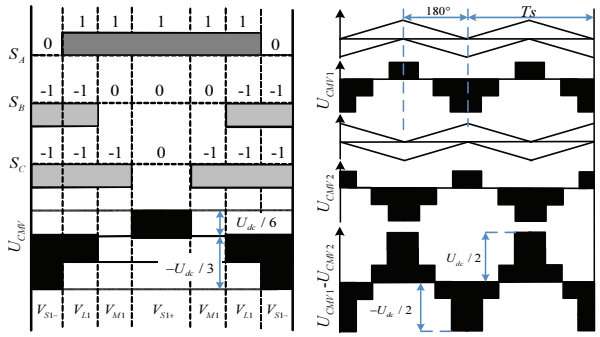
III. Excitation Sources of ZSCC Analysis

From Eq. (6), the difference of CMVs two parts. Part I is caused by the mismatch of the switching instant. Part II is caused by the mismatch of the switching instant and the difference in DC capacitor voltage. To obtain a good output current/voltage waveform performance, the voltage of neural points is typically kept at half of the DC voltage. Thus, the voltage difference of DC capacitors ΔU_j is nearly zero. Therefore, Part I is the primary cause of ZSCC. In this section, the voltage difference of DC capacitors ΔU_j is considered zero, and the primary cause of ZSCC is discussed.

If ΔU_j = 0, then the voltages of DC capacitors are balanced. The CMV of inverter $j^{\#}$, labeled as U_{B_CMVj}, can be expressed as follows:

$$U_{B\_CMVj}=\frac{1}{3}\times\sum_{m=A,B,C}\left(U_{mjN}-\frac{U_{dc}}{2}\right)=\frac{U_{dc}}{6}\times\sum_{m=A,B,C}S_{mj}. \tag{8}$$

For three-level NPC inverters with balanced DC capacitor voltages, CMV can be analyzed in two time scales: the switching period and the grid fundamental



(a) Pulse pattern and CMV (b) Difference in CMVs

Fig. 4. High-frequency excitation source.

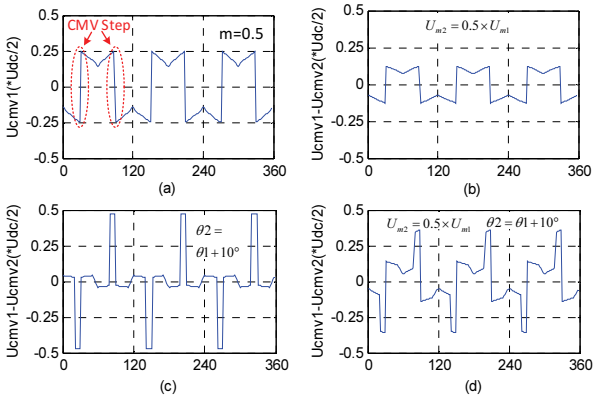


Fig. 5. Low-frequency excitation source: normalized CMV.

period. The CMV in the switching period is called the high-frequency excitation source, whereas the CMV in the grid fundamental period is called the low-frequency excitation source.

A. High-frequency Excitation Source

Different vectors generate different CMV values in a switching period. Fig. 4(a) shows the pulse pattern of SVPWM for a reference vector with $0°<\theta<30°$ (when the reference vector coincides with phase *a*, θ = zero). As shown in the figure, the amplitudes of CMV for vectors V_{S1-}, V_{L1}, V_{M1}, and V_{S1+} are $-U_{dc}/3$, $-U_{dc}/6$, 0, and $U_{dc}/6$, respectively. When the paralleled inverters have the same reference modulation signals, the same carrier frequencies, and synchronized carrier waves ($\Delta\varphi = 0$), the CMVs of the paralleled inverters are nearly the same. Thus, the difference in CMVs will be minimal. If the paralleled inverters have different frequencies and/or unsynchronized carrier waves, then the difference in CMVs will vary with the difference in the phase angles of the carrier waves. In particular, when the phase angle difference of the carrier waves ($\Delta\varphi$) is 180°, the difference in CMVs will exhibit the largest value, as shown in Fig. 4(b).

The difference in CMVs within a switching period is the high-frequency excitation source of ZSCC, which will cause high-frequency ZSCCs. High-frequency ZSCCs cannot be eliminated via closed-loop control. Carrier wave synchronization can reduce high-frequency ZSCCs. However, carrier wave synchronization is beyond the requirement of a modularized inverter. In this study, the high-frequency excitation source is eliminated using the ZCMV-PWM method.

B. Low-frequency Excitation Source

The average value of CMV in a fundamental period is the low-frequency CMV. The sine-triangle-based PWM can be functionally equivalent to the standard SVPWM [21]. The low-frequency CMV can be easily obtained in the sine-triangle-based PWM. For the standard SVPWM, the low-frequency CMV in modulation index m = 0.5 is shown in Fig. 5(a) (modulation index m is equal to $\sqrt{3}U_m/U_{dc}$, and U_m is the peak value of the reference voltage). The waveform in Fig. 5(a) is the CMV of the modulation signals for the sine-triangle-based PWM in a fundamental period ($0°<\theta<360°$).

The low-frequency CMV is thrice the fundamental frequency. Figs. 5(b), 5(c), and 5(d) show the differences in the CMVs of the inverters with varying amplitudes, phases, and amplitudes and phases of the reference voltage, respectively. The difference in CMVs is also thrice the fundamental frequency, which causes low-frequency ZSCCs that are thrice the fundamental frequency.

In two-level inverters, the strategy is to eliminate low-frequency ZSCCs by using ZSCC feedback control. The principle of ZSCC feedback control in two-level inverters is implemented by adjusting the CMV value for each inverter. However, this control method cannot be implemented in three-level NPC inverters. One reason for this limitation is the step changes of CMV and the difference in CMV (as shown in Fig. 5). The step changes of CMV generate high instantaneous ZSCCs. The harmonic components are considerably more than those of two-level inverters. Another reason is that CMV injection will change the neutral point voltage. Thus, the traditional ZSCC feedback control method cannot be implemented in three-level inverters. In this study, the low-frequency excitation source will be eliminated by using the proposed ZCMV-PWM method and NPP control.

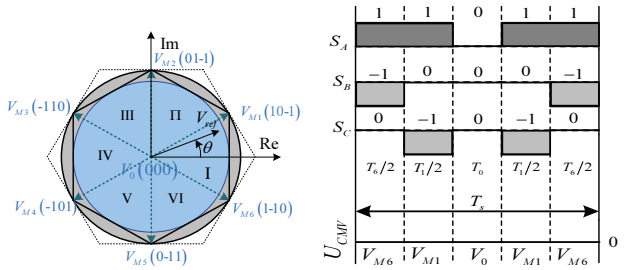
IV. Strategy for ZSCC Elimination

To eliminate ZSCCs between parallel operating three-level NPC inverters with common AC and DC buses, a novel strategy based on the ZCMV-PWM technique and ZSCC feedback control is proposed in this section. The ZCMV-PWM method is used to minimize the primary excitation source, whereas an NPP circuit is used to realize ZSCC feedback control.

A. ZCMV-PWM Method

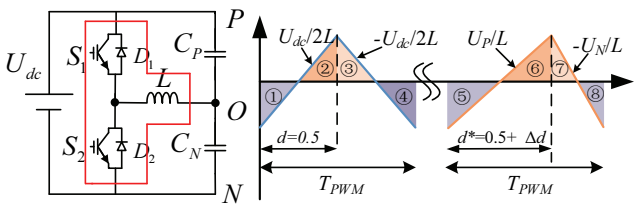
To reduce CMV and CMV fluctuation, a zero CMV modulation method for three-level NPC inverters, called 2MV1Z, is used in this study. 2MV1Z takes two medium vectors and a zero vector to synthesize the reference vector [22–23]. For 2MV1Z, $S_A + S_B + S_C$ is always equal to zero. Thus, the CMV of the inverter with 2MV1Z can be maintained at zero. Meanwhile, 2MV1Z achieves good DC voltage utilization, harmonic distortion, and DC current ripple and losses [24]. The voltage vector space and pulse pattern of the 2MV1Z method are shown in Fig. 6.

The voltage vector space of 2MV1Z in Fig. 6(a) consists of six medium vectors and a zero vector. As shown in Fig. 6(b), the five-stage pulse pattern is adopted and CMV can be maintained at zero within a switching period. In practical implementations, however, dead time must be added at the instant of state switching to ensure the safe switching of insulated-gate bipolar transistors (IGBTs). Thus, CMV fluctuation is caused by a new vector during dead time. However, ZSCC is determined by the excitation voltage and it affects time. Dead time is extremely short, with a typical duration of 2–5 μs. Therefore, the unexpected fluctuations of CMV will have minimal effect on ZSCC.



(a) Voltage vector space. (b) Pulse pattern.

Fig. 6. Voltage vector space and pulse pattern of 2MV1Z.



(a) Electric circuit. (b) Inductance current.

Fig. 7. NPP control circuit.

B. NPP Control

As mentioned in Sections II and III, Part II of the excitation source is the difference in NPPs. Although this difference should be extremely small for the sinusoidal output waveform, it can be used to eliminate ZSCCs by adjusting their magnitude and function time. To control NPPs, the traditional strategy is implemented by allocating small vectors. However, the ZCMV-PWM method will cause NPP fluctuations and cannot balance such fluctuations. In this study, an electric circuit is used to control NPPs.

The NPP control topology is shown in Fig. 7(a). The NPP control circuit consists of two IGBTs (S_1 and S_2) and an inductance (L). This circuit is a typical bidirectional buck/boost chopper. The two IGBTs work in complementary mode. As shown in Fig. 7(b), the inductance current is positive when current is injected into point O. The duty circle of the upper IGBT S_1 is d ($0 < d < 1$). In the beginning of the PWM period, the duty circle d is 0.5 and the voltage of the two capacitors is balanced. When S_1 is on, the current rises in the slope of $U_{dc}/2L$. When S_2 is on, the current declines in the slope of $-U_{dc}/2L$. A positive current indicates that current is injected into point O, then the voltage of C_N (U_N) will increase. Similarly, a negative current indicates the absorption of current from point O and the decrease of the voltage of C_N (U_N). The injected current is equal to the absorbed current in a switching period. The value of the capacitors and the frequency of PWM are sufficiently large; hence, the voltage of the capacitors slightly fluctuates. If the duty circle is increased to 0.5 + Δd, then the relationship of the capacitor voltage will be $U_N > U_P$. The voltage will reach another steady state. Similarly, if the duty circle is decreased to 0.5 – Δd, then the relationship of the capacitor voltage will be $U_N < U_P$. In conclusion, NPP can be adjusted by using this NPP control circuit.

In the NPP control circuit, inductance is determined by the output current and the voltage ripple requirements. The design process can be referenced to the design principle of the boost-and-buck converter [25]. The parameter of the inductor can be calculated by Eq. (9):

$$L \geq \frac{1.25 U_{dc} T_{PWM}}{I_{\max .out}}, \tag{9}$$

where T_{PWM} is the switching period of an IGBT, and $I_{max.out}$ is the maximum current of a neural point.

From Eqs. (6) and (7), when ZSCC is greater than zero, the process for eliminating ZSCCs is shown as follows:

Case 1: $i_0 > 0 \rightarrow d \downarrow \rightarrow U_{N1} \downarrow \rightarrow U_{P1} \uparrow \rightarrow \Delta U \uparrow \rightarrow i_0 \downarrow$.

Similarly, when ZSCC is less than zero, the process for eliminating ZSCCs is shown as follows:

Case 2: $i_0 < 0 \rightarrow d \uparrow \rightarrow U_{N1} \uparrow \rightarrow U_{P1} \downarrow \rightarrow \Delta U \downarrow \rightarrow i_0 \uparrow$.

In conclusion, ZSCC feedback control is executed by using this NPP control circuit. ΔU must be limited within a small range to avoid distorting the output voltage waveform. ZSCC control is mainly implemented by controlling the function time of ΔU.

C. Strategy for ZSCC Elimination

The block diagram of ZSCC feedback control is shown in Fig. 8. The ZSCC control loop is a cascaded double loop. The inner loop is the NPP control loop; the outer loop is the ZSCC control loop.

C_u(s) is the NPP controller. C_i(s) is the ZSCC controller.

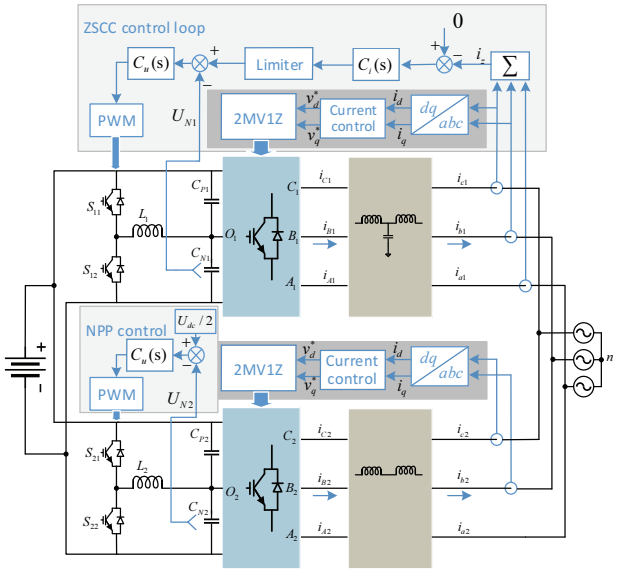


Fig. 8. Block diagram of ZSCC feedback control.

The set value of the outer loop is zero, and the output of the outer loop controller is the given value of the inner loop via a limiter. The output of the total control loop is the duty cycle d of the switching device in the NPP control circuit. This double-loop controller can realize NPP and ZSCC control. When N inverters are paralleled, N–1 ZSCC controllers are necessary [4]. Furthermore, each ZSCC controller is implemented by each inverter. In additional interconnected circuits between inverters, carrier synchronization buses are not essential. This condition is highly convenient for modular design.

As shown in the block diagram of ZSCC feedback control, inverter $1^{\#}$ adopts ZSCC control and NPP control. The control block diagram for inverter $1^{\#}$ is shown in Fig. 9. The terms of U_{N2} and $(U_{B\_CMV1} - U_{B\_CMV2})$ are disturbances.

The NPP control circuit operates in continuous mode. In accordance with small signal modeling theory, transform function $G_u(s)$ can be obtained as

$$G_u(s) = \frac{d(s)}{U_{N1}(s)} = U_{dc} \frac{R_{ESR}C_\Sigma s + 1}{LC_\Sigma s^2 + R_{ESR}C_\Sigma s + 1}, \tag{10}$$

where C_Σ is the sum of the capacitor values of C_P and C_N, and R_{ESR} is the sum of the equivalent series resistances of inductance (L) and the DC capacitor (C_P).

For the three-level inverter with the ZCMV-PWM method, the neutral voltage ripple frequency is the third harmonic of the output frequency. If the grid frequency is 50 Hz, then the frequency of NPP variation will be 150 Hz. The proportional–integral (PI) control ($C_u(s) = K_{p.u} + K_{i.u}/s$) is adopted to control NPP. A control bandwidth of five times the frequency of the NPP variation is selected. In practical applications, compensator $C_u(s)$ is designed using the control design toolbox in MATLAB, called the "SISO tool."

The main purpose of ZSCC feedback control is to eliminate the DC component. The control bandwidth is

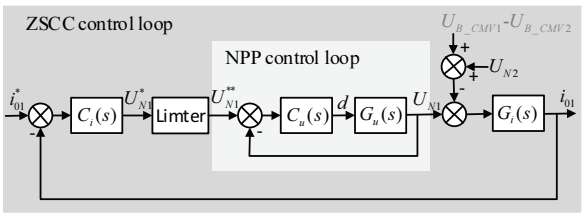


Fig. 9. Control block diagram of ZSCC.

selected to less than one of five times the bandwidth of the NPP control loop. Thus, the closed-loop transform function of NPP control is proportional factor 1. The ZSCC controller also adopts PI control, and the control law is shown as follows:

$$C_i(s) = \frac{U_{N1}^*(s)}{i_{01}(s)} = K_{p.i}(1 + \frac{1}{T_i s}), \tag{11}$$

where $K_{p.i}$ is the proportional gain, and T_i is an integral time constant.

As shown in Fig. 9, the *Limiter* keeps the neural point within a certain range to reduce output voltage distortion.

$$U_{N1}^{**} = \begin{cases} U_{N1}^*, \frac{U_{dc}}{2} - \sigma \le U_{N1}^* \le \frac{U_{dc}}{2} + \sigma; \\ \frac{U_{dc}}{2} - \sigma, U_{N1}^* < \frac{U_{dc}}{2} - \sigma; \\ \frac{U_{dc}}{2} + \sigma, U_{N1}^* > \frac{U_{dc}}{2} + \sigma; \end{cases}, \tag{12}$$

where σ (σ>0) is the allowable range of NPP fluctuation.

The transform function $G_i(s)$ can be obtained as follows by applying Laplace transform to Eq. (7). To simplify the analysis, $3-(|S_{A1}|+|S_{B1}|+|S_{C1}|)$ is seen as 1.

$$G_i(s) = \frac{i_{01}(s)}{U_{N1}(s)} = \frac{1}{L_\Sigma s + R_\Sigma} \tag{13}$$

The open-loop and closed-loop transfer functions of ZSCC control can be obtained from Fig. 9. The *Limiter* is ignored in the linear system design.

$$\varphi_o(s) = C_i(s)G_i(s) = \frac{K_{p.i}(T_i s + 1)}{T_i s(L_\Sigma s + R_\Sigma)}, \tag{14}$$

$$\varphi_c(s) = \frac{\varphi_o(s)}{1 + \varphi_o(s)} = \frac{K_{p.i}}{L_\Sigma} \times \frac{s + 1/T_i}{s^2 + ((K_{p.i} + R_\Sigma)/L_\Sigma)s + K_{p.i}/(L_\Sigma T_i)}, \tag{15}$$

where $\varphi_o(s)$ is the open-loop transfer function, and $\varphi_c(s)$ is the closed-loop transfer function.

The closed-loop transfer function of ZSCC is a typical second-order system. The system can be simplified to a first-order system via pole zero cancellation. The integral time constant is set to

$$T_i = \frac{L_\Sigma}{R_\Sigma}. \tag{16}$$

Thus, the following equations can be obtained:

$$\varphi_o(s) = \frac{K_{p.i}}{L_\Sigma s}, \tag{17}$$

TABLE I
PARAMETERS IN THE SIMULATION AND EXPERIMENT

Parameter	Value
Filter for inverter 1#	L_v = 1.2 mH, L_g = 0.2 mH, C_f = 20 μF, damping resistance = 0.5 Ω
Filter for inverter 2#	L_v = 1.2 mH, L_g = 0.2 mH
ESR	$R + R_g$ = 70 mΩ, R_{ESR} = 100 mΩ (simulation)
DC voltage	600 V (simulation), 300 V (experiment)
DC capacitor	$C_P = C_N$ = 4100 μF
NPP inductor	L = 1 mH
Switching frequency	Inverter 1#: 10 kHz, 20 kHz (NPP); Inverter 2#: 9 kHz, 18 kHz (NPP); 220 V (line-to-line RMS)/50 Hz (simulation)
Main grid	110 V (line-to-line RMS)/50 Hz (experiment)
Dead time	3 μs (Inverter 1#), 4 μs (Inverter 2#)
Limiter	0.5% U_{dc}
C_u(s)	$K_{p.u}$ = 0.1, $K_{i.u}$ = 3
C_i(s)	$K_{p.i}$ = 0.3, $T_{i.i}$ = 0.02

$$\varphi_c(s) = \frac{1}{1+\frac{L_\Sigma}{K_{p.i}}s} = \frac{1}{1+\tau s}. \quad (18)$$

If the bandwidth of ZSCC control is set as ω_c (rad/s), then the proportional gain can be obtained as follows:

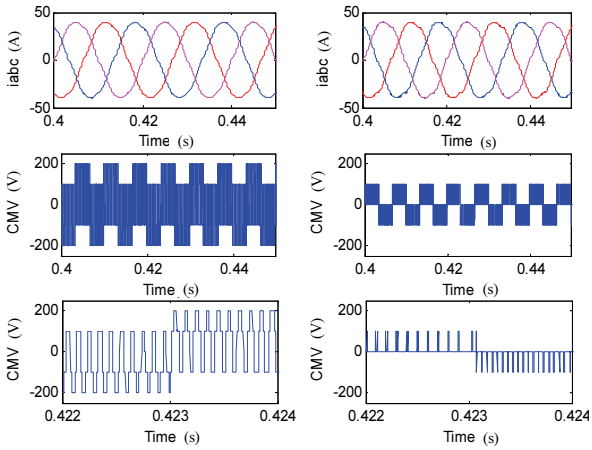
$$K_{p.i} = \omega_c L_\Sigma. \quad (19)$$

V. SIMULATION VALIDATION

To validate the effectiveness of the proposed strategy for ZSCC elimination, simulations are conducted in MATLAB/Simulink. Two paralleled T-type NPC three-level inverters with different filters (Fig. 8) are used in the simulation. The inverter and control parameters are listed in Table I.

To validate the effectiveness of the 2MV1Z method in reducing CMV fluctuation, the simulation result is presented in Fig. 10.

The peak-to-peak value of CMV for the three-level SVPWM is 400 V, which is reduced to 200 V for 2MV1Z. Furthermore, the number of CMV fluctuations is also reduced



(a) SVPWM. (b) 2MV1Z.

Fig. 10. Simulated phase current and CMV waveform.

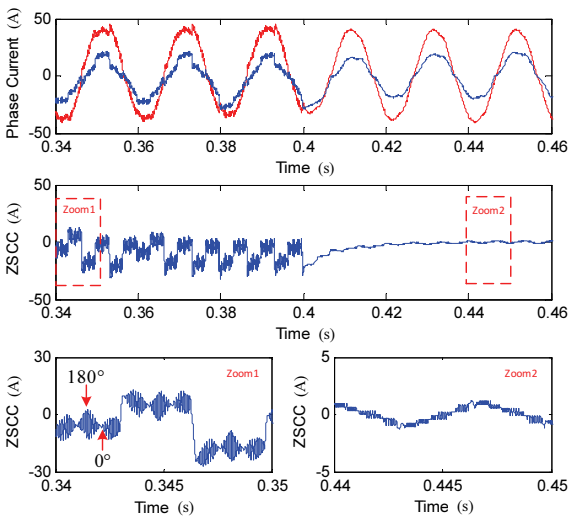


Fig. 11. Simulated phase currents and ZSCCs. From top to bottom: phase current (i_{a1}: red; i_{a2}: blue), ZSCC, ZSCC of SVPWM, and ZSCC of 2MV1Z with ZSCC control.

within a switching period. Thus, the amplitude and frequency of CMV for the 2MV1Z method are significantly reduced compared with those in SVPWM. The CMV fluctuation in Fig. 10(b) is caused by dead time. The duration of each CMV pulse is equal to the dead time. The simulation results verify the analysis in Section III and demonstrate the effectiveness of the ZCMV-PWM method. Although the magnitudes of non-designed CMV fluctuations are U_{dc}/3, their effective acting time is extremely short, i.e., only 3 μs (dead time), which will have minimal impact on ZSCC.

To verify the proposed strategy for ZSCC elimination, the simulation result is presented in Fig. 11.

In the beginning, SVPWM is implemented in the two inverters. The proposed ZSCC elimination method starts working at 0.4 s. Before 0.4 s, ZSCC is significantly large and phase currents are immensely distorted. ZSCC fluctuates in low and high frequencies. The low-frequency fluctuation is

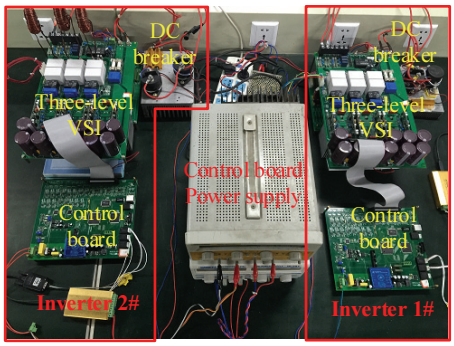


Fig. 12. Experimental platform.

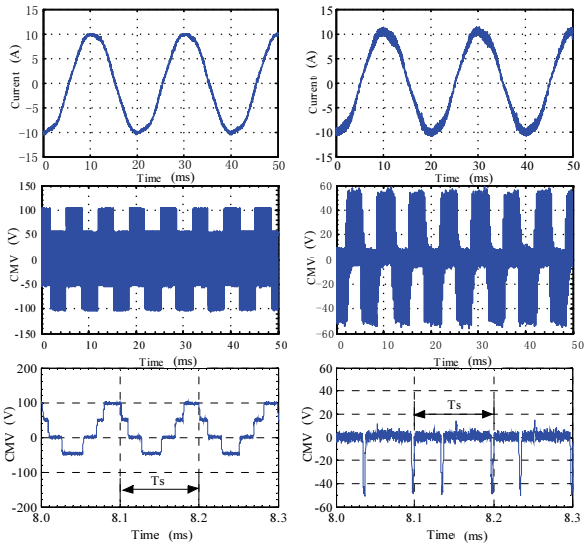
the third-order fundamental frequency (similar waveform as that in Fig. 5(b)). The high-frequency fluctuation depends on the phase shift of the two carrier waves. When the phase shift is $180°$, the high-frequency part of ZSCC obtains the largest value. When the phase shift is $0°$, the high-frequency part of ZSCC obtains the smallest value. The simulated result validates the analysis in Section III.A. After 0.4 s, ZSCC is significantly reduced and the distortion of phase currents is also decreased. ZSCC is unaffected by the phase shift of the two carrier waves. The high-frequency part of ZSCC is eliminated effectively by using the 2MV1Z method. The low-frequency part of ZSCC is eliminated by the feedback control strategy. The simulated result verifies the proposed strategy for ZSCC elimination.

VI. Experimental Validation

To validate the developed model and the proposed elimination schemes, experiments are performed on a prototype system. The experimental platform is shown in Fig. 12. The prototype is composed of two paralleled three-level T-type NPC voltage source inverters. The inverter and control parameters are provided in Table I. The control strategy is implemented by a digital signal processor chip (TMS320F28335). Furthermore, all the experiments are tested without carrier synchronization.

To validate the effectiveness of the 2MV1Z method in reducing CMV fluctuation, the experimental results are presented in Fig. 13. The results are tested on inverter $1^{\#}$. The CMV curve is calculated by $(U_{AIN}+ U_{BIN}+ U_{CIN})/3 - U_{dc}/2$. U_{m1N} is measured using an oscilloscope.

As shown in Fig. 13, the peak-to-peak value of CMV for SVPWM is 200 V, which is reduced to 100 V for 2MV1Z. The fluctuation times are also reduced within a switching period. Thus, the amplitude and frequency of CMV for the 2MV1Z method are significantly reduced compared with those for the standard three-level SVPWM. The CMV fluctuation in Fig. 13(b) is caused by dead time. The duration of each CMV pulse is equal to the dead time. The experimental result verifies the analysis in Section III and the effectiveness of the proposed ZCMV-PWM method.



(a) SVPWM (b) 2MV1Z

Fig. 13. Experimental phase current and CMV waveform.

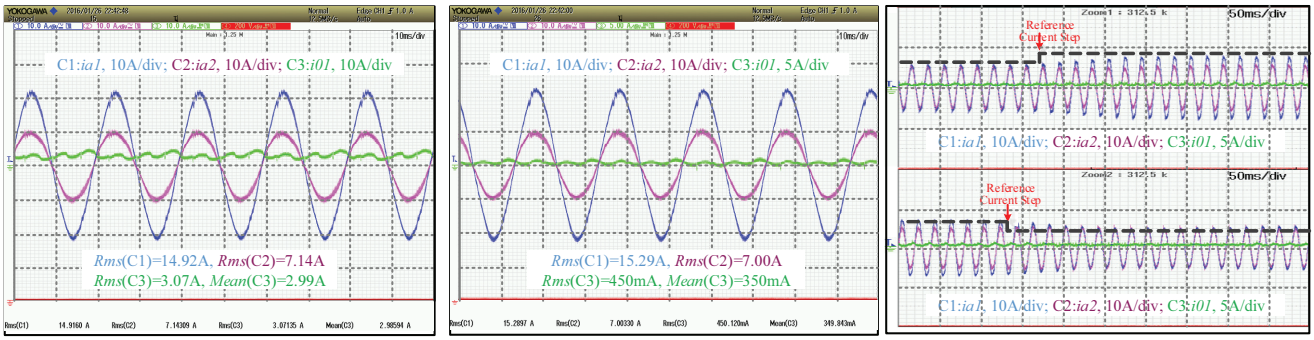
In Fig. 13, the THDs of the inverter-side phase current for each modulation method are 4.4% (SVPWM) and 5.49% (2MV1Z). In SVPWM, the most adjacent vectors are always used to synthesize the reference vector. Thus, the least harmonic distortions of voltage can be obtained.

In the experiment, the inverters with SVPWM cannot work in parallel because ZSCC is extremely large and the phase current causes current protection. Thus, the experiment results are all tested using the 2MV1Z method. The experimental results are presented in Fig. 14. All results are tested on paralleled inverters with different reference currents, control periods, and filter types.

The experimental waveforms of the 2MV1Z method without ZSCC control are shown in Fig. 14(a). Even without ZSCC feedback control, ZSCC is smaller than the phase current. Although ZSCC fluctuates in low frequencies and has a DC component, the high-frequency parts of ZSCC are eliminated effectively by using the 2MV1Z method. With regard to harmonic distortion performance, the THD of i_{a1} is 2.32% and that of i_{a2} is 4.92%. The THD value of inverter $2^{\#}$ is higher than that of inverter $1^{\#}$ because L-type filters are used in inverter $2^{\#}$.

The experimental waveforms of the 2MV1Z method with ZSCC control are shown in Fig. 14(b). The phase currents present a good sinusoidal waveform, and ZSCC is extremely small. Compared with the ZSCC in Fig. 14(a), the result in Fig. 14(b) shows the effectiveness of ZSCC feedback control. The DC component is immensely reduced, and ZSCC fluctuation is also eliminated. In terms of harmonic distortion performance, the THD of i_{a1} is 2.22% and that of i_{a2} is 4.54%. Compared with that in Fig. 14(a), the THD value in Fig. 14(b) is reduced because ZSCC is eliminated.

The experiment result in the reference step condition is presented in Fig. 14(c). As shown in the figure, the phase



(a) 2MV1Z method without ZSCC control. (b) 2MV1Z method with ZSCC control. (c) Dynamic response of ZSCC control.

Fig. 14. Experimental results of the proposed ZSCC eliminating method. (*CH1: grid side current of inverter 1#, CH2: grid side current of inverter 2#, CH3: ZSCC*).

currents exhibit a good sinusoidal output wave and ZSCC is minimal. The experimental result validates the proposed ZSCC elimination method. Through the proposed method, ZSCCs are eliminated under steady and dynamic states.

VII. Conclusion

This study proposes a novel strategy based on the ZCMV-PWM technique and ZSCC feedback control to eliminate ZSCCs between parallel operating three-level NPC inverters with common AC and DC buses. The ZCMV-PWM method is used to reduce CMV, whereas a simple electric circuit is adopted to control NPP and ZSCC. ZSCC between paralleled inverters is eliminated effectively by using the proposed strategy. The results show the good performance of the proposed method under steady and dynamic states. This method not only has a small ZSCC and phase current distortion, but also does not require carrier synchronization. Furthermore, the proposed method is not limited by filter type. It can be utilized in paralleled inverter applications with different types of filter.

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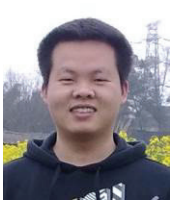

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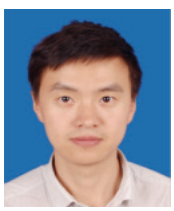

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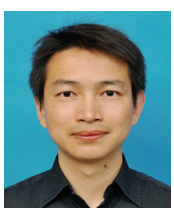

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