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# Double Line Voltage Synthesis Strategy for Three-to-Five Phase Direct Matrix Converters

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**Abstract**

This paper proposes a double line voltage synthesis (DLVS) strategy for three-to-five phase direct matrix converters. In the proposed strategy, the input and expected output voltages are divided into 6 segments and 10 segments, respectively. In addition, in order to obtain the maximum voltage transfer ratio (VTR), the input line voltages and "source key" should be selected reasonably according to different combinations of input and output segments. Then, the corresponding duty ratios are calculated to determine the switch sequences in different segment combinations. The output voltages and currents are still sinusoidal and symmetrical with little lower order harmonics under unbalanced or distorted input voltages by using this strategy. In addition, the common mode voltage (CMV) can be suppressed by rearranging some of the switching states. This strategy is analyzed and studied by a simulation model established in MATLAB/Simulink and an experimental platform, which is controlled by a DSP and FPGA. Simulation and experimental results verify the feasibility and validity of the proposed DLVS strategy.

**Key words:** Common mode voltage, Direct matrix converter, Double line voltage synthesis strategy, Source key, Three-to-five phase, Unbalanced or distorted input voltages

## I. INTRODUCTION

Compared with traditional three-phase machines drives, the multi-phase machines drives have some advantages such as reducing torque pulsations, reducing the current per phase without increasing the phase voltage, designs with a lower voltage for the same total power, and most importantly high system reliability and stability [1]-[7]. The fault-tolerant property results in multi-phase systems being widely used for high performance applications where reliability is improntant such as electric/hybrid electric vehicle drives, electric ship propulsion, aircraft drives, locomotive traction, offshore wind generation, aerospace drives and some high power industrial applications [3]-[9].

Multi-phase power converters are energy conversion devices that are matched with multi-phase system drives, and they can achieve high power energy transformations under limited voltage levels. Multi-phase matrix converters are one of the most advanced AC-AC conversion technologies among the multiphase power converters. In addition, the three-to-five phase direct matrix converter (DMC) is the most representative of these converters, and its topology is shown in Fig. 1. There are bidirectional switches connecting each phase of the input with five-phase of the output. The benefits of the three-to-five phase DMC are similar to those of the three-to-three phase DMC since it has no large energy storage component requirements, a compact structure, a bidirectional energy flow, an unrestricted output frequency, and a controllable input power factor [10]-[12]. In addition, the maximum VTR of the three-to-five phase DMC is 0.7885 [12], [13].

At present, the most widely used modulation methods for the three-to-five phase DMC include the space vector pulse width modulation (SVPWM) and carrier-based pulse width modulation (CBPWM) methods. The duty ratio of each vector is obtained based on the division and combination of the input and output sectors in the SVPWM method [12]-[14]. This method is convenient for the elimination of narrow pulses and voltage compensation. The CBPWM method has recently been adopted in [15], [16] since it is easier to implement compared with the SVPWM method. However, the anti-disturbance capability of the above two methods is

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poor, and the total harmonic distortion (THD) of the output waveform is high under unbalanced or distorted input voltages. The direct transfer function approach was adopted in [17]. The relations of the output voltages to input voltages, and the input currents to output currents can be defined by the switching matrix in terms of the switching action. As a result, the switching states can be determined directly according to the relation. Even if the input voltages are unbalanced or distorted, a good output performance can be achieved by this method. However, the computation is complex when compared with other methods.

The DLVS strategy has not been applied in the modulation approaches for the three-to-five phase DMC. In this paper, based on the topology and operational principles of the three-to-five phase DMC, a DLVS strategy is proposed. According to the segments of the input and output reference voltages, the input line voltages and source key should be selected reasonably to synthesize the output voltages. The advantages of the proposed DLVS strategy are that the output voltages and currents are sinusoidal and symmetrical under unbalanced or distorted input voltages, and the calculation of the duty ratio is very simple. In addition, the CMV can also be reduced by rearranging some of the switching states. In order to show the validity of the proposed DLVS strategy, simulation models and an experimental platform are established.

## II. Operational Principles of the DLVS Strategy

### A. Topology of the Three-to-Five Phase DMC

The topology of the three-to-five phase DMC is illustrated in Fig. 1. It can be seen that it has fifteen bidirectional switches connecting the input with the output.

$u_a$, $u_b$, $u_c$ and $i_a$, $i_b$, $i_c$ are the three-phase input voltages and currents respectively; $i_A$, $i_B$, $i_C$, $i_D$, $i_E$ are the five-phase output currents; and $R$-$L$ is the resistance-inductance load. $R_f$, $L_f$ and $C_f$ are the resistor, inductor and capacitor of the input filter. The bidirectional switches of the three-to-five phase DMC are defined by $S_{jk}$ ($j \in \{A, B, C, D, E\}$; $k \in \{a, b, c\}$).

### B. Division Principle of the Input and Output Segments

Assume that the input three-phase voltages are:

$$\begin{cases} u_a = U_{im}\cos(\omega_i t) \\ u_b = U_{im}\cos(\omega_i t - 2\pi/3) \\ u_c = U_{im}\cos(\omega_i t + 2\pi/3) \end{cases} \quad (1)$$

where $U_{im}$ and $\omega_i$ are the amplitude and angular frequency of the input voltages, respectively. One period of the input voltages can be divided into six segments, as shown in Fig. 2. Each segment has common characteristics: two of the input phase voltages are positive or negative, while the polarity of the other one is opposite. $x$, $y$ and $z$ ($x$, $y$, $z \in \{a, b, c\}$) denote the corresponding phases that possess the maximum, medium, and minimum absolute values of the input voltages, respectively. Take segment 1 as an example. It can be divided into two parts equally. $x$, $y$, $z$ denote a, b, c in the first part, and they denote a, c, b in the latter part.

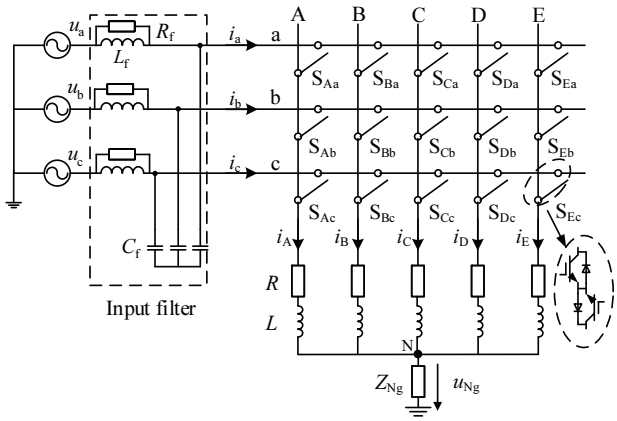



Fig. 1. Three-to-five phase DMC topology.

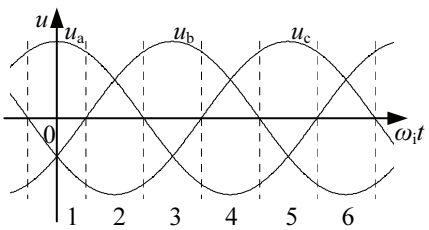



Fig. 2. Segments of the input three-phase voltages.

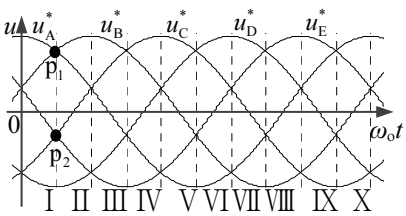



Fig. 3. Segments of the expected output five-phase voltages.

Assume that the expected fundamental output voltages are:

$$\begin{cases} u_A^* = U_{om}\cos(\omega_o t) \\ u_B^* = U_{om}\cos(\omega_o t - 2\pi/5) \\ u_C^* = U_{om}\cos(\omega_o t - 4\pi/5) \\ u_D^* = U_{om}\cos(\omega_o t - 6\pi/5) \\ u_E^* = U_{om}\cos(\omega_o t - 8\pi/5) \end{cases} \quad (2)$$

where $U_{om}$ and $\omega_o$ are the amplitude and angular frequency of the output phase voltages, respectively. The expected output five-phase voltages are divided into ten segments, as shown in Fig. 3. As can be seen, the dividing lines of the segments pass through the intersections of the phase voltages, and the values order of the phase voltages remain unchanged in each segment. Take segment Ⅰ and Ⅱ as an example. The dividing line passes through $p_1$ and $p_2$, and the values orders

are $u_A^* \geq u_B^* \geq u_E^* \geq u_C^* \geq u_D^*$ and $u_B^* \geq u_A^* \geq u_C^* \geq u_E^* \geq u_D^*$ in Ⅰ and Ⅱ, respectively. The corresponding phases that possess the absolute values of the output voltages in descending order are denoted by *U*, *V*, *W*, *X*, and *Y* (*U*, *V*, *W*, *X*, *Y*∈{A, B, C, D, E}). Take segment Ⅰ as an example. It can also be divided into two parts equally. *U*, *V*, *W*, *X*, *Y* denote A, D, C, B, E in the first part, and they denote D, A, B, C, E in the latter part.

### *C. Operational Principles of the DLVS Strategy*

In order to gain the maximum VTR, two larger input line voltages in every segment should be selected for synthesis. The following two cases are discussed.

*1)* $u_x \cdot u_U^* > 0$

Three input line voltages can be used to synthesize the output voltages, the control function can be expressed as:

$$\begin{bmatrix} u_{UV} \\ u_{UW} \\ u_{UX} \\ u_{UY} \end{bmatrix} = \begin{bmatrix} d_{11} & d_{12} & d_{13} & d_{10} \\ d_{21} & d_{22} & d_{23} & d_{20} \\ d_{31} & d_{32} & d_{33} & d_{30} \\ d_{41} & d_{42} & d_{43} & d_{40} \end{bmatrix} \begin{bmatrix} u_{xy} \\ u_{xz} \\ u_{zy} \\ u_{xx} \end{bmatrix} \tag{3}$$

where $d_{i1}$, $d_{i2}$, $d_{i3}$, $d_{i0}$ ($i$=1, 2, 3, 4) are the duty ratios of $u_{xy}$, $u_{xz}$, $u_{zy}$, $u_{xx}$ within one sampling period, respectively, and their value range is [0, 1].

In addition, the relationship among these duty ratios can be described as follows:

$$d_{i1} + d_{i2} + d_{i3} + d_{i0} = 1 \ \ (i = 1,\ 2,\ 3,\ 4) \tag{4}$$

Define the value of each duty ratio is proportional to the input voltage, so that the duty ratios can be expressed as:

$$\begin{cases} d_{11} = \alpha_1 u_{xy};\ \ d_{12} = \alpha_1 u_{xz};\ d_{13} = \alpha_1 u_{zy} \\ d_{21} = \alpha_2 u_{xy};\ d_{22} = \alpha_2 u_{xz};\ d_{23} = \alpha_2 u_{zy} \\ d_{31} = \alpha_3 u_{xy};\ d_{32} = \alpha_3 u_{xz};\ d_{33} = \alpha_3 u_{zy} \\ d_{41} = \alpha_4 u_{xy};\ d_{42} = \alpha_4 u_{xz};\ d_{43} = \alpha_4 u_{zy} \\ d_{i0} = 1 - d_{i1} - d_{i2} - d_{i3} \ \ (i = 1,\ 2,\ 3,\ 4) \end{cases} \tag{5}$$

where $\alpha_1$, $\alpha_2$, $\alpha_3$, $\alpha_4$ are the proportion coefficients of the corresponding voltages. Therefore, the duty ratios can be obtained by equation (3) and (5) as follows:

$$\begin{cases} d_{11} = k u_{UV}^* u_{xy};\ \ d_{12} = k u_{UV}^* u_{xz};\ d_{13} = k u_{UV}^* u_{zy} \\ d_{21} = k u_{UW}^* u_{xy};\ d_{22} = k u_{UW}^* u_{xz};\ d_{23} = k u_{UW}^* u_{zy} \\ d_{31} = k u_{UX}^* u_{xy};\ d_{32} = k u_{UX}^* u_{xz};\ \ d_{33} = k u_{UX}^* u_{zy} \\ d_{41} = k u_{UY}^* u_{xy};\ d_{42} = k u_{UY}^* u_{xz};\ \ d_{43} = k u_{UY}^* u_{zy} \\ d_{i0} = 1 - d_{i1} - d_{i2} - d_{i3} \ \ (i = 1,\ 2,\ 3,\ 4) \end{cases} \tag{6}$$

where $k$ is defined by:

$$k = \frac{1}{u_{ab}^2 + u_{bc}^2 + u_{ac}^2} \tag{7}$$

However, a line voltage can be indicated by the other two line voltages in the input side. In order to gain the maximum VTR, and to ensure the minimum switching number within one sampling period, the two input line voltages $u_{xy}$, $u_{xz}$ and zero voltage $u_{xx}$ are selected, and $u_{zy}$ can be described as:

$$u_{zy} = u_{xy} - u_{xz} \tag{8}$$

The control function in equation (3) and duty ratios in equation (6) can be described as:

$$\begin{bmatrix} u_{UV} \\ u_{UW} \\ u_{UX} \\ u_{UY} \end{bmatrix} = \begin{bmatrix} d_{11}' & d_{12}' & d_{10}' \\ d_{21}' & d_{22}' & d_{20}' \\ d_{31}' & d_{32}' & d_{30}' \\ d_{41}' & d_{42}' & d_{40}' \end{bmatrix} \begin{bmatrix} u_{xy} \\ u_{xz} \\ u_{xx} \end{bmatrix} \tag{9}$$

$$\begin{cases} d_{11}' = k u_{UV}^* (u_{xy} - u_{yz});\ \ d_{12}' = k u_{UV}^* (u_{xz} + u_{yz}) \\ d_{21}' = k u_{UW}^* (u_{xy} - u_{yz});\ d_{22}' = k u_{UW}^* (u_{xz} + u_{yz}) \\ d_{31}' = k u_{UX}^* (u_{xy} - u_{yz});\ \ d_{32}' = k u_{UX}^* (u_{xz} + u_{yz}) \\ d_{41}' = k u_{UY}^* (u_{xy} - u_{yz});\ \ d_{42}' = k u_{UY}^* (u_{xz} + u_{yz}) \\ d_{i0}' = 1 - d_{i1}' - d_{i2}' \ \ (i = 1,\ 2,\ 3,\ 4) \end{cases} \tag{10}$$

According to the control function described in (9), in the modulation, the switch $S_{Ux}$, which is defined as the "source key", must always be kept on in the whole sampling period. At the same time, $S_{Uy}$ and $S_{Uz}$ must be kept off. When the output line voltage $u_{UV}^*$ is synthesized, the switch $S_{Vy}$ is kept in the ON state during the time $d_{11}' T_s$ ($T_s$ is the sampling period), the switch $S_{Vz}$ is kept in the ON state during the time $d_{12}' T_s$, and the switch $S_{Vx}$ is kept in the ON state during the time $d_{10}' T_s$. The synthetic principles of the voltages $u_{UW}^*$, $u_{UX}^*$ and $u_{UY}^*$ are similar to those of the voltage $u_{UV}^*$. The input voltage in segment 1 and the output voltage in segment I are taken as an example. Then, the switching sequence can be rearranged as shown in Fig. 4.

*2)* $u_x \cdot u_U^* < 0$

This case is similar to the case (1). However, in order to ensure the minimum switching number within one sampling period, the output line voltages $u_{VU}^*$, $u_{VW}^*$, $u_{VX}^*$ and $u_{VY}^*$, are selected. Thus, the control function is as follows:

$$\begin{bmatrix} u_{VU} \\ u_{VW} \\ u_{VX} \\ u_{VY} \end{bmatrix} = \begin{bmatrix} d_{11}' & d_{12}' & d_{10}' \\ d_{21}' & d_{22}' & d_{20}' \\ d_{31}' & d_{32}' & d_{30}' \\ d_{41}' & d_{42}' & d_{40}' \end{bmatrix} \begin{bmatrix} u_{xy} \\ u_{xz} \\ u_{xx} \end{bmatrix} \tag{11}$$

The relationship of the duty ratios is the same with case (1). And the duty ratios in equation (11) are obtained as follows:

$$\begin{cases} d_{11}' = k u_{VU}^* (u_{xy} - u_{yz});\ \ d_{12}' = k u_{VU}^* (u_{xz} + u_{yz}) \\ d_{21}' = k u_{VW}^* (u_{xy} - u_{yz});\ d_{22}' = k u_{VW}^* (u_{xz} + u_{yz}) \\ d_{31}' = k u_{VX}^* (u_{xy} - u_{yz});\ \ d_{32}' = k u_{VX}^* (u_{xz} + u_{yz}) \\ d_{41}' = k u_{VY}^* (u_{xy} - u_{yz});\ \ d_{42}' = k u_{VY}^* (u_{xz} + u_{yz}) \\ d_{i0}' = 1 - d_{i1}' - d_{i2}' \ \ (i = 1,\ 2,\ 3,\ 4) \end{cases} \tag{12}$$

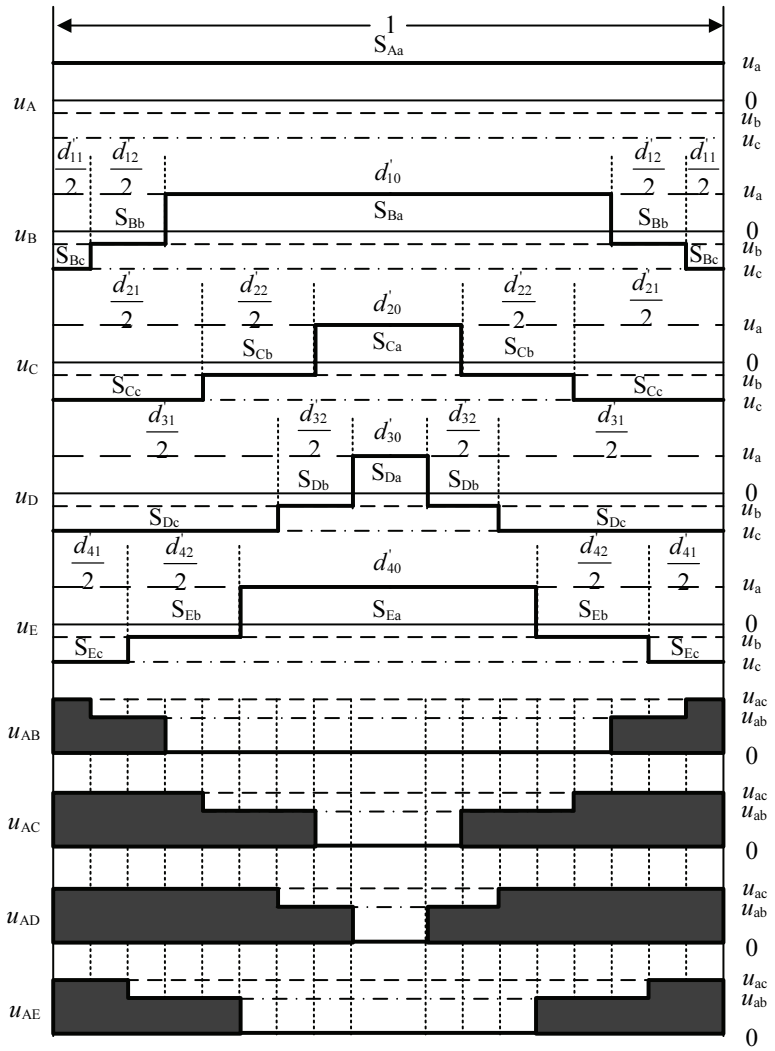



Fig. 4. Switching sequence with output voltage synthesis.

where $k$ is defined in equation (7), and the switch $S_{Vx}$ is selected to be the "source key".

All of the above equations are derived under balanced input voltages. When the input voltages are unbalanced or distorted, it is assumed that the unbalanced or distorted input line voltages are given by $\tilde{u}_{ab}$, $\tilde{u}_{bc}$ and $\tilde{u}_{ac}$. The output voltage $u_{AB}$ is obtained by:

$$u_{AB}=\frac{(\tilde{u}_{ab}-\tilde{u}_{bc})\tilde{u}_{ab}+(\tilde{u}_{ac}+\tilde{u}_{bc})\tilde{u}_{ac}}{\tilde{u}_{ab}^2+\tilde{u}_{bc}^2+\tilde{u}_{ac}^2}u_{AB}^*=u_{AB}^* \tag{13}$$

$u_{AC}=u_{AC}^*$, $u_{AD}=u_{AD}^*$ and $u_{AE}=u_{AE}^*$ can be derived in the same way. Obviously, the control function based on the DLVS can be adjusted by itself under unbalanced or distorted input voltages. Therefore, sinusoidal and symmetrical output waveforms can also be obtained.

The output voltages are composed of input voltages, and the input currents can be synthesized by output currents. Take $i_x$ in case (1) as an example. It can be described as:

$$i_x=i_U+d_{10}^{'}i_V+d_{20}^{'}i_W+d_{30}^{'}i_X+d_{40}^{'}i_Y \tag{14}$$

It can be obtained by equation (10) and (14) as follows:

$$i_x=k(u_{xy}+u_{xz})P_L \tag{15}$$

Where $P_L$ is the five phase load power, which is defined by:

$$P_L=u_Ui_U+u_Vi_V+u_Wi_W+u_Xi_X+u_Yi_Y \tag{16}$$

It can be seen from equation (15) that when the input voltages are symmetrical, the input current $i_x$ is equal to $3ku_xP_L$, the input current is proportional to the input voltage and there is no phase difference between them. In addition, the unity input power factor can be achieved, and the input currents are distorted when the input voltages are unbalanced or distorted.

## III. Suppression of Common Mode Voltage by the Improved Strategy

The common mode voltage (CMV) is the zero sequence component of the output voltages. The output voltages are high frequency pulse waves. As a result, the CMV is also a high frequency pulse wave. The CMV $u_{Ng}$ is the voltage

TABLE I
VALUES OF THE CMV UNDER DIFFERENT SWITCHING STATES

| Values of $u_{Ng}$ | Ranges of $u_{Ng}$ | $\lvert u_{Ng} \rvert_{max}$ |
|---|---|---|
| $(u_a+4u_b)/5$ | $[-3\sqrt{3}U_{im}/10,\ \sqrt{3}U_{im}/10]$ | $3\sqrt{3}U_{im}/10$ |
| $(u_a+3u_b+u_c)/5$ | $[-\sqrt{3}U_{im}/10,\ 0]$ | $\sqrt{3}U_{im}/10$ |
| $(u_a+2u_b+2u_c)/5$ | $[-0.2U_{im},\ -\sqrt{3}U_{im}/10]$ | $0.2U_{im}$ |
| $(u_a+u_b+3u_c)/5$ | $[-\sqrt{3}U_{im}/5,\ 0]$ | $\sqrt{3}U_{im}/5$ |
| $(u_a+4u_c)/5$ | $[-3\sqrt{3}U_{im}/10,\ \sqrt{3}U_{im}/10]$ | $3\sqrt{3}U_{im}/10$ |
| $(2u_a+3u_b)/5$ | $[-\sqrt{3}U_{im}/10,\ \sqrt{3}U_{im}/5]$ | $\sqrt{3}U_{im}/5$ |
| $(2u_a+2u_b+u_c)/5$ | $[0,\ \sqrt{3}U_{im}/10]$ | $\sqrt{3}U_{im}/10$ |
| $(2u_a+u_b+2u_c)/5$ | $[0,\ \sqrt{3}U_{im}/10]$ | $\sqrt{3}U_{im}/10$ |
| $(2u_a+3u_c)/5$ | $[-\sqrt{3}U_{im}/10,\ \sqrt{3}U_{im}/5]$ | $\sqrt{3}U_{im}/5$ |
| $(3u_a+2u_b)/5$ | $[\sqrt{3}U_{im}/10,\ 3\sqrt{3}U_{im}/10]$ | $3\sqrt{3}U_{im}/10$ |
| $(3u_a+u_b+u_c)/5$ | $[\sqrt{3}U_{im}/5,\ 0.4U_{im}]$ | $0.4U_{im}$ |
| $(3u_a+2u_c)/5$ | $[\sqrt{3}U_{im}/10,\ 3\sqrt{3}U_{im}/10]$ | $3\sqrt{3}U_{im}/10$ |
| $(4u_a+u_b)/5$ | $[3\sqrt{3}U_{im}/10,\ 0.7211U_{im}]$ | $0.7211U_{im}$ |
| $(4u_a+u_c)/5$ | $[3\sqrt{3}U_{im}/10,\ 0.7211U_{im}]$ | $0.7211U_{im}$ |
| $u_a$ | $[\sqrt{3}U_{im}/2,\ U_{im}]$ | $U_{im}$ |

between the load neutral point and the ground as shown in Fig. 1. The circuit equation of the output side can be expressed as:

$$\begin{cases} u_{Ag}-u_{Ng}=Ri_A+Ldi_A/dt \\ u_{Bg}-u_{Ng}=Ri_B+Ldi_B/dt \\ u_{Cg}-u_{Ng}=Ri_C+Ldi_C/dt \\ u_{Dg}-u_{Ng}=Ri_D+Ldi_D/dt \\ u_{Eg}-u_{Ng}=Ri_E+Ldi_E/dt \end{cases} \tag{17}$$

Since the five phase output currents are symmetrical, namely $i_A+i_B+i_C+i_D+i_E=0$, $u_{Ng}$ can be derived by equation (17) as follows:

$$u_{Ng}=\frac{u_{Ag}+u_{Bg}+u_{Cg}+u_{Dg}+u_{Eg}}{5} \tag{18}$$

Take the input voltage in segment 1 and the output voltage in segment Ⅰ as an example, and assume that the input voltages are balanced. There are many possible switching states. However, the values of $u_{Ng}$ may be the same. Take $S_{Aa}$, $S_{Bb}$, $S_{Cb}$, $S_{Dc}$, $S_{Ec}$ switch on and $S_{Aa}$, $S_{Bc}$, $S_{Cc}$, $S_{Db}$, $S_{Eb}$ switch on as an example, $u_{Ng}$ is equals to $(u_a+2u_b+2u_c)/5$ under the two switching states. On this basis, the values of the CMV under different switching states are listed in Table Ⅰ.

TABLE II
SIMULATION PARAMETERS

| | |
|---|---|
| Root mean square (RMS) of input phase voltage | 100V |
| Input frequency | 50Hz |
| Input filter | $R_f$=0.5Ω, $L_f$=1mH, $C_f$=20μF |
| Five-phase R-L load | $R$=16Ω, $L$=12mH |
| Switching frequency | 10kHz |
| Root mean square (RMS) of output phase voltage | 70V |
| Output frequency | 20Hz |

As can be seen from table I, the absolute value of $u_{Ng}$ reaches its maximum when the output phases all connected to the input phase a, and the output line voltages are all 0. In fact, the output line voltages can achieve 0 as long as the output phases all connected to the same input phase. In order to reduce the CMV, when the five phase output line voltages are all 0 in a switching cycle, the five output phases can be connected to the input phase which possesses the minimum absolute value in the three input phases.

In this improved strategy, the action of the switches remain unchanged as described in the last paragraph of part Ⅱ. C. (1), except that when the output line voltages should all be 0, and the concept of the "source key" disappears in this duration. By the improved strategy, the maximum value of the CMV can be effectively reduced to approximately 72% of the input phase voltage amplitude without affecting the quality of output. However, at the same time, the switching losses increase slightly due to the increase of switching times.

## IV. SIMULATION AND EXPERIMENTAL RESULTS

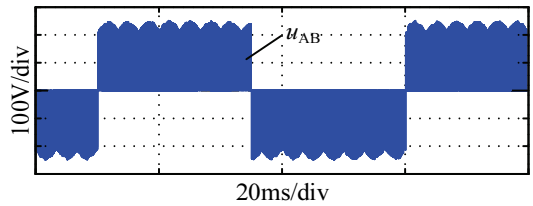
### *A. Simulation Results*

In order to verify the feasibility of the proposed DLVS strategy, a simulation of a three-to-five phase DMC based on Matlab/Simulink and S-function was carried out. The simulation analysis is divided into the following two cases.

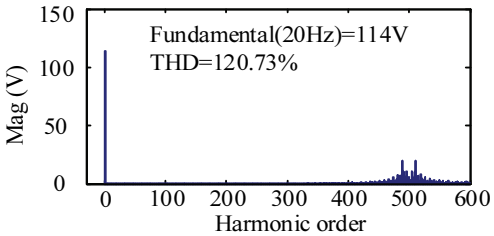
#### *1) Balanced Input Voltages*

The parameters of the simulation model are listed in Table II.

The simulation results under balanced input voltages are shown in Figs. 5-8. Fig. 5 shows the waveform of the adjacent line-to-line voltage $u_{AB}$ in (a), and its harmonics analysis in (b). It can be observed that the THD of the output line-to-line voltage is 120.73%. It can also be seen that it contains very little lower order harmonics, and that the higher harmonics with a larger amplitude are mainly concentrated near the switching frequency. In Fig. 6, the output five-phase currents are sinusoidal and symmetrical. This indicates that the fundamental output voltages are sinusoidal and symmetrical. Waveforms of $u_{Ng}$ with the two strategies are




(a) Waveform of $u_{AB}$.




(b) Harmonics analysis of $u_{AB}$.

Fig. 5. Output adjacent line-to-line voltage $u_{AB}$ under balanced input voltages and its harmonics analysis.

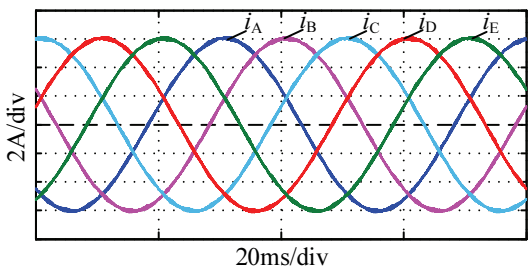
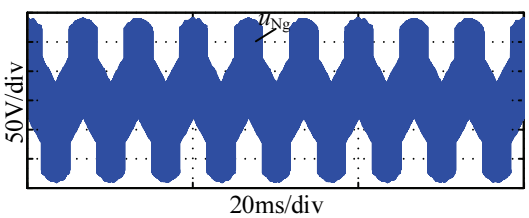
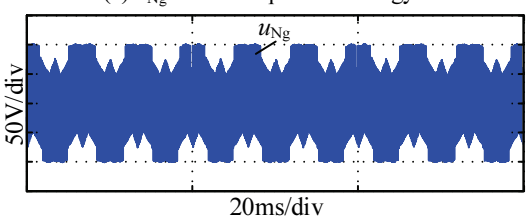



Fig. 6. Output phase currents under balanced input voltages.




(a) $u_{Ng}$ with unimproved strategy.




(b) $u_{Ng}$ with improved strategy.

Fig. 7. Waveforms of $u_{Ng}$ with the two strategies under balanced input voltages.

shown in Fig. 7. The frequency of $u_{Ng}$ is three times of the input frequency. The peak value of $u_{Ng}$ with the unimproved strategy in (a) is about 140V, which is approximately equal to the amplitude of the input phase voltage. However, peak value of $u_{Ng}$ with the improved strategy in (b) is about 100V, which is approximately 72% of the amplitude of the input phase voltage.

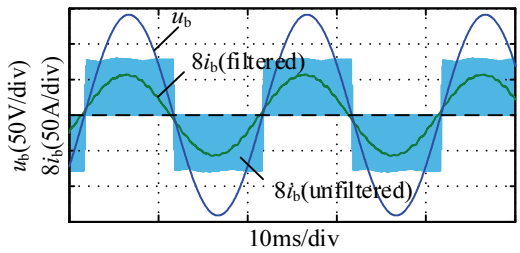



Fig. 8. Input phase voltage and current under balanced input voltages.

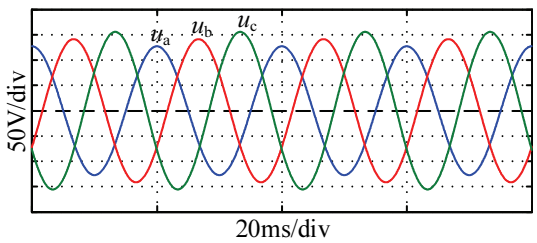
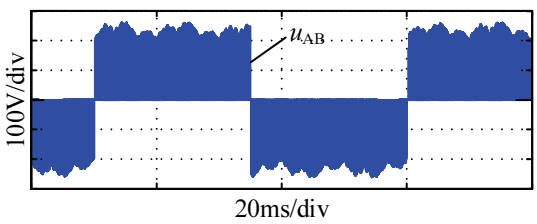
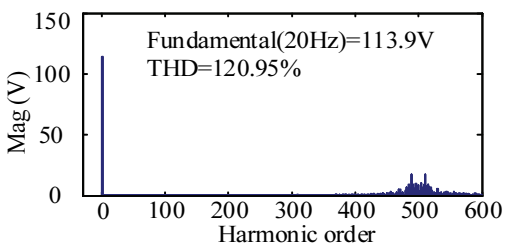



Fig. 9. Unbalanced input voltages.




(a) Waveform of $u_{AB}$.




(b) Harmonics analysis of $u_{AB}$.

Fig. 10. Output adjacent line-to-line voltage $u_{AB}$ under unbalanced input voltages and its harmonics analysis.

As shown in Fig. 8, the unfiltered input current is a pulse wave, and there is no angle difference between the input voltage and the unfiltered input current. However, the input filter causes a displacement angle between the input voltage and the filtered current. Despite this, the input power factor is close to the unity power factor.

*2) Unbalanced or Distorted Input Voltages*

The simulation parameters are the same as those in Table II except that the input voltages are unbalanced, and the RMS of the three phase input voltages are 90V/100V/110V, as shown in Fig. 9. The output results in Figs. 10-11 are similar to those under balanced input voltages. The shape of $u_{AB}$ is irregular in Fig. 10(a) compared with that in Fig. 5(a).

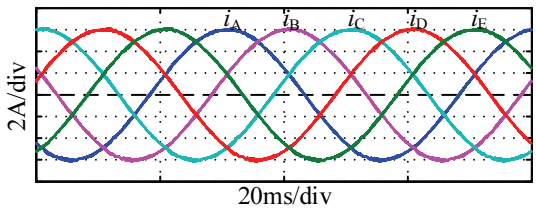
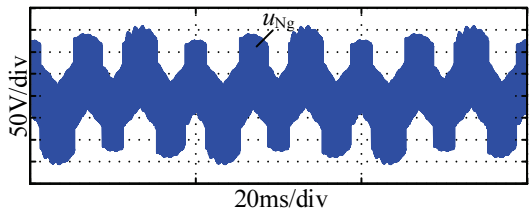
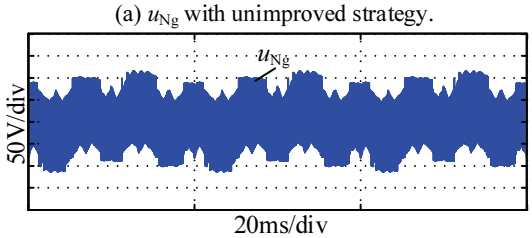



Fig. 11. Output phase currents under unbalanced input voltages.




(a) $u_{Ng}$ with unimproved strategy.




(b) $u_{Ng}$ with improved strategy.

Fig. 12. Waveforms of $u_{Ng}$ with the two strategies under unbalanced input voltages.

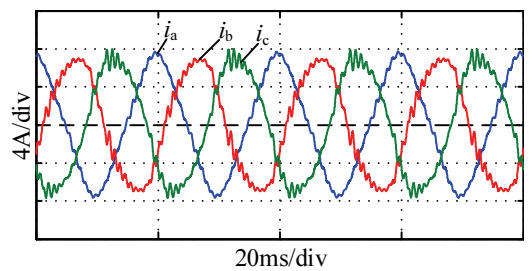



Fig. 13. Input currents under unbalanced input voltages.

However, the harmonics analysis shows that the output voltages hardly contains any lower order harmonics, and that the fundamental amplitudes are almost equal in the two cases. The output five-phase currents show that the output is still sinusoidal and symmetrical. The waveforms of $u_{Ng}$ in Fig. 12 are not as regular as those in Fig. 7 because of the unbalanced input voltages. However, the relations are the same. The maximum value of $u_{Ng}$ with the unimproved strategy reaches the maximum value of the input phase voltage, and improved strategy can reduce it to 72% of the maximum value. Since the MC does not have an energy dissipating element, and the converter loss is ignored, the average output power and input power are equal. Thus, the input three-phase currents are abnormal as shown in Fig. 13 because of the unbalanced or distorted input voltages. In addition, due to the unbalanced input voltages, there is a displacement angle between the input voltage and unfiltered input current in Fig. 14.

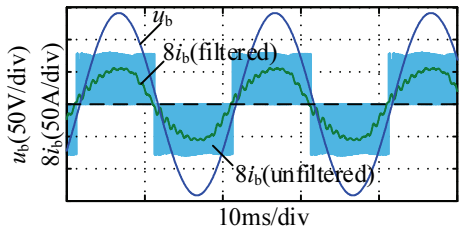



Fig. 14. Input phase voltage and current under unbalanced input voltages.

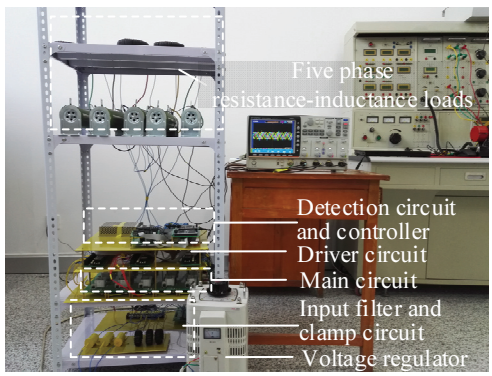



Fig. 15. Three-to-five phase DMC prototype.

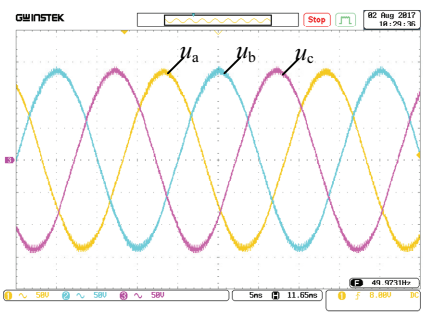
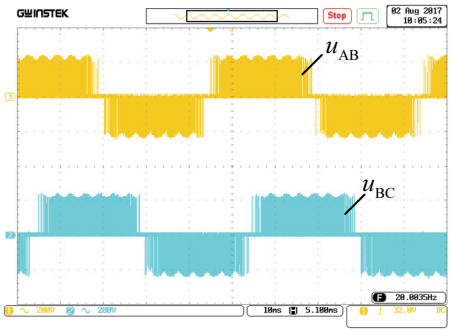


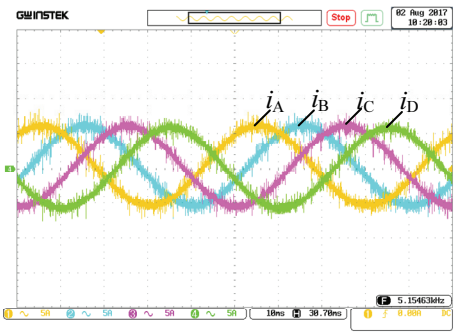

Fig. 16. Three phase balanced input voltages.

## B. *Experimental Results*

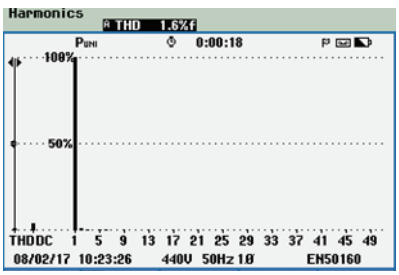
An experimental prototype of three-to-five phase DMC based on a DSP (TMS320F28335) and a FPGA (XC6SLX9) was implemented to verify the feasibility of the proposed DLVS strategy, as shown in Fig. 15. The input of the experimental prototype was connected to the power grid through a voltage regulator, and an input R-L-C filter was adopted to suppress the switching harmonics. The function of clamp circuit fitted between the input and the output is to protect the matrix converter against the overcurrent and overvoltage that occur on both sides of the converter. Each of the bidirectional switches of the main circuit is constituted by two MOSFETs and diodes, and the driving voltages of the switches supplied by the driver circuit are isolated from each other. The controller consists of two parts, a DSP for the proposed DLVS strategy and a FPGA for the switch commutation. The parameters of the experimental prototype are the same as those of the simulation.



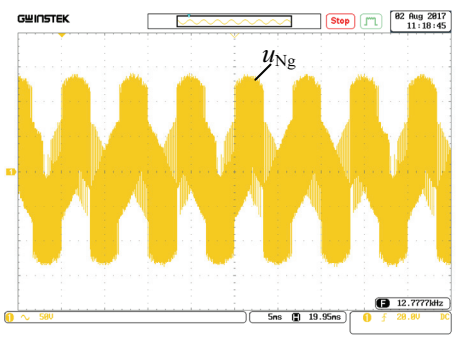

(a) Output adjacent line-to-line voltage.



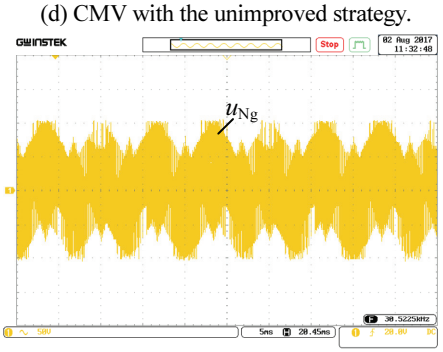

(b) Output phase currents.



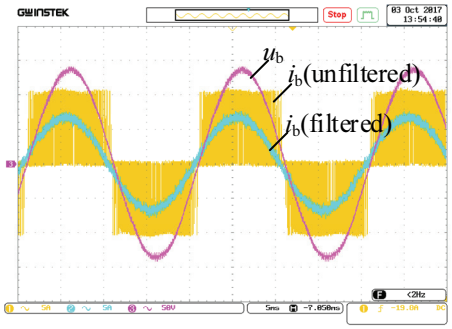

(c) Harmonics analysis of $i_A$.




(d) CMV with the unimproved strategy.




(e) CMV with the improved strategy.




(f) Input phase voltage and current.

Fig. 17. Experimental results under balanced input voltages.

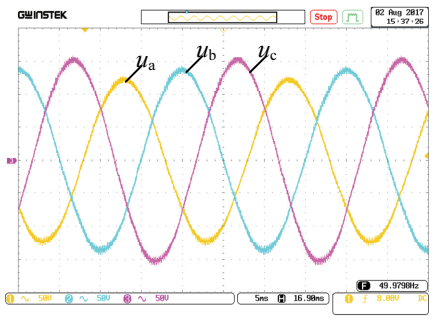
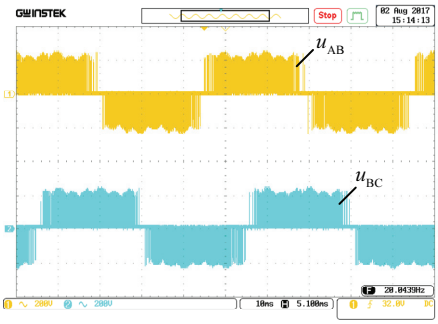



Fig. 18. Three phase unbalanced input voltages.

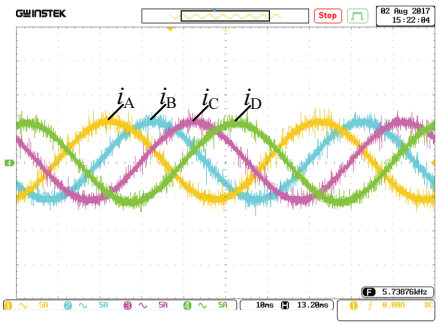
Three phase balanced input voltages are shown in Fig. 16, and the RMS of each phase is 100V. Fig. 17 shows experimental results under balanced input voltages. The output waveforms of the adjacent line-to-line voltages are shown in Fig. 17(a). As can be seen, the output voltages are high frequency pulse waves. It can also be observed that sinusoidal and symmetrical output currents are achieved under balanced input voltages from Fig. 17(b). In addition, the harmonics analysis of the phase current in Fig. 17(c) shows that there are little lower order harmonics and that the value of the THD is very small, which meets the expectations. The waveforms of the common mode voltage in Fig. 17(d) and Fig. 17(e) are in accordance with those of the simulation. The maximum value of the CMV can be reduced to 72% with the improved strategy. Fig. 17(f) presents the input phase voltage and current under balanced input voltages, phase angle of unfiltered input current is same as that of input voltage. The filtered input phase current is sinusoidal with very little distortion, and the current leads the voltage by a little displacement angle caused by the capacitive filter.

Three phase unbalanced input voltages are shown in Fig. 18. The RMS of each phase is 90V/100V/110V. Figs. 19-20 show experimental results under unbalanced input voltages, where Fig. 19 shows results with the proposed DLVS strategy, and Fig. 20 shows results with the conventional SVPWM strategy.

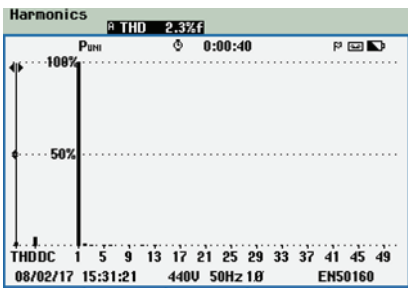
Similar output results are achieved under unbalanced input voltages with the proposed DLVS strategy, as shown in Fig. 19. As displayed in Fig. 19(a), the waveform of the



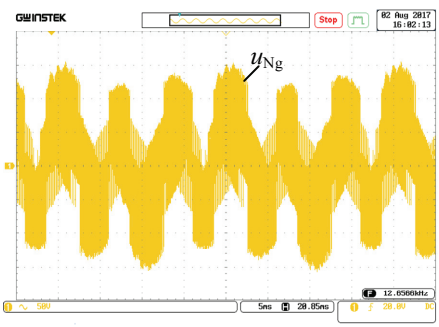

(a) Output adjacent line-to-line voltage.



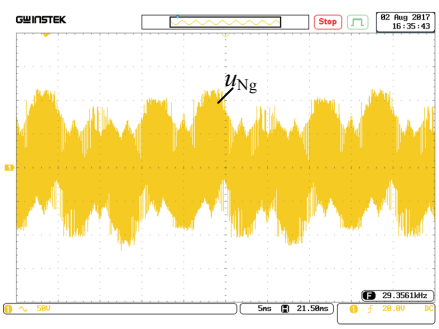

(b) Output phase currents.



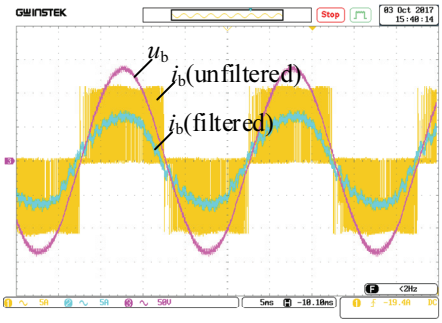

(c) Harmonics analysis of $i_A$.




(d) CMV with the unimproved strategy.

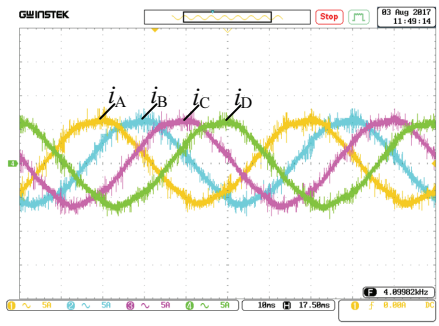



(e) CMV with the improved strategy.

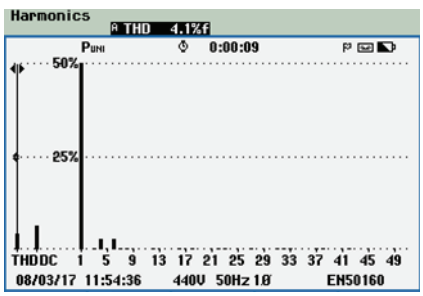



(f) Input phase voltage and current.

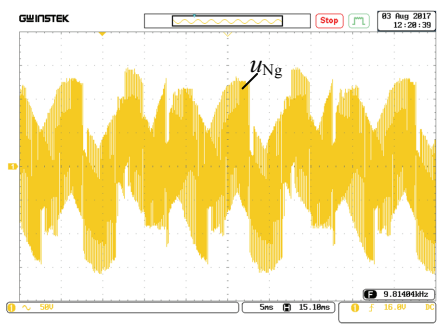
Fig. 19. Experimental results under unbalanced input voltages.




(a) Output phase currents.




(b) Harmonics analysis of $i_A$.




(c) CMV with the SVPWM strategy.

Fig. 20. Experimental results under unbalanced input voltages with the SVPWM strategy.

output adjacent line-to-line voltage is a little different from that under balanced input voltages because of the unbalanced input voltages. However, the output phase currents are still sinusoidal and symmetrical in Fig. 19(b), and the harmonics distributions are similar. It can be seen that unbalanced or

distorted input conditions do not deteriorate the quality of the output. Waveforms of common mode voltage are also similar to those of the simulation. The maximum absolute values of the CMV under the two strategies are about 155V and 110V, respectively. Fig. 19(f) gives the input phase voltage and current under unbalanced input voltages. There is also a displacement angle, and the distortion of the input current under unbalanced input voltages is worse due to the unbalanced input voltages.

Furthermore, an experiment was conducted with the conventional SVPWM strategy under unbalanced input voltages. Fig. 20(a) and Fig. 20(b) clearly show that the output phase currents are no longer sinusoidal, and there are low-order harmonics in the waveform. The output waveforms are heavily distorted when the degree of unbalance increases. The shape of the CMV in Fig. 20(c) is different from that under the proposed DLVS strategy. However, the maximum absolute value of the CMV is about 155V, which is equal to the maximum value under the unimproved DLVS strategy proposed in this paper.

The experiment results matched expectations and they are consistent with the theoretical analysis and simulation.

## V. Conclusion

In this paper, a DLVS strategy is proposed that is suitable for the three-to-five phase DMC. In order to gain the maximum VTR, two larger input line voltages should be selected for synthesis. The duty ratios are calculated by the input voltages and the expected output voltages. The calculating process is very simple. Moreover, in order to reduce the number of switchings within one sampling period, the source key is selected reasonably in each of the input and output intervals. The feasibility and validity of the proposed method were verified by means of computer simulations and experiments. The results of the simulations and experiments all show that both the output voltages and the input currents can be effectively modulated when the input voltages are sinusoidal and symmetrical. In addition, the output voltages and currents are still sinusoidal and symmetrical with little lower order harmonics under unbalanced or distorted input voltages, desirable output can be achieved under different input conditions, and the CMV can be effectively reduced by rearranging some of the switch states at the price of the switching loss slightly increasing.

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