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Compact Wireless IPT System Using a Modified Voltage-fed Multi-resonant Class EF_2 Inverter

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Abstract

Wireless inductive power transfer (IPT) technology is used in many applications today. A compact and high-frequency primary side inverter is one of the most important parts of a WPT system. In this study, a modified class EF-type voltage-fed multi-resonant inverter has been proposed for WPT application at a frequency range of 85–100 kHz. Instead of an infinite input choke inductor, a resonant inductor is used to reduce loss and power density. The peak voltage stress across the MOSFET has been reduced to almost 60% from a class-E inverter using a passive clamping circuit. A simple yet effective design procedure has been presented to calculate the various component values of the proposed inverter. The overall system is simulated using MATLAB/SimPowerSystem to verify the theoretical concepts. A 500-W prototype was built and tested to validate the simulated results. The inverter exhibited 90% efficiency at nearly perfect alignment condition, and efficiency reduced gradually with the misalignment of WPT coils. The proposed inverter maintains zero-voltage switching (ZVS) during considerable load changes and possesses all the inherent advantages of class E-type inverters.

Key words: Class E inverter, Class EF inverter, High-frequency inverter, Inductive power transfer, Misalignment tolerance

I. INTRODUCTION

Wireless power transfer (WPT) is an emerging research area that shows great potential to redefine the way electrical power is consumed by communities. Among the various types of WPT methods, inductive power transfer (IPT) or resonance inductive power transfer (RIPT) has gained increasing popularity and research attention over the last decade. Studies in the implementation of IPT systems on various applications, ranging from low-power level (1 W) to medium-power level (> 1 kW), have been increasing.

Biomedical devices and sensors, electric appliances, portable devices, automotive assembly lines, clean factories, industrial automation applications, and electric vehicle (EV) charging are the most attractive application areas, considering the aforementioned power levels. Some of these applications operate at relatively higher frequency (>500 kHz to several MHz) and shorter distance (up to 3 cm), whereas others operate at a lower frequency (<200 kHz) and greater distance (10–30 cm) [1], [2].

In a typical IPT/WPT system, a high-frequency inverter delivers high-frequency, time-varying voltage/current to a primary coil, which induces a time-varying magnetic field. This magnetic field travels over a distance to energize a secondary coil to transfer power. Subsequently, the induced secondary voltage is conditioned to deliver power to a specific load or battery charger of an EV. High-resonance frequency is required to enhance the range and power transfer capability of the induced secondary voltage [3], [4]. Thus, a primary inverter that can deliver maximum power at a higher operating frequency plays a vital role in an IPT system.

Several primary inverter topologies have been described in the current literature. Full-bridge-series LC resonant (SLC) and series-parallel resonant (LCL) topologies [5]-[11] are primarily used in applications in which the required power level is 1 kW or higher. However, a single-switch class-E resonant inverter can also meet the requirements of the WPT system because of its capability to deliver medium power (1–

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3 kW) at higher switching frequencies [3], [12], [13]. This inverter also has a simple topology with lower component count and timing control, and requires a relatively simple gated drive because of the absence of high- and low-side complimentary switches.

Thus, a passive resonant network can be added parallel to the load network to reduce the high switching stress of a class E inverter. This type of modified class E inverter is referred to as Class EF (class E/F) inverter [14], [15]. Voltage stress in this family of inverters is reduced to 40% from class E. The performance and power output capability of this inverter are also higher. Voltage stress could be reduced further by placing a passive resonant circuit between the finite DC-feed inductor and the semiconductor switch. These types of inverters are referred to as class Φ inverter in the literature [14]. These two families of inverters have demonstrated potentiality for various IPT applications. In the contemporary literature, detailed designs of these types of inverters are confined to the frequency range between 800 kHz and 13.6 MHz, although some WPT applications operate on a 20 kHz–100 kHz frequency range [15], [16]. Therefore, a clear scope for the performance evaluation of these types of inverters under above-frequency constraint exists. In this study, a modified class EF_2 voltage-fed multi-resonant single switch inverter topology has been proposed for IPT applications. A medium-frequency (85–100 kHz) region with practical IPT coil parameters is used to evaluate the performance and effectiveness of the inverter. The proposed inverter has all the advantages of a class E inverter. The contributions of this paper can be summarized as follows:

1. Design and analysis of a modified class EF_2 inverter for WPT EV charging system. A 500-W experimental prototype that exhibits 90% efficiency at nearly perfect aligned condition has been built.
2. Considerable reduction of peak voltage stress across semiconductor devices has been achieved.
3. A simple design procedure has been introduced to calculate the various component parameters of the inverter for a pre-built WPT coil.

This rest of this paper is organized as follows. Section II discusses the working principle, pros, and cons of a current-fed class E resonant inverter. Section III describes the proposed voltage-fed multi-resonant class EF_2 inverter, and discusses the design procedure of the proposed inverter for IPT application and simulation model. Sections IV and V contain the discussion of simulation and experimental results, respectively. Finally, Section VI concludes the paper.

II. Current-fed Class E Resonant Inverter

Figs. 1 and 2 show the current-fed class E resonant inverter topology and operating waveform during nominal condition.

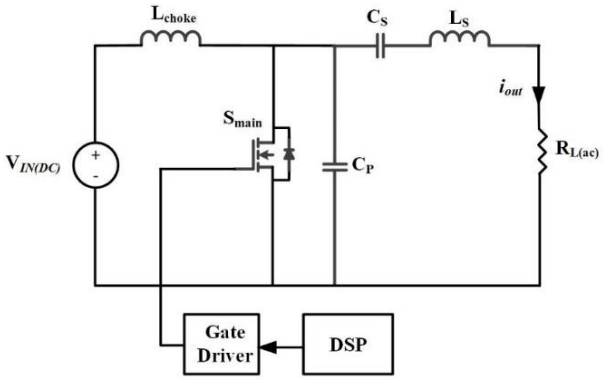


Fig. 1. Current-fed class E inverter.

This inverter was first introduced by Sokal [16]. A conventional current-fed class E inverter (Fig. 1) usually consists of a dc-supply $V_{IN(DC)}$, an input choke (dc-feed) inductance, L_{choke}, power MOSFET, which is used as a switching device, a shunt capacitor, C_P, and load circuit (combination of series-resonant circuit L_S-C_S and ac load resistance, R_L).

During nominal operation, the class E inverter maintains zero-voltage switching (ZVS) and zero-derivative switching (ZDS) simultaneously. Thus, high-power conversion at higher frequencies is achieved. Switching loss was also reduced significantly because of zero-voltage and jumpless current at a turn-on instance. The ZVS/ZDS condition is expressed in Equation (1):

$$v_{DS(2\pi D)} = 0 \text{ and } \frac{dv_S}{d(\omega t)}(\omega t) = 0, \quad (1)$$

where ωt = 2πD. These conditions are referred to as "nominal condition" for class E inverter operation. In case of maximum power conversion efficiency, conduction losses for ESR components and switch-on/off time resistance must be considered. This operating condition, including ESR, is referred to as "optimal condition." Fig. 2 shows the nominal operating waveforms of a class E inverter when D = 0.5 (duty cycle). The difference of currents through the dc-feed inductance (or choke inductance), L_{choke}, and resonant network (L_S–C_S) flows through the capacitor C_P during a switch turn-off interval. The selected operating frequency is greater than the resonant frequency of L_S–C_S but less than the resonant frequency of L_S–C_S–C_P. Furthermore, the output resonant circuit of a class E inverter usually has a high-quality factor Q. Thus, load current i_{out} is regarded as a sinusoid.

Class E inverters have a smaller component count, simple gate drive configuration, inherent sine-wave voltage/current output, and efficient high-frequency operation because of ZVS/ZDS. ZDS operation reduces Miller effects. Although class E inverters have significant advantages, they are also prone to few severe consequences, such as the peak switch voltage stress across the semiconductor switch. Fig. 2 shows that drain-to-source voltage, V_{DS}, is 3-3.5 times higher

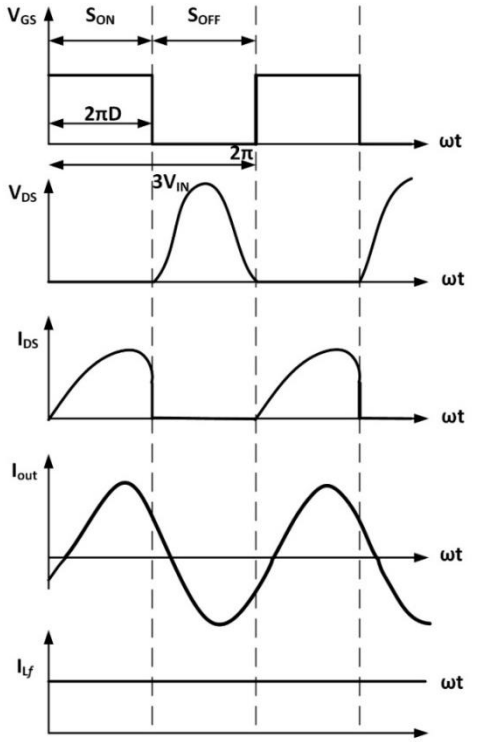


Fig. 2. Nominal operating waveforms of current-fed class E inverter (D = 0.5).

than the input DC voltage. This phenomenon is not desired in high-power and high-frequency conditions. Another major disadvantage of a class E inverter is its high input dc-feed inductor loss because of its bulky size. Thus, core loss and ESR loss are high.

Several topologies have been proposed in the literature to overcome these limitations and increase the efficiency of the inverter at higher frequency ranges (tens of megahertz) [14], [17], [18]. As previously stated, most of the designs of the inverter were concentrated for very high-frequency (MHz) operations. In this study, a new voltage source single-switch multi-resonant inverter topology is introduced. The new inverter can maintain a sine-wave output similar to that of a class E inverter while maintaining a reduced peak switch voltage stress. The new inverter also has a higher power conversion efficiency than the class E inverter. Moreover, the new inverter is suitable for contactless power transfer application ranging from 85–100 kHz. The proposed inverter design focuses on reducing the peak-voltage stress and input inductor loss while maintaining power output capability. In the following sections, a detailed design of this inverter is presented.

III. VOLTAGE-FED MODIFIED CLASS EF_2 RESONANT INVERTER

Fig. 3 shows the proposed inverter topology. The input dc-feed inductance is replaced with a resonant inductance L_R. In a class E inverter, the input dc-feed choke inductance is

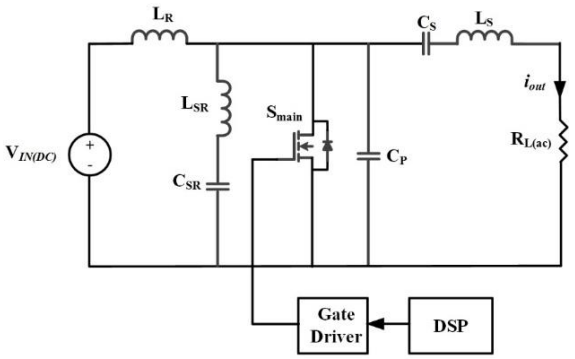


Fig. 3. Proposed voltage-fed multi-resonant class EF_2 inverter.

bulky and produces high losses while operating in a frequency region of 30–100 kHz. This loss has been substantially reduced using a resonant inductor. Thus, the volume and value of the inductor have been reduced because this inductor now resonates with a frequency higher than the switching frequency. Thus, a small core area is required to construct the inductor with less turn, which will result in small magnetic and ESR loss.

Furthermore, a series resonant circuit (L_{SR}–C_{SR}) has been inserted between the input resonance inductor and switch to reduce the peak voltage stress across the switching device. This series resonant circuit is tuned to resonate with the second harmonic of the switching frequency. The extra resonant circuit with selected harmonic elimination is used to reduce the switching stress that has been discussed comprehensively in [14], [17]-[19]. The second harmonic elimination contributes in the reduction of peak switch voltage stress. For a class E current source inverter, the maximum peak voltage across the switch can reach up to 3.5 times the input DC voltage. However, the voltage peak in the proposed multi-resonant inverter is limited to only 2 times of the input DC, which is shown in following sections. This peak switch stress reduction is necessary when high input DC is used (rectified from utility). In case of a conventional class E, when a rectified voltage of 300 V is applied, the peak switch stress will reach up to 1 kV, which is not desirable. However, in case of the proposed inverter, the peak switch stress will reach up to 600 V, which is desirable in the range of the safe operating area (SOA) of the switch. Many commercial semiconductor switches are available for the practical implementation of the inverter.

The components of the inverter are calculated such that the peak voltage amplitude across the switch decreases and maintains the switch-mode operation through near zero-voltage at turn-on and turn-off at a given frequency and duty ratio. Fig. 4 shows a simplified circuit diagram of the proposed inverter.

A. Circuit Operation

When the switch is ON, the current through the MOSFET is given by Equation (2). The total switch current can be

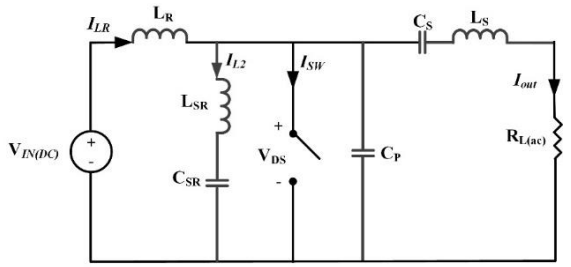


Fig. 4. Circuit diagram of voltage-fed single-switch multi-resonant inverter for analysis.

found by determining i_{L_r}, i_{L_2} , $and\ i_{out}$.

$$i_{sw}(\omega t)_{ON} = i_{L_r}(\omega t)_{ON} - i_{L_2}(\omega t)_{ON} - i_{out}(\omega t)_{ON} \quad (2)$$

The current through the input inductor is the resonant current, which can be defined as Equation (3) for any duty cycle *D*.

$$i_{L_R}(2\pi D) = 2\pi D \frac{V_{IN}}{\omega L_R} + i_{L_R}(2\pi D)_{OFF}. \quad (3)$$

The current through the series-tuned second harmonic termination branch (L_{SR}–C_{SR}) can be found using Equation (4).

$$i_{L_{SR}}(\omega t) = K_1 \cos(4\pi f t) + K_2 \sin(4\pi f t). \quad (4)$$

The coefficients K_1 and K_2 are determined based on the equation boundary conditions. Finally, the output current, i_{out}, can be evaluated as sinusoid using the fundamental harmonic approximation (FHA):

$$i_{out}(\omega t) = I_m \sin(\omega t + \alpha), \quad (5)$$

where I_m is the magnitude of the output current, and "α" is the initial phase between the current and the voltage.

When the switch is OFF, the maximum voltage across the drain to the source port of the MOSFET can be calculated by determining the voltage across the capacitor C_P. The parallel capacitor will charge within an arbitrary time and reach a maximum point. The maximum voltage and shape of the drain to the source voltage, V_{DS}, will depend on the overall drain-to-source (Z_{ds}) characteristic. Fig. 5 shows that the V_{DS} will be a quasi-resonant wave. The current through C_P based on the duty cycle is given by Equation (6).

$$i_{C_P}(\omega t)_{OFF} = i_{L_R}(\omega t)_{OFF} - i_{L_2}(\omega t)_{OFF} - i_{out}(\omega t)_{OFF} \quad (6)$$

During the OFF condition, the current in the L_{SR}–C_{SR} branch can be determined by applying KCL at the drain node

$$i_{L_2}(\omega t)_{OFF} = i_{L_r}(\omega t)_{OFF} - i_{C_P}(\omega t) - i_{out}(\omega t). \quad (7)$$

Equation (8) can be written as:

$$i_{L_2}(\omega t)_{OFF} = i_{L_r}(\omega t)_{OFF} - \omega C_P \frac{dV_{DS}}{d\omega t} - I_m \sin(\omega t + \alpha) \quad (8)$$

The total voltage across the L_{SR}–C_{SR} branch is [14]:

$$V_{DS}(\omega t) = \omega L_{SR} \frac{di_{L_2}(\omega t)}{d\omega t} + \frac{1}{\omega C_{SR}} \int_{2\pi D}^{\delta} i_{L_2}(\omega t) d\omega t + v_{C_{SR}}(2\pi D) \quad (9)$$

The final equation of the current through the L_{SR} – C_{SR} branch can be obtained by differentiating Equation (9) and

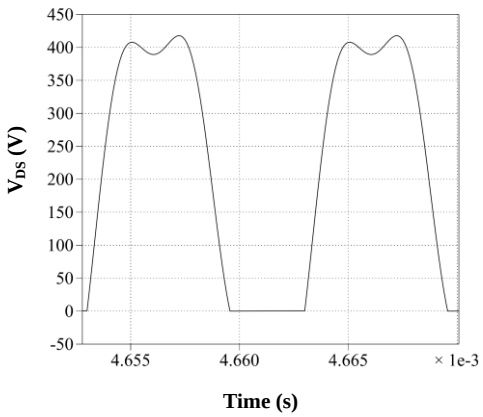


Fig. 5. Simulated drain-to-source voltage of proposed inverter (Input: 200 VDC).

substituting $\frac{dV_{DS}(\omega t)}{d\omega t}$ in Equation (8), as follows:

$$i_{L_2}(\omega t) = 1 - I_m \sin(\omega t + \alpha) - \omega^2 L_{SR} C_P \frac{d^2 i_{L_2}(\omega t)}{d\omega t^2} - \frac{C_P}{C_{SR}} i_{L_2}(\omega t). \quad (10)$$

The general solution of Equation 10, which is a linear, non-homogeneous, differential equation, is the current through the series resonant branch during OFF condition, and can be given as follows:

$$I_{L_2}(\omega t^-) = K_3 \cos(4\pi f t) + K_4 \sin(4\pi f t) - \frac{m_2^2 n}{m_2^2 - 1} \sin(\omega t + \alpha) + \frac{1}{F+1}, \quad (11)$$

where $F = \frac{C_P}{C_{SR}}$, $m_2 = 2\sqrt{\frac{F+1}{F}}$, and $n = \frac{1}{F+1} I_m$.

K_3 and K_4 values can be determined using the boundary conditions of the equation. The voltage and current continuity conditions when switching ON and OFF determine the boundary condition. The current through parallel capacitor can be obtained using Equation (9).

$$I_{C_P}(\omega t)_{OFF} = 2\pi D \frac{V_{IN}}{\omega L_R} - n(F+1) \sin(\omega t + \alpha) - I_{L_2}(\omega t)_{OFF}, \quad (12)$$

The voltage across the C_P, which is the drain-to-source voltage of the MOSFET, is given by Equation (13)

$$V_{DS}(\omega t) = \frac{1}{\omega C_P} \int_{2\pi D}^{\omega t = 2\pi} I_{C_P}(\delta) d\delta, \quad (13)$$

where δ is a constant that indicates the maximum drain-to-source voltage slew rate. Equation (9) can be rewritten by incorporating the ZVS condition as follows:

$$\frac{1}{\omega C_P} \int_{2\pi D^-}^{2\pi} (2\pi D \frac{V_{IN}}{\omega L_R} - n(F+1) \sin(\omega t + \alpha) - K_3 \cos(4\pi f t) + K_4 \sin(4\pi f t) - \frac{m_2^2 n}{m_2^2 - 1} \sin(\omega t + \alpha) + \frac{1}{F+1}) d\delta = 0, \quad (14)$$

MATLAB function "fsolve" can be used to compute the values of unknown variables K_3, K_4, n, and α for the specific values of D, m, and F. This is one method of calculating the various component of the proposed voltage-fed inverter. However, in this study, a different design technique has been implemented to obtain the desired result. (11) shows that V_{DS}

is dependent on m, n, F, and D, and "m" and "n" are dependent on F. Therefore, the values of F have been deduced first. The peak voltage stress of the semiconductor switch is dependent upon the ratio of "F". Furthermore, the values of L_S–C_S can be calculated independently. Thus, the overall new design procedures are described in the following section based on the two aforementioned insights.

B. Derivation of I_m

The switch current can be given as

$$i_{sw}(\omega t) = 1 - n(F+1)\sin(\omega t + \alpha) - K_1\cos(4\pi f t) + K_2\sin(4\pi f t). \quad (15)$$

The average switch current is equal to the DC input current [14]; thus,

$$\frac{1}{2\pi}\int_0^{2\pi} i_{sw}(\omega t)d(\omega t) = 1 = \frac{n}{2\pi}(\cos(2\pi D + \alpha) - \cos\alpha)(F+1) + D - \frac{1}{4\pi f t}(K_1\sin(4\pi f t D) + 2K_2\, sin^2(4\pi f t D)) \quad (16)$$

Solving (16), we have

$$n = \frac{2\pi(1-D) + (K_1\, sin(4\pi f t D) + 2K_2\, sin^2(4\pi f t D)}{(F+1)(\cos(2\pi D + \alpha) - cos\alpha)}. \quad (17)$$

As $n = \frac{1}{F+1} I_m$, substituting (17) into this equation

$$I_m = \frac{2\pi(1-D) + (K_1\, sin(4\pi f t D) + 2K_2\, sin^2(4\pi f t D)}{cos(2\pi D + \alpha) - cos\alpha}. \quad (18)$$

C. Design of Modified Voltage-Fed Class EF_2 Resonant Inverter

Calculation of L_S–C_S and C_P

The values of L_S can be computed according to the specific application requirement. In this work, L_S is the inductance of the primary coil of a loosely coupled transformer. These types of transformers are widely used in WPT application. In the case of WPT system, reflected impedance is also added with L_S.

C_S is calculated such that the resonance frequency of L_S–C_S becomes lower than the switching frequency. A proper selection of this frequency is necessary to maintain the appropriate voltage gain. The combined effect of L_S–C_S contributes to the reduction of switch voltage stress.

The value of C_P is calculated to maintain the ZVS operation of MOSFET. The following criteria must be met while calculating the value of C_P.

$$f_{L_S-C_S} < f_s \leq f_{L_S-(C_S||C_P)}, \quad (19)$$

where f_s, is the switching frequency and $f_{L_S-C_S}$ and $f_{L_S-(C_S||C_P)}$ are given by

$$f_{L_S-C_S} = \frac{1}{2\pi\sqrt{L_S C_S}}$$

and

$$f_{L_S-(C_S||C_P)} = \frac{1}{2\pi\sqrt{L_S C_S C_P/(C_S+C_P)}}. \quad (20)$$

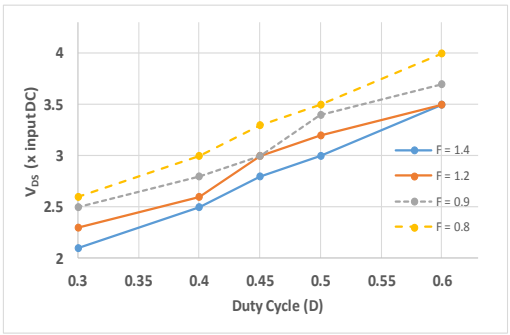


Fig. 6. Duty cycle and V_{DS} for different F values.

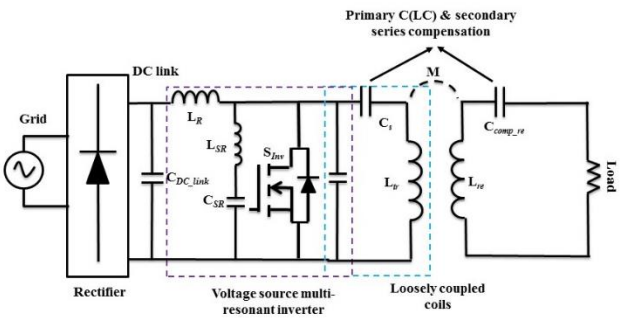


Fig. 7. IPT system configuration schematic with proposed inverter.

After calculating the value of C_P, we determine the value of C_{SR} using the value of F. Different values of F will result in different levels of voltage and current stress on the semiconductor switch. Fig. 6 shows that a family of curves has been given for duty cycle and V_{DS} based on various F. The x-axis represents the duty cycle and y-axis represents the peak switch voltage stress (multiple of input DC voltage). When F values lie between 1.2 and 1.4, V_{DS} decreases within the duty cycle range of 30%-40%. Peak voltage stress increases rapidly with duty cycle when threshold and ZVS cannot be maintained.

Values of L_R, L_{SR}–C_{SR}

When the values of F and C_P are calculated, the value of C_{SR} can be calculated using $F = \frac{C_P}{C_{SR}}$. L_{SR} is calculated such that it resonates with C_{SR} on the second harmonic of the switching frequency. The value of L_{SR} can be calculated using (21). Equation (22) shows that the resonance frequency of L_R and C_P will be slightly higher than the switching frequency. When the value of C_P is determined, L_R is calculated using (22). The resonant frequency of L_R and C_P could work as design criteria of the inverter. This resonant frequency is selected such that the ZVS of the MOSFET can be achieved up to 60% of the load change.

$$L_{SR} = \frac{1}{16\pi^2 f_s^2 C_{SR}} \quad (21)$$

$$f_{L_R-C_P}\left(= \frac{1}{2\pi\sqrt{L_R C_P}}\right) > f_S \quad (22)$$

In summary, the overall design procedure can be described

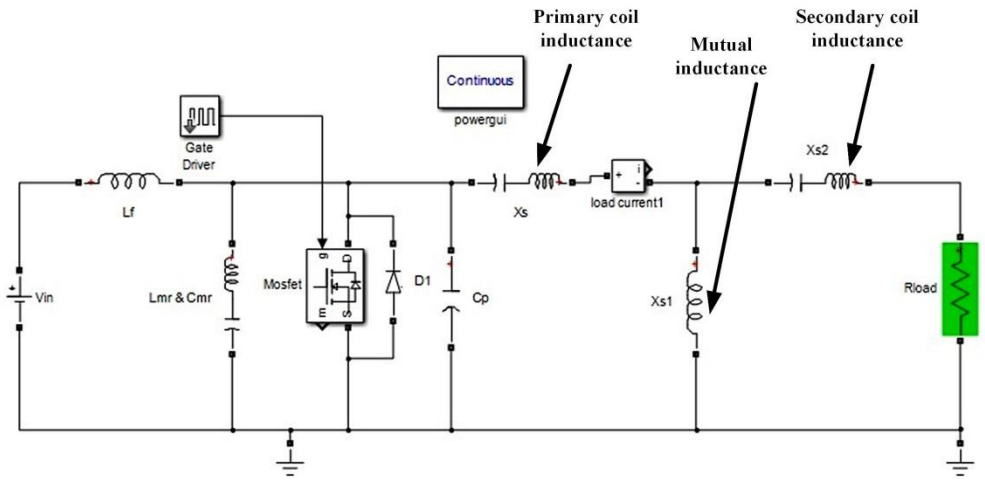


Fig. 8. Simulation model.

as follows:

- L_S is calculated according to the application specification.
- C_S and C_P are determined according to the conditions specified in (19) and (20).
- C_{SR} is calculated based on C_P and F.
- L_{SR} is calculated using (21).
- The value of L_R is calculated based on Equation (22).

D. Simulation Model

A simulation model of the proposed voltage source multi-resonant inverter with a IPT (WPT) system has been built using MATLAB/SimPowerSystem toolbox to verify the design concept.

Figs. 7 and 8 show the schematic of the complete system and the simulation model, respectively. The simulation model is designed to transfer 1 kW power across a vertical gap distance of 8 cm. Primary inductance, secondary inductance, and mutual inductance have been measured using a LCR meter with 8 cm vertical gap and up to 30% horizontal misalignment [20]. Subsequently, these inductances are inserted into the simulation model. The rest of the inverter components are calculated using the method described in the previous section. Fig. 7 shows that the primary or transmitter side forms a *capacitor-inductor-capacitor (CLC)* compensation. Series compensation has been used in the secondary or vehicle side of the system.

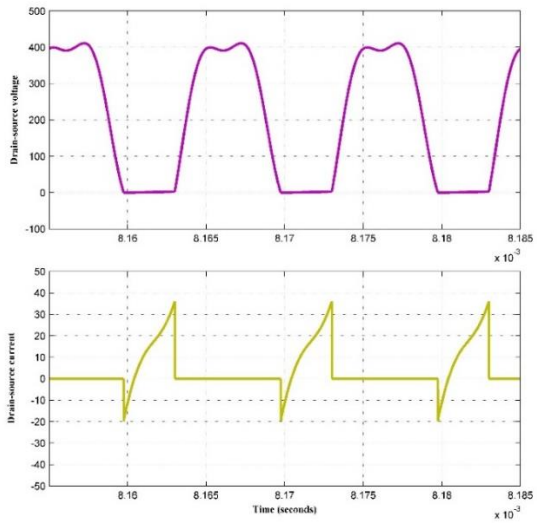
The value of C_S is obtained by setting the resonance frequency of L_S–C_S to 95 kHz according to (12). The switching frequency in this study is selected as 100 kHz. C_P is obtained again using (12). The curve in Fig. 6 shows that the selected "F" value ranges from 1.4–1.5. Then, C_{SR} is calculated according to (8), and other component values have been solved using consecutive steps that are described in the previous section. The duty cycle has been maintained at 30% all the time, according to Fig. 6. The values of L_R, C_{SR}, C_P, and C_S have been changed for further tuning during the simulation to obtain the final inverter model. The inverter maintains ZVS even in considerable load changes (60%) and provides good power output with reduced switch voltage stress. The peak voltage stress is reduced considerably compared with other single-switch inverters [3], [14], [15]. The simulation result shows that the peak voltage only reaches up to 2 times the input DC voltage. However, for other single-switch inverters, this peak voltage stress increases up to 2.5–3.5 times with the same output power transfer capability. Besides, the proposed inverter has all the inherent advantages of a class E-type inverter. Table I shows the final component values of the simulated model.

TABLE I
SIMULATION PARAMETERS

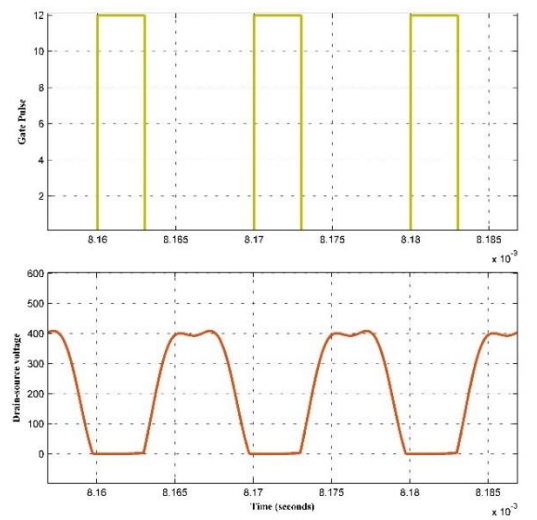
Components	Values
L_R	15 µH
L_{SR}	6.5 µH
C_{SR}	100 nF
C_S	26 nF
C_P	146 nF
Inductance of primary coil of IPT system, L_S	100.38 µH
Inductance of secondary coil of IPT system	103.77 µH
Secondary side compensation capacitor	24.5 nF
Mutual inductance	14.85 µH
Load resistance	25 Ω
Duty cycle	30%
$f_{L_S-C_S}$	98.517 kHz
$f_{L_R-C_P}$	107.55 kHz
$f_{L_S-(C_S\|\|C_P)}$	107.1 kHz

IV. SIMULATION RESULT AND DISCUSSION

Fig. 9(a) shows the drain-source voltage (V_{DS}) and the current (I_{DS}) waveform of the proposed inverter. V_{DS} has



(a)

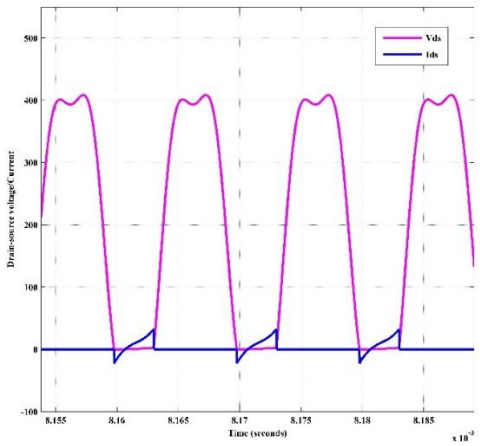


(b)

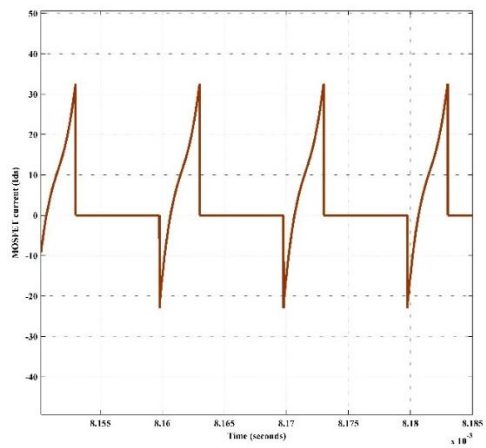
Fig. 9. (a) V_{DS} and I_{DS} at full load (DC Input: 200V) (b) V_{GS} and V_{DS}

maintained ZVS/ZDS at turn-on and provided less peak stress, as calculated theoretically using Figure (6). Given 200 V DC input voltage, the peak stress across the switch is 400 V. However, I_{DS} is slightly higher in the simulation because of the simulation method used in the Simulink/SimPowerSystem toolbox. This problem may be solved by developing a custom component model of inductor and capacitor. However, this problem is beyond the scope of this work. Thus, existing component models have been used.

Fig. 10 shows that this inverter exhibits good operating characteristics during considerable load changes. DC equivalent ac resistance is used for practical and simulation purposes to observe the load voltage and current. Fig. 11(a) shows load voltage and current waveforms. Voltage and current are in phase and resonance, indicating efficient power transfer. Fig. 11(b) shows that drain-to-source impedance (Z_{DS}) characteristic depicts the magnitude and phase at 100



(a)



(b)

Fig. 10. (a) V_{DS} and I_{DS} at 40% load change (DC Input: 200V), (b) I_{DS} (magnified).

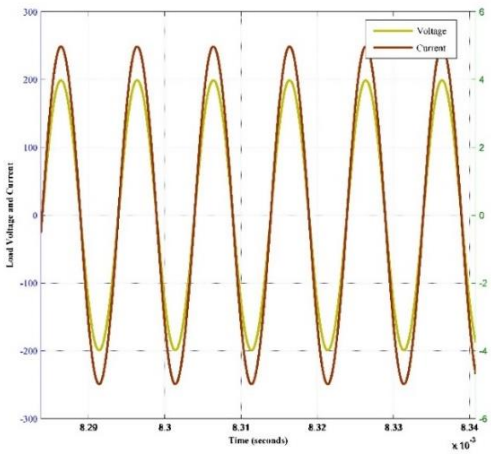
kHz operating frequency. A certain Z_{DS} magnitude and phase must be observed to maintain ZVS and reduce peak switch stress. Fig. 11(b) shows the selected operating point for this design. Some other operating points could also be selected when impedance magnitude and phase are not below 20 Ω and 23°.

Below these limits of impedance magnitude and phase, the proposed inverter could not maintain efficient operation because of hard switching. Fig. 12 shows that the overall system has constant output voltage characteristics with load change.

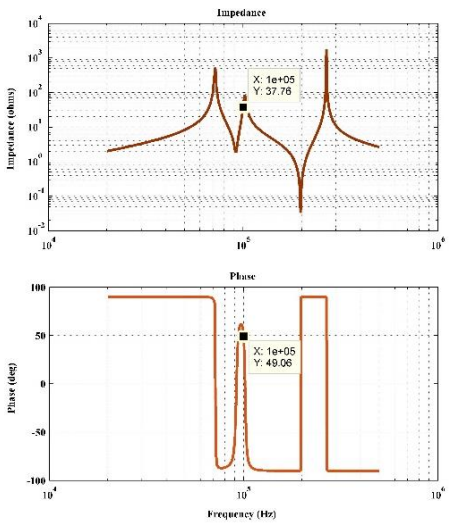
Inverter efficiency is calculated after subtracting the losses of L_R, $L_{SR} - C_{SR}$ branch, switch conduction loss, off time loss, and loss through C_P. This detailed simulation model is used to build the experiment setup. The details of the experimental result and discussion are provided in the next section.

V. EXPERIMENT RESULT AND DISCUSSION

A 500-W experiment setup was built to verify the operation and performance of the proposed voltage source multi-resonant inverter with WPT system, as shown in Fig.



(a)



(b)

Fig. 11. (a) Load voltage and current (b) Drain-source impedance magnitude and phase.

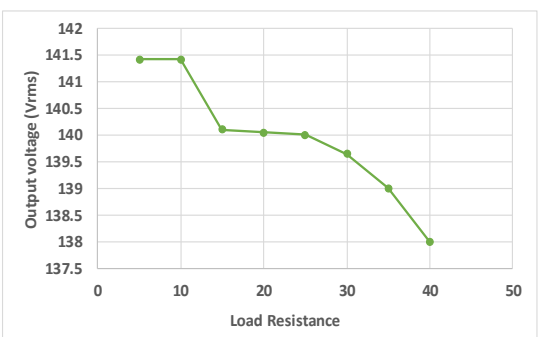
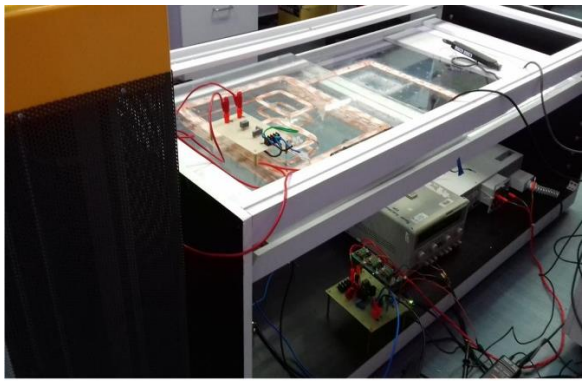
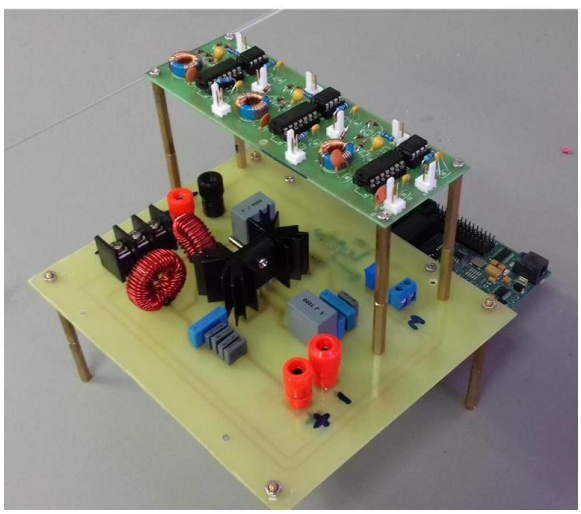


Fig. 12. Output voltage and Load resistance (Input DC: 200V).

13. The specifications of the prototype are listed in Table II. A maximum of 150 W has been transferred to measure the efficiency and other parameters because of limited proper electromagnetic shielding and to maintain the safety of the digital controller. The gate signal was generated using an



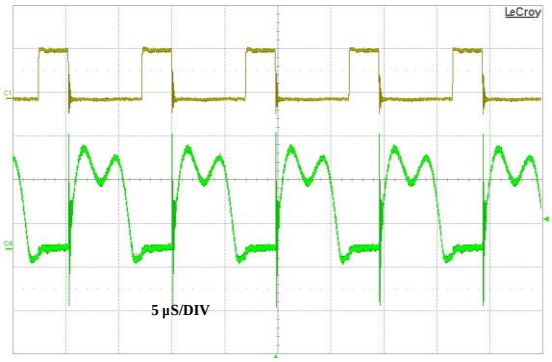
(a)



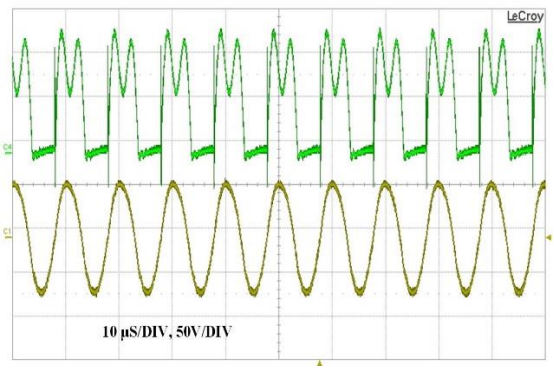
(b)

Fig. 13. (a) Complete experiment setup (b) Proposed single-switch inverter.

ePWM module of Texas Instruments TMS320F28335 digital signal processor. Figs. 14 to 16 show the experimental results. V_{DS} and V_{GS} completely agree with the simulation result. The voltage waveshape and peak stress of the V_{DS} is exactly similar to the designed model. V_{DS} has a spike during turn-off instant because of the mismatch between gate-to-source and gate-driver output impedance. This mismatch can be mitigated by modifying the gate driver circuit design. In the current gate driver, the output impedance is controlled using a fixed resistor. However, the output impedance of the gate drive circuit can be varied to match the gate-source impedance of the MOSFET by introducing a variable resistor. This resistor will eliminate unwanted ringing during turn-of condition, which will reduce the spike of V_{DS}. Primary side voltage and current are not in resonance because of the multi-resonance characteristic in the primary side. Load voltage and current have a small phase shift. This phenomenon occurs because of the out-of-resonance operation of the secondary side and the high leakage magnetic field of the IPT coils, which could be reduced by properly designing the coil. This phase-shift increases and affects the power transfer efficiency during misalignment condition.



(a)



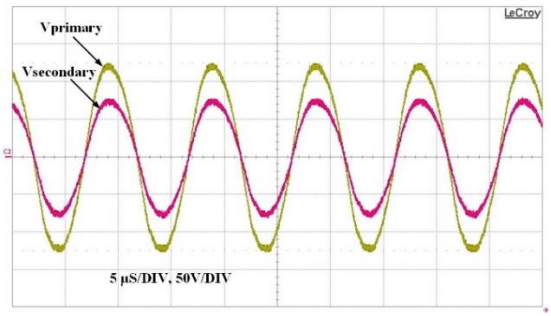
(b)

Fig. 14. (a) V_{GS} and V_{DS} (b) V_{DS} and Load voltage.

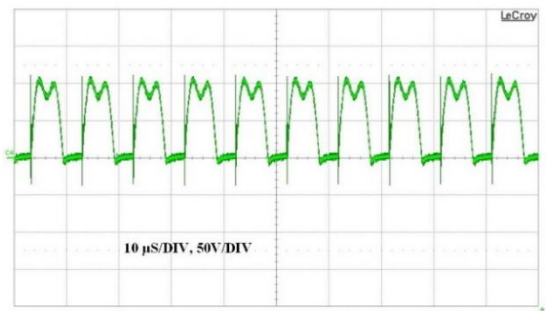
TABLE II
SPECIFICATIONS OF THE PROTOTYPE

Inverter components	Value	Manufacturer
L_R	14 µH – 15 µH	Coilcraft
L_{SR}	6.5 µH	Coilcraft
C_{SR}	98.55 nF (Polypropylene)	KEMET
C_P	146 nF (Polypropylene)	KEMET
C_S	26 nF (Polypropylene)	KEMET
C_{sec_comp}	25.2 nF (Polypropylene)	KEMET
MOSFET	CREE C2M0080120D SiC MOSFET (V_{DS} = 1200 V, I_D = 36 A at 25 ℃	
DSP (for inverter control)	Texas Instruments TMS320F28335 eZDSP board and gate driver circuit	
Coil parameters	$L_{Primary}$	$L_{Secondary}$
	100.38 µH	103.77 µH
Total power	500 W (150 W used in the experiment)	
Input Voltage	100- 130V	

Fig. 15(a) shows that primary and secondary side voltages are in phase, indicating proper magnetic coupling. Fig. 15(b) shows the V_{DS} recorded at 30% misalignment. The peak voltage stress could be maintained at 30% misalignment



(a)



(b)

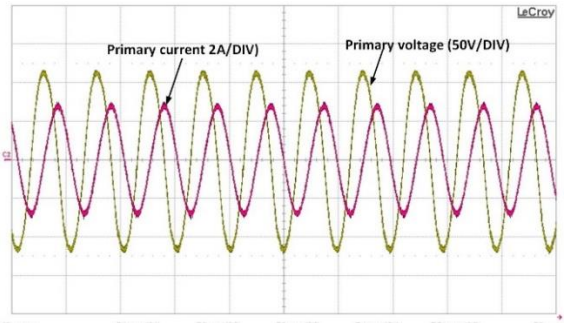
Fig. 15. (a) Primary-side voltage and secondary-side voltage (b) Peak V_{DS} at 30% misalignment condition (input voltage: 50 V DC).

TABLE III
PERFORMANCE EVALUATION OF PROPOSED MODIFIED VOLTAGE-FED MULTI-RESONANT CLASS EF_2 INVERTER WITH CLASS E AND CONVENTIONAL CLASS EF_2 INVERTERS

Parameters	Class E [3, 4, 21]	Class EF_2 [14, 15, 19, 22]	Modified voltage-fed class EF_2
V_{DS} (V) (times input DC)	3.5	2.5	2
Input DC voltage (V)	100–200	100–200	100–350
Output voltage and current waveshape	Sinusoidal	Sinusoidal	Sinusoidal
Misalignment tolerance	-	-	High
Input inductor loss	High	High	Low
Circulating current	-	-	Low
Efficiency	90%	88%	90%±2

condition of IPT coils. This feature is important for primary side inverters used in IPT system.

A performance evaluation of the proposed inverter with two class E and class EF_2 high- frequency resonant inverter topologies, as shown in Table III. In every category, the proposed inverter has demonstrated better operating characteristics. The drain-to-source voltage across MOSFET in the proposed inverter is less than that of the conventional class EF_2 inverter. L_R is a resonant inductor in the proposed topology that reduces losses and size. Thus, the system can be



(a)

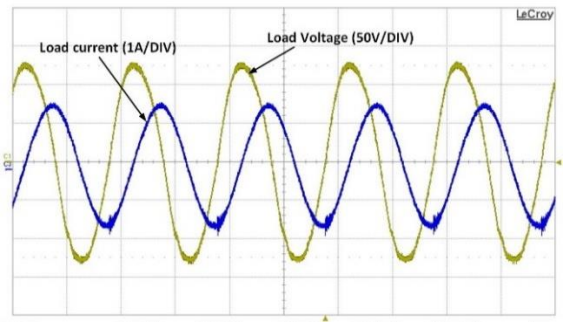


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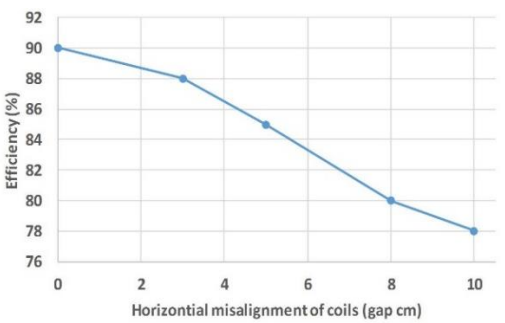
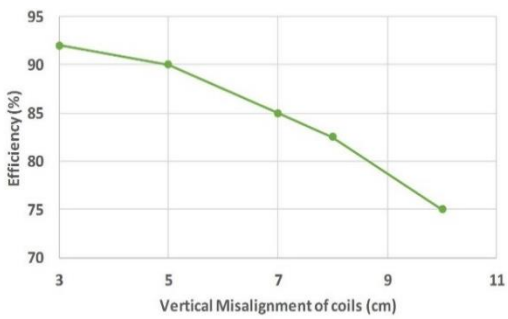
Fig. 16. (a) Primary voltage and current (b) Secondary voltage and current.



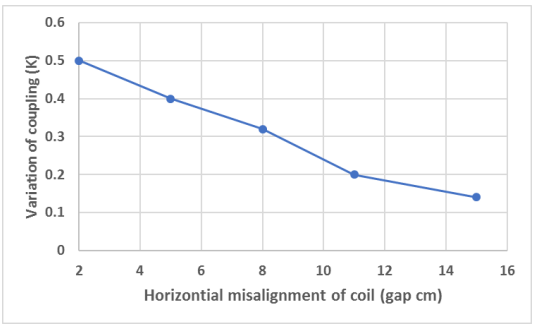
(a)



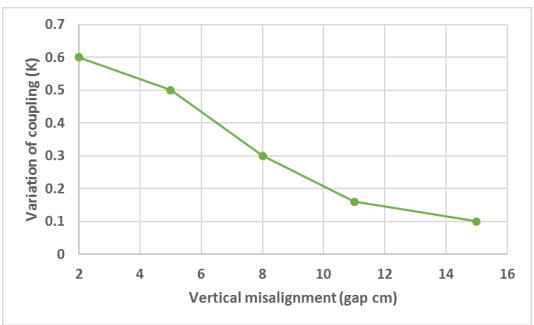
(b)

Fig. 17. Inverter efficiency (a) during horizontal misalignment, (b) during vertical misalignment.

designed to become compact and power density could be increased. The constant voltage characteristics could be maintained (Fig. 12), which is desirable for IPT application. Besides, these inverters have the inherent sine-wave characteristics similar to those of conventional class EF_2 and



(a)



(b)

Fig. 18. Changes of coupling coefficient (a) during horizontal misalignment, (b) during vertical misalignment.

class E inverter. The proposed modified class EF_2 inverter can deliver similar output power with less device stress and losses than its conventional counterpart.

Fig. 17(a) and (b) show the efficiency of the inverter for two types of misalignment condition. Fig. 18(a) and (b) shows the coupling variations of the WPT coil used for this experiment. Efficiency during vertical misalignment is lower than in horizontal misalignment because of the low coupling and high leakage magnetic field of the coils. This efficiency measurement was conducted during 150-W power transfer condition. Power transfer was maintained in this range because of some experimental limitation. At this operating condition, the losses in L_R, $L_{SR} - C_{SR}$ branches, switch conduction, off time loss, and loss through C_P were calculated using Equations (16) to (19).

The loss in the input resonant inductor is equal to

$$P_{L_R} = (I^2_{L_R(rms)}) r_{L_R} \ , \quad (23)$$

where r_{L_R} is the ESR of the resonant inductor measured by the LCR meter.

The switch conduction loss is calculated using (17) with switch rms current and on-time resistance $r_{DS}(ON)$.

$$P_{cond} = I^2_{S(rms)} r_{DS} = [\left(\sqrt{\frac{1}{2\pi}\int_0^{2\pi D} i_s^2 d(\omega t)}\right)] r_{DS}. \quad (24)$$

The power loss in C_P due to ESR r_{C_P} is calculated by (25)

$$P_{C_P} = [(\sqrt{\frac{1}{2\pi}\int_{2\pi D}^{2\pi} (i_{C_p})^2 \, d(\omega t)})] r_{C_P} \ , \quad (25)$$

and the total power loss in L_{SR}-C_{SR} is

$$P_{L_{SR}-C_{SR}} = I^2_{L_{SR}(rms)} (r_{L_{SR}} + r_{C_{SR}}. \quad (26)$$

VI. CONCLUSIONS

This paper presents a modified single-switch voltage-fed multi-resonant class EF_2 inverter and its application in IPT system. An intuitive design method was described to calculate the various component values of the proposed inverter for an IPT system. Through the same design procedure, the component value of the proposed inverter can be calculated for other applications. The following are the main highlights of the proposed inverter compared with conventional class EF_2 and class E inverters:

- Input choke inductor loss is reduced using resonant inductor.
- Peak voltage stress across the switching device is reduced considerably using a passive resonant circuit.
- Zero-voltage switching operation.
- Inherent advantages of single-switch class E inverter are maintained.
- Constant output voltage characteristics for the IPT system are provided.

The inverter is experimentally verified using a 500-W IPT setup with a frequency range of 95 kHz–100 kHz. The maximum efficiency of the inverter is 90%±2 and maintains good operation during misaligned conditions of the IPT system.

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