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A Fault Tolerant Control Technique for Hybrid Modular Multi-Level Converters with Fault Detection Capability

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Abstract

In addition to its modular nature, a Hybrid Modular Multilevel Converter (HMMC) assembled from half-bridge and full-bridge sub-modules, is able to block DC faults with a minimum number of switching devices, which makes it attractive for high power applications. This paper introduces a control strategy based on the Root-Least Square (RLS) algorithm to estimate the capacitor voltages instead of using direct measurements. This action eliminates the need for voltage transducers in the HMMC sub-modules and the associated communication link with the central controller. In addition to capacitor voltage balancing and suppression of circulating currents, a fault tolerant control unit (FTCU) is integrated into the proposed strategy to modify the parameters of the HMMC controller. On advantage of the proposed FTCU is that it does not need extra components. Furthermore, a fault detection unit is adapted by utilizing a hybrid estimation scheme to detect sub-module faults. The behavior of the suggested technique is assessed using PSCAD offline simulations. In addition, it is validated using a real-time digital simulator connected to a real time controller under various normal and fault conditions. The proposed strategy shows robust performance in terms of accuracy and time response since it succeeds in stabilizing the HMMC under faults.

Key words: Fault detection unit, Fault tolerant control unit, Hardware in the loop, Hybrid modular multilevel converter, Recursive least square

I. INTRODUCTION

Modular multilevel converters (MMC) have a lot of potential for use in various industrial and energy systems. They have the same advantages as two-level voltage source converters (VSC) such as independent control of active and reactive powers, and a small footprint when compared to line commutated converters (LCC). However, the MMC has some unique features that make it very suitable for use in high voltage and high current applications. These features include improved quality of the output voltage and current due to an increased number of the voltage levels without the need for filtering devices, a reduced switching frequency that is translated into lower switching losses, and elimination of the dc-link capacitor [1], [2]. The MMC is constructed from either half-bridge sub-modules (HBSM) or full-bridge sub-modules (FBSM) depending on the application it will be used in. The main advantage of the HBSM-MMC is a reduced number of switching devices, which means that the switching losses are low. However, it fails to protect the system against DC faults since the HBSM has only two quadrant operation. Therefore, it cannot reverse the current. The DC fault blocking capability

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TABLE I
HBSM MODES OF OPERATION

Mode	I	II
S1	Switched on	Switched off
S2	Switched off	Switched on
Description	The output voltage from the sub-module has a positive polarity. The capacitor is charging or discharging, depending on the current direction.	The sub-module is bypassed and the current flows towards the next sub-module keeping the capacitor charge constant.

TABLE II
FBSM MODES OF OPERATION

Mode	I	II	III	IV	V
S1	Switched on	Switched off	Switched on	Switched off	Switched off
S2	Switched off	Switched on	Switched off	Switched on	Switched off
S3	Switched off	Switched off	Switched on	Switched on	Switched off
S4	Switched on	Switched on	Switched off	Switched off	Switched off
Description	The output voltage from the sub-module has a positive polarity. The capacitor is charging or discharging, depending on the current direction.	The sub-module is bypassed and the current flows towards the next sub-module keeping the capacitor charge constant.		The output voltage from the sub-module has a negative polarity. The capacitor is charging or discharging, depending on the current direction.	The sub-module is blocked and no energy can be exchanged.

can be easily achieved using a FBSM-MMC since the FBSM has a four quadrant operation. Therefore, it can stop the propagation of DC faults. However, when looking at the performance of the converter itself, the switching losses are increased since the current passes through two IGBTs instead of one. In addition, the capital cost of a FBSM-MMC is doubled when compared to the HBSM-MMC since each sub-module needs four IGBTs instead of two [3]. This has motivated researchers to innovate a new type of multi-level converter called the hybrid modular multi-level converter (HMMC), which is able to compromise a new structure that mixes the advantages of the HBSM-MMC and the FBSM-MMC [4].

To guarantee stable and accurate operation for a HMMC, the sub-module capacitors must be charged to the same voltage level. This process is called capacitor voltage balancing. Furthermore, these voltages should follow a pre-defined reference to reach a desired level of output voltage [5]-[7].

Due to the modular nature of the HMMC and the series connection of differently structured sub-modules, any sub-module fault threatens the safety of the other healthy sub-modules since a fault may propagate and cause cascading failure for the whole arm. On the other hand, it is not recommended to shut-down the whole converter to recover a sub-module from a fault. All of these challenges have directed research to the concept of fault detection and fault tolerant control that enable the HMMC to operate under the fail-to-safe principle with acceptable performance even if some of the sub-modules are subjected to faults [8], [9]**.** The first step to implement the fault detection algorithm is to classify the faults of the HMMC sub-modules. The sub-module is the building identity of the HMMC and it is subject to different open-circuit or short-circuit faults in the switches or capacitors, which affect the reliability of the HMMC [8], [9]. It was found that 30% of the failures in power electronic converters occur in the switches [10]. In addition, it is important to mention that the time required to identify an internal fault should be less than 5ms to be able to block the converter before the short circuit current reaches its full value. Therefore, the quick detection of switch faults is essential to enhancing the reliability of the HMMC.

A fault tolerant control system aims to outperform a faulty sub-module and to stabilizing the HMMC [11]. In the literature, most fault tolerant control systems depend on either redundant components or special circuits which add an extra cost for items that are not be used during normal operation [12].

This paper presents a controller for the capacitor voltage balancing of a HMMC based on the capacitor voltage estimation algorithm instead of direct measurements of the sub-module capacitor voltages. Moreover, the fault detection and fault tolerant control techniques, proposed for the MMC in [13], are generalized for the HMMC and integrated into the proposed control strategy. The main contribution of the proposed technique when compared to other techniques is that the indicated strategy controls the HMMC in both normal and abnormal conditions without the incorporation of any capacitor voltage measurements, extra power circuits or special power circuits while keeping perfect power quality in both conditions. As a result, the cost is significantly reduced and the reliability of the control system is increased due to the reduced number of components and the limited number of communication channels, which make the proposed strategy attractive for practical implementations of a HMMC with a large number of sub-modules. The proposed control is tested using the concept of the hardware in the loop (HIL) by connecting a real-time digital simulator to a physical controller

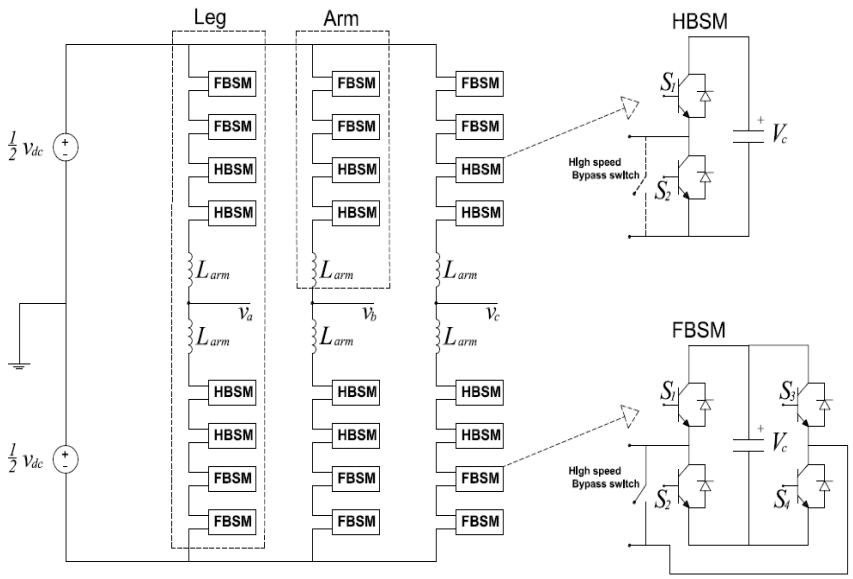


Fig. 1. Three-phase HMMC topology and sub-module circuits.

to practically evaluate its dynamic performance. Different operation scenarios are considered to assess the performance of the proposed unified control scheme.

II. Hybrid Modular Multi-Level Converter Modelling

A. The HMMC Structure and Theory of Operation

The three-phase HMMC is assembled from three legs as shown in Fig. 1. Each leg is formed from two arms where each arm includes a number of HBSMs and FBSMs connected in series. The sub-modules, which are considered to be the building blocks of the HMMC, transfer the energy between the dc and the ac sides through different operation modes as illustrated in Table I and Table II.

B. The HMMC Mathematical Model

To estimate the capacitor voltages of a HMMC, it is necessary to find a mathematical model of the converter. Neglecting the difference between HBSM and FBSM, the output phase voltage v_o is given by [13], [14]:

$$v_o = \frac{v_{dc}}{2} - L_{arm}\frac{di_u}{dt} - m_{arm\,u}\,\Sigma v_{Cu} \tag{1}$$

$$v_o = -\frac{v_{dc}}{2} + L_{arm}\frac{di_l}{dt} + m_{arm\,l}\,\Sigma v_{Cl} \tag{2}$$

where i_u and i_l are the upper and lower arm currents, respectively, L_{arm} is the arm inductance, $m_{arm\,u}$ and $m_{arm\,l}$ are the modulation values of the upper and lower arms, respectively, and Σv_{Cu} and Σv_{Cl} are the sums of the upper and lower arm capacitor voltages, respectively. To find the minimum number of the FBSMs needed to block DC faults, let the number of the FBSMs per arm be N_F and the number of the HBSMs per arm be N_H, where $N = N_H + N_F$ is the number of sub-modules per arm. When all of the arm sub-modules are inserted, the maximum line-to-line output voltage is given by:

$$v_{o\,max} = \frac{\sqrt{3}}{2}v_{dc} \tag{3}$$

The voltage generated by the FBSMs in each arm is:

$$v_{FBSM\,arm} = \frac{N_F}{\mathrm{N}}v_{dc} \tag{4}$$

To successfully block any DC-side fault from transmitting to the AC-side through the converter, the FBSM voltage of the two arms, $2\,v_{FBSM\,arm}$, should be higher than the maximum line to line output voltage, $v_{o\,max}$, which results in:

$$\frac{2N_F}{\mathrm{N}}v_{dc} \geq \frac{\sqrt{3}}{2}v_{dc} \tag{5}$$

Rearranging (5), the number of FBSMs should satisfy the following condition:

$$N_F \geq \frac{\sqrt{3}}{4}\mathrm{N} \tag{6}$$

C. The Switching of the HMMC using the Phase Shifted Carrier based Modulation Technique

There are many carriers based modulation techniques that can be used in the switching of HMMCs [15]-[18]. Phase shifted pulse width modulation (PS-PWM) is more suitable for this particular application due to its promising advantages such as its ease of implementation and stable performance in normal and abnormal operating conditions [15].

As shown in Fig. 2, each of the sub-modules has a devoted carrier signal with a different phase shift. The gating signals for a sub-module result from comparing its associated carrier signal with the voltage reference signal v_o^*. It is worth

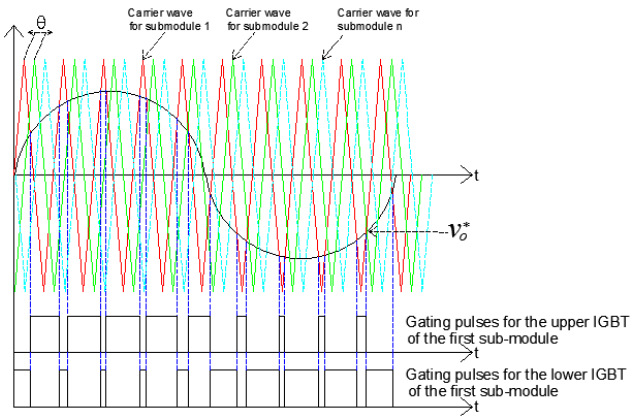


Fig. 2. Phase shifted carrier PWM.

mentioning that the phase shift between two consecutive carrier signals is calculated from:

$$\theta = 360/(N-1) \tag{7}$$

III. Capacitor Voltage Estimation

The process of the capacitor voltage estimation is critical since the performance of the HMMC is fully depending on the accuracy of the estimated voltages. The proposed control system of the HMMC incorporates two capacitor voltage estimation techniques for the proposed fault detection unit. The first estimation technique is based on the ADAptive LInear NEuron (ADALINE) and the second technique is centered on the Recursive Least Squares (RLS) algorithm, which is also utilized to feedback estimated capacitor voltages to the proposed capacitor voltage balancing scheme.

A. The ADALINE Technique for Capacitor Voltages Estimation

ADALINE is an adaptive online tracking technique which is known for its unique features such as reduced calculations, improved accuracy and fast behavior [19]-[22]. To estimate the capacitor voltages, three voltage sensors are required for the estimation process. Two are used to measure the arm voltages v_{Lu} and v_{Ll} while the third is used to measure the output voltage. Rearrange the model of the HMMC, given by (1) and (2), as follows:

$$\frac{v_{dc}}{2} - v_o - v_{Lu} = [S_{u1} \quad S_{u2} \quad \dots \quad S_{uN}] \begin{bmatrix} v_{cu1\_est} \\ v_{cu2\_est} \\ \vdots \\ v_{cuN\_est} \end{bmatrix} \tag{8}$$

$$\frac{v_{dc}}{2} + v_o - v_{Ll} = [S_{l1} \quad S_{l2} \quad \dots \quad S_{lN}] \begin{bmatrix} v_{cl1\_est} \\ v_{cl2\_est} \\ \vdots \\ v_{clN\_est} \end{bmatrix} \tag{9}$$

where S_{xi} is the switching state of the i^{th} sub-module, the sub-suffix $x = u$ *or* l for the upper or lower arm, respectively, $v_{Lu} = L_{arm}\frac{di_u}{dt}$, and $v_{Ll} = L_{arm}\frac{di_l}{dt}$. From (8) and (9), the input vector is given by:

$$\boldsymbol{X}(k) = [S_{x1}(k) \quad S_{x2}(k) \quad \dots \quad S_{xN}(k)] \tag{10}$$

While the weighting vector is:

$$\boldsymbol{W}(k) = \begin{bmatrix} v_{cx1\_est} \\ v_{cx2\_est} \\ \vdots \\ v_{cxN\_est} \end{bmatrix} \tag{11}$$

The actual output signal is represented by the left hand side of (8) and (9), and is given by:

$$y(k) = \frac{v_{dc}}{2} \mp v_o - v_{Lx} \tag{12}$$

Multiplying (10) by (11) results in the predicted output signal from the ADALINE algorithm, $\hat{y}(k) = \boldsymbol{X}(k)\boldsymbol{W}(k)$, which gives the right hand side components of (8) and (9). Consequently, the weight vector **W**(k) is updated by minimizing the error between the predicted $\hat{y}(k)$ and the measured $y(k)$ signals. This step is done using the Widro-Hoff delta rule given by [22]:

$$W(k+1) = W(k) + \alpha \frac{X(k)(y(k)-\hat{y}(k))}{X(k)^T X(k)} \tag{13}$$

where α is the reduction factor that is responsible for controlling the speed of the conversion. Based on many studies, α is limited to between 0 and 0.1 [23]. Once the predicted signal $\hat{y}(k)$ converges to the measured signal $y(k)$, the ADALINE technique estimates the capacitors voltages. The reduced calculations of this algorithm enables the implementation of a low cost centralized controller for the HMMC with a large number of sub-modules due to the elimination of the sub-module voltage measurements and their associated communication link.

B. The RLS Technique for Capacitor Voltages Estimation

The RLS algorithm is an iterative-based on-line tracking technique, which offers stable and accurate behavior. The advantage of the RLS algorithm over other on-line tracking algorithms comes from its ability to update higher weighting vectors using the present inputs instead of the previous captured inputs, which reduces the dependency on older inputs as time passes [24], [25]. The RLS algorithm is formed by two equations. One equation is used to update the estimate vector $\hat{\theta}(k)$ of the sub-module capacitor voltages, as formulated in (14), and the other equation is for updating the weighting matrix *P(k)*, as formulated in (15).

$$\hat{\theta}(k) = \hat{\theta}(k-1) + P(k)\hat{\theta}(k)\left[y(k) - \phi(k)^T\hat{\theta}(k-1)\right] \tag{14}$$

$$P(k) = \frac{1}{\lambda}\left[P(k-1) - \frac{P(k-1)\phi(k)\phi(k)^T P(k-1)}{\lambda+\phi(k)^T P(k-1)\phi(k)}\right] \tag{15}$$

where $\phi(k)$ symbolizes the switching state vector $[S_{x1} \quad S_{x2} \quad \dots \quad S_{xN}]^T$ at time *k*, and λ is the forgetting factor that regulates the convergence rate. The predicted signal $\hat{y}$ is calculated from $\phi(k)^T\hat{\theta}(k-1)$ which is

subtracted from the measured signal, and the error is utilized to update the estimate vector [26]. When the prediction error diminishes, convergence is achieved and the capacitor voltages are estimated.

IV. Proposed HMMC Centralized Controller

The key advantage of the proposed control system for the HMMC is its capability to operate under normal and fault conditions. The proposed centralized control strategy for the HMMC integrates three main sub-control units. The three units are the capacitor voltages balancing control unit, the fault detection unit, and the fault tolerant control unit.

A. The Capacitor Voltage Balancing Control Unit

Since a fault tolerant control scheme is standard and suitable for many capacitor voltage balancing strategies, two capacitor voltage schemes are introduced to demonstrate this concept.

The first technique was developed to provide a simple method for balancing the capacitor voltages instead of depending on complex techniques which makes it suitable for a HMMC with a high number of voltage levels.

In this method, the arm current is observed to determine whether it is charging or discharging the sub-modules. In the case of charging the capacitors, the algorithm calculates the number of sub-modules that need to be inserted N_{new} based on the measured capacitor voltages. Then, it calculates the difference between this number and the old number of sub-modules that is already inserted ($\Delta N_{on} = N_{on} - N_{on_{old}}$). If ΔN_{on} is zero, then the switching is kept as it is and nothing changes. However, if ΔN_{on} is greater than zero, the arm current is checked to determine whether it is charging or recharging the arm capacitors. If the arm current i_{arm} is higher than zero, the algorithm inserts ΔN_{on} submodules that have the lowest voltages depending on the estimation of the RLS schemes. Meanwhile the algorithm bypasses ΔN_{on} submodules that have the highest RLS estimated voltage if i_{arm} is less than zero. Finally, if ΔN_{on} is lower than zero and the arm current i_{arm} is higher than zero, the algorithm inserts ΔN_{on} submodules that have the highest RLS estimated voltages. Meanwhile the algorithm bypasses ΔN_{on} submodules that have lowest RLS estimated voltages if the i_{arm} is less than zero [27]. This method enhances the performance of the HMMC since the converter losses are lowered due to the relatively low switching frequency. Moreover, there are no complex calculations or sophisticated Proportional Integral Derivative (PID) control loops, which make it simpler than other techniques. This scheme is used in PSCAD offline simulations.

The second scheme is formed from two main parts. The first is the averaging part, while the second is the balancing part. The averaging control is responsible for balancing the energy between two arms through regulating the average voltage of the whole leg. It includes two cascaded loops per phase to control the average voltage based on PI controllers [14]. The outer loop generates the reference of the differential current i^*_{diff} by managing the error between the average voltage estimated by the RLS algorithm, $\hat{v}_{avg} = (\sum v_{cui\ RLS} + \sum v_{cli\ RLS})/2N_{eff}$, and the desired capacitor voltage v^*_C, where N_{eff} is the number of effective sub-modules per arm. The inner loop sets the averaging voltage signal v^*_{avg} to regulate the differential current defined by $i_{diff=}(i_u + i_l)/2$ at its reference i^*_{diff}.

The balancing control is formed from *N* separate P-controllers to process the error between the reference and the estimated signals of the capacitor voltage. The sign of the arm current is multiplied by the actions of the P controllers to form reference signals to balance the voltage across the corresponding arm capacitors, v_{cul_bal}, … ,v_{cuN_bal}, v_{cll_bal}, … , v_{clN_bal}. Finally, the voltage balancing signal for each sub-module, the average voltage reference, v^*_{avg}, and the desired phase voltage, v^*_o, are added together to form modulating signals for the sub-modules. The PS-PWM technique is adopted to produce switching signals for the sub-modules of the HMMC. This balancing strategy is used in the real-time simulation part.

B. The Fault Detection Unit

Fig. 3 presents the proposed fault detection unit (FDU), which is based on the percentage of the reduction in the estimated voltage and the rate of change of the deviation among the estimated voltages using the ADALINE and RLS techniques. The estimated capacitor voltages, $v_{cxi\ RLS}$, for each sub-module *i* = 1,2,3…..,N using the RLS algorithm are normalized by dividing the reference capacitor voltage v^*_C to get their per-unit values $v_{cxi\ RLS\ pu}$. In addition, the deviation among the estimated capacitor voltages using ADALINE and RLS is determined for each sub-module. Hence, the rate of change of the deviation signal e_{xi} is calculated. The proposed FDU benefit from the dynamic behavior variations among the ADALINE and RLS techniques due to their diverse objectives. If the estimated per-unit voltage for any sub-module exceeds 85%, the sub-module is considered healthy. Otherwise, if the rate of change of the deviation signal surpasses a predefined level that is set according to the desired sensitivity, the FDU registers a possible fault in the corresponding sub-module. To indicate a faulty sub-module, a counter is devoted to ensure the constancy of the estimated signals for a given amount of time. Finally, the FDT set flags for the faulty sub-modules that are accessed by the fault tolerant control unit.

The hybrid decision making of the proposed FDU results in robust performance. In addition, no extra circuits or components are required since the proposed FDU employs

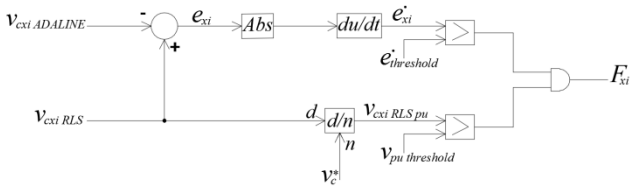


Fig. 3. Block diagram of the proposed fault detection unit.

estimation algorithms that are already developed for the proposed control of the HMMC.

C. The Fault Tolerant Control Unit

The main tasks of the proposed fault tolerant control unit (FTCU) are to disconnect faulty sub-modules and to modify the capacitor voltage balancing unit. The proposed FTCU utilizes the flags of faulty sub-modules set by the FDU to define the number of faulty sub-modules N_{xf}. For a faulty sub-module in the upper arm, the FTCU isolates it with one in the lower arm. Bypass switches are used to isolate sub-modules. To keep the balance between the upper and lower arms, a healthy sub-module in the adjacent arm is isolated to make the number of activate sub-modules in the two arms equal. Consequently, the reference capacitor voltage v_C^* is increased by N/N_{eff} to substitute for the reduction of active sub-modules. Simultaneously, the proposed FTCU adapts the phase shift of the carrier signals for the active sub-modules of the leg according to (3).

The proposed fault tolerant strategy allows a HMMC to continue operation if the number of faulty sub-modules does not exceed a certain percentage and there is no external DC short circuit. Otherwise, the control system should block all of the FBSMs and deactivate the converter. The maximum percentage of faulty sub-modules per arm is selected based on the number of sub-modules per arm and the ratings of the power electronic devices. For example, for the eight level MMC used in the simulation, the maximum percentage of faulty sub-modules per arm can be 25%. Increasing the number of voltage levels, decreases the allowable percentage of faulty sub-modules.

It is clear that the proposed control strategy avoids the need for an enormous numbers of voltage sensors for the sub-module capacitors and their correlated communication links with the central controller. As a result, the proposed control strategy renders its implementation for an HMMC with many sub-modules.

V. Offline Simulation Results

Unlike the detailed model presented in the previous subsection, an average model of a 77-level MMC is considered to facilitate calculations due to the relatively high number of sub-modules. The average model used in the simulation depends on converting the detailed model of the sub-module into its Thevenin equivalent [28]. As shown in

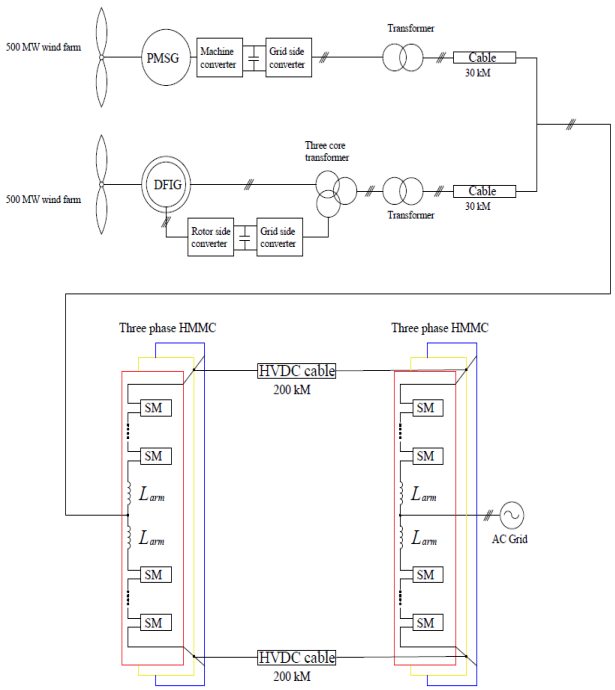


Fig. 4. Circuit diagram of the second MMC model.

Fig. 4, the model contains two wind farms, where each has a rating of 500 MW. The first wind farm delivers energy through a permanent magnet synchronous generator (PMSG), and the output voltage of the PMSG is 0.69 kV. The terminals of the PMSG are connected to a back-to-back two-level VSC.

The generator used in the second wind farm is a double-fed induction generator (DFIG), which generates power at 0.69 kV. The rotor winding of the DFIG is connected to a back-to-back two-level VSC. The output of this VSC and the stator winding of the DFIG are both connected to a three-core transformer. Since both of the wind farms are working on the same voltage level, a point of common coupling is formed, which connects the two wind farms together with the rectifier stage of the HVDC. The HVDC link is formed from two MMCs connected through a 200 kM cable. The output of the inverter stage of the HVDC system is connected to a 220 kV AC grid.

The rated power of both MMCs is selected to be 1,000 MW, while the rated DC voltage is 640 kV. The size of the sub-module capacitor is calculated in the same manner as presented in the previous subsection. Table III shows the parameters of the offline simulation model.

The simulated case is developed to evaluate the proposed capacitor voltage estimation technique, when applied to an HMMC-based HVDC system that integrates offshore wind power with the grid. It was also developed to investigate the accuracy of the proposed capacitor voltage estimation techniques for an HMMC with a relatively high number of voltage levels. Furthermore, the dynamic performance of the proposed capacitor voltage estimation technique is assessed under external grid faults. The RLS capacitor voltage

TABLE III
HMMC GRID CONNECTED MODEL PARAMETERS

HMMC Model Parameters	
Rated power	500 MW
Sub-module rated voltage	4.2 kV
Rated dc Voltage	640 kV
Arm inductance	70 mH
Sub-module capacitance	220 µF
Number of HBSM per leg	4
Number of FBSM per leg	152

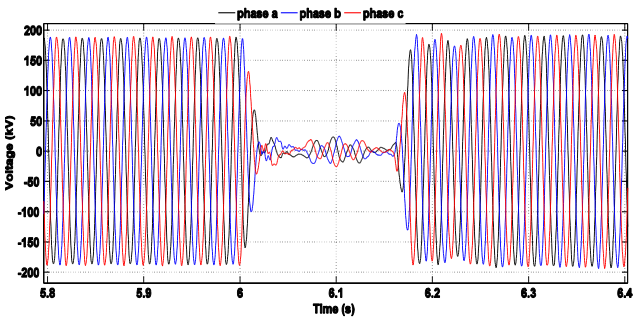


Fig. 5. Grid voltages [28].

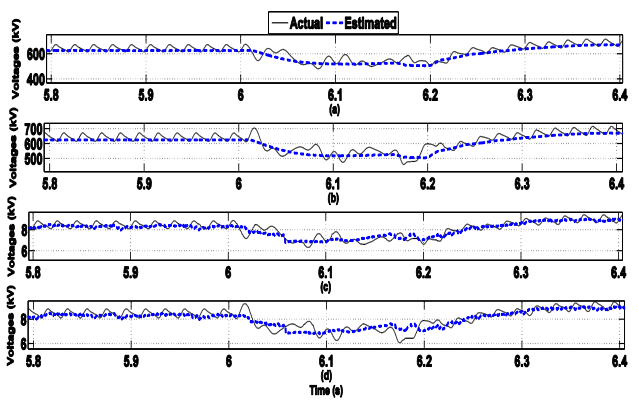


Fig. 6. Actual and estimated sub-module capacitor voltages in leg a: (a) summation of the capacitor voltages in the upper arm; (b) summation of the capacitor voltages in the lower arm; (c) capacitor voltage of one sub-module in the upper arm; (d) capacitor voltage of one sub-module in the lower arm [28].

estimation technique provides it with estimated capacitor voltages instead of using direct measurements. This is done to prove that the proposed RLS capacitor voltage estimation can be adopted for different capacitor voltage balancing techniques. In this case, the reference DC voltage signal is 640 kV. Then, at t = 6 s, a three-phase fault is applied at the grid side, which lasts for 0.2 s. The capacitor voltage estimation-based voltage balancing technique succeeds in balancing the capacitor voltages, as shown in the balanced three-phase voltages presented in Fig. 5. The RLS estimation algorithm provided balancing control over the whole period even during the external fault period. Fig. 6(a) and (b) illustrate the summation of the capacitor voltages of the upper and lower

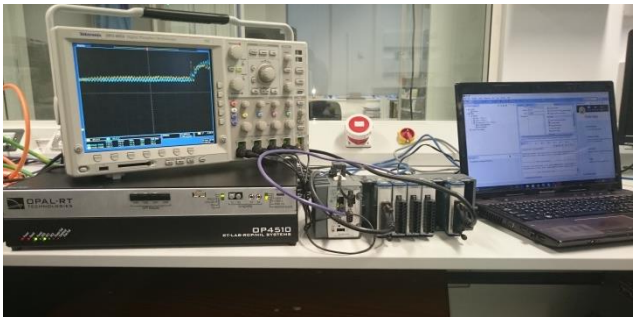


Fig. 7. HIL platform.

TABLE IV
HMMC MODEL PARAMETERS

HMMC Model Parameters	
Rated power	1 MW
Sub-module rated voltage	2250 V
Rated dc Voltage	9000 V
Arm inductance	3 mH
Sub-module capacitance	1900 µF
Number of HBSM per leg	4
Number of FBSM per leg	4
Load impedance	30 Ω , 6 mH

arms. Moreover, the capacitor voltages of one sub-module from the upper and lower arms are portrayed in Fig. 6(c) and (d), respectively. They follow the traces of the actual capacitor voltages of the upper and lower arms, even during a grid fault. Results obtained in this case prove that the proposed capacitor voltage estimation algorithm is not affected by external AC faults or grid power controls. Therefore, the proposed capacitor voltage estimation algorithm is suitable for HMMCs with a high number of voltage levels, which are normally used in HVDC circuits.

VI. HARDWARE IN THE LOOP OF THE SIMULATION RESULTS

Validation of the proposed control scheme for a HMMC is done using the concept of hardware in the loop (HIL) of the simulation through the incorporation of an OPAL-RT type OP4510 real-time digital simulator with a NI type cRIO-9024 real-time physical FPGA as illustrated in Fig. 7. The HMMC model is simulated using the real-time digital simulator including the whole network with the support of the RT-LAB software, the DC supply and the AC system. Meanwhile, the proposed HMMC centralized controller is programmed on the FPGA using LABVIEW software. The real-time digital simulator provides the FPGA controller with the values of the output and arm voltages through its analog outputs. Meanwhile, the FPGA controller provides the simulator with gating signals through its digital outputs. Moreover, the FPGA controller estimates the capacitor voltages required for the balancing control unit and the FDU. It also executes the proposed FTCU. The system parameters are given in Table IV.

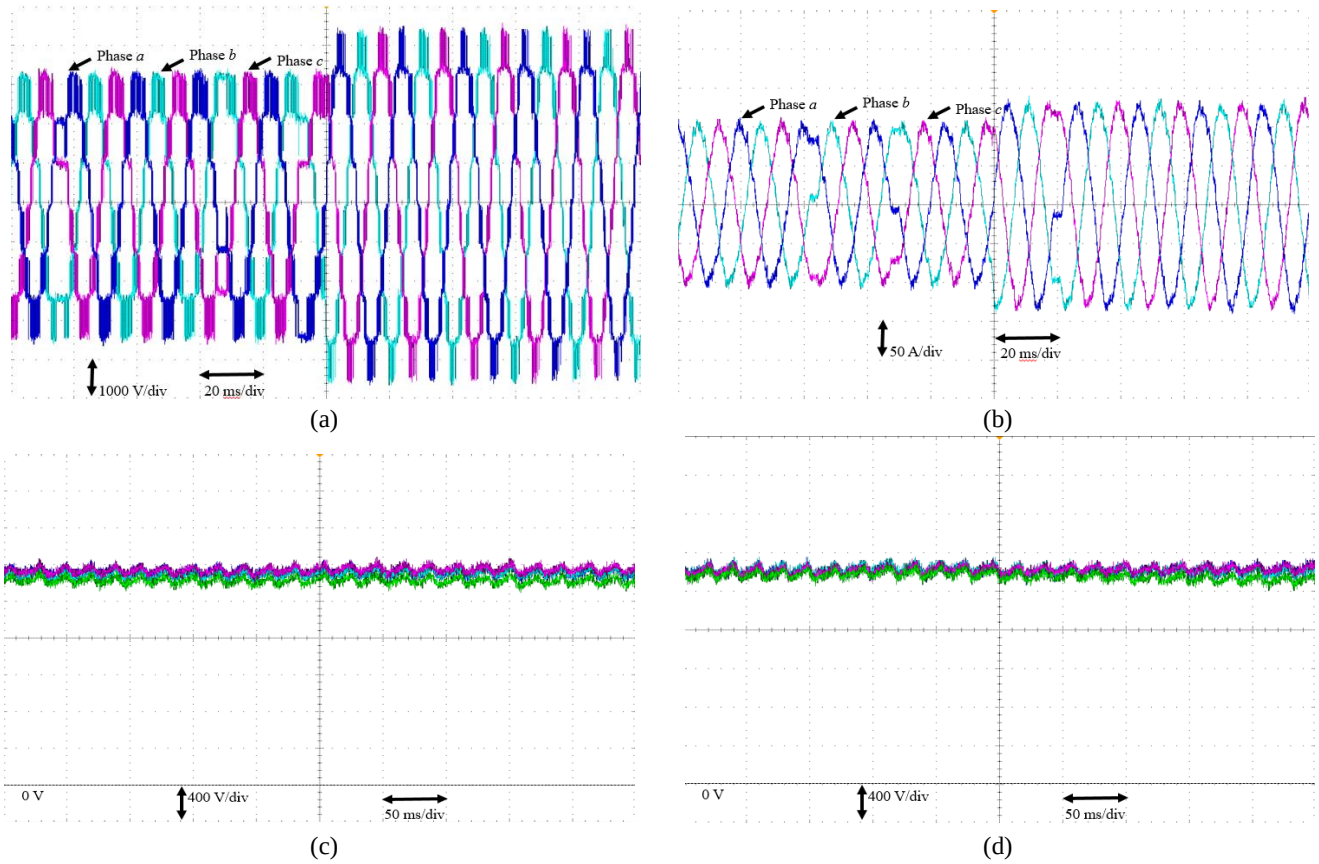


Fig. 8. Enabling the proposed estimation unit: (a) three-phase voltages; (b) three-phase load currents; (c) sub-module voltages of the upper arm of leg *a*; (d) sub-module voltages of the lower arm of leg *a*.

The simulated HMMC has four HBSMs and four FBSMs to satisfy (6). Different operation scenarios are considered to assess the performance of the proposed strategy for the HMMC. Moreover, the dynamic performance of the proposed FDU is examined under various healthy and faulty conditions. The first case study is devoted to examining the performance of the proposed control system for the HMMC using the RLS algorithm for capacitor voltage estimations. The second task is dedicated to evaluating the dynamic performance of the proposed FDU and the FTCU.

A. Performance of the Proposed Capacitor Voltage Estimation Based Control Strategy

This case is devoted to examining the dynamic performance of the proposed capacitor voltage estimation based control algorithm for the HMMC under a dynamic change of the reference phase voltage. The reference capacitor voltage v_c^* is set at v_{dc}/N = 2.25KV, while the reference phase voltage signal v_o^* is dynamically changed from 0.7pu to 1pu. The measured three-phase ac voltages follow their reference signals, as illustrated in Fig. 8(a). At the beginning, when $v_o^* = 0.7\ pu$, six sub-modules are utilized and when $v_o^* = 1\ pu$, and all of the sub-modules are encompassed. Fig. 8(b) displays the three-phase load currents. Fig. 8(c) and 8(d) show the capacitor voltages that are grouped in two main trajectories, one for the upper arm and the other for the lower arm. The proposed HMMC controller is able to balance the capacitor voltages at their reference value of 2.25 KV. Moreover, Fig 9 (a) shows the estimated capacitor voltage of the first sub-module, and compares it with its corresponding actual voltage. The fast tracking and accurate performance of the proposed scheme based on the RLS algorithm for estimating the sub-modules capacitor voltages are evident. Furthermore, the circulating current closely follows its reference signal as demonstrated in Fig. 9(b). Fig. 9(c) and Fig. 9(d) illustrate the actions of the averaging controller and the balancing controller for the first sub-module in the upper arm $v_{cu1\ bal}^*$, respectively. These results reveal the efficient utilization of the proposed capacitor voltage estimation scheme for the control algorithm of the HMMC.

B. Performance Under an Open Switch Fault

This task is dedicated to evaluate the potential of the proposed control system, the FDU, and the FTCU under an open switch fault in a sub-module. To simulate an open switch fault, the upper switch of the third sub-module in the upper arm of phase *a* is purposely opened. Fig 10 indicates that the proposed FDU manages to detect and localize the sub-module fault after 35.6 ms. Considering the rate of change of the capacitors voltages, a 35.6 ms detection period

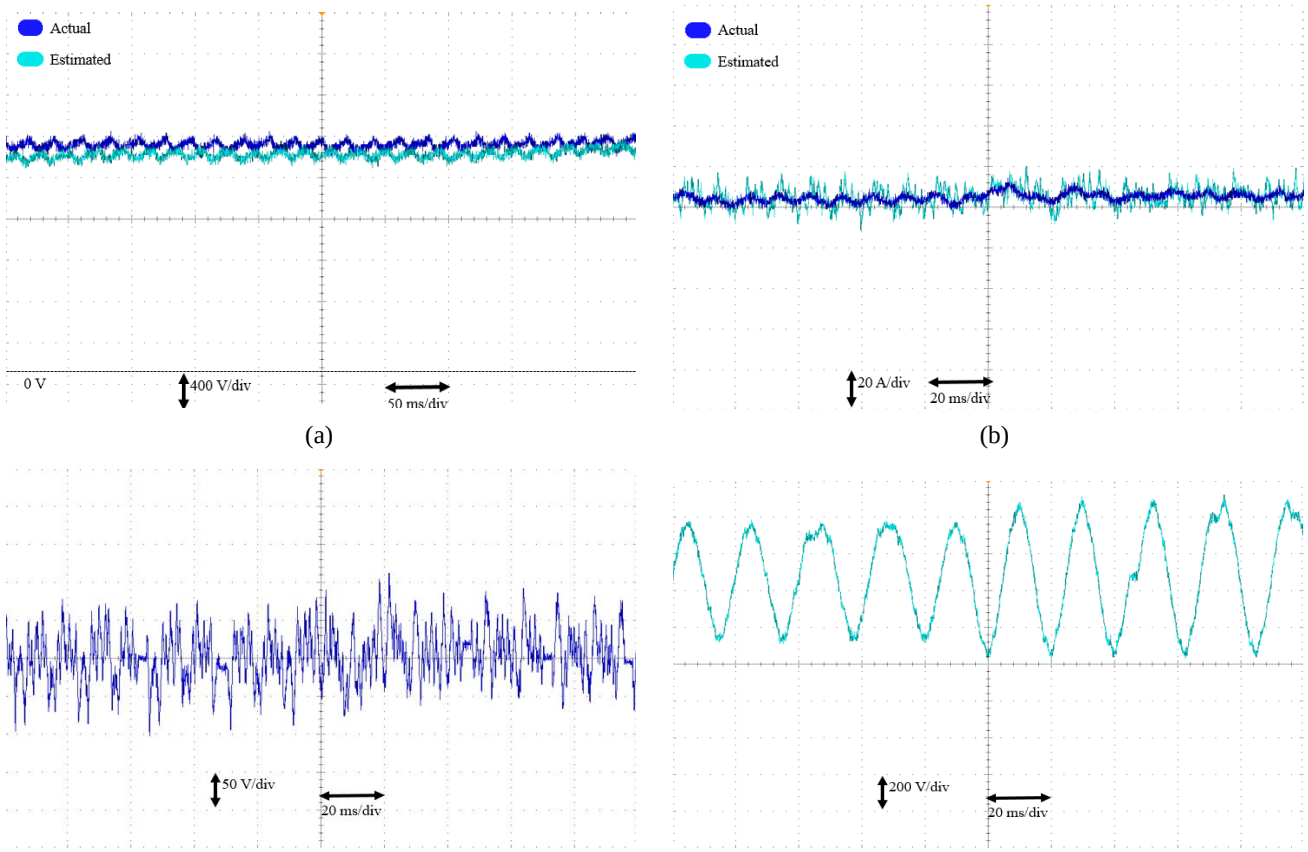


Fig. 9. Performances of different controllers: (a) voltage of the first sub-module; (b) circulating current; (c) averaging voltage reference; (d) modulating signal for the first sub-module of the upper arm of leg *a*.

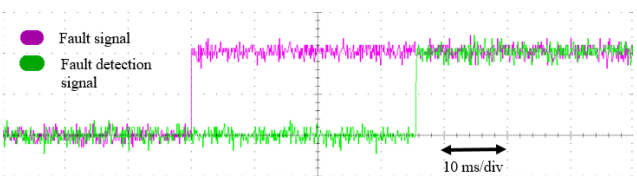


Fig. 10. Dynamic performance of the proposed FDU under an open switch fault.

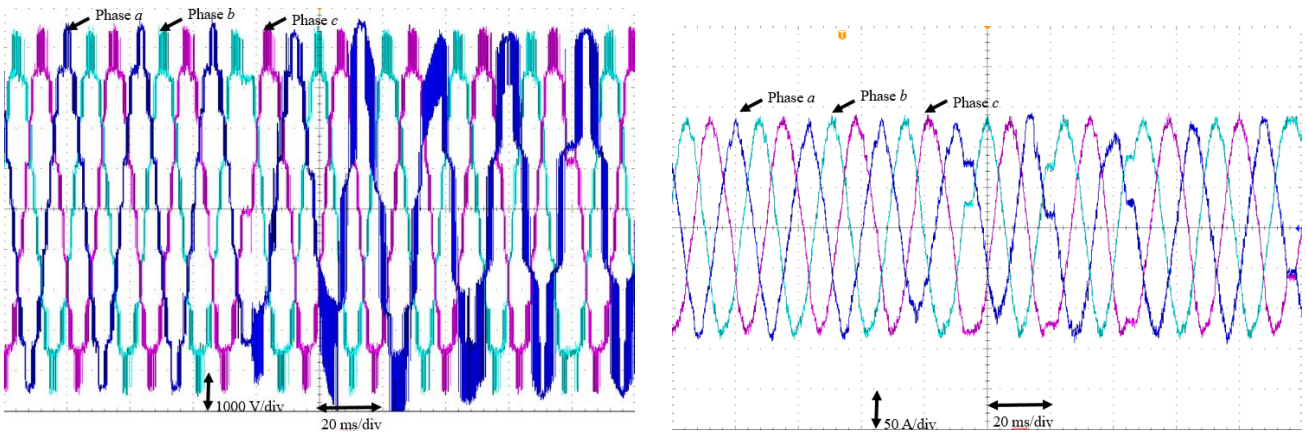
is sufficient to secure the operation of the HMMC. Once the faulty sub-module is detected, the FTCU disconnects it with a sub-module in the lower arm to balance the voltages of the two arms.

Moreover, the FTCU boosts v_c^* from 2250 V to 3000 V, and modifies the carrier phase shift to 60° instead of 45° to account for the two disconnected sub-modules. These arrangements are adequate for fault tolerance and to sustain the operation of the HMMC as indicated from Fig. 11, where the three-phase voltages and currents are balanced. Fig. 12 demontrates that the capacitor voltages of the activated sub-modules reinstate their balance at the new set value of the FTCU. As expected, the disconnected sub-modules have constant capacitor voltages. The capacitor voltage estimation unit succeeds in estimating the voltage even under an open switch fault for all of the healthy sub-modules as illustrated in Fig. 13(a). As shown in Fig. 13(b), the RLS estimated signal for the faulty sub-module is accurate until the instant of interruption.

The ADALINE and RLS algorithms provide the FDU and the FTCU with accurate data that results in precise performance during transient periods. Fig. 14(a) reveals that the actions of the proposed FTCU results in limiting the differential current to its pre-fault setting. In addition, the averaging control loop succeeds in overcoming the consequences of the fault as indicated in Fig. 14(b). Moreover, the balancing control signal is quickly stabilized as manifested from the modulating signal of the first sub-module in the upper arm of leg *a* as shown in Fig. 14(c).

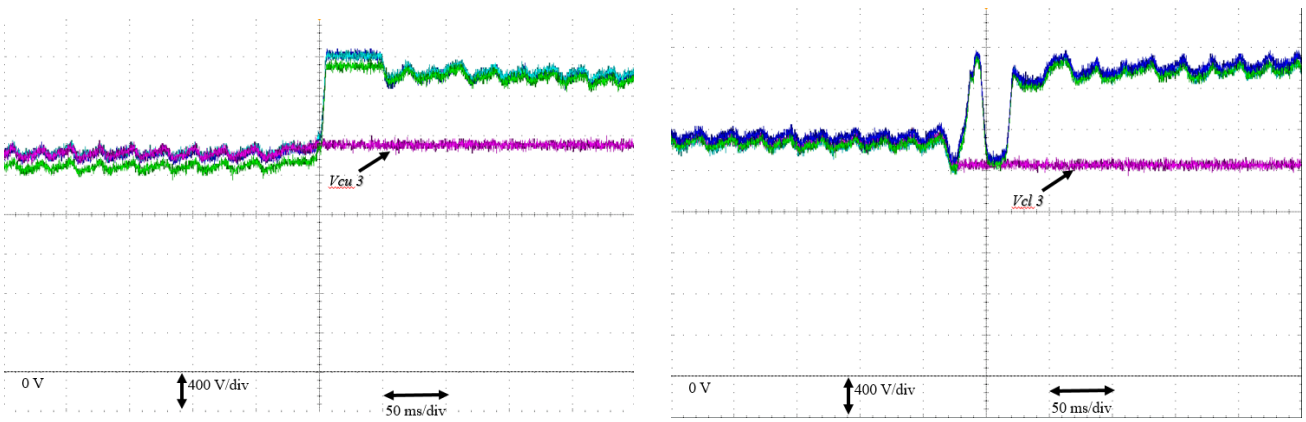
C. Performance Under a Sub-module Short Circuit Fault

This task is devoted to the assessment of the dynamic performance of the proposed strategy under a short circuit fault in a sub-module. The upper switch of the third sub-module in the upper arm of phase *a* is closed to simulate a short circuit fault. The FDU detects and localizes the fault after 3.2 ms as shown in Fig 15. The detection time is very fast especially since short circuit faults are very destructive and needs to be cleared quickly. Consequently, the FTCU



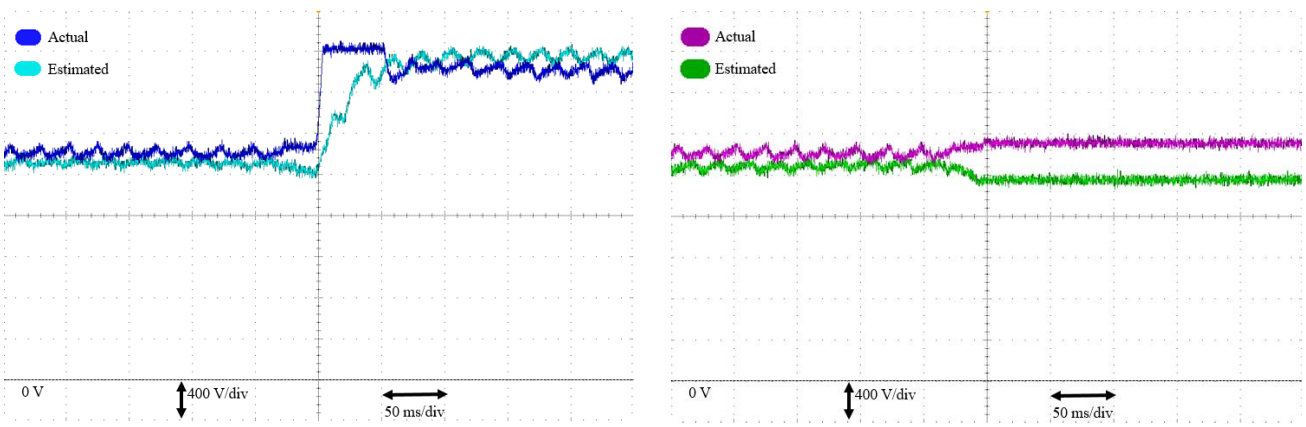
(a) (b)

Fig. 11. Waveforms under an open switch fault: (a) three-phase voltages; (b) three-phase load currents.



(a) (b)

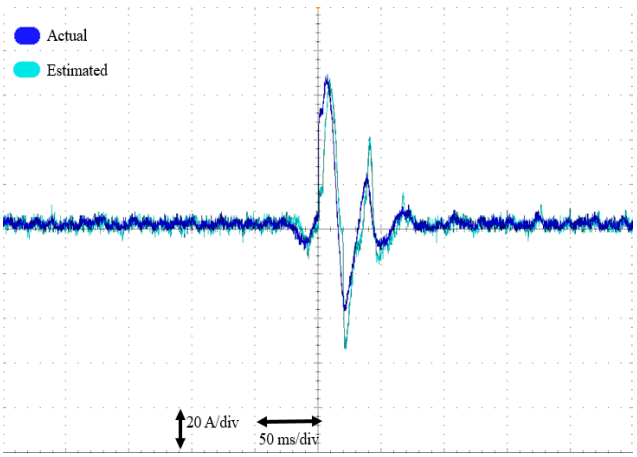
Fig. 12. Waveforms under an open switch fault: (a) sub-modules voltages of the upper arm in leg *a*; (b) sub-modules voltages of the lower arm in leg *a*.



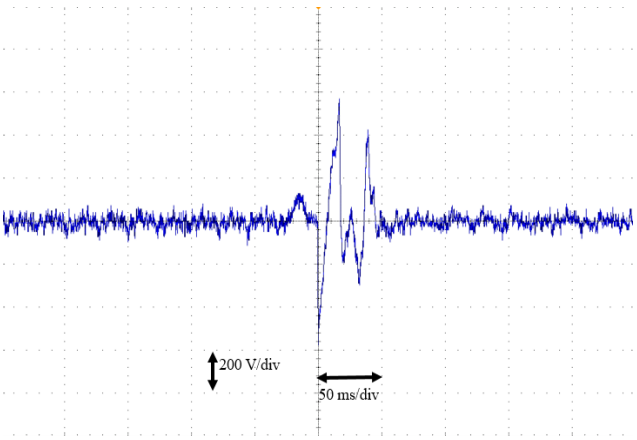
(a) (b)

Fig. 13. RLS estimated signals in the upper arm of leg *a* under an open switch fault: (a) first sub-module (healthy); (b) third sub-module (faulty).

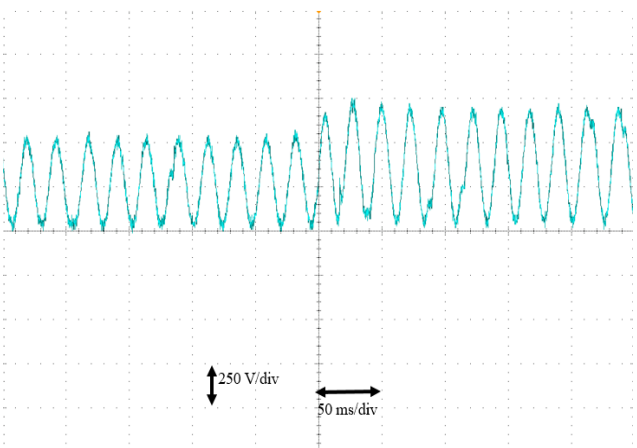
disconnects the faulty sub-module along with another one from the lower arm to sustain the voltage balance of the two arms. As in a pen switch fault, the FTCU modifies v_c^* and the carrier phase shift. These procedures are obligatory to keep the operation of the HMMC as indicated from the results in Fig. 16. The capacitor voltages of the effective



(a)



(b)



(c)

Fig. 14. Performance of different controllers under an open switch fault: (a) circulating current; (b) averaging voltage reference; (c) modulating signal for the first sub-module of the upper arm of leg *a*.

sub-modules are balanced at a new boost setting by the FTCU as illustrated in Fig. 17 (a) and (b) for the upper arm and lower arm sub-modules, respectively. The capacitor voltage estimation unit succeeds in estimating a voltage even in the

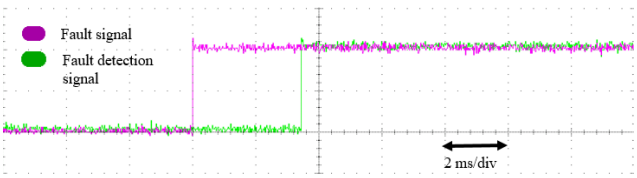


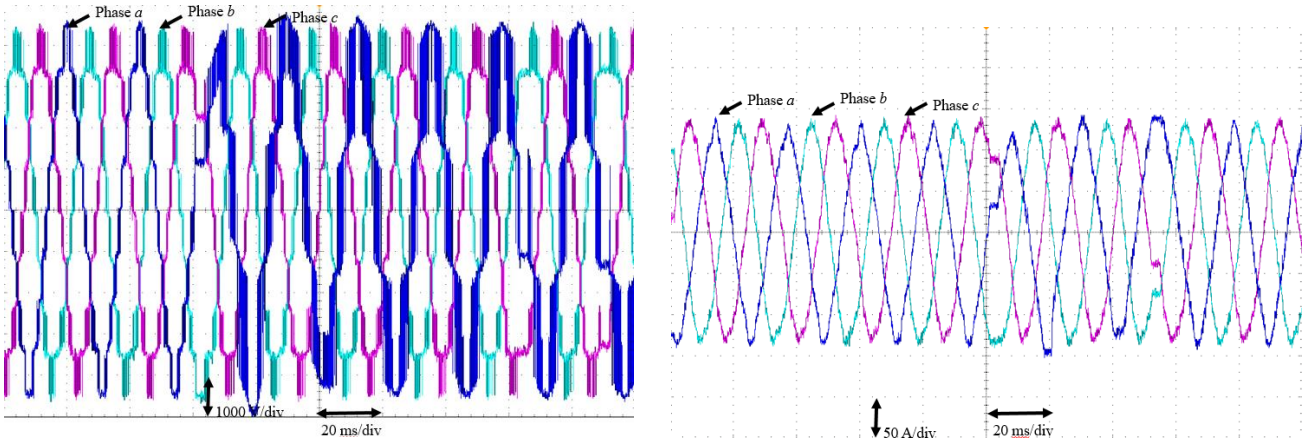
Fig. 15. Dynamic performance of the proposed FDU under a short circuit fault in a sub-module.

case of a short circuit fault as shown in Fig. 18. Fig. 18 (b) shows the estimated signal of the faulty sub-module. The differential current, averaging and voltage balancing signals are quickly stabilized as shown in Fig. 19.

D. Practical Assessment of the Proposed Techniques

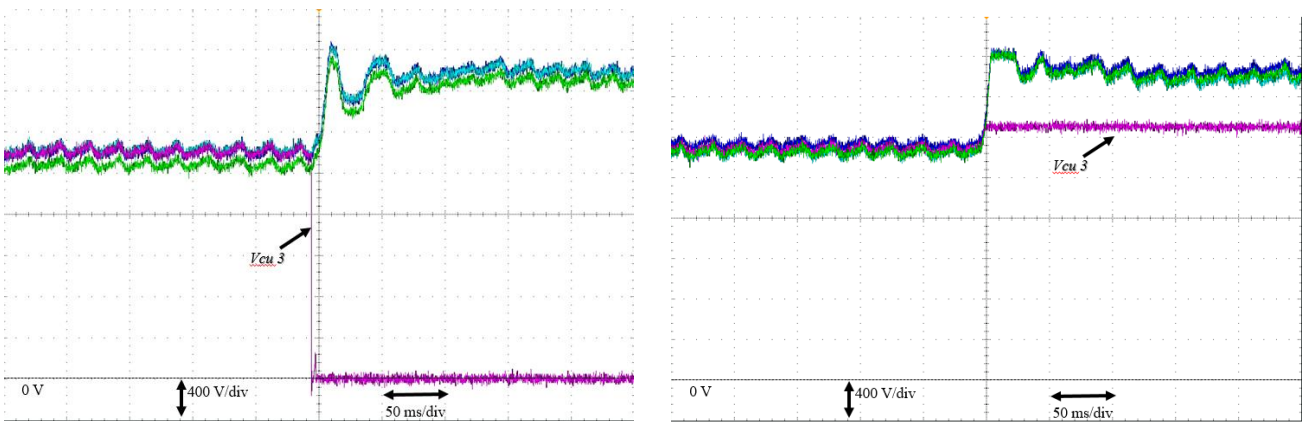
The main aim of building a HIL platform is its ability to assess any proposed control technique by determining whether or not it can be implemented industrially. In addition, the use of HIL simulations ascertains the feasibility of any developed algorithms. In terms of the proposed techniques for the HMMC inner control, fault detection and tolerant control algorithms, the great challenge in implementing these control functions is the required computational volume, since all of the tasks depend on the estimation of the capacitor voltages for all of the sub-modules, which may total at least 800 per leg. If the computational burden is too high, a computer with a very large processor is required. In this case the control technique would require code optimization and several reductions in the calculations. For this purpose, the computational burden of the simulated HMMC is presented. Based on this a conception is shown for a real HMMC project with 800 sub-modules per arm. The computational burden can be calculated with the number of logical resources consumed inside the FPGA. The building unit of an FPGA is its lookup table (LUT). The 4-input LUT is a small piece of RAM that is connected in the form of combinational logic to perform a specific function. The relationship between the 4 inputs and the outputs are simply a truth table, which is built through a synthesizing process.

The implementation of the proposed control on a cRIO virtex 5 based FPGA controller for controlling a HMMC with 8 modules per arm consumed 19,872 LUTs, with the physical controller having an embedded FPGA system with a maximum number of 28800 LUTs, which means that only 70% of the FPGA's resources are utilized. This means that when selecting a controller for an HMMC with 800 sub-modules per leg, applying the proposed control technique requires 1,987,200 LUTs. This can easily be achieved by using a VIRTEX 7s three FPGA controller, which has 2,000,000 LUTs inside its processing unit. Therefore, 99% of the logic capacity of the controller is utilized, which means the proposed control techniques can be implemented practically in terms of its computational burden.



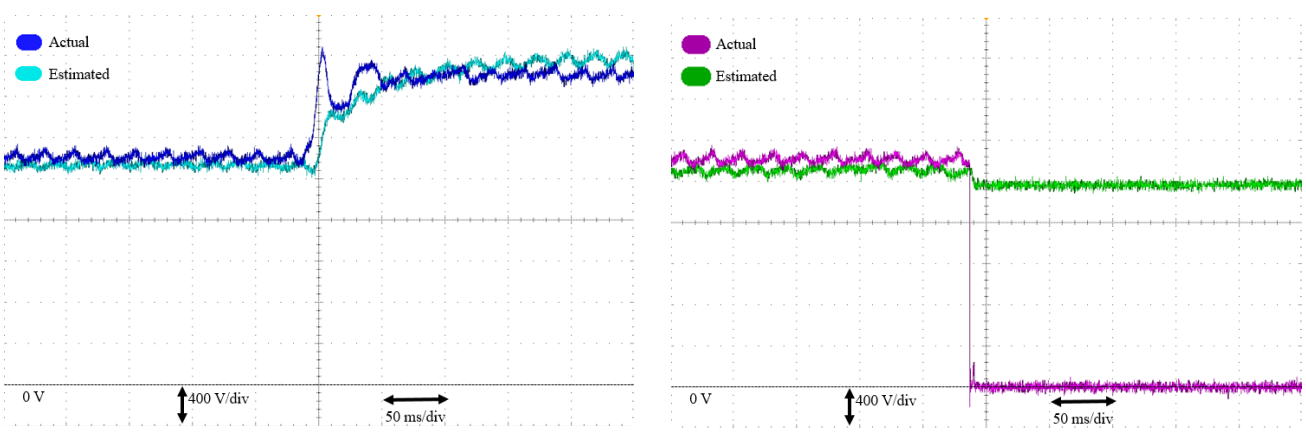
(a) (b)

Fig. 16. Waveforms under a short circuit fault: (a) three-phase voltages; (b) three-phase load currents.



(a) (b)

Fig. 17. Waveforms under a short circuit fault: (a) sub-module voltages of the upper arm in leg *a*; (b) sub-module voltages of the lower arm in leg *a*.



(a) (b)

Fig. 18. RLS estimated signals in the upper arm of leg *a* under a short circuit*:* (a) first sub-module (healthy); (b) third sub-module (faulty).

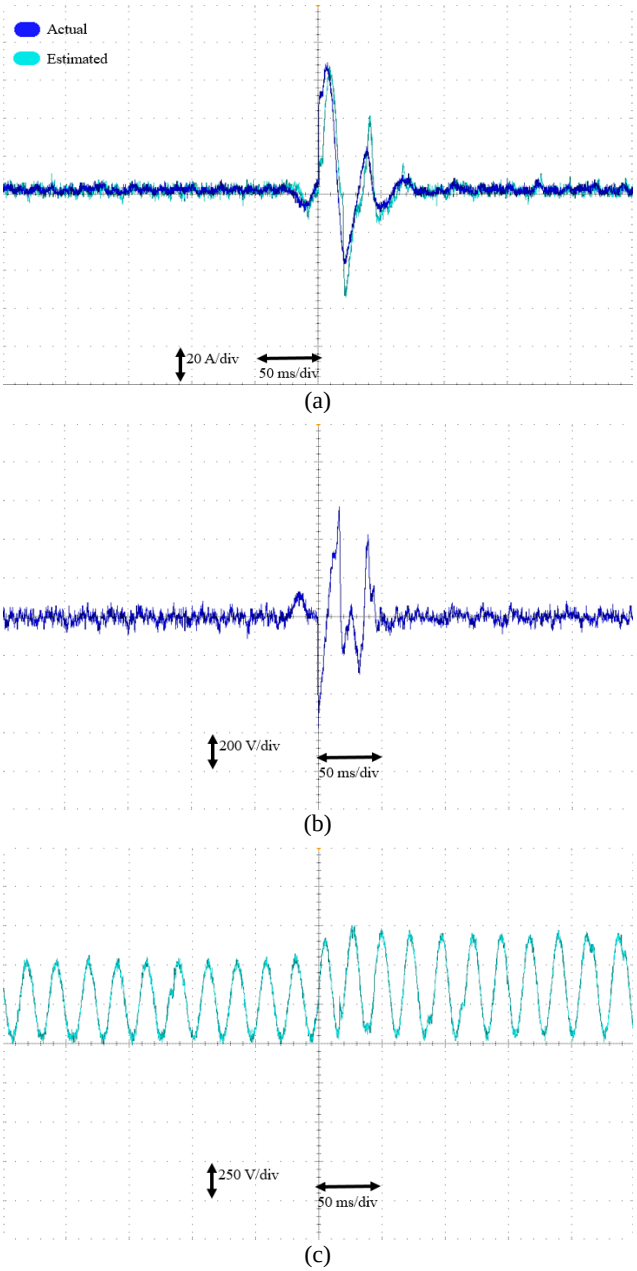


Fig. 19. Performance of different controllers under a short circuit fault: (a) circulating current; (b) averaging voltage reference; (c) modulating signal for the first sub-module of the upper arm of leg *a*.

VII. CONCLUSION

This paper presents a control scheme for the HMMC that does not need to sense the capacitor voltages to balance the DC voltages between sub-modules. A model of the HMMC is derived for the estimation of the capacitor voltages from the measured phase voltage, the arm reactors voltages, and the switching signals. An estimation unit is proposed for the capacitor voltages based on the RLS algorithm. Moreover, a hybrid estimation unit based on the ADALINE and RLS techniques for without sensing capacitor voltages of sub-modules is adopted to detect and identify faulty sub-modules. Furthermore, a FTCU is proposed to boost the capacitor voltages and to adjust the shift angles between carrier signals after isolating the faulty sub-modules to deal with the reduced number of effective sub-modules. One advantage of the proposed centralized strategy is the elimination of the sensors used to measure capacitors voltages and their required communication link. This action renders the proposed control scheme suitable for implementation with a low cost centralized controller for the HMMC. Additionally, the proposed FTCU does not require further elements. A real-time digital simulator connected to a physical controller is utilized to investigate the dynamic response of the proposed control system. The accurate performance and fast response of the proposed units for sub-modules capacitor voltage estimation are revealed from the results under different dynamic conditions. In addition, the proposed centralized strategy manages to balance the capacitors voltages. Furthermore, the circulating current follows its reference signal. The accurate operation of the proposed hybrid estimation based FDU results from the fact that decisions are based on the magnitude and rate of the change in the deviation among the estimated voltages from the proposed ADALINE and RLS techniques. Finally, the obtained results demonstrate the ability of the integrated FTCU to stabilize the operation of the HMMC under different fault conditions.

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