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Input Voltage Range Extension Method for Half-Bridge LLC Converters by Using Magamp Auxiliary Post-Regulator

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Abstract

An improved half-bridge LLC converter with a magamp auxiliary post-regulator is proposed in this paper. The function of the magamp is bypassed when the converter works within the low input-voltage range. Meanwhile, it operates as an auxiliary post-regulator when the input voltage is high. By changing the blocking time of the magamp, the dc gain of the converter can be extended. Hence, the input voltage range of the converter is extended. The realization of proposed topology does not require a complicated circuit. The controller of the magamp can be easily implemented using only passive components, transistors and an OP amp. The generalized operational principle is analyzed and the design criterion for the magamp is presented. Finally, a 25V output, 400W experimental prototype was built and tested for a 160–300V input-voltage range to verify the feasibility of the proposed method.

Key words: LLC converter, Magamp, Post-regulator, Resonance, Wide range

I. INTRODUCTION

LLC series resonant converters are very popular these days in applications such as adapters, PC power supplies and energy storage systems due to its advantages of high efficiency, high power density and simplicity [1]-[4]. Pulse frequency modulation (PFM) is generally used to control LLC converters. Thus, a wide input-voltage range usually requires a wide switching frequency variation range. However, the slope of the gain curve is extremely flat when the converter operates above the resonant frequency f_0, i.e., when the input voltage is high, the operating point moves far right away from f_0. This leads to a significantly increment of the switching loss, and even the output-voltage of the converter may not be regulated to the demanded range. Therefore, a tradeoff between the frequency variation range and the input voltage range are usually made in the conventional LLC converter design process.

To extend the input-voltage range of an LLC converter, the methods proposed in previous literatures can be cataloged into three groups: 1) precise modeling and parameter optimizing [5]-[7]; 2) multi-stage conversion [8], [9]; 3) topology morphing [10]-[13].

In [5], an accurate LLC converter model is used to estimate the peak gain point, which is useful for wide input-voltage range designs. However, this does not fundamentally change the gain characteristics of an LLC converter. The topology proposed in [8] combines an LLC resonant converter with a boost converter. The LLC converter operates in a relatively narrow frequency range, while the boost converter works with a constant output-voltage. This topology is not conducive to improving the power density of the converter. In [10], the converter works as a full-bridge (FB) LLC converter in the low input-voltage range. Meanwhile, for the high input voltage range, it is changed to a half-bridge (HB) LLC converter. However, its output exhibits severe overshoots/ undershoots at the topology transition instants. The control method proposed in [11] improved the idea in [10] by maintaining a tight regulation of the output during transitions. However, it

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is not suitable for applications that require a fast feedback response due to its long transition period. The topology reported in [12] employed a bidirectional switch which can halve the input-voltage of the resonant tank when a low voltage gain is needed. However, there are six MOSFETs which increase the complexity and the cost of the circuit. The topology proposed in [13], integrates two half-bridges in series to construct a three-level LLC converter, which can double the input voltage range. However, a potential voltage unbalance on the input capacitors may occur due to the mismatch of the switching periods and/or transformer windings. Furthermore, there is no simple method specifically for HB LLC converters in the literatures.

In order to overcome the problems mentioned above, an input voltage range extension method for HB LLC converters is proposed in this paper using magamp auxiliary post-regulators. The magamp has been well investigated for use in multiple output converters, including LLC converters [14]. In multiple output applications, magamp is used to distribute the conduction time for different outputs. The energy transmission between the primary side and the secondary side is not completely blocked. Unlike [14], for the proposed single output LLC converter, the magamp is used to completely cut off the energy exchange between the primary and secondary sides to change the dc gain curve of the converter. In the low input voltage range, the converter works as a conventional HB LLC converter. In the high input voltage range, the output voltage of the converter can be regulated by changing the blocking time of the magamp with a fixed switching frequency.

This paper is organized as follows. Section II analyzes the operating principle of the proposed converter in detail. Section III presents the characteristics and design consideration of the proposed converter. In section IV, an experimental prototype is built and tested to verify the theoretical analysis. Finally, section V gives the conclusion.

II. Proposed HB LLC Converter with Auxiliary Magamp Post-Regulator

A. Limitations of an LLC Converter in Wide Input-Voltage Range Applications

Traditional HB LLC converters usually change the switching frequency to regulate the output against input voltage changes. Frequency control is achieved by operating the switches with a constant duty cycle of approximately 0.5. A proper switching dead-time between the two switches is provided to achieve zero voltage switching (ZVS) [15]. The dc gain curve of an HB LLC converter according to fundamental harmonic approximation (FHA) is shown in Fig. 1. The converter is designed to work in the inductive region where the ZVS of the primary switches can be achieved over the entire input voltage condition. Since the input voltage of the converter is changed

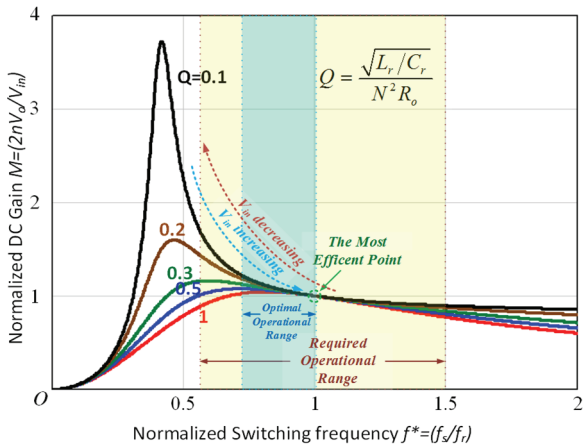


Fig. 1. DC Gain curve of a conventional HB LLC converter.

and the output current of the converter varies, the dc voltage gain value of the converter is changed. In order to meet the varied gain value, a conventional LLC converter can operate below or above the resonant frequency. As can be seen in Fig. 1, the dc gain increases as the frequency increases and the Q factor decreases, while the dc gain decreases when the frequency increases. The most efficient point occurs around the resonant frequency f_0. When the switching frequency f_s is lower than f_0, the lower f_s is, the larger the circulating current is. On the other hand, the switching losses increases as the frequency increases. When the switching frequency is above f_0, the rectification diodes D_1 and D_2 at the secondary side lose the ZCS condition. To meet an optimal frequency, the LLC converter should be operated under a very small frequency range around f_0, as illustrated in Fig. 1. On the other hand, a wide input voltage or load-current range requires a wide switching frequency range. In order to reduce the switching frequency variation range, a low K (denoted by h in some studies) [16], i.e., the inductor ratio (L_m /L_r), is typically used in the LLC converter design. However, the inductor L_m decreases as K becomes lower. Since a small L_m means an increase in the conduction loss, it is not beneficial to improve the efficiency of the converter.

B. Proposed Topology Description

The proposed HB LLC converter with magamp auxiliary post-regulator (LLC-MAP) is illustrated in Fig. 2(a). When compared with the conventional HB LLC converter, the proposed topology adds two magamps (S_{r1} and S_{r2}) in serial with the rectification diodes D_1 and D_2 respectively on the secondary side. Moreover, a switch S_W and a frequency limiter are added to the feedback loop. The "on/off" status of S_W is determined by the switching frequency f_s and the upper frequency limit f_{max}. In practice, f_{max} is set slightly smaller than f_0 to insure ZCS of D_1 and D_2. In the low input-voltage range, f_s is lower than f_0 and S_W is gated off. V_o is regulated by changing f_s the same as the conventional HB LLC converter. This state is called the variable-frequency mode (VF Mode). When the

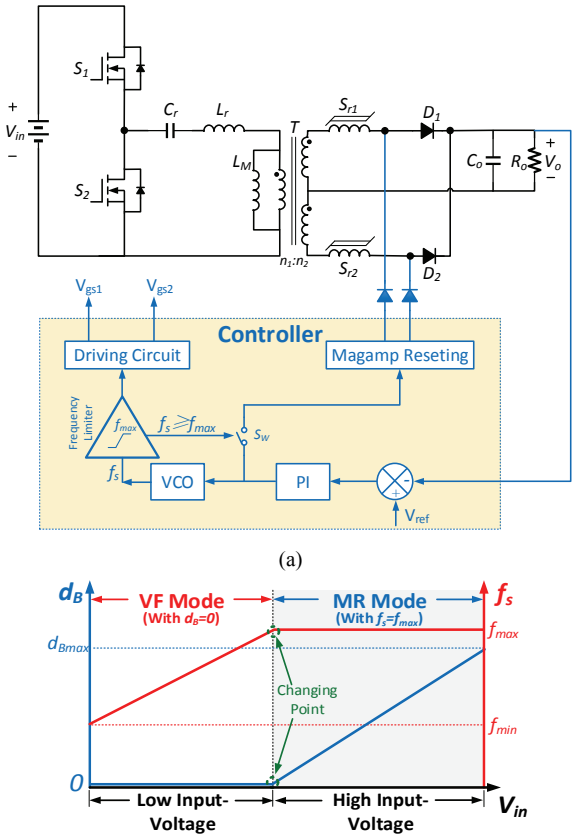


Fig. 2. Proposed topology: (a) LLC resonant converter with magamp post-regulator; (b) Conceptual control diagram of an LLC-MAP converter.

input-voltage increases, f_s moves up accordingly to reduce the dc gain of the converter. Once f_s meets the upper limit f_{max}, f_s is restricted to the constant value f_{max} and S_W turns on. Then V_o is regulated by the magamp regulator loop at a fixed-frequency as shown in Fig. 2(b). This state is called the magamp-regulation mode (MR Mode).

C. Operational Principle

As mentioned previously, the proposed LLC-MAP converter has different operational principle during different modes. In the VF mode, the magamps are equivalent to copper wires with very small impedances. The LLC-MAP converter has the same structure as a conventional HB LLC converter. The operational principle is also the same as that of a conventional HB LLC converter.

In the MR mode, as shown in the operational waveforms in Fig. 3, one switching cycle can be divided into eight stages. Equivalent circuits of the stages 1-4 are shown in Fig. 4. For convenience, the following assumptions should be made.

1) The output capacitor C_o is large enough to neglect the voltage ripple on V_o. Thus, V_o is assumed to be constant.

2) The parasitic capacitors of the primary switches and the junction capacitors of the secondary diodes are not shown in the circuit for the sake of simplicity.

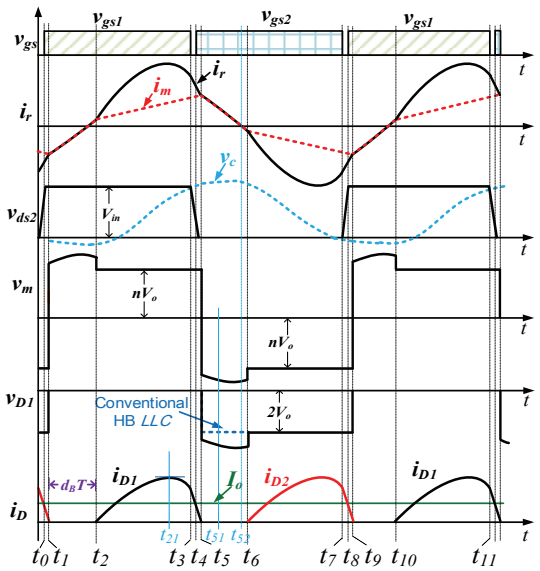


Fig. 3. Principle waveforms of an LLC-MAP converter in the MR mode.

Stage 1 [t_0-t_1] [see Fig. 4(a)]: Before t_0, the body diode of S_1 has conducted. The differential current between i_m and i_r feeds the load through D_2. At $t=t_0$, S_1 turns on under the ZVS condition. Due to forward biasing of D_2, the voltage across L_m is clamped by ($-nV_o$). Resonance occurs between L_r and C_r. The resonance frequency is $f_0 = 1/(2\pi\sqrt{L_r C_r})$. When i_m is equal to i_r at t_1, D_2 turns off under the ZCS condition.

Stage 2 [t_1-t_2] [see Fig. 4(b)]: S_{r1} was reset in the previous switching cycle. At $t=t_1$, a voltage (v_{Tsec}-V_o) appears across S_{r1} and D_1 in series. This is in the direction to drive the magamp core up towards the saturated state. There are only very small coercive current flows through S_{r1}. Thus, S_{r1} is equivalent to an "opened" switch. In the meantime, S_{r2} is reset by the voltage v_{Tsec}. On the primary side, resonance occurs between C_r and (L_m+L_r). The resonance frequency is $f_m = 1/[2\pi\sqrt{(L_r + L_m)C_r}]$. This stage ends when S_{r1} is saturated at t_2.

In this stage, the resonant current only circulates through the resonant tank and S_1, and there is almost no power transferred to the secondary side. Thus, this stage is named the blocking interval. The blocking time can be expressed as the following expression according to Faraday's Law:

$$t_B = t_2 - t_1 = \frac{n_{Sr}\Delta B A_e}{V_{T\,\mathrm{sec}}^B - V_0} \tag{1}$$

where n_{Sr} is the turn number of the magamp, A_e is the effective core area of the magamp core, ΔB is the magnetic induction intensity increment from the initial state to the saturated state, and $V_{T\,\mathrm{sec}}^B$ is the average voltage of v_{Tsec} during the blocking interval. The blocking duty ratio is d_B=$2t_B/T$.

Stage 3 [t_2-t_3] [see Fig. 4(c)]: At t_2, S_{r1} has been magnetized to the saturated state, and is equivalent to a "closed" switch. D_1

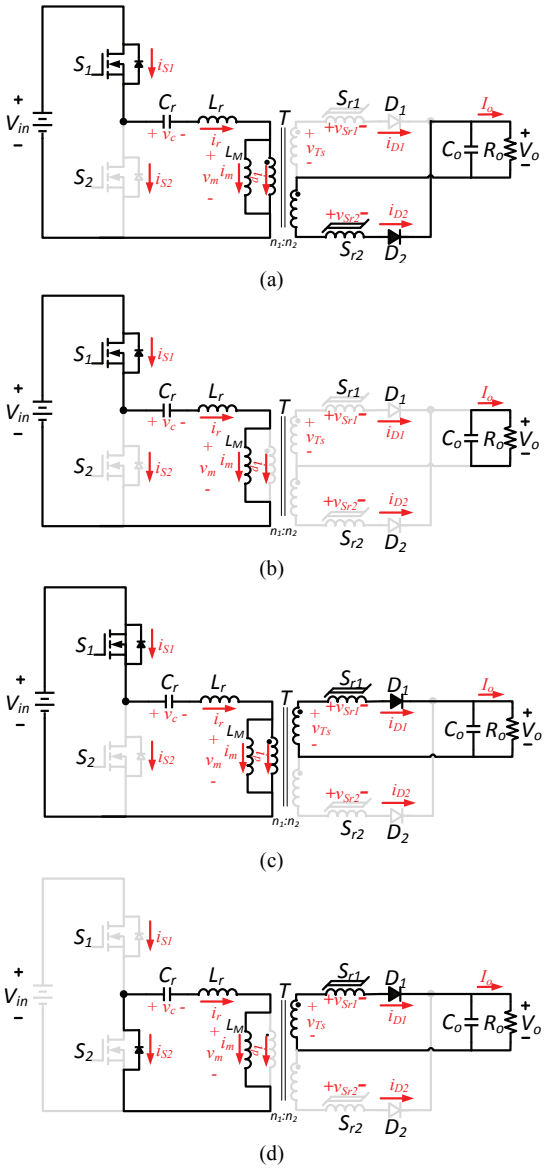


Fig. 4. Equivalent circuits of the proposed LLC-MAP converter: (a) [t_0-t_1]; (b) [t_1-t_2]; (c) [t_2-t_3]; (d) [t_3-t_4].

is forward biased and the primary side of the transformer is clamped by nV_o. Resonance occurs between L_r and Cr. The current i_r increases rapidly with a sinusoidal wave type, while i_m increases linearly. The deference between i_r and i_m is transfered to the secondary side. This stage is terminated at t_2 when i_r=i_m.

Stage 4 [t_3-t_4] [see Fig. 4(d)]: At t_3, S_1 is turned off. The parasitic capacitance of S_1 is charged by the resonant current and the drain-source voltage of S_1 increases. In the meantime, the parasitic capacitance of S_2 is discharged until its body-diode conducts. Then the ZVS turning on condition for S_2 can be achieved.

Due to symmetry, the operation stages 5-8 are the same as 1-4 except that the resonance is initiated by the storage energy in the resonant capacitor C_r.

III. Characteristics and Design Considerations

A. DC Voltage Gain

In this paper, the normalized input-to-output dc voltage gain of the LLC-MAP converter is defined as:

$$M = \frac{2nV_0}{V_{in}} \tag{2}$$

Since the proposed HB LLC converter should operate below or close to the limit frequency f_{max} in the VF mode, as shown in Fig. 2, the FHA approach can be used for the dc gain analysis of the converter. This means that only the fundamental component of the input square wave is effective for transferring energy to the output. At this state, the dc voltage gain of the LLC-MAP is the same as that of a conventional HB LLC converter as shown in Fig. 5(a).

When the LLC-MAP converter works in the MR mode, the switching frequency is fixed at $f_s = f_{\max} \cong f_0$. It is obvious that M=1 if d_B=0, and that M=0 if d_B =1. Therefore, it is easy to understand that the output voltage is proportional to d_B, and that the voltage gain can be continuously regulated to between 1 and 0 by varying d_B between 0 and 1. Next, an accurate derivation of the dc gain is made for the MR mode. Because there are more high-order harmonics that cannot be neglected when the LLC-MAP converter works in the MR mode, the FHA method is not accurate enough. Hence, the steady-state method is employed in the following derivation process. In order to simplify the analysis in this section, normalized variables are used in the following expressions. Define the voltage, current, and frequency bases as:

$$\begin{cases} V_{\text{BASE}} = nV_o \\ I_{\text{BASE}} = nV_o / Z_r \\ f_{\text{BASE}} = f_r \end{cases} \tag{3}$$

where the characteristic impedance of the converter is $Z_r = \sqrt{L_r / C_r}$. In the following description, x^* is the normalized value of x, i.e., x^*=x/x_{BASE}. Therefore, i_r^*, i_m^* and v_C^* are the normalized values of the inductor current i_r, i_m and the capacitor voltage v_C.

In stage 1, the expressions of i_r, i_m and v_C can be normalized as:

$$\begin{cases} i_{r1}^*(\theta) = I_{r1}^* \sin(\theta + \theta_{10}) \\ i_{m1}^*(\theta) = I_{m1}^* - \dfrac{\theta}{m-1} \\ v_{C1}^*(\theta) = \dfrac{1}{M} + 1 - I_{r1}^* \cos(\theta + \theta_{10}) \end{cases} \tag{4}$$

Where $\theta = 2\pi f_0 t$, $m = (L_m + L_r)/L_r$ and θ_{10} is the initial phase angle in stage 1. I_{r1} and I_{m1} are the initial values of i_r and i_m in stage 1.

In stage 2, the expressions of i_r, i_m and v_C can be normalized as:

$$\begin{cases} i_{r2}^*(\theta)=i_{m2}^*(\theta)=I_{r2}^*\sin(\dfrac{\theta}{\sqrt{m}}+\theta_{20}) \\ v_{C2}^*(\theta)=\dfrac{1}{M}-\sqrt{m}I_{r2}^*\cos(\dfrac{\theta}{\sqrt{m}}+\theta_{20}) \\ v_{m2}^*(\theta)=\dfrac{(m-1)I_{r2}^*}{\sqrt{m}}\cos(\dfrac{\theta}{\sqrt{m}}+\theta_{20}) \end{cases} \tag{5}$$

where θ_{20} is the initial phase angle in stage 2. I_{r2} is the initial value of i_r and i_m in stage 2.

In stage 3, the expression of i_r, i_m and v_C can be normalized as:

$$\begin{cases} i_{r3}^*(\theta)=I_{r3}^*\sin(\theta+\theta_{30}) \\ i_{m3}^*(\theta)=I_{m3}^*+\dfrac{\theta}{m-1} \\ v_{C3}^*(\theta)=\dfrac{1}{M}-1-I_{r3}^*\cos(\theta+\theta_{30}) \end{cases} \tag{6}$$

where is the initial phase angle in stage 3. I_{r3} and I_{m3} are the initial values of i_r and i_m in stage 3.

For the sake of simplicity, stage 4, which is short enough, is neglected in the dc gain analysis. Each of the operating phases is limited by the boundary conditions at the connection and switching moments of their adjacent phases. The current flows through the inductor and the voltage across the capacitor should maintain continuity between the two stages. Thus, the continuity conditions can be expressed as:

$$\begin{cases} i_{r1}^*(\theta_1)=i_{r2}^*(0) \\ i_{m1}^*(\theta_1)=i_{m2}^*(0) \\ v_{C1}^*(\theta_1)=v_{C2}^*(0) \\ i_{r2}^*(\theta_2)=i_{r3}^*(0) \\ i_{m2}^*(\theta_2)=i_{m3}^*(0) \\ v_C^*(\theta_2)=v_{C3}^*(0) \end{cases} \tag{7}$$

For periodic operation, the ending values of i_r and i_m in stage 3 should be opposite their initial values in stage 1 due to symmetry in a half cycle, as shown in Fig. 3. Thus, the symmetry conditions are given by:

$$\begin{cases} i_{r3}^*(\theta_3)=-i_{r1}^*(0) \\ i_{m3}^*(\theta_3)=-i_{m1}^*(0) \end{cases} \tag{8}$$

Because there is a $V_{in}/2$ dc voltage bias on C_r for half-bridge converters, the symmetry condition of v_C is:

$$v_{C3}^*(\theta_3)=\frac{1}{M}-v_{C1}^*(0) \tag{9}$$

Only stage 1 and stage 3 are involved in the power delivery between the primary side and the secondary side in a half cycle. Thus, the normalized output power can be expressed as:

$$p_o^*=\frac{f_s^*}{\pi}\left[\int_0^{\theta_1}\left(i_{m1}^*-i_{r1}^*\right)d\theta+\int_0^{\theta_3}\left(i_{r3}^*-i_{m3}^*\right)d\theta\right] \tag{10}$$

The output power can also be expressed as:

$$p_o^*=V_o^*I_o^*=\frac{8Q}{\pi^2} \tag{11}$$

Substituting (11) into (10) yields:

$$\frac{8Q}{\pi}=\int_0^{\theta_1}\left(i_{m1}^*-i_{r1}^*\right)d\theta+\int_0^{\theta_3}\left(i_{r3}^*-i_{m3}^*\right)d\theta \tag{12}$$

Note that $\theta_1+\theta_2+\theta_3=\pi/f_s^*$. Therefore, it is possible to obtain:

$$d_B=1-(\theta_1+\theta_3)/\pi \tag{13}$$

By combining (4)-(9), (12) and (13) after a proper manipulation, the following simplified constrain equations can be derived:

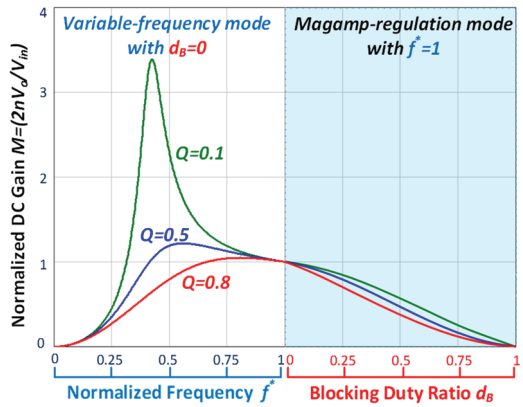
$$\begin{cases} I_{r1}^*\sin(\theta_1+\theta_{10})-I_{r2}^*\sin(\theta_{20})=0 \\ 1+\sqrt{m}I_{r2}^*\cos(\theta_{20})-I_{r1}^*\cos(\theta_1+\theta_{10})=0 \\ I_{r2}^*\sin(\theta_2/\sqrt{m}+\theta_{20})-I_{r3}^*\sin(\theta_{30})=0 \\ 1-\sqrt{m}I_{r2}^*\cos(\theta_2/\sqrt{m}+\theta_{20})+I_{r3}^*\cos(\theta_{30})=0 \\ I_{r3}^*\sin(\theta_3+\theta_{30})+I_{r1}^*\sin(\theta_{10})=0 \\ I_{r2}^*\sin(\theta_2/\sqrt{m}+\theta_{20})+I_{r2}^*\sin(\theta_{20})+(\theta_1+\theta_2)/m-1=0 \\ 1/M-I_{r3}^*\cos(\theta_3+\theta_{30})-I_{r1}^*\cos(\theta_{10})=0 \\ I_{r2}^*[\cos(\theta_{20})-\cos(\theta_2+\theta_{20})-\theta_2]-\theta_2^2/(2m-2)-8Q/\pi=0 \\ 1-d_B-(\theta_1+\theta_3)/\pi=0 \end{cases} \tag{14}$$

There are ten unknown variables (I_{r1}^*, I_{r2}^*, I_{r3}^*, θ_1, θ_3, θ_{10}, θ_{20}, θ_{30}, M and d_B) in the above function. Since (14) is a transcendental function, the results of M versus d_B cannot be directly obtained. When $m=7$ and $f_s^*=1$, by numerically solving the distribution equation (14) with the *fsolve(x)* function in MATLAB, the characteristics of M versus d_B can be depicted for different values of Q as shown in Fig. 5(a). As can be seen, when d_B is zero, the converter works as a traditional HB LLC converter if the initial blocking time of the magamp is neglected. When d_B is 1, there is no energy transferred to the load when the transformer works in the open state. The quality factor Q has a slight effect on the dc gain, and the dc gain is mainly determined by d_B.

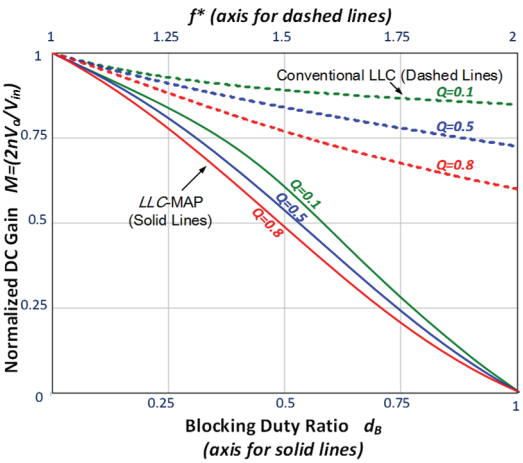
A comparison between the LLC-MAP converter in the MR mode and the conventional LLC converter is illustrated in Fig. 5(b). As can be seen, a much higher frequency is needed in the conventional LLC converter when the same dc gain is required. In addition, it is not sensitive to Q, the output load in other words, when the LLC-MAP converter works in the MR mode.

B. Design of the Magamp Auxiliary Post-Regulator

As shown in Fig. 6(a), a current reset circuit can be adopted for the magamp due to a reduced phase delay and no need for negative voltage power [17]. The blocking time of the magamp is regulated by means of its resetting current I_{rst}, which is proportional to the error voltage v_{EA}. As can be seen



(a)



(b)

Fig. 5. Voltage gain curves of: (a) Proposed LLC-MAP converter; (b) Comparison between the LLC-MAP converter and the conventional HB LLC converter.

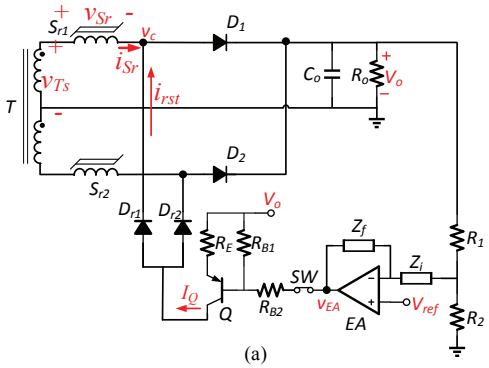
in Fig. 6(b), during [t_5-t_{51}], the magamp current i_r decreases from zero to I_{rst} almost linearly. The diode D_{r1} conducts. Therefore, v_{Sr}=v_{Tsec}. When i_r reaches I_{rst} at t=t_{51}, v_{Sr} decrease to zero exponentially. The decreasing transient interval is relatively short and can be neglected. The magamp inductor reset is finished at t=t_{51}. The relationship between unsaturated inductance of the magamp L_{Sr}^{unsat} and I_{rst} is:

$$L_{Sr}^{unsat} = \frac{V_{T\,\mathrm{sec}}^{rst} t_{rst}}{I_{rst}} \tag{15}$$

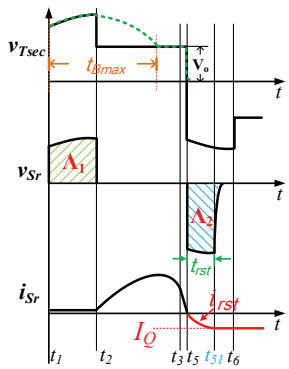
where, $V_{T\,\mathrm{sec}}^{rst}$ is the average voltage of v_{Tsec} during the resetting interval. The volt-second balance during the blocking and resetting intervals yields:

$$(V_{T\,\mathrm{sec}}^{B} - V_0)\cdot t_B = V_{T\,\mathrm{sec}}^{rst} t_{rst} \tag{16}$$

i.e., $\Lambda_1 = \Lambda_2$ in Fig. 6(b). It should be noted that, at the blocking interval, v_{Sr}=v_{Tsec}-V_o should be positive to ensure that the magamp core can reach saturation. The maximum t_B can be achieved when v_{Sr}=0. A proper magamp core can be selected according to its maximum blocking time and unsaturated inductance.



(a)



(b)

Fig. 6. Operating principle of the magamp: (a) Resetting circuit of the magamp; (b) Key waveforms for the magamp regulator.

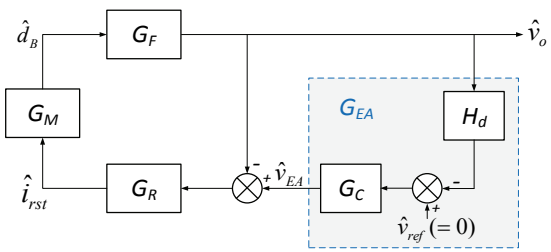


Fig. 7. Control block diagram of the magamp post-regulator in the LLC-MAP converter.

C. Design of the Feedback Controller

Small signal control block diagrams for the magamp post-regulator in the *LLC*-MAP converter are illustrated in Fig. 7, where the ^ sign denotes the small-signal ac quantity, G_R presents the reset circuit transfer function, G_M presents the magnetic modulator transfer function, and G_F presents the duty cycle to output the voltage transfer function.

According to the specific circuit in Fig. 6(a), by equating the ac perturbation quantities in the small-signal model, the gain of each of the blocks can be exacted as:

$$G_R = \frac{\hat{i}_{rst}}{\hat{v}_o - \hat{v}_{EA}} = \frac{-R_{B1}}{(R_{B1}+R_{B2})R_E} \tag{17}$$

$$G_M = \frac{\hat{d}_B}{\hat{i}_{rst}} = \frac{L_{sr}^{unsat} f_s}{V_{Ts} - V_o} \tag{18}$$

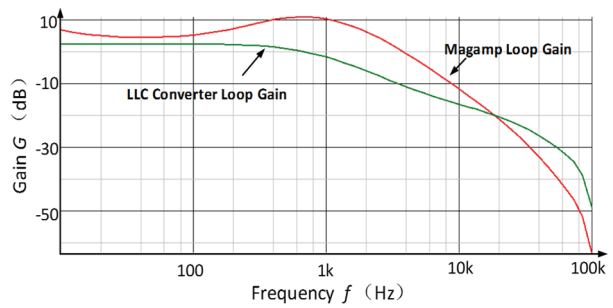


Fig. 8. Comparison of the open loop gain curves between the magamp loop and the LLC loop.

$$G_F = \frac{\hat{v}_o}{\hat{d}_B} = \frac{sR_oV_{Ts}}{s^2R_oL_{sr}^{sat}C_o + sL_{sr}^{sat} + R_o} \tag{19}$$

where, L_{sr}^{sat} is the inductance of the saturated magamp. The open loop transfer function of the magamp post-regulator can be expressed as:

$$G_{VC\_MAG} = \frac{\hat{v}_o}{\hat{v}_{EA}} = \frac{G_RG_MG_F}{1 + G_RG_MG_F} \tag{20}$$

Given specific parameters, as shown in Fig. 8, a comparison of the open loop gain curves between the magamp loop and the LLC loop can be obtained by a mathematic tool. As can be seen, the two loops exhibit strong intersections. In other words, the magamp post-regulator can share a controller with the LLC loop. In practice, the compensator parameters need to be selected based on the worst case of the bandwidth.

D. Loss Analysis of the Magamp

As mentioned previously, the output diode turns off under the ZVS condition. The dead-time problem of the magamp is neglectable in the LLC converter [14]. In the VF mode, the reset current is zero and the magamp is equivalent to a short circuit. There is only the copper loss introduced into the converter. The power dissipated in the magamps can then be written as:

$$P_{Mag}^{Cu} = \frac{I_o^2\rho n_{Sr}M_{LT}}{A_W} \tag{21}$$

where ρ is the wire resistivity, M_{LT} is the mean length per turn of the winding, and A_W is the size of the wire. Since the winding of the magamp is only a few turns, in the total loss, the copper loss accounts for no more than 0.3% in the experimental prototype.

In the MR mode, the core loss of the magamp should also be considered. It can be expressed as:

$$P_{Mag}^{Core} = 2\Delta BH_RA_Cl_mf_s \tag{22}$$

where $\Delta B = (V_{T\sec}^B - V_0)\cdot t_B$, H_R is the coercive force needed for the reset, A_C is the core cross-sectional area, and l_m is the length of the magnetic path. The core loss data in W/kg as a function of the flux density and the frequency can also be found in datasheets in the form of a table or an equation. After giving the specific parameters of the prototype, the loss reaches the maximum proportion, which is about 0.9% at the maximum blocking time.

In the VF mode, the LLC-MAP converter fully inherits the high efficiency advantages of the conventional LLC converter. In the MR mode, despite the conversion efficiency decreases caused by the magamp core loss, a wide input-voltage range can be achieved without varying the switching frequency in a wide range, which reduces the switching losses. Therefore, the efficiency impact of the two magamps is affordable.

In summary, when the input-voltage is within the working range of the traditional LLC, the conversion efficiency of the LLC-MAP is basically the same. When the input voltage is out of the working range of the traditional LLC, the LLC-MAP converter makes a tradeoff for a wider input-voltage range with acceptable losses increase.

E. Performance Comparison

The proposed method gives a hint that the input-voltage range of an LLC converter may also be regulated through the secondary-side post-regulator. Although adding two magamps leads to additional cost, the proposed converter uses two MOSFETs less than the primary-side variable-structure LLC converters presented in [13]-[15]. The price of a magamp in this application is roughly equal to the price of a MOSFET. However, the proposed control circuit only adds several diodes, transistors and resistors to the control circuit, while a more expensive digital processor and isolated MOSFET drivers should be employed in a primary-side variable-structure. Therefore, considering the entire system, the proposed method has a price advantage.

On the other hand, primary-side variable-structures usually suffer from overshoot/undershoot problems on the output during mode transitions. In general, to overcome these problems, some complex algorithms have been applied. In the LLC-MAP converter, the LLC loop and the magamp loop have essentially the same frequency-response characteristics. Both of them can share a feedback controller, which is very simple. This gives the converter the advantage of a fast response. Therefore, during mode transitions, the output voltage can be smoothly regulated.

It should be noted that each of the solutions has advantages and disadvantages. The structure proposed is a good candidate for a wide input analog-controlled LLC converter. The LLC-MAP converter can be combined with a primary-side variable-structure to further extend the operational range in a future work.

IV. Experimental Performance Evaluation

A laboratory prototype is built to verify the performance of the proposed converter. The main parameters of the prototype

TABLE I
KEY PARAMETERS OF THE CONVERTER

Component	Parameter
L_r	20μH
C_r	150nF
L_m	120μH
S_1 and S_2	Infineon's IPP50R199CP
D_1 and D_2	ST's STPS41L60CT
n	13:3
Magamp core	VAC W481
n_{Sr}	11ts
LLC Controller	TI's UCC25600

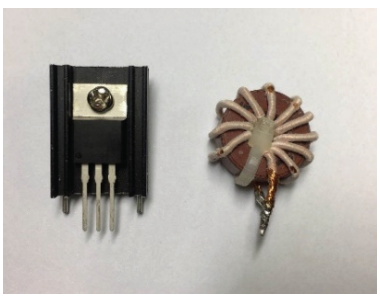


Fig. 9. Size comparison between a magamp and a MOSFET.

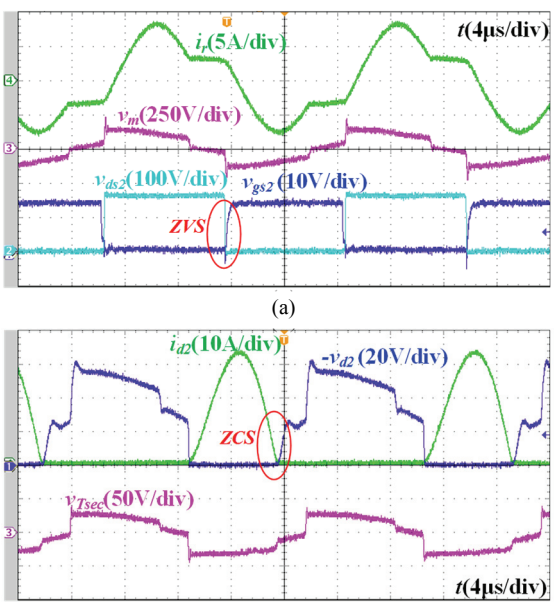


Fig. 10. Switching waveforms in the VF mode: (a) i_r, v_m, v_{gs2} and v_{ds2}; (b) i_{d2}, v_{d2} and v_{Tsec}.

are shown as follows: V_{in}=160-300V, V_o=25V, output power P_o=400W and f_0=92kHz. The key components of the prototype are shown in Table I. The diameter of the magamp core is 15.5 mm and the height is 5.7 mm. A size comparison between a magamp and a MOSFET with a TO-220 package is shown in Fig. 9.

Fig. 10(a) and Fig. 10(b) show steady state experimental waveforms of the LLC-MAP converter in the VF mode with V_{in}=160V and I_o=16A. As shown in these waveforms, S_1 and S_2 operate under the ZVS condition and the full ZCS of D_1 and D_2 have been achieved.

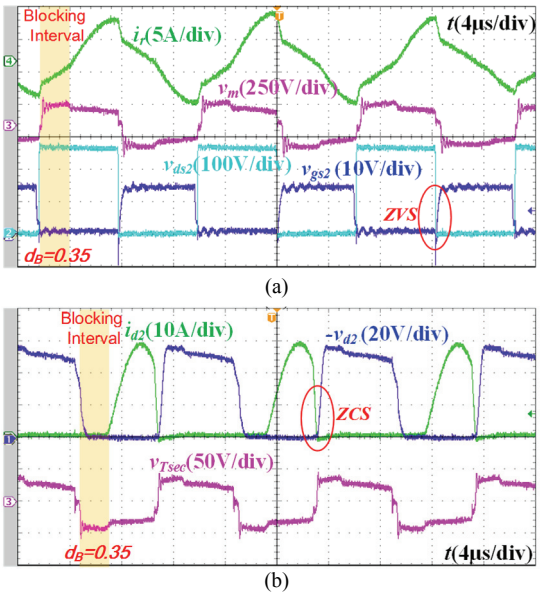


Fig. 11. Switching waveforms in the MR mode: (a) i_r, v_m, v_{gs2} and v_{ds2}; (b) i_{d2}, v_{d2} and v_{Tsec}.

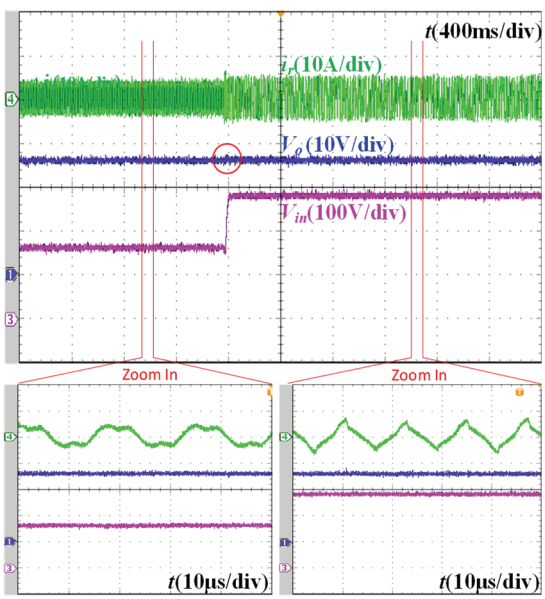


Fig. 12. Experimental waveforms of mode transitions.

Fig. 11(a) and Fig. 11(b) show steady state experimental waveforms in the MR mode with V_{in}=300V and I_o=15A. As can be seen, the blocking ratio d_B is 0.35. S_1 and S_2 operate under the ZVS condition. Since the slope of the current flowing through D_2 in the MR mode is greater than that in the VF mode, D_2 has a slight reverse recovery current. However, due to the current limiting effect of the primary side resonant inductor L_r, the reverse recovery of D_2 is negligibly small. It is still considered that D_1 and D_2 satisfy the ZCS condition. These waveforms are well matched with the analysis.

Dynamic waveforms with input-voltage steps from 160V

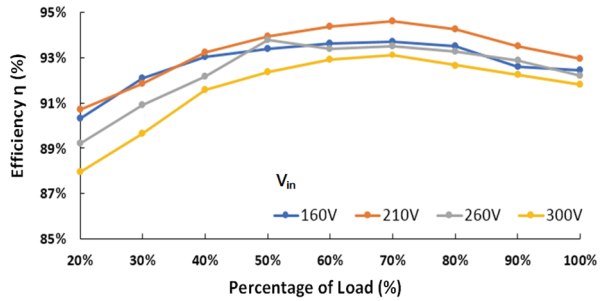


Fig. 13. Measured efficiency with different values of V_{in}.

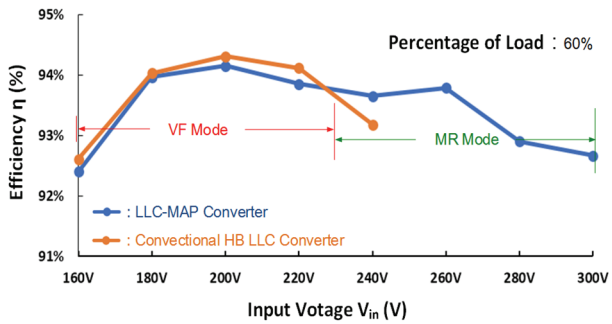


Fig. 14. Efficiency Comparison.

up to 280V are shown in Fig. 12. The overshoot of the output, which is about 2% of the output regulation, is extremely small. This indicates a good performance between the mode transition periods since the magamp loop and the LLC loop share the same controller.

Efficiency curves tested under different loads are shown in Fig. 13. When the input voltage varies from 160V to 300V, the highest efficiency is up to 94.6%. The best efficiency curve is obtained when V_{in}=210V since both the switching losses and conduction losses achieve an optimal balance. When the input voltage is 160V, the inverter operates in the VF mode within the full load range. Correspondingly, when the input voltage is 300V, the LLC-MAP converter operates in the MR mode within the full range. Moreover, since the conduction loss associated with the circulation current and the loss of the magamp increase when a wide input-voltage range is covered by the MR mode, the curve at 300V is below the one at 210V. However, in practical applications, the converter usually operates at half load or 3/4 load. Even if the input voltage is 300V, the efficiency of the converter is still above 92%.

Fig. 14. shows an efficiency comparison between the LLC-MAP converter and the conventional HB LLC converter at a 60% load with the same key parameters. The LLC-MAP converter setting f_{max} is 100 kHz. Since the maximum frequency of the utilized controller chip is 350 kHz, the upper limit of the operating frequency of the conventional HB LLC converter is about 340 kHz. The measured efficiency of the conventional HB LLC converter is approximately 0.3% higher than the LLC-MAP converter in the VF mode region. This difference can be attributed to the copper loss of the magamp auxiliary post-regulator. At 240V, the efficiency of the conventional HB LLC converter is lower than that of the LLC-MAP converter due to the increasing of the switching loss since the converter operates at a very high frequency. A conventional HB LLC converter cannot regulate the output when the input-voltage is higher than 240V due to limitations on the switching frequency. However, the LLC-MAP converter switches to the MR mode as early as when the input voltage is 230V. In the MR mode region, since V_{in} increases, t_B increases accordingly. As a result, the increment of the core loss of the magamp leads to a reduction in efficiency. However, the overall efficiency is still high. To improve the efficiency, a synchronous rectifier can be used in the converter. It should be noted that this is a compromise between the conversion efficiency and the operational voltage range.

The input-voltage range of the proposed LLC-MAP converter is 1.75 times that of the conventional HB LLC converter. The proposed converter can be combined with the primary-side topology morphing solutions to further extend the operation ranges of the conventional LLC resonant converter.

V. Conclusions

A very simple method for extending the input-voltage range of a HB LLC resonant converter has been proposed and verified in this paper. In comparison with the conventional HB LLC converter, magamp auxiliary post-regulators are added. Duty cycle control of the magamp post-regulator is applied to the converter when a dc gain smaller than unity is needed for the high input-voltage range. This method can narrow the switching-frequency range of a converter. ZVS have been achieved for the primary switches and ZCS has been realized for the secondary diodes. Experimental results from a laboratory prototype verify the effectiveness and feasibility of the proposed solution.

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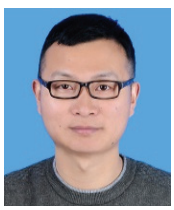

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