JPE 19-1-6

https://doi.org/10.6113/JPE.2019.19.1.58
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

# Multi-Output LED Driver Integrated with 3-Switch Converter and Passive Current Balance for Portable Applications

Sen Song*, Kai Ni*, Guipeng Chen**, Yihua Hu*, and Dongsheng Yu†

*Department of Electrical Engineering and Electronics, University of Liverpool, Liverpool, ENG, UK
**School of Aerospace Engineering, Xiamen University, Xiamen, China
†School of Electrical and Power Engineering, China University of Mining and Technology, Xuzhou, China

**Abstract**

This study presents a new portable eight-output light emitting diode (LED) driver. The eight output-channels are divided into two equal groups, and their output powers can be controlled individually by three active switches. In addition, a simple capacitor-based passive current balancing circuit (CBC) is employed in each port to guarantee that the currents of the four LEDs are the same. When compared with the conventionally used separate two-output isolated converters, the proposed one uses one less active switch. Moreover, zero-voltage-switching (ZVS) is achieved, which improves the power efficiency of the driver. Finally, a highly compact prototype is built, which can reach an efficiency of 94.6%.

**Key words:** Multiple outputs, Passive current balance, Reduced switches, Zero-voltage-switching (ZVS)

## I. INTRODUCTION

The light emitting diode (LED) has enormous potential in replacing conventional lamps in residential, automotive, decorative and medical applications due to its advantageous features such as high power density, high luminous efficiency, long lifespan, mercury free nature and quick response [1], [2]. For high illuminance application scenarios, numerous LEDs are connected in series or parallel. For series-connected LEDs, a high voltage stress is caused on the output capacitor and other insulation components. For parallel-connected LEDs, regulating the current through different LED strings requires current balancing technology due to the LED's current-voltage characteristic and negative temperature coefficient [3].

Achieving a high power efficiency while maintaining high compactness of the whole system is still a challenge for LED drivers. The authors of [4] removed the output capacitor of the buck converter to achieve a high power density, which decreases the power efficiency to under 90%. The authors of [5] used a switched capacitor converter (SCC) to drive LEDs, whose efficiency can only reach around 85%, in spite of the systems simple structure. Fortunately, from the analysis of a SCC [6], [7], significant power losses can be avoided by employing inductors. In [8]-[10], the flyback converter has a simple structure. To increase its power efficiency, different types of snubbers are utilized. However, all of them have their deficiencies. For instance, the active snubber in [8] and the TCR snubber in [9] increase the circuit complexity and cost. The RCD snubber in [10] cannot recycle the leakage inductance power, which leads to hard-switching and causes massive switching losses. With at least two more inductors, the LLC [11], [12] and CLCL topologies [13] can improve the power efficiency by achieving soft-switching operation of the active switches. These projects improve the power efficiency with a sacrifice in terms of compactness, which is not an ideal trade-off.

Current regulating for different LED strings can be achieved by applying active current balancing circuits (CBCs) [14], [15] and passive CBCs [16]-[19]. The active method demands at least one active switch for each output channel,

Manuscript received Apr. 20, 2018; accepted Nov. 10, 2018
Recommended for publication by Associate Editor Fuxin Liu.
†Corresponding Author: dongsiee@163.com
Tel: +86 516 83592000, China Univ. Mining & Tech.
*Dept. of Electrical Eng. & Electron., University of Liverpool, UK
**School of Aerospace Engineering, Xiamen University, China

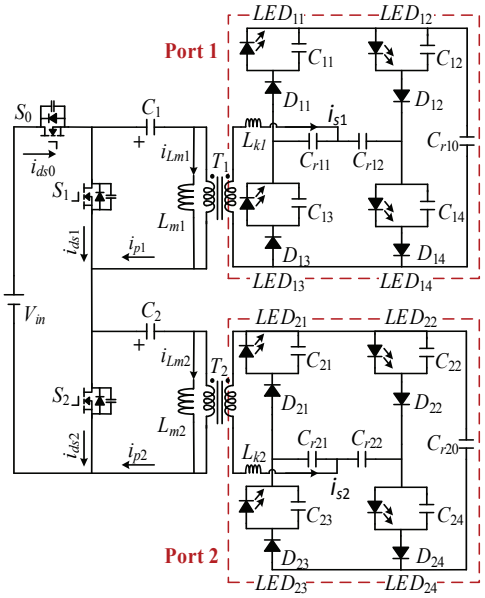



Fig. 1. Equivalent topology of the proposed LED driver.

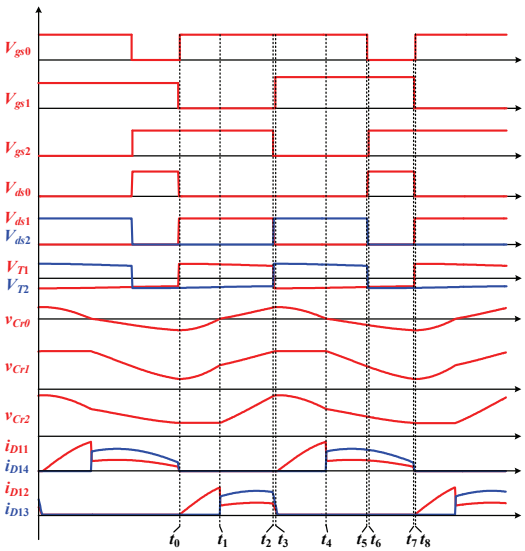



Fig. 2. Key waveforms of the proposed LED driver.

which results in a large switching loss. To avoid high costs and power losses, most current products adopt passive methods, which can be realized by employing inductors [16], [17] or capacitors [18], [19]. The inductor-based method uses transformers to balance the currents through different branches. However, deviations of transformers and the output voltages reduce the balance accuracy. The capacitor-based method can provide precise current balancing with a high power density and a low cost.

This study designs an LED driver with several merits. For instance, it has features such as multi-output, high power efficiency, controllable brightness and reduced component count. With these advantages, the driver is suitable for high power portable applications such as camping lights, vehicle headlights, emergency lights, etc. The topology of the proposed LED driver is shown in Fig. 1.

This paper is organized as follows. Section II analyses the operation modes of the circuit. Section III discusses some of the main features of the topology. Section IV introduces a design guide for the proposed topology. Section V presents some experiment results. Section VI concludes the paper.

## II. Operation Mode Discussion

The operation principles are discussed in this section. As depicted in Fig. 1, the primary power stage consists of an input DC voltage $V_{in}$, three active switches $S_0$~$S_2$, two switched capacitors $C_1$~$C_2$, and two transformers $T_1$~$T_2$ with magnetic inductances $L_{m1}$~$L_{m2}$ as well as leakage inductances $L_{k1}$~$L_{k2}$. The three active switches, $S_0$, $S_1$ and $S_2$, control the two output ports: $S_0$&$S_1$ for Port 1, and $S_0$&$S_2$ for Port 2. The two ports are identical CBCs. More precisely, Port 1 has three resonant capacitors $C_{r10}$~$Cr_{12}$, four diodes $D_{11}$~$D_{14}$, four output capacitors $C_{11}$~$C_{14}$, and four LED-loads $LED_{11}$~$LED_{14}$.

Following assumptions are made to simplify the analysis.

1. All of the switches and diodes are ideal.
2. The transformers $T_1$ and $T_2$ are identical, with the same voltage ratio $n$:1 and secondary side referred leakage inductance $L_k$.
3. The input voltage is an ideal DC voltage.
4. The capacitance of the resonant capacitors $C_{r10}$, $C_{r11}$, $C_{r12}$, $C_{r20}$, $C_{r21}$ and $C_{r22}$ are equal.

   $C_{r10}$=$C_{r11}$=$C_{r12}$=$C_{r20}$=$C_{r21}$=$Cr_{22}$=$C_r$.
5. The voltages of the capacitors $C_1$~$C_2$ are constant.
6. The switches $S_1$ and $S_2$ have the same duty cycle, $D_{S1}$=$D_{S2}$=$D$.

Fig. 2 shows key waveforms corresponding to the eight operating modes depicted in Fig. 3. $V_{gs0}$-$V_{gs2}$ and $V_{ds0}$-$V_{ds2}$ are control signals and drain-to-source voltages of the switches $S_0$-$S_2$ respectively. $V_{T1}$-$V_{T2}$ are the primary voltages of the transformers $T_1$-$T_2$; $V_{Cr0}$-$V_{Cr2}$ are the voltages of the three resonant capacitors $C_{r10}$-$C_{r12}$; and $i_{D11}$-$i_{D14}$ are the currents through the diodes $D_{11}$-$D_{14}$. The two passive CBCs have similar operations. Thus, the operation of Port2 is not discussed.

According to the volt-second balance, the voltage across $C_1$~$C_2$ can be obtained.

$$V_C \cdot D \cdot T_s = (V_{in} - V_C) \cdot (1-D) \cdot T_s \quad (1)$$

$$V_C = V_{in}(1-D) \quad (2)$$

where $D = t_{on}/t_s$ and $t_{on}$ are the on-times of the switches $S_1$~$S_2$ in each switching cycle.

*Mode 1* [$t_0$–$t_1$]: At time $t_0$, the switch $S_0$ is turned on, and the switch $S_1$ is off. The voltage across the transformer $T_1$ is $V_{in}$-$V_c$. The current through $L_{m1}$ keeps increasing linearly until $t_2$.

$$i_{Lm1}(t) = \frac{V_{in} - V_C}{L_{m1}}(t - t_0) \quad (3)$$

At time $t_0$, the total voltage across $C_{r10}$, $C_{r11}$ and $C_{11}$ is lower than that of $C_{r12}$ and $C_{14}$.

$$v_{Cr10}(t_0)+v_{Cr11}(t_0)+V_{C11}<v_{Cr12}(t_0)+V_{C14} \tag{4}$$

Therefore, $D_{11}$ is forward biased to transfer power to the $LED_{11}$. Then $C_{r10}$ and $C_{r11}$ are charged. The state equations of this mode are obtained as:

$$\begin{cases} L_{k1}\dfrac{di_{S1}}{dt}=\dfrac{V_{in}-V_C}{n}-v_{Cr10}-v_{Cr11}-V_{C11} \\ i_{S1}(t)=i_{Cr10}(t)=i_{Cr11}(t) \\ i_{Cr10}(t)=C_{r10}\dfrac{dv_{Cr10}}{dt} \\ i_{Cr11}(t)=C_{r11}\dfrac{dv_{Cr11}}{dt} \\ i_{Cr12}(t)=0 \end{cases} \tag{5}$$

With Eq. (5), the secondary side current and the voltages across the capacitors $C_{r10}$, $C_{r11}$ and $C_{r12}$ can be calculated as:

$$\begin{cases} v_{Cr10}(t)=-\dfrac{\Delta v_{Cr-\mathrm{ini}}}{2}\cos\omega_a(t-t_0)+\dfrac{\Delta v_{Cr-\mathrm{ini}}}{2}+v_{Cr10}(t_0) \\ v_{Cr11}(t)=-\dfrac{\Delta v_{Cr-\mathrm{ini}}}{2}\cos\omega_a(t-t_0)+\dfrac{\Delta v_{Cr-\mathrm{ini}}}{2}+v_{Cr11}(t_0) \\ i_{S1}=i_{Cr11}(t)=\dfrac{\Delta v_{Cr-\mathrm{ini}}}{Z_n}\sin\omega_a(t-t_0) \end{cases} \tag{6}$$

where $\Delta v_{Cr\text{-}ini}=(V_{in}-V_C)/n-v_{Cr10}-v_{Cr11}-V_{C11}$ is the voltage across the leakage inductance $L_{k1}$ at time $t_0$. $Z_n$ is the characteristic impedance of the resonant tank formed by $L_{k1}$, $C_{r10}$ and $C_{r11}$; and $\omega_a$ is the resonant angular frequency. $Z_n=\sqrt{L_k/0.5C_r}$ and $\omega_a=1/\sqrt{0.5L_kC_r}$. At time $t_1$, the total voltage across $C_{r10}$, $C_{r11}$ and $C_{11}$ is the same as that of $C_{r12}$.

$$v_{Cr10}(t_1)+v_{Cr11}(t_1)+V_{C11}=v_{Cr12}(t_1)+V_{C14} \tag{7}$$

Then, $D_{14}$ is conducted. The time duration of Mode 1 is determined as:

$$\tau_1=\frac{1}{\omega_a}\arccos\left(\frac{(V_{in}-V_{C1})/n-v_{Cr12}(t_0)-V_{C14}}{\Delta v_{Cr-\mathrm{ini}}}\right) \tag{8}$$

*Mode 2* [$t_1$–$t_2$]: From $t_1$, $D_{14}$ begins to be forward biased, and the power is transferred to $LED_{11}$ and $LED_{14}$. In the secondary circuit, the resonant tank is composed of $C_{r10}$, $C_{r11}$, $C_{r12}$ and $L_{k1}$ in this mode. The state equation of Mode 2 is:

$$\begin{cases} L_{k1}\dfrac{di_{s1}(\mathrm{t})}{dt}=\dfrac{V_{in}-V_{C1}}{n}-v_{Cr10}-v_{Cr11}-V_{C11} \\ \qquad\qquad=\dfrac{V_{in}-V_{C1}}{n}-v_{Cr12}-V_{C14} \\ i_{s1}(\mathrm{t})=i_{Cr10}(\mathrm{t})+i_{Cr12}(\mathrm{t})=i_{Cr11}(\mathrm{t})+i_{Cr12}(\mathrm{t}) \\ i_{Cr12}(\mathrm{t})=C_{r12}\dfrac{dv_{Cr12}(\mathrm{t})}{dt} \\ i_{Cr10}(\mathrm{t})=C_{r10}\dfrac{dv_{Cr10}(\mathrm{t})}{dt}=i_{Cr11}(\mathrm{t})=C_{r11}\dfrac{dv_{Cr11}(\mathrm{t})}{dt} \end{cases} \tag{9}$$

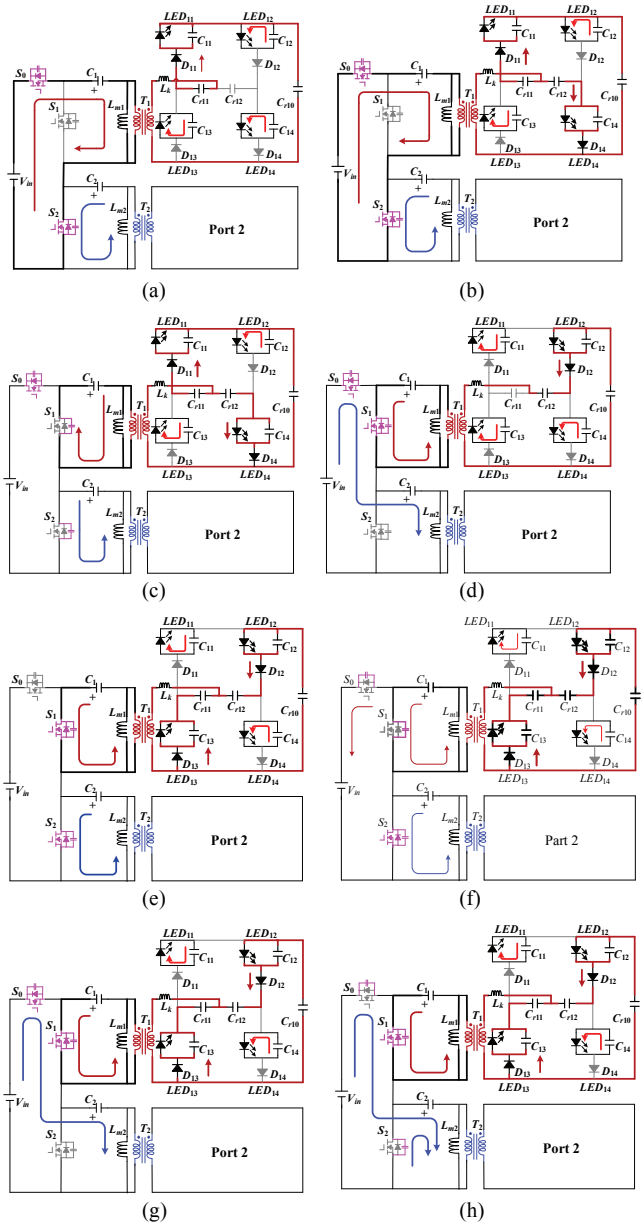



Fig. 3. Operation Modes 1-8 of the proposed LED driver: (a) Mode 1 [$t_0$-$t_1$]; (b) Mode 2 [$t_1$-$t_2$]; (c) Mode 3 [$t_2$-$t_3$]; (d) Mode 4 [$t_3$-$t_4$]; (e) Mode 5 [$t_4$-$t_5$]; (f) Mode 6 [$t_5$-$t_6$]; (g) Mode 7 [$t_6$-$t_7$]; (h) Mode 8 [$t_7$-$t_8$].

According to Eq. (9), the secondary current $i_{s1}$ is derived as:

$$\begin{aligned} i_{s1}(t)&=1.5i_{Cr1}=3i_{Cr2} \\ &=\frac{k\Delta v_{Cr-\mathrm{ini}}}{Z_n}\sin[\omega_b(t-t_1)+\theta] \end{aligned} \tag{10}$$

The time duration of Mode 2 is:

$$\tau_2=t_{off}-t_1 \tag{11}$$

where $t_{off}$ is the off-time of the switches $S_1$ and $S_2$; $k=\sin\omega_a\tau_1/\sin\omega b\tau_{com}$, $\theta=\pi-\omega b\tau_{com}$ is the initial phase of $i_s$ at $t_1$, $\omega_b=1/\sqrt{1.5L_kC_r}$ is the resonant angular frequency according to Fig. 3(b), and $\tau_{com}=t_{com}-t_1$. Where $t_{com}$ is the time taken for

the resonant tank to achieve completing resonance, and $t_{com}$ can be derived as:

$$t_{com} = \tau_{\text{com}} + \tau_1 = \frac{\pi-\theta}{\omega_b} + \frac{1}{\omega_a}\arccos\left(\frac{(V_{in}-V_{C1})/n - v_{Cr12}(t_0) - V_{C14}}{\Delta v_{Cr-\text{ini}}}\right) \quad (12)$$

*Mode 3* [$t_2$–$t_3$]: $S_2$ is turned off at time $t_2$. During Mode 3, the parasitic capacitor of $S_1$ is discharged while the parasitic capacitor of $S_2$ is charged. The voltage across $S_1$ drops from $V_{in}$ to zero to achieve ZVS turn-on. The resonant processes of the power stage are given below.

$$\begin{cases} L_{m1}\dfrac{di_{Lm1}}{dt} = v_{ds1}(t) - V_{C1} \\ L_{m2}\dfrac{di_{Lm2}}{dt} = V_{in} - v_{ds2}(t) - v_{ds1}(t) - V_{C2} \\ i_{p2} - i_{p1} = 2C_S\dfrac{dv_{ds1}(t)}{dt} \end{cases} \quad (13)$$

where $C_s$ represents the parasitic capacitance of the active switches.

*Modes 4-5* [$t_3$–$t_5$]: At time $t_3$, the switch $S_1$ is turned on with ZVS. During Modes 4-5, the transformer $T_1$ is powered by the capacitor $C_1$, and the polarity of the voltage across $T_1$ is opposite that of Modes 1-3. The current through $L_{m1}$ keeps decreasing linearly.

$$i_{Lm1}(t) = i_{Lm1}(t_3) - \frac{V_{C1}}{L_{m1}}(t-t_3) \quad (14)$$

Modes 4-5 are similar to Modes 1-2 except that the three resonant capacitors given the reference of the capacitors here are discharged due to the reversed power flow direction. During Mode 4, $D_{12}$ is forward biased to transfer power from the input to $LED_{12}$. At $t_4$, $v_{Cr0}+v_{Cr2}+V_{C12}=v_{Cr1}+V_{C13}$, and $D_{13}$ is conducted when power is transferred to $LED_{12}$ and $LED_{13}$.

*Mode 6* [$t_5$–$t_6$]: $S_0$ is turned off at $t_5$. The energy stored in the parasitic capacitor of $S_2$ is released while the parasitic capacitor of $S_0$ is charged. The resonant process can be expressed as:

$$i_{s1}(t) = 1.5i_{Cr1} = 3i_{Cr2} = \frac{k\Delta v_{Cr-\text{ini}}}{Z_n}\sin[\omega_b(t-t_1)+\theta] \quad (15)$$

*Mode 7* [$t_6$–$t_7$]: At $t_6$, the switch $S_2$ is turned on with zero voltage. Mode 6 takes a relatively short. Thus, it can be neglected. Mode 7 is a continuation of Mode 5.

*Mode 8* [$t_7$–$t_8$]: $S_1$ is turned off at $t_7$. The parasitic capacitor of $S_0$ is discharged while the parasitic capacitor of $S_1$ is charged. The voltage across $S_0$ is decreased with the rising of the voltage across $S_1$. Therefore, at the start of the next switching cycle, $S_0$ can achieve ZVS. The resonant process in Mode 8 can be expressed by the following equations:

$$\begin{cases} L_{m1}\cdot\dfrac{di_{Lm1}(t)}{dt} = V_{in} - v_{ds0}(t) - V_{C2} \\ 2C_s\dfrac{dv_{ds1}(t)}{dt} = i_{p1}(t) \end{cases} \quad (16)$$

## III. Topology Characteristics Analysis

### A. Passive Current Balancing

By the charge balance of the resonant capacitors, the energy charged to $C_{r11}$ through $D_{11}$ in Modes 1-3 is equal to the energy discharged from $C_{r11}$ through $D_{13}$ in Modes 5-8. Because Modes 3, 6 and 8 are very short, they are ignored in this discussion. The balance of $C_{r11}$ is between Modes 1-2, 5 and 7. The average current of $D_{11}$ and $D_{13}$ in a switching cycle $T_s$ is:

$$i_{D11\text{-avg}} = \frac{Q_{11\_\text{ch}}}{T_s} = \frac{Q_{11\_\text{dis}}}{T_s} = i_{D13\text{-avg}} \quad (17)$$

where $Q_{11\_\text{ch}}$ is the energy charged to $C_{r11}$ in Modes 1-2, and $Q_{11\_\text{dis}}$ is the energy discharged from $C_{r11}$ in Modes 5 and 7.

Similarly, the charge balance of $C_{r10}$ is achieved through $D_{11}$ and $D_{12}$. $C_{r12}$ is charged through $D_{14}$ and discharged through $D_{12}$. Then, Eq. (18)-(20) are obtained as:

$$i_{D11\text{-avg}} = \frac{Q_{10\_\text{ch}}}{T_s} = \frac{Q_{10\_\text{dis}}}{T_s} = i_{D12\text{-avg}} \quad (18)$$

$$i_{D14\text{-avg}} = \frac{Q_{12\_\text{ch}}}{T_s} = \frac{Q_{12\_\text{dis}}}{T_s} = i_{D12\text{-avg}} \quad (19)$$

Therefore, according to Eq. (17)-(19), the relationship among the average currents of the diodes $D_{11}$-$D_{14}$ are shown as:

$$i_{D11-\text{avg}} = i_{D12-\text{avg}} = i_{D13-\text{avg}} = i_{D14-\text{avg}} \quad (20)$$

Additionally, because the output capacitors $C_{11\text{-}14}$ are large enough, the four output currents and the notations of the four currents are equal to the diodes average currents. Hence:

$$i_{LED11} = i_{LED12} = i_{LED13} = i_{LED14} \quad (21)$$

Due to the CBC, the currents of the four LED-loads are balanced. Moreover, in accordance with Eq. (17)-(20), the non-ideal factors of $C_{r10}$, $C_{r11}$ and $C_{r12}$ are tolerable.

### B. Operation of Resonant Capacitors

According to the operations in Modes 1-2 and 4-7, power is delivered to the four output channels through four paths, which are $C_{r10}$-$C_{r11}$-$LED_{11}$, $C_{r12}$-$LED_{14}$, $C_{r10}$-$C_{r12}$-$LED_{12}$ and $C_{r11}$-$LED_{13}$. When $S_1$ is open, $C_{r10}$-$C_{r11}$ and $C_{r12}$ are charged. When $S_1$ is closed, $C_{r10}$-$C_{r12}$ and $C_{r11}$ are discharged. Based on the current balancing analysis, the average currents through $LED_{11}$ and $LED_{14}$ are equal. Therefore, Eq. (22) is derived.

$$\frac{0.5C_r(\Delta v_{Cr10-\text{charge}} + \Delta v_{Cr11-\text{charge}})}{T_s} = \frac{C_r(\Delta v_{Cr12-\text{charge}})}{T_s} \quad (22)$$
$$\rightarrow \Delta v_{Cr10-\text{charge}} + \Delta v_{Cr11-\text{charge}} > \Delta v_{Cr12-\text{charge}}$$

Hence, at time $t_0$, Eq. (4) is verified. After $t_0$, power is delivered to $LED_{11}$ and then to $LED_{14}$. Similarly, when $S_1$ is turned on, power is transferred to $LED_{12}$ and then to $LED_{13}$.

### C. Control System

As illustrated in Fig. 4(a), the currents through all of the LED strings in Port 1 and Port 2 are controlled by the PWM

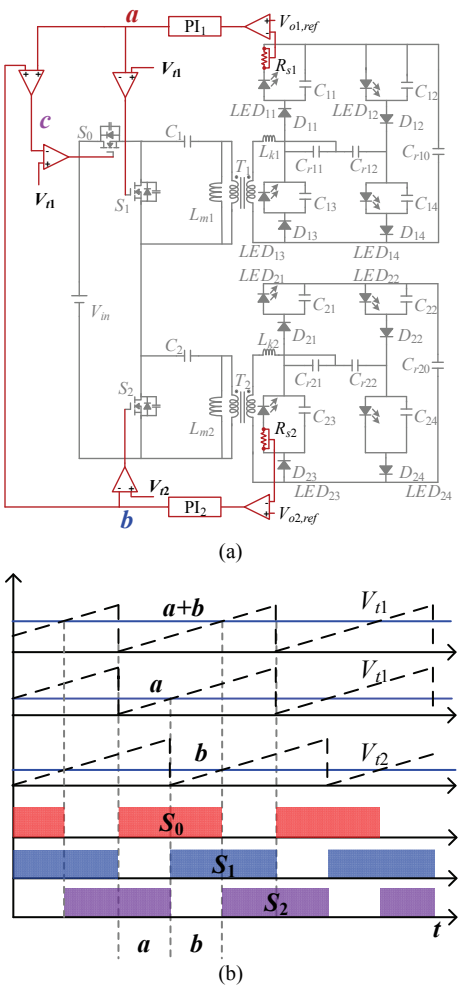



Fig. 4. Control systems: (a) Control system schematic; (b) Control signals for three switches.

control where two individual proportion-integrator (PI) compensators are adopted. Due to the current balancing characteristic, the currents through the four LED strings in port 1 $LED_{11}$-$LED_{14}$ have the same value as $i_{o1}$, and the value of the currents through the four LED strings $LED_{21}$-$LED_{24}$ have the same value as $i_{o2}$. To collect the output currents $i_{o1}$ and $i_{o2}$, two sample resistors $R_{s1}$ and $R_{s2}$ are series connected to one LED string in each port. Thus, $i_{o1}$ and $i_{o2}$ are regulated as $V_{o1,ref}/R_{s1}$ and $V_{o2,ref}/R_{s2}$. The control variables $a$ and $b$ are received from two individual PI compensators according to the error voltage between the reference voltages $V_{o1,ref}$–$V_{o2,ref}$ and the voltages $V_{o1}$ and $V_{o2}$ across the sample resistors $R_{s1}$ and $R_{s2}$.

As shown in Fig. 4(b), the control signals for the switches $S_0$, $S_1$ and $S_2$ are obtained by comparisons of ($a$+$b$, $V_{t1}$), ($V_{t1}$, $a$) and ($V_{t2}$, $b$), respectively. $D_{S0}$, $D_{S1}$ and $D_{S2}$ are the duty cycles of the three switches. When compared with the saw tooth $V_{t1}$, $V_{t2}$ is delayed by $a \times T_s$. To achieve the same operation of two ports, $V_{o1,ref}$=$V_{o2,ref}$ and $R_{s1}$ = $R_{s2}$ so that the control variables $a$=$b$ and $D_{S1}$=$D_{S2}$. The duty cycles of the three switches can be calculated by (23).

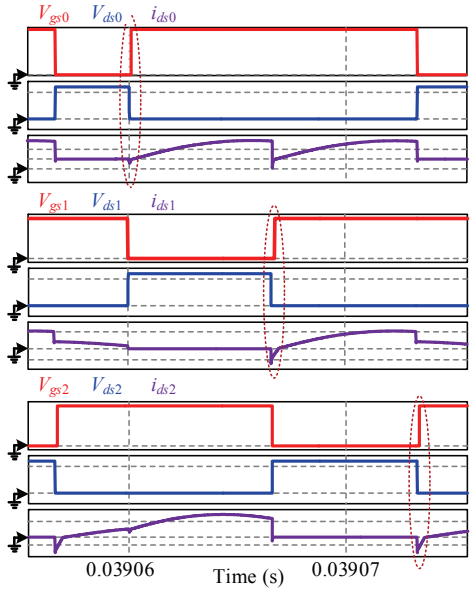



Fig. 5. ZVS turn on of three switches in a simulation.

$$\begin{cases} D_{S1} = 1 - a \\ D_{S2} = 1 - b \\ D_{S0} = a + b \end{cases} \tag{23}$$

To adjust the brightness, the switch $S_2$ can be short-circuited by an external wire so there is no power transferred to Port 2. The variable c becomes zero. Therefore, the LED driver can provide two-stage brightness: 100% when both $S_1$ and $S_2$ are working and 50% when only one of them is operating. Furthermore, the driver provides two-stages brightness and increases reliability due to the two individual PI compensators and two isolated ports.

### *D. Soft Switching Analysis*

As illustrated in Fig. 5, all three of the power switches can achieve ZVS turn on. In Mode 3, before the switch $S_1$ is turned on, the energy stored in the parasitic capacitor of the switch $S_1$ is released to zero. Then the body diode of the switch is forward biased to conduct $S_1$ with zero voltage. Furthermore, because $L_{m1}$ and $L_{m2}$ are large enough, the parasitic capacitor of $S_1$ can be completely discharged. According to Eq. (13), if the dead time $t_{ds1}$ is shorter than $t_3$–$t_2$, $S_1$ can achieve the ZVS operation. Similarly, in Eq. (15)-(16), if the dead time $t_{ds2}$ is shorter than $t_6$–$t_5$, $S_2$ can obtain ZVS. In addition, $S_0$ can achieve ZVS when $t_{ds0}$<$t_8$–$t_7$.

$$\begin{cases} t_{ds1} > \tau_3 = \dfrac{2 \cdot C_s \cdot V_{in}}{i_{Lm1}(t_3) - i_{Lm2}(t_3)} \\ t_{ds2} > \tau_6 = \dfrac{2 \cdot C_s \cdot V_{in}}{i_{Lm2}(t_6)} \\ t_{ds0} > \tau_8 = \dfrac{2 \cdot C_s \cdot V_{in}}{-i_{Lm1}(t_8)} \end{cases} \tag{24}$$

where $\tau_3$ is the time duration of mode 3; $\tau_6$ is the time duration of mode 6; and $\tau_8$ is the time duration of mode 8.

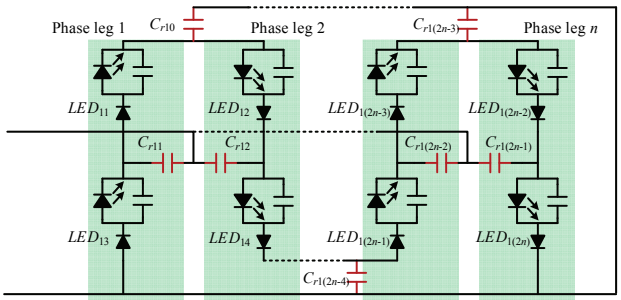



Fig. 6. Expandable topology.

### E. Expandable Topology

As illustrated in Fig. 6, the converter can be extended in terms of the output channels by adding resonant capacitors. According to the current balancing operation, one phase leg requires one resonant capacitor, e.g. $C_{r11}$-$C_{r12}$ for phase legs 1-2 respectively, and one more resonant capacitor, e.g. $C_{r10}$ is connected between the two phase legs. Hence, by adding $2n$-1 resonant capacitors, $2n$ output channels can be achieved.

## IV. Design Guide

This section introduces the design considerations including the relationships among the switching frequency, leakage inductor and the resonant capacitors, as well as the operating characteristics of the components.

### A. Passive Current Balancing

The average input current can be calculated as:

$$i_{in-avg} = \frac{t_{\text{off}} \cdot i_{p1}(t_2)}{2} \cdot \frac{2}{T_s} \tag{25}$$

The output power can be derived as:

$$i_{in-avg} = \frac{t_{\text{off}} \cdot i_{p1}(t_2)}{2} \cdot \frac{2}{T_s} \tag{26}$$

With the analysis and the trade-off between the power dissipation in the active switches and transformers, the switching frequency is set at 60 kHz in the experiment. To achieve ZVS turn-on of the switches, the on/off time of the switches should be larger than the resonant time based on $\omega_a$ and $\omega_b$. As a result, there is always primary current $i_p$ to discharge the parasitic capacitance of the active switches. Moreover, the off-time of the two switches $S_1$ and $S_2$ are shorter than their on-time. Hence, according to (12), the following equation can be obtained:

$$t_{off} < t_{com} \rightarrow$$
$$L_k C_r > \frac{t_{off}^2}{0.5 \cdot A^2 + 1.5 \cdot (\pi - \theta)^2 + \sqrt{3} \cdot A \cdot (\pi - \theta)} \tag{27}$$

where $A=arccos\{[(V_{in}\text{-}V_{C1})/n\text{-}v_{Cr12}(t_0)\text{-}V_{C14}]/\Delta v_{Cr\text{-}ini}$.

However, with a large leakage inductance, the secondary current $i_s$ cannot return to zero immediately after the turn-on/turn-off of active switches. Hence, the leakage inductance is chosen as 9μH, and the 3.3μF resonant capacitance $C_r$ is designed to satisfy Eq. (27).

Based on the primary side referred leakage inductance and switching frequency, the minimum value of the switched capacitors is determined according to:

$$C_r > \frac{1}{4\pi^2 f_s^2 (L_k / n^2)} \tag{28}$$

For the switched capacitors $C_1$-$C_2$, a large capacitance can reduce their voltage ripple. However, to reduce the volume of the proposed converter, the switched capacitors are designed as 20μF.

### B. Voltage and Current Stress of Active Switches

The voltage stress of three switches is equal to the input voltage $V_{in}$. According to Fig. 3, the current through $S_1$ reaches its maximum value during the interval [$t_3$~$t_5$]. With the primary currents, the current stress of the switch $S_1$ can be obtained as:

$$\begin{aligned} i_{s1}(t) &= i_{p2}(t) - i_{p1}(t) \\ &= \frac{1}{n} i_{s2}(t) + i_{Lm2}(t) - \frac{1}{n} i_{s1}(t) - i_{Lm1}(t) \\ &\approx \frac{1}{n}(i_{s2}(t) - i_{s1}(t)) \end{aligned} \tag{29}$$

Due to the large magnetic inductances and the voltage clamping transformers, the currents through the magnetic inductances are ignored. The maximum current of the switch $S_2$ is obtained at time $t_7$, which has the same value as that of $S_1$. The current through $S_0$ is either $i_{p1}$ or $i_{p2}$. Therefore, the current stress of the switches can be derived as:

$$\begin{cases} i_{ds0\_\max} = \dfrac{k\Delta v_{Cr-\text{ini}}}{n \cdot Z_n} \\ i_{ds1\_\max} = i_{ds2\_\max} = \dfrac{k\Delta v_{Cr-\text{ini}}}{n \cdot Z_n} - \dfrac{k\Delta v'_{Cr-\text{ini}}}{n \cdot Z_n} \end{cases} \tag{30}$$

where $\Delta v'_{Cr\text{-}ini}=\text{-}V_{C1}/n\text{-}v_{Cr10}+v_{Cr12}\text{-}V_{C12}$ indicates the voltage across the leakage inductance $L_{k1}$ at time $t_4$.

### C. Voltage Variation of Resonant Capacitors

According to Eq. (17)-(19) and (22), Eq. (31) can be derived as:

$$\begin{cases} Q_{Cr10ch} = Q_{Cr10dis} = Q_{Cr11ch} = Q_{Cr11dis} = Q_{Cr12ch} = Q_{Cr12dis} \\ \Delta v_{Cr10-A} + \Delta v_{Cr10-B} = \Delta v_{Cr11-A} + \Delta v_{Cr11-B} = \Delta v_{Cr12-A} + \Delta v_{Cr12-B} \end{cases} \tag{31}$$

where $\Delta v_{cr\text{-}A}$ and $\Delta v_{cr\text{-}B}$ are the voltage changes of the corresponding switches in modes 1 and 2, respectively. Additionally, in mode 2, $i_{Cr12}(t)=2i_{Cr10}(t)=2i_{Cr11}(t)$. Hence:

$$Q_{Cr12ch} = 2Q_{B\_ch} = 2Cr\Delta v_{Cr10-B} = 2Cr\Delta v_{Cr11-B} \tag{32}$$

where $Q_{B\_ch}$ indicates the energy stored in $C_{r10}$ or $C_{r11}$ in mode 2, and $Q_{A\_ch}$ is the energy stored in $C_{r10}$ or $C_{r11}$ in mode 1. Then the relationships among the voltage and energy variations of three resonant capacitors can be obtained by:

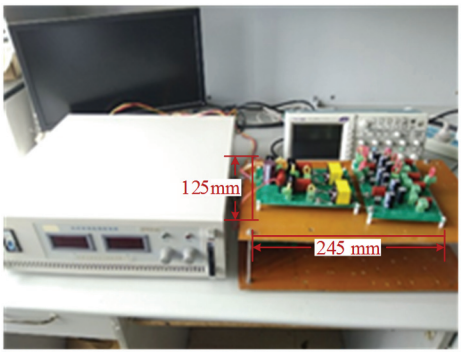



Fig. 7. Prototype of the proposed LED driver.

TABLE I
EXPERIMENT PARAMETERS

| Symbols | Definitions | Values |
|---|---|---|
| $V_{in}$ | Input voltage | 24 V |
| $P_{out}$ | Output power | 100 W |
| $C_r$ | Resonant capacitor | 3.3 μF |
| $C_{out}$ | Output capacitor | 440μF |
| $C_{1i}$~$C_{2i}$ | | |
| $C_1$~$C_2$ | Converter capacitor | 20μF |
| $V_{out}$ | Output voltage | 30.8 V |
| $i_{out}$ | Output current | 0.4A |
| **Transformer:** | | |
| $n$ | Voltage ratio | 1:3 |
| $L_m$ | Magnetic inductance | 203/201μH |
| $L_k$ | Leakage inductance | 8.27/8.46μH |
| *Core* | PQ3525 | / |
| **Semiconductor components:** | | |
| $S_0$~$S_2$ | SFP65N06 | / |
| $D_{1i}$~$D_{2i}$ | MBR20100CT | / |

$$\begin{cases} Q_{A\_ch} = Q_{B\_ch} = 0.5Q_{ch} \\ \Delta v_{Cr10-A} = \Delta v_{Cr10-B} = \Delta v_{Cr11-A} = \Delta v_{Cr11-B} = \Delta v_{Cr12-A} = \Delta v_{Cr12-B} = \Delta v_{Cr} \end{cases} \quad (33)$$

Based on Eq. (8), (10) and (33), the following equation is obtained by:

$$C_r \Delta v_{Cr} = Q_{chA} = Q_{chB} \rightarrow$$
$$\int_{t_0}^{t_1} \frac{3\Delta v_{Cr-ini}}{Z_n} \sin \omega_a (t - t_0) dt = \int_{t_1}^{t_2} \frac{k \cdot \Delta v_{Cr-ini}}{Z_n} \sin[\omega_b (t - t_1) + \theta] dt \quad (34)$$

With the assumption of $C_{r10}$=$C_{r11}$=$C_{r12}$=$C_r$, the variables in Eq. (26) can be achieved as $\theta$=1.37rad and $k$=0.962.

## V. EXPERIMENT RESULTS

To test and verify the performance of the designed LED driver, a prototype with a 24V DC input is built and displayed in Fig. 7.

Table I shows the elements employed in the prototype. The power efficiency of this prototype can reach 94.6% with a 60 kHz switching frequency. Due to the similar operation of the two ports, only the experiment results of the primary power stage and Port 1 are illustrated.

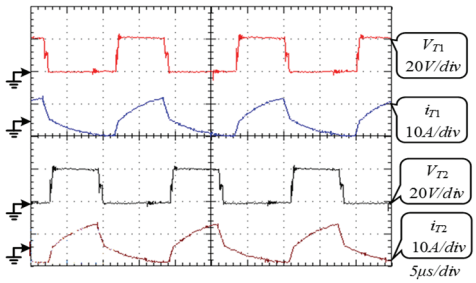



Fig. 8. Currents and voltages of the transformers $T_1$~$T_2$.

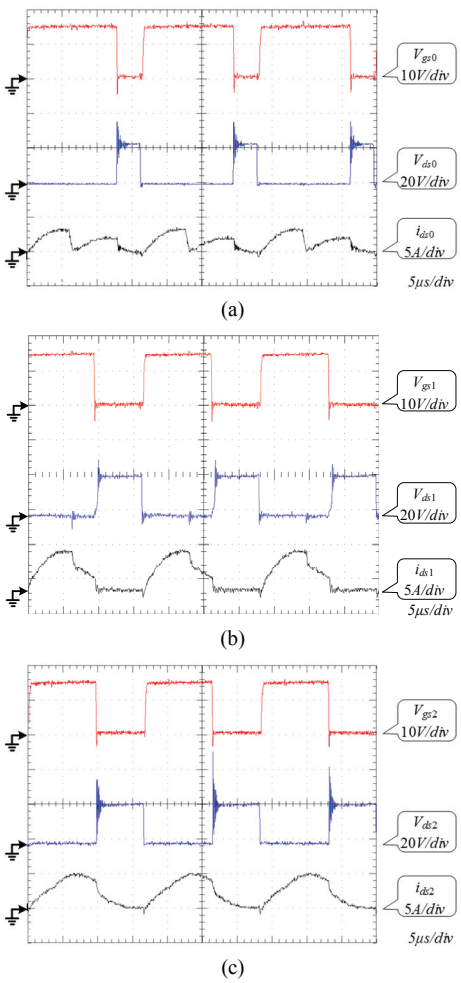



Fig. 9. ZVS operation of three MOSFET switches: (a) $S_0$; (b) $S_1$; (c) $S_2$.

Fig. 8 shows the voltages and primary currents of the two transformers. The obtained experimental waveform is consistent with that in the theoretical analysis. When $S_1$ is closed, the voltage of the transformer $T_1$ is negative as $-V_c$, and the current $i_{p1}$ keeps decreasing. When $S_1$ is open, the voltage across the transformer $T_1$ is positive as $V_{in}-V_c$, and the current $i_{p1}$ keeps increasing. Due to the large magnetic inductance, the primary side current $i_{p1}$ is mainly affected by the secondary side current $i_{s1}$. Moreover, for the same reason, there is a delay for $i_{p1}$ to return to zero after the switch's state changed. Port 2 has a similar operation based on the on/off

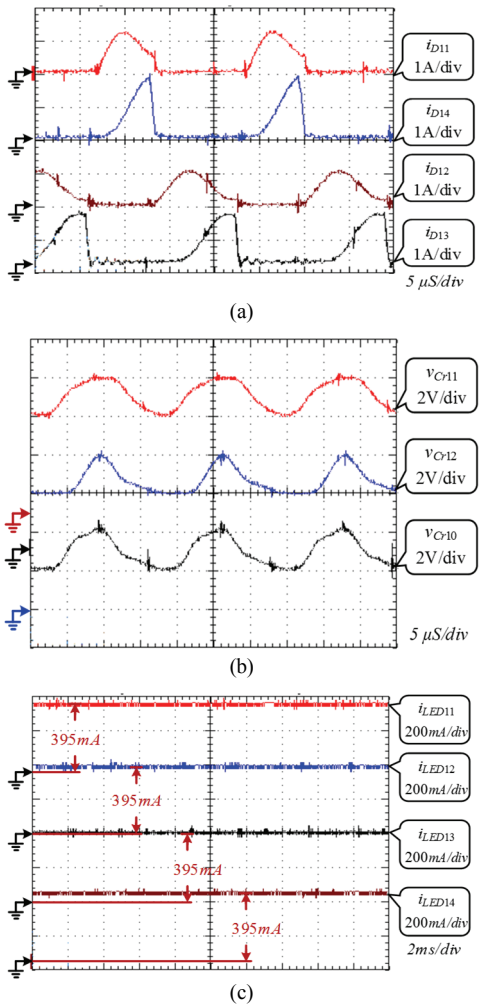



Fig. 10. Current balance operation based on resonant capacitors: (a) currents through the diodes $D_{11}$-$D_{14}$; (b) voltages of the resonant capacitors $C_{r10}$-$C_{r12}$; (c) output currents through the four LED-loads $LED_{11}$-$LED_{14}$.

states of the switch $S_2$. Additionally, when $S_0$ is off, the voltages of both transformers are negative.

As illustrated in Fig. 9, the ZVS operations of the active switches are verified. For example, the drain-source $i_{ds1}$ increases to $i_{p2}$-$i_{p1}$ after $S_1$ is closed. Meanwhile, when $S_0$ is open, $i_{ds1}$ drops to -$i_{p1}$. The drain-source current $i_{ds}$ flows through the parasitic diode before the turn-on of the corresponding switch and the ZVS turn-on of the switch is achieved. As a result, the switching loss is significantly decreased.

In Fig. 10, the charge and discharge processes of the resonant tank are tested and shown. The two pairs of diodes, $D_{11}$&$D_{14}$ and $D_{12}$&$D_{13}$ have the same operations. In Fig. 10 (a), $D_{14}$ is conducted after $D_{11}$ with a time delay of $\tau_1$. Then they are reverse biased at the same time. Additionally, according to Fig. 10(b), $C_{r10}$ and $C_{r11}$ are charged before $C_{r12}$. Then $C_{r10}$ and $C_{r12}$ are discharged before $C_{r11}$. The voltages across $C_{r11}$ and $C_{r12}$ are always positive. However, for $C_{r10}$, the voltage crosses zero at $t_1$ and $t_4$ when the voltages of the

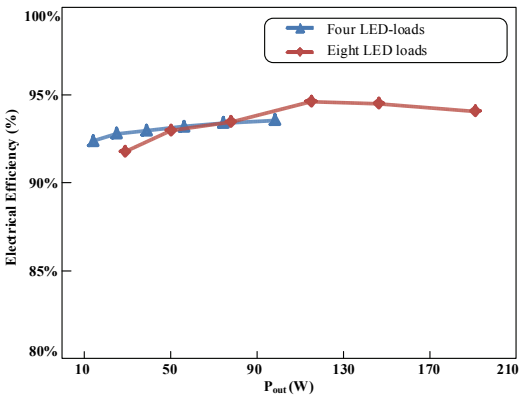



Fig. 11. Power efficiency curve of the proposed LED driver.

TABLE II
COMPARISON AMONG THE PROPOSED AND OTHER LED DRIVERS

| LED drivers | Design complexity | Power efficiency | Output power |
|---|---|---|---|
| Switched capacitor [5] | Low | 83% | Low |
| Flyback converter [9] | Low | 90% | Low |
| CLCL resonant [13] | Medium | 94.5% | High |
| Inductor-based CBC [16] | High | 96.4% | High |
| Proposed | Low | 94.6% | High |

two branches are equal. Fig. 10(c) displays the constant balanced output currents of the four output channels in Port 1.

The power efficiency of the LED driver is recorded under different input voltage values as shown in Fig. 11. The red line with diamond markers is obtained when both $S_1$ and $S_2$ are working with 8 LED strings. The blue line with triangle markers is obtained when only $S_1$ is working with 4 LED strings in Port 1. The output power in the case presented by the blue line is half of that of the red line. With 8 LED strings, the efficiency can reach its highest point at 94.6%.

Comparative results in terms of design complexity, power efficiency and output power scale are shown in Table II. The non-isolated LED driver with a switched capacitor [5] has the most straightforward design and smallest number of components. The LED driver with a flyback converter [9] uses only one active switch to achieve high compactness. However, their power efficiency is less than 90%, and they are preferred for low power applications. For high illuminance applications, [13] and [16] can achieve a power efficiency of around 95%. However, two external inductors are applied in [13] to construct the CLCL resonant tank, which increases the design complexity and volume. Thanks to the transformers installed for current balancing among different LED strings, [16] is suitable for high power applications, while the non-ideal factors of these transformers result in a high control complexity. From the aforementioned characteristic analysis, the proposed LED driver can achieve a high efficiency of 94.6% with a reduced component count. Additionally, the current balancing of LED strings is obtained by resonant capacitors whose values do not need to be the same.

## VI. CONCLUSION

This study proposes a novel LED driver designed for portable applications. The primary power stage uses only 3 active switches which is one less than conventionally used separate 2 output isolated converters. The following advantages are achieved.

1. High power efficiency: thanks to the ZVS turn-on and the passive CBCs, high power efficiency of 94.6% is obtained.
2. Low design complexity: the power stage uses only two magnetic components and two capacitors to achieve ZVS for all of the active switches. The current balancing operation is achieved due to the three resonant capacitors. Additionally, when compared with the conventional two isolated output converter, the proposed one uses one fewer active switch.
3. Multiple outputs: due to the two separate ports power stage and the two CBCs, the driver provides eight LED output-channels, which are divided into two parts with the same structure.

Experiment results are presented to verify the ZVS of the active switches, the operation of the two isolated ports and the balanced output currents of the proposed LED driver. This project is suitable for high power portable applications such as camping lights, vehicle lights and emergency lights.

## REFERENCES

[1] H. S.-H. Chung, N.-M. Ho, W. Yan, P. W. Tam, and S. Hui, "Comparison of dimmable electromagnetic and electronic ballast systems-An assessment on energy efficiency and lifetime," *IEEE Trans. Ind. Electron*., Vol. 54, No. 6, pp. 3145-3154, Dec. 2007.

[2] M. K. Richard and P. K. Sen, "Compact fluorescent lamps and their effect on power quality and application guidelines," in *Industry Applications Society Annual Meeting (IAS)*, pp. 1-7, 2010.

[3] X. Liu, Q. Yang, Q. Zhou, J. Xu, and G. Zhou, "Single-stage single-switch four-output resonant LED driver with high power factor and passive current balancing," *IEEE Trans. Power Electron*., Vol. 32, No. 6, pp. 4566-4576, Jun. 2017.

[4] M. Al-Absi, Z. Khalifa, and A. Hussein, "A new capacitor-less buck DC-DC converter for LED applications," *Active and Passive Electronic Components*, Vol. 2017, Article ID 2365848, 5 pages, 2017.

[5] E. E. dos Santos Filho, P. H. Miranda, E. M. Sá, and F. L. Antunes, "A LED driver with switched capacitor," *IEEE Trans. Ind. Appl*., Vol. 50, No. 5, pp. 3046-3054, Sep.-Oct. 2014.

[6] C.-K. Cheung, S.-C. Tan, Y.-M. Lai, and K. T. Chi, "A new visit to an old problem in switched-capacitor converters," in *Circuits and Systems (ISCAS), Proceedings of 2010 IEEE International Symposium on*, pp. 3192-3195, 2010.

[7] S.-C. Tan, S. Kiratipongvoot, S. Bronstein, A. Ioinovici, Y. Lai, and K. T. Chi, "Adaptive mixed on-time and switching frequency control of a system of interleaved switched-capacitor converters," *IEEE Trans. Power Electron.*, Vol. 26, No. 2, pp. 364-380, Feb. 2011.

[8] C.-Y. Wu, T.-F. Wu, J.-R. Tsai, Y.-M. Chen, and C.-C. Chen, "Multistring LED backlight driving system for LCD panels with color sequential display and area control," *IEEE Trans. Ind. Electron*., Vol. 55, No. 10, pp. 3791-3800, Oct. 2008.

[9] S. Jung and G.-H. Cho, "Transformer coupled recycle snubber for high-efficiency offline isolated LED driver with on-chip primary-side power regulation," *IEEE Trans. Ind. Electron*., Vol. 61, No. 12, pp. 6710-6719, Dec. 2014.

[10] B. Poorali and E. Adib, "Analysis of the integrated SEPIC-flyback converter as a single-stage single-switch power-factor-correction LED driver," *IEEE Trans. Ind. Electron*., Vol. 63, No. 6, pp. 3562-3570, Jun. 2016.

[11] Y. Wang, J. Huang, G. Shi, W. Wang, and D. Xu, "A single-stage single-switch LED driver based on the integrated SEPIC circuit and class-E converter," *IEEE Trans. Power Electron.*, Vol. 31, No. 8, pp. 5814-5824, Aug. 2016.

[12] H. Ma, J.-S. J. Lai, C. Zheng, and P. Sun, "A high-efficiency quasi-single-stage bridgeless electrolytic capacitor-free high-power AC–DC driver for supplying multiple LED strings in parallel," *IEEE Trans. Power Electron*., Vol. 31, No. 8, pp. 5825-5836, Aug. 2016.

[13] Y. Wang, Y. Guan, D. Xu, and W. Wang, "A CLCL resonant DC/DC converter for two-stage LED driver system," *IEEE Trans. Ind. Electron*., Vol. 63, No. 5, pp. 2883-2891, May 2016.

[14] T.-J. Liang, W.-J. Tseng, J.-F. Chen, and J.-P. Wu, "A novel line frequency multistage conduction LED driver with high power factor," *IEEE Trans. Power Electron*., Vol. 30, No. 9, pp. 5103-5115, Sep. 2015.

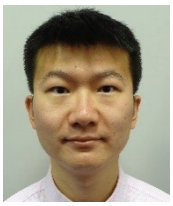
[15] E. S. Lee, B. H. Choi, D. T. Nguyen, B. G. Choi, and C. T. Rim, "Static regulated multistage semiactive LED drivers for high-efficiency applications," *IEEE Trans. Power Electron*., Vol. 31, No. 9, pp. 6543-6552, Sep. 2016.

[16] J. Wang, J. Zhang, X. Wu, Y. Shi, and Z. Qian, "A novel high efficiency and low-cost current balancing method for multi-LED driver," in Energy Conversion Congress and Exposition (ECCE), pp. 2296-2301, 2011.

[17] J.-I. Baek, J.-K. Kim, J.-B. Lee, H.-S. Youn, and G.-W. Moon, "Integrated asymmetrical half-bridge Zeta (AHBZ) converter for DC/DC stage of LED driver with wide output voltage range and low output current," *IEEE Trans. Ind. Electron*., Vol. 62, No. 12, pp. 7489-7498, Dec. 2015.

[18] K. Hwu and W. Jiang, "Nonisolated two-channel LED driver with automatic current balance and zero-voltage switching," *IEEE Trans. Power Electron*., Vol. 31, No. 12, pp. 8359-8370, Dec. 2016.

[19] S. M. Baddela and D. S. Zinger, "Parallel connected LEDs operated at high to improve current sharing," in *Industry Applications Conference, 2004. 39th IAS Annual Meeting. Conference Record of the 2004 IEEE*, Vol. 3, pp. 1677-1681, 2004.



**Sen Song** was born in Hebei, China. He received his B.S. (with Honors) degrees in Electrical Engineering and Automation from Xi'an Jiaotong-Liverpool University, Suzhou, China, and in Electrical Engineering from the University of Liverpool, Liverpool, ENG, UK, in 2016, where he is presently working towards his Ph.D. degree. His current research interests include power electronic converters and HVDC transmission.

**Kai Ni** (S'17) was born in Jiangsu, China. He received his B.S. (with Honors) degrees in Electrical Engineering and Automation from Xi'an Jiaotong-Liverpool University, Suzhou, China, and in Electrical Engineering from the University of Liverpool, Liverpool, ENG, UK, in 2016, where he is presently working towards his Ph.D. degree. His current research interests include the operation and control of asynchronized synchronous machines, power electronic converters and power systems.

**Guipeng Chen** received the B.S. and Ph.D. degrees from the Department of Electrical Engineering, Zhejiang University, Hangzhou, China, in 2011 and 2017, respectively. He joined the Fuji Electric Matsumoto Factory as a Summer Intern in 2014, and was invited to the University of Liverpool, Liverpool, ENG, UK, as a Research Assistant for a half-year program in July 2016. He is presently working as a Postdoctoral Researcher in the Instrument Science and Technology Postdoc Center, School of Aerospace Engineering, Xiamen University, Xiamen, China. His current research interests include automatic topology derivations of dc–dc converters and fault-tolerant converters.

**Yihua Hu** received his B.S. and Ph.D. degrees from the School of Information and Electrical Engineering, China University of Mining and Technology, Xuzhou, China, in 2003 and 2011, respectively. From 2011 to 2013, he was a Postdoctoral Fellow in the College of Electrical Engineering, Zhejiang University, Hangzhou, China. From 2013 to 2015, he worked as a Research Associate in the Power Electronics and Motor Drive Group, University of Strathclyde, Glasgow, SCT, UK. He is presently working as a Lecturer in the Department of Electrical Engineering and Electronics, University of Liverpool (UoL), Liverpool, ENG, UK. He has published 60 papers in IEEE Transactions journals. His current research interests include renewable generation, power electronics converters and control, electric vehicles, more electric ship/aircraft, smart energy systems and non-destructive test technology. He is the Associate Editor of the IET Renewable Power Generation, IET Intelligent Transport Systems and Power Electronics and Drives.

**Dongsheng Yu** received his B.S. and Ph.D. degrees from the School of Information and Electrical Engineering, China University of Mining and Technology, Xuzhou, China, in 2005 and 2011, respectively. From 2009 to 2010, he was a Visiting Student at the University of Western Australia, Perth, WA, Australia. From 2014 to 2015, he was an Endeavour Research Fellow at the University of Western Australia. He is presently working as an Associate Professor in the School of Electrical and Power Engineering, China University of Mining and Technology. His current research interests include power electronics, renewable energy, electric drives, nonlinear dynamics and memristive systems. He has published two books and over 50 papers in these areas.