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Neutral-point Voltage Balancing Strategy for Three-level Converter based on Disassembly of Zero Level

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Abstract

The neutral-point (NP) voltage of three-phase three-level NP-clamped converters is needed for balance. To maintain NP potential and suppress ripple, a novel NP voltage balancing strategy is proposed in this work. The mechanism of NP voltage variation is studied first. Then, the relationship between the disassembly of zero level (*O* level) and NP current is studied comprehensively. On these bases, two methods for selecting one of three output phases for the disassembly of its *O* level are presented. Finally, simulation and experimental results verify the validity and practicability of the proposed algorithms.

Key words: Balancing algorithm, Neutral-point-clamped, Neutral-point voltage, Zero-level disassembly

I. INTRODUCTION

Compared with the traditional two-level converters, three-phase three-level neutral-point (NP)-clamped (3L NPC) converters have been widely studied. This topology has the advantages of low voltage rating for switching devices and reduced output harmonics and electromagnetic interference (EMI) [1], [2]. However, NP voltage balancing must be maintained and ripple must be suppressed in practical applications [3], [4]. If the NP voltage is not well-controlled, then the output voltage would deviate from the reference value; moreover, the switching devices might be damaged. Numerous strategies have been proposed for solving this problem and can be mainly divided into two categories.

The first kind is based on the space vector pulse width modulation (PWM) (SVPWM) strategy. A three-level NPC converter has 27 vectors of 19 kinds. NP voltage control can be achieved through modification of the appropriate redundant small vectors and adjustment of dwell time [5]-[8]. However, as the output levels increase, the vectors and the corresponding redundant states increase significantly as well, thereby rendering this strategy unsuitable for digitization [9].

The other kind is based on carrier-based pulse width modulation (CPWM). In a three-phase three-wire system, when zero-sequence voltage is injected into three-phase reference voltages, the output line voltage will not change. By contrast, the additional zero-sequence component will affect the NP voltage [10]-[12]. For the searching optimization algorithm, after analysis of all the available zero-sequence voltages, the one that leads to a superior effect on NP voltage balancing is selected as the optimal zero-sequence voltage. According to the optimal zero-sequence injection algorithm, the algebraic relations between the NP potential and the zero-sequence voltage is calculated first. Then, the optimal zero-sequence voltage is obtained by the interpolation method.

However, studies show that all the strategies above are based on the nearest-three-vector PWM (NTV-PWM). Thus, they cannot fully suppress the low-frequency fluctuation of the NP potential [13]-[15]. The virtual SVPWM (VSVPWM) has been proposed for solving this problem. New virtual vectors are redefined by combination of the original small and middle vectors, thereby achieving a zero NP average current [16], [17]. Recently, scholars discovered an easy means of implementing this idea in CPWM [18]-[22]. A strategy called two modified modulation algorithm was proposed. It can maintain the NP potential and suppress the ripple simultaneously. However, no study has provided a clear formula for calculating the compensation value until now [23]-[28].

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According to the analysis above, the NP potential and the low-frequency fluctuation should be well-organized for the normal operation of a three-phase 3L NPC converter. In this work, the mechanism of NP voltage variation is studied first. Then, the relationship between the disassembly of the zero level and the NPC is investigated. A simple and direct way of determining one of the three phases to be disassembled is presented. On the basis of the middle zero-sequence injection, an easy means of determining the phase to be disassembled is finally proposed. The two strategies presented are verified by simulation and experiments.

II. NP Voltage Fluctuation Mechanism of 3L NPC Converter

The typical topology of a three-phase 3L NPC converter is shown in Fig. 1. The following are reasonable assumptions adopted for simplifying the analysis.

1) V_{dc} is always stable under any condition.

2) C_1 and C_2 are identical.

3) Three-phase loads are symmetrical.

4) The switching frequency is higher than the fundamental frequency of the load current, which is constant over a switching period.

$V_{dc}/2$ is chosen as the base value in calculating the per-unit value of the output voltages. If a symmetrical load is connected to the converter, then the output voltage v_j (j = a, b, c) and the current i_j (j = a, b, c) are expressed as Eq. (1). The variables are defined as follows.

M: Modulation ratio, $0 \le m \le 1$. The maximum of m is 0.866 for SPWM without zero-sequence voltage injection and can reach 1.0 for SVPWM and the SPWM with zero-sequence voltage injection.

θ: phase angle

I_m: phase current amplitude

φ: power factor angle

Thus, the reference directions of currents i_{C1} and i_{C2} and NP current i_o are shown in Fig. 1. If $i_o > 0$, then the upper capacitor will be charged and the lower capacitor will be discharged; if $i_o < 0$, the situation is the opposite. Both situations will make the NP voltage unbalanced.

$$\begin{cases} v_a = \dfrac{2}{\sqrt{3}} \cdot M \cdot \cos(\theta), & i_a = I_m \cos(\theta - \varphi) \\ v_b = \dfrac{2}{\sqrt{3}} \cdot M \cdot \cos(\theta - 2\pi/3), & i_b = I_m \cos(\theta - 2\pi/3 - \varphi) \\ v_c = \dfrac{2}{\sqrt{3}} \cdot M \cdot \cos(\theta + 2\pi/3), & i_c = I_m \cos(\theta + 2\pi/3 - \varphi) \end{cases} \quad (1)$$

For one of the three phases, three kinds of voltages can be generated: $0.5V_{dc}$ (P level), 0 (O level), and $-0.5V_{dc}$ (N level). Only when the output voltage of phase j (j = a, b, c) is O level will the NP current i_o be changed. For convenience, s_{jo} (j = a, b, c), a variable that indicates the output voltage as follows, is defined:

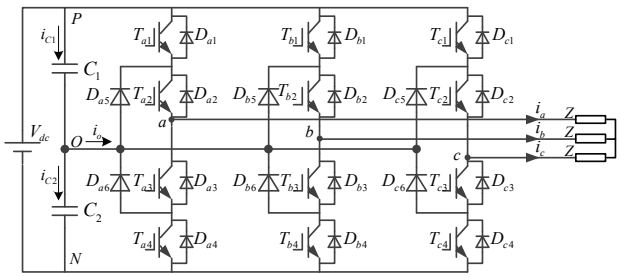

Fig. 1. Topology of diode-clamped three-level converter.

$$S_{jo} = \begin{cases} 1, & Output\ O\ level \\ 0, & Output\ P\ or\ N\ level \end{cases} \quad j = \{a, b, c\}. \quad (2)$$

Thus, the instantaneous value of NP current i_o in Fig. 1 can be derived as

$$i_o = S_{ao} \cdot i_a + S_{bo} \cdot i_b + S_{co} \cdot i_c. \quad (3)$$

Eq. (3) is integrated in one switching period, and the average value of the NP current is obtained.

$$\overline{i_o} = d_{ao} \cdot i_a + d_{bo} \cdot i_b + d_{co} \cdot i_c = \sum_{j=a,b,c} d_{jo} \cdot i_j, \quad (4)$$

where d_{jo} represents the duty cycle of the O level of phase j during one switching period T_s. When the modulation voltage is positive, $d_{jo} = 1 - v_j$. When v_j is negative, $d_{jo} = 1 + v_j$. The relationship between d_{jo} and v_j can be defined as follows [29]:

$$d_{jo} = 1 - |v_j|. \quad (5)$$

The voltage of the upper and lower capacitors C_1 and C_2 are v_{C1} and v_{C2}, respectively. In the introduction of the node current equation into Fig. 1, NP current i_o can be expressed as

$$i_o = i_{C1} - i_{C2} = C(v_{C1} - v_{C2})/T_s. \quad (6)$$

According to the above analysis, if an NP compensation current i_{ox}, $i_{ox} = -i_o$, can be generated, then the NP voltage can be well-controlled.

III. Basic Principle of NP Balancing Strategy Based on Disassembly of Zero Level

Studies show that in SVPWM, the selection of redundant switching states and adjustment of the dwell time are identical to the process of identifying the zero-sequence voltage in CPWM. If CPWM is adopted, then the control of the NP potential can be considered a problem of identifying the optimal zero-sequence voltage. However, the relationship between the zero-sequence voltage and the NP potential is a piecewise function, which renders its implementation difficult.

The duty cycle of the O level influences the NP current. Accordingly, the NP voltage can be balanced by an adjustment of the duty cycle of the O level. With Fig. 2 as example, ① represents how the original modulation signal v_j

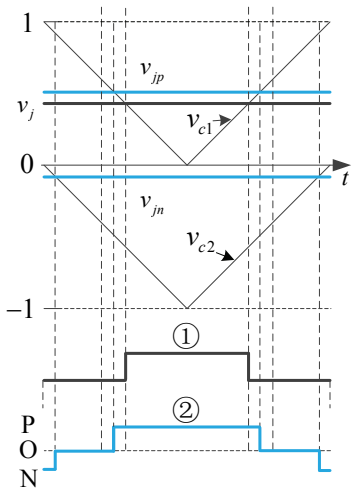

Fig. 2. Principle of disassembly of *O* level.

generates the output voltage. Meanwhile, ② shows that when the disassembly of the *O* level is adopted, the original modulation signal v_j is reconstructed into a positive modulation wave v_{jp} and a negative modulation wave v_{jn}. $v_{jp} + v_{jn} = v_j$. ② shows that the *O* level duty cycle d_{jo} of phase *j* is evenly distributed to the *P* and *N* levels. Therefore, d_{jo} is reduced, the average NP current is changed, and ripple is suppressed, thereby leading to increased switching frequency. Consequently, only one phase is disassembled at each switching period.

With phase *a* as an example, when the *O* level is not disassembled, the original NP current is i_o and the NP current becomes $i_{o(j)}$ when the *O* level d_{jo} of phase *j* is completely disassembled. $i_{o(j)}$ and i_o can be defined as Eqs. (7) and (8), respectively.

$$i_{o(a)} = d_{bo} \cdot i_b + d_{co} \cdot i_c \tag{7}$$

$$i_o = d_{ao} \cdot i_a + d_{bo} \cdot i_b + d_{co} \cdot i_c \tag{8}$$

A larger value $i_{o(j)\max}$ and a smaller value $i_{o(j)\min}$ must exist between $i_{o(j)}$ and i_o, and they represent the compensation current domain $[i_{o(j)\min}, i_{o(j)\max}]$ of phase *j* (*j* = *a, b, c*).

Two cases can be obtained after an analysis of the relationship between NP compensation current i_{ox} and the three NP compensation current domains.

1). When i_{ox} is within any of the three $[i_{o(j)\min}, i_{o(j)\max}]$, the phase that has the largest *O* level duty cycle d_{jo} will be chosen for disassembling the *O* level.

2). When i_{ox} is not within any of the three $[i_{o(j)\min}, i_{o(j)\max}]$ and if any of the three $i_{o(j)}$ has the same sign as i_{ox}, then the phase whose $i_{o(j)}$ is nearest i_{ox} will be chosen as the *O* level disassembly phase. For example, if $i_{o(a)} = -0.2$, $i_{o(b)} = -0.5$, $i_{o(c)} = 0.3$, and $i_{ox} = -0.7$, then phase *b* will be chosen.

When the signs of all three $i_{o(j)}$ are opposite to that of i_{ox}, then the NP voltage fluctuation cannot be compensated. No phase will be chosen for the disassembly of its *O* level.

O level disassembly quantity Δd_j should be calculated after determining the *O* level disassembly phase. If phase *a* is chosen to disassemble its *O* level and when the disassembly quantity is Δd_a, $i_{ox} = -i_o$, according to Eqs. (4) and (5), i_{ox} is derived as follows:

$$i_{ox} = \left(d_{ao} - \Delta d_a\right) \cdot i_a + d_{bo} \cdot i_b + d_{co} \cdot i_c \ . \tag{9}$$

Then, Eq. (6) is substituted into (9) to obtain the disassembly quantity Δv_a of phase *a* as follows:

$$\Delta d_a = d_{ao} - \left(i_{ox} - d_{bo} \cdot i_b - d_{co} \cdot i_c\right) / i_a \ . \tag{10}$$

The NP voltage can be easily balanced by the procedures above, which are straightforward and concise.

A. Analysis of Control Domain

After simulation and experiments, the fluctuation still cannot be fully compensated in some conditions. When the voltage fluctuation in a switching period is ignored and if the NP current can be maintained zero, then the NP potential can always be balanced. When the *O* level disassembly algorithm is adopted,

$$i_{o(j)\min} \le 0 \le i_{o(j)\max} \ . \tag{11}$$

If Eq. (11) is established under any modulation ratio and power factor, then the NP voltage can always be fully controlled. That is, if a three-phase 3L NPC converter is under any power factor angle φ and modulation ratio *m*, at least one phase *j* satisfies the following relationship:

$$i_{o(j)} \cdot i_o \le 0 \ . \tag{12}$$

Then, the NP voltage can be balanced by the *O* level disassembly. For ease of analysis of Eq. (12), the maximum and minimum NP currents provided by all the three phases at each time are plotted in Fig. 3. No zero-sequence voltage is injected into the original modulation waves v_j at this point.

In Fig. 3, the variation trend of the NP current control domain indicates that the smaller the modulation ratio (*m*) and the larger the power factor angle (ψ), the larger the NP current control domain. When ψ = 90°, Eq. (12) is always established. However, this situation does not satisfy the requirement of a controllable NP current under any condition.

For the three-phase 3L NPC system shown in Fig. 1, the zero-sequence voltage can be injected to the original modulation wave to improve the DC-link voltage utilization. To determine the zero-sequence voltage that is suitable for the proposed algorithm, the figures contain different available zero-sequences (v_z) (Fig. 4). Maximum and minimum zero-sequence 1 are the largest and smallest zero-sequences that can be injected to the modulation voltage at each time under the following limitation:

$$-1 - v_{\min} \le v_z \le 1 - v_{\max} \ . \tag{13}$$

Maximum and minimum zero-sequences 2 are the largest and smallest zero-sequences that satisfy Eq. (12) at any time. According to the figures, zero-sequences 1 and 2 are coincident

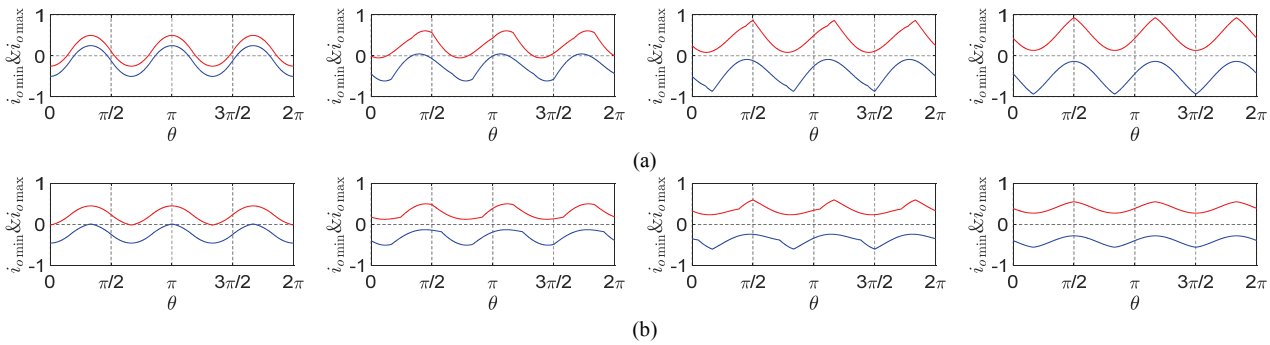

Fig. 3. Enveloping curves without zero-sequence voltage injection (ψ = 0°, 30°, 60°, 90°, from left to right): (a) $m = \sqrt{3}/2$; (b) m = 0.6.

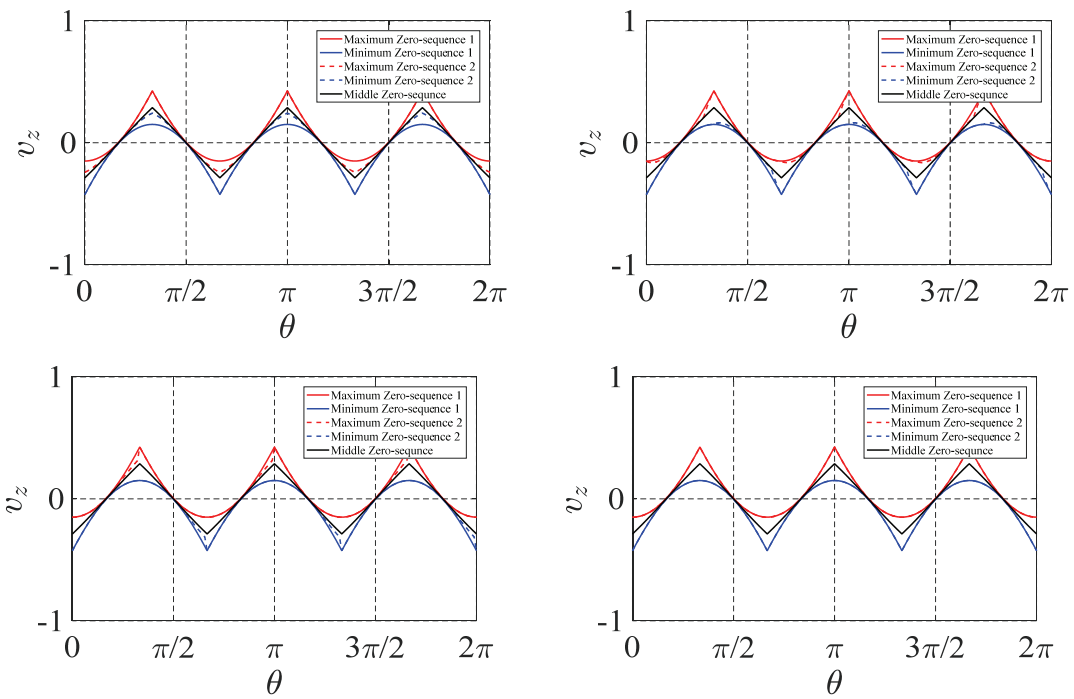

Fig. 4. Available zero-sequence when modulation ratio is m = 1.0 (ψ = 0°, 30°, 60°, 90° from left to right, top to bottom)

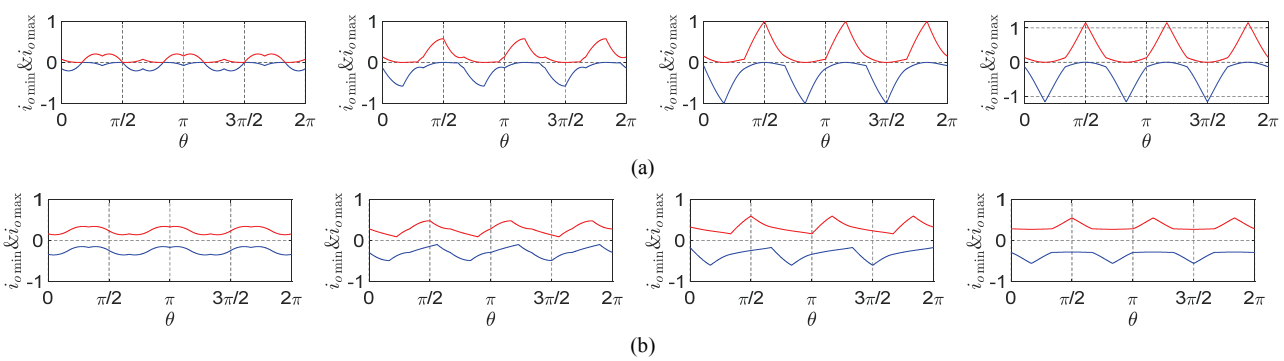

Fig. 5. Enveloping curves with middle zero-sequence voltage injection (ψ = 0°, 30°, 60°, 90°, from left to right): (a) m = 1.0; (b) m = 0.6.

in some areas. The middle zero-sequence represents $v_z = v_{mid}/2$. v_{mid} is the middle voltage of v_a, v_b, and v_c.

As for the condition ψ = 90°, maximum and minimum zero-sequences 1 and 2 are identical, which means that all the available zero-sequences can be injected to the modulation signals. However, when ψ decreases, for a certain θ, only the middle zero-sequence is within the maximum and minimum zero-sequence 2. Middle zero-sequence is the one and only choice. Thus, to compensate the NP voltage ripple at any time, the middle zero-sequence will be injected to the three-phase

original modulation voltages. The enveloping curves are replotted in Fig. 5. Now, all the curves contain line i_o=0. The NP voltage fluctuation is controllable under any modulation ratio m and power factor angle φ. The following formulas are provided to verify this conclusion.

Eq. (4) can be used to derive the $2\pi/3$ period of i_o. Meanwhile, $d_{ao}i_a$, $d_{bo}i_b$, and $d_{co}i_c$ are $2\pi/3$ out of each other. If $i_{o(j)}$ and i_o satisfy Eq. (12) in $\omega t \in [0, \pi/3]$, then the NP current is completely controllable in [0, 2π]. In the following discussion, $0 \le \varphi \le \pi/2$, $0 \le m \le 1$.

① $\omega t \in [0, \pi/6]$

$$\begin{aligned} i_{o(b)} \cdot i_o &= \left(d_{ao}i_a + d_{co}i_c\right) \cdot i_o \\ &= 2mI_m{}^2 \sin\omega t \left(m\sin\left(\omega t + \frac{\pi}{3}\right) - 1 \right) \cos^2\left(\omega t - \varphi + \frac{\pi}{3}\right) \end{aligned} \tag{14}$$

② $\omega t \in [\pi/6, \pi/3]$

$$\begin{aligned} i_{o(b)} \cdot i_o &= \left(d_{ao}i_a + d_{co}i_c\right) \cdot i_o \\ &= 2mI_m{}^2 \cos\left(\omega t + \frac{\pi}{6}\right) \left(m\sin\left(\omega t + \frac{\pi}{3}\right) - 1 \right) \cdot \cos^2\left(\omega t - \varphi + \frac{\pi}{3}\right. \end{aligned} \tag{15}$$

During interval ①, $\sin\omega t \ge 0$, $\cos^2(\omega t - \varphi + \pi/3) \ge 0$, $m\sin(\omega t+\pi/3)$-1≤0, thus satisfying Eq. (12). During interval ②, $m\sin(\omega t+\pi/3)$-1≤0, $\cos^2(\omega t - \varphi + \pi/3) \ge 0$, $\cos(\omega t+\pi/6) \ge 0$ also satisfies the equation. In summary, Eq. (12) is always true when $\omega t \in [0, \pi/3]$. Thus, the NP current (voltage) is totally controllable when middle zero-sequence voltage v_z=v_{mid}/2 is injected to the modulation voltage.

According to the idea of middle zero-sequence injection, another means of determining the phase to be disassembled is proposed in the next section.

B. Zero-level Disassembly Strategy under Middle Zero-sequence Voltage Injection

The strategy proposed at the beginning of Section III is called Strategy One. It notably selects the disassembly phase by comparing i_{ox} with [$i_{o(j)\min}$, $i_{o(j)\max}$]. The zero-sequence voltage injection does not influence the strategy itself but affects the NP voltage control domain. In some circumstances, such as the three-phase four-wire system, the output voltage will change if zero-sequence is injected to the original modulation signal. Consequently, Strategy One can be implemented.

However, for the topology in Fig. 1, injecting middle zero-sequence is desirable for improving the DC voltage utilization and compensation current domain. Following this analysis, an easy method of determining the phase to be disassembled is derived and called Strategy Two. It does not require as many calculations as does Strategy One and is thus simpler and more straightforward.

When middle zero-sequence is injected to the three-phase modulation voltage, the maximum, median, and minimum values of the three-phase modulation voltages are

$$\begin{aligned} v'_{\max} &= \left(v_{\max} - v_{\min}\right)/2 \\ v'_{\mathrm{mid}} &= v_{mid} - \left(v_{\max} + v_{\min}\right)/2 \\ v'_{\min} &= \left(v_{\min} - v_{\max}\right)/2 \end{aligned} . \tag{16}$$

$v'_{\max}$ and $v'_{\min}$ have the same value with opposite signs. According to Eq. (5), their O level duty cycles are the same.

$$d_{v'_{\max}} = d_{v'_{\min}} = 1 - \left|(v_{\max} - v_{\min})/2\right| \tag{17}$$

However, the O level duty cycle of v'_{mid} is

$$d_{v'_{\mathrm{mid}}} = 1 - \left|v_{\mathrm{mid}} - (v_{\max} + v_{\min})/2\right| . \tag{18}$$

The three-phase modulation voltages are balanced, $v_{\max}$+v_{mid}+$v_{\min}$=0. Thus, v'_{mid} satisfies

$$v'_{\mathrm{mid}} = v_{\mathrm{mid}} - (v_{\max} + v_{\min})/2 = 1.5v_{\mathrm{mid}} . \tag{19}$$

By substituting Eq. (18) into (17), we derive the following:

$$d_{v'_{\mathrm{mid}}} = 1 - \left|v_{\mathrm{mid}} - (v_{\max} + v_{\min})/2\right| = 1 - \left|1.5(v_{\max} + v_{\min})\right| . \tag{20}$$

The comparison of Eqs. (17) and (20) indicates that the O level duty cycle of v'_{mid} is larger than those of $v'_{\max}$ and $v'_{\min}$. Thus, the corresponding phase of v'_{mid} is chosen for disassembling its O level.

The disassembly quantity should also be calculated. The disassembly quantity is d_{com}. The O level of v'_{mid} can be disassembled to zero at most. Accordingly, the disassembly quantity satisfies

$$0 \le d_{com} \le d_{v'_{\mathrm{mid}}} . \tag{21}$$

After the disassembly of the O level, the NP current changes to

$$i_{v'_{\mathrm{mid}}} = \left(d_{v'_{\mathrm{mid}}} - d_{com}\right) i_{v'_{\mathrm{mid}}} + d_{v'_{\max}} \left(i_{v'_{\max}} + i_{v'_{\min}}\right) . \tag{22}$$

By substituting the upper equation into Eq. (6), we can obtain the following:

$$d_{com} = d_{v'_{\mathrm{mid}}} - \left(i_{ox} - d_{v'_{\max}} \left(i_{v'_{\max}} + i_{v'_{\min}}\right)\right) / i_{v'_{\mathrm{mid}}} . \tag{23}$$

Whether the d_{com} calculated by Eq. (23) satisfies Eq. (21) should be determined. If d_{com} exceeds the range, then the nearest boundary value $d_{v'_{\mathrm{mid}}}$ or 0 should be selected.

Finally, only one phase is chosen at each switching period to minimize the switching loss.

IV. Simulation and Experimental Results

The proposed strategies are verified by simulation and experiments. The simulation and experiments parameters are as follows: DC-link voltage of 540 V, DC-link capacitors of

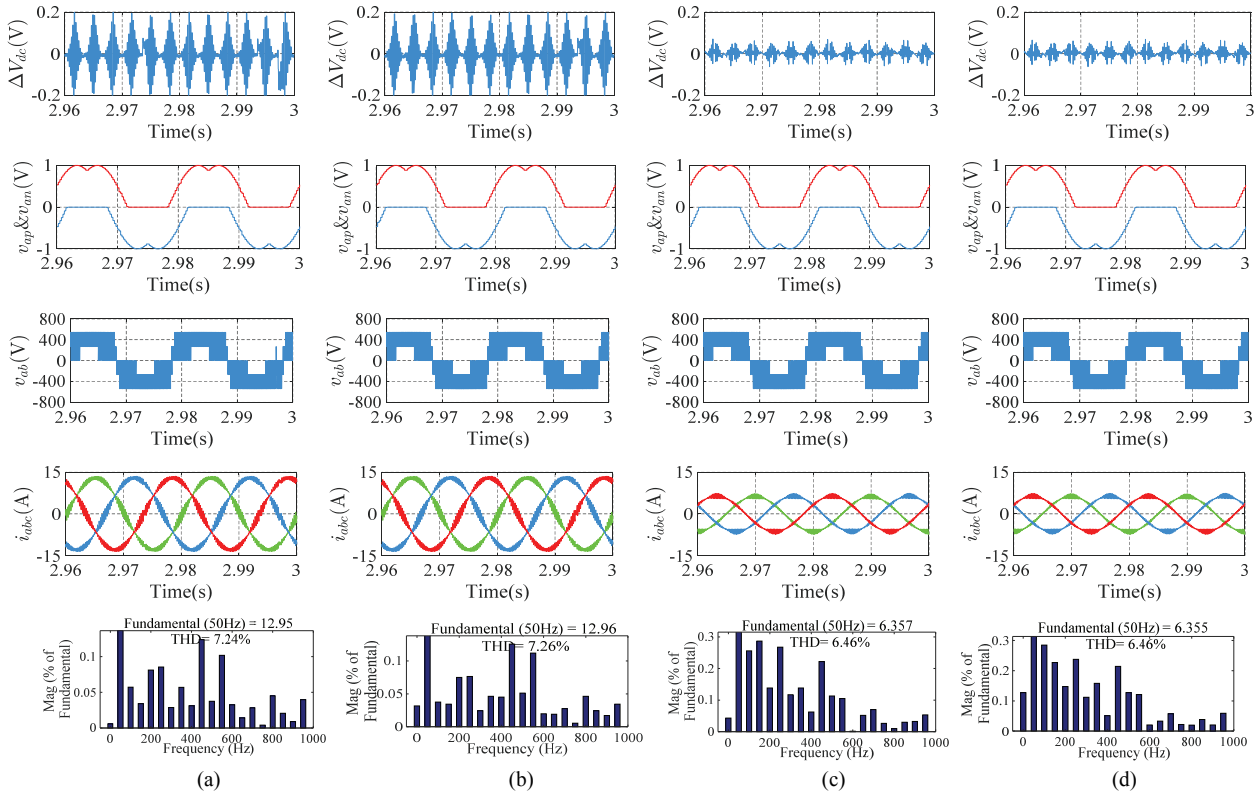

Fig. 6. Simulation with middle zero-sequence voltage injection: (a) Strategy One with m = 1.0, RL load; (b) Strategy Two with m = 1.0, RL load; (c) Strategy One with m = 1.0, no-load motor; (d) Strategy Two with m = 1.0, no-load motor.

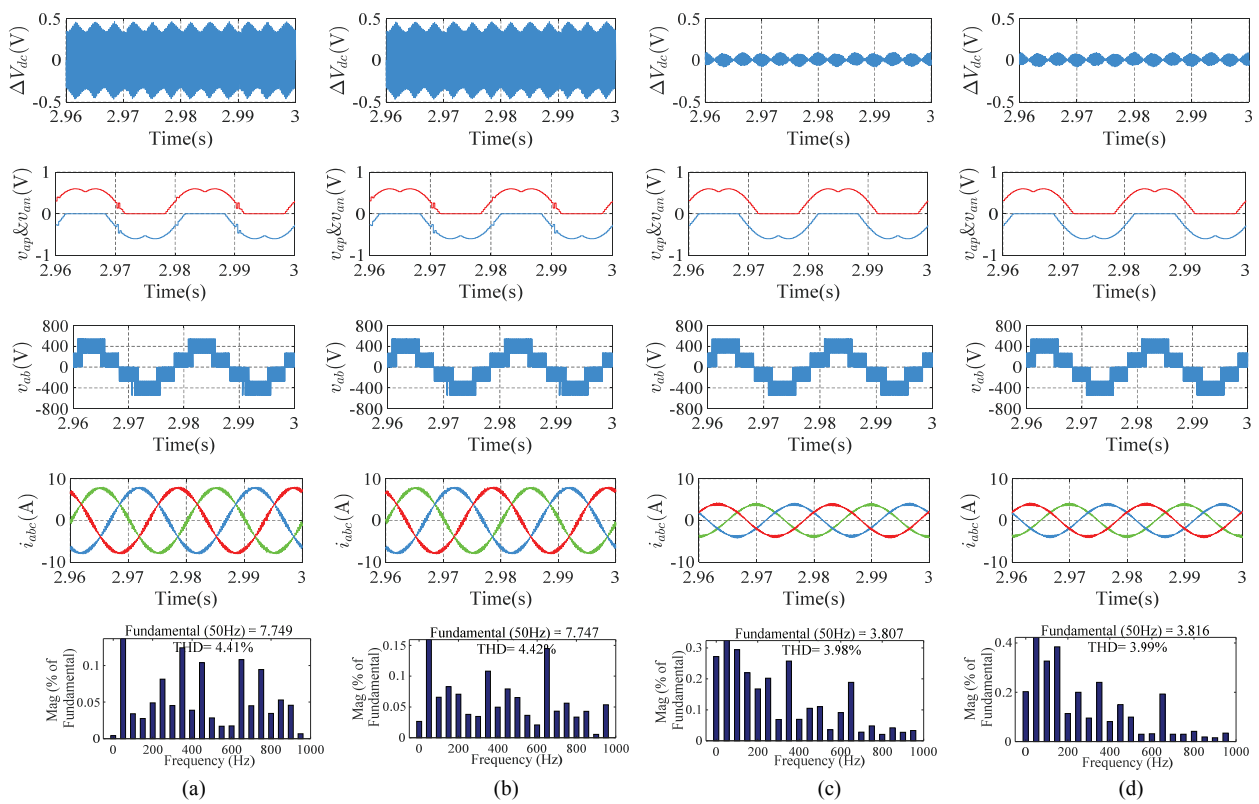

Fig. 7. Simulation with middle zero-sequence voltage injection: (a) Strategy One with m = 0.6, RL load; (b) Strategy Two with m = 0.6, RL load; (c) Strategy One with m = 0.6, no-load motor; (d) Strategy Two with m = 0.6, no-load motor.

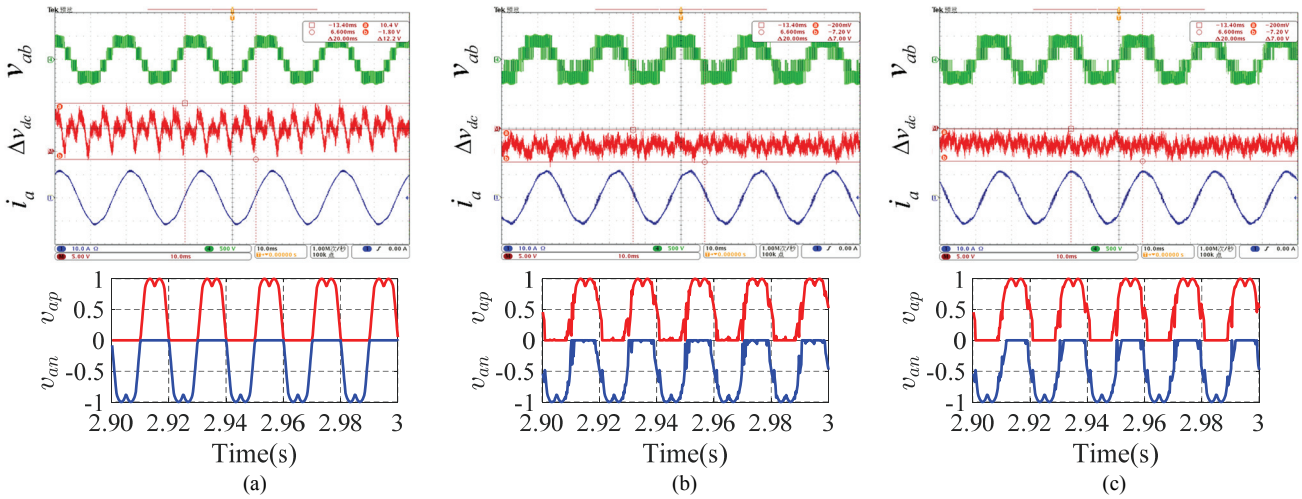

Fig. 8. Experimental results with middle zero-sequence voltage injection: (a) without NP control; (b) Strategy One with m = 1.0, RL load; (c) Strategy Two with m = 1.0, RL load (Y-axis scales are 500 V/div for v_{ab}, 5 V/div for Δv_{dc}, 10 A/div for i_a).

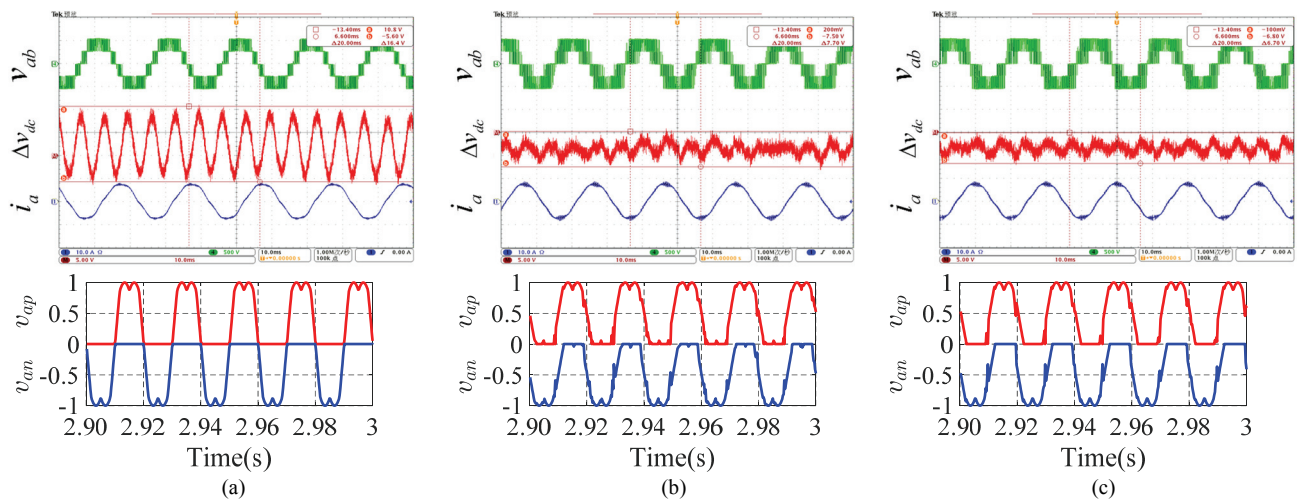

Fig. 9. Experimental results with middle zero-sequence voltage injection: (a) without NP control; (b) Strategy One with m = 1.0, no-load motor; (c) Strategy Two with m = 1.0, no-load motor (Y-axis scales are 500 V/div for v_{ab}, 5 V/div for Δv_{dc}, 10 A/div for i_a).

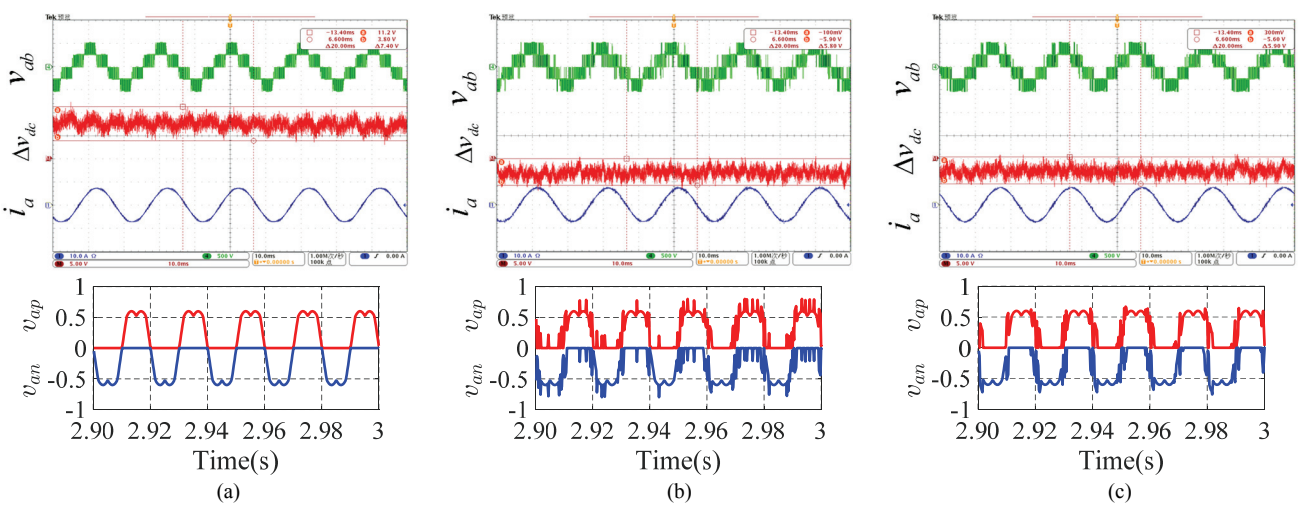

Fig. 10. Experimental results with middle zero-sequence voltage injection: (a) Without NP control; (b) Strategy One with m = 0.6, RL load; (c) Strategy Two with m = 0.6, RL load (Y-axis scales are 500 V/div for v_{ab}, 5 V/div for Δv_{dc}, 10 A/div for i_a).

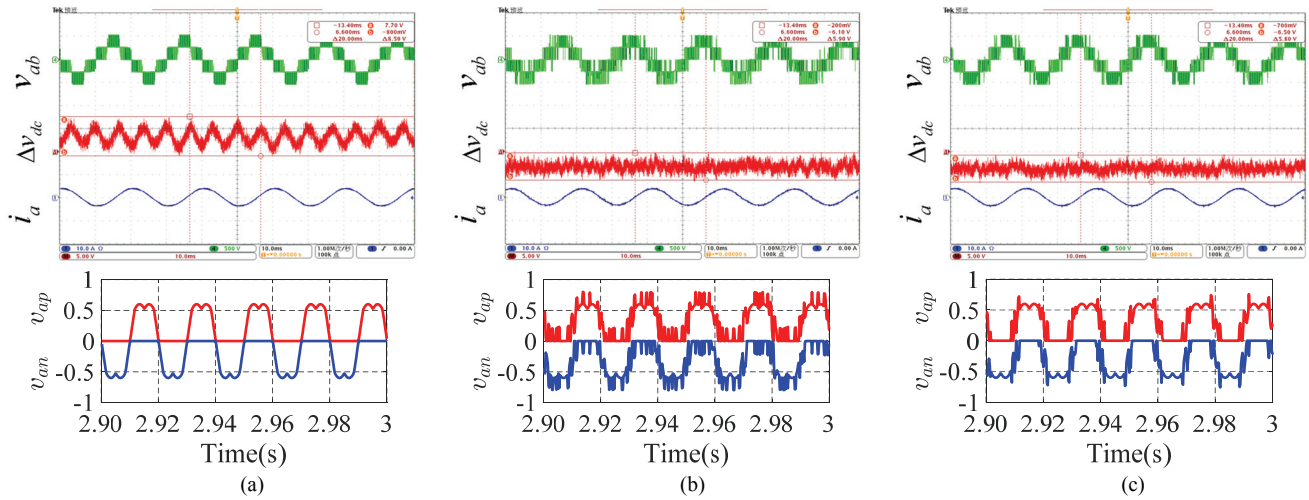

Fig. 11. Experimental results with middle zero-sequence voltage injection: (a) Without NP control; (b) Strategy One with m = 0.6, no-load motor; (c) Strategy Two with m = 0.6, no-load motor (Y-axis scales are 500 V/div for v_{ab}, 5 V/div for Δv_{dc}, 10 A/div for i_a).

1000 μF, switching frequency of 4 kHz, and modulation voltage frequency of 50 Hz. The two NP voltage control strategies in Section III are described as Strategy One and Strategy Two.

The parameters of the three-phase RL loads in the star connection scheme are as follows. The resistance of each phase is R = 24 Ω, L = 5 mH, and the power factor is 0.999. These parameters represent the condition of a high-power factor. The parameters of the induction motor are as follows: rated power of 5.5 kW, rated voltage of 380 V, rated frequency of 50 Hz, rated current of 11.9 A, number of pole-pairs of 2, and no-load-operation motor. These parameters represent the condition of a low power factor of approximately 0.016.

Fig. 6 shows the simulation results of Strategy One and Strategy Two under m = 1.0, with the middle zero-sequence voltage injection of both, connected to RL load or no-load motor. Fig. 7 shows the simulation results of Strategy One and Strategy Two under m = 0.6. ΔV_{dc}=v_{C1}-v_{C2} is the voltage fluctuation of the DC-link. The five waveforms in the figures above represent NP voltage fluctuation ΔV_{dc}; modulation voltages v_{ap} and v_{an}; output line voltage v_{ab}; three-phase currents i_a, i_b, and i_c; and the FFT analysis of the current (i_a) of phase a from top to bottom.

Figs. 6 and 7 indicate that Strategy One and Strategy Two have noticeable effects on NP voltage fluctuation under the condition of middle zero-sequence voltage injection. The voltage fluctuations of Strategy One and Strategy Two are nearly the same, and the modulation signals are identical as well. Consequently, the THD of the two strategies are nearly the same. Thus, the two proposed strategies are almost identical when middle zero-sequence is injected to the original modulation signals. They are all based on the O level disassembly and phase, with the largest d_{jo} chosen as the disassembly phase.

However, zero-sequence is not indispensable to Strategy One. Thus, it can be adopted to those conditions where zero-sequence voltage is not needed, such as in a three-phase four-wire system. Strategy Two is more straightforward than Strategy One, and its computational complexity is thus lower. According to calculation and deduction, v'_{mid} has the largest d_{jo}. Consequently, v'_{mid} is chosen for O level disassembly. However, this is true only when middle zero-sequence is injected, which is the commonality and difference between the two methods. Accordingly, the switching frequency is 4/3 times higher than before. As the FFT analysis shows, the number of low-frequency harmonic invasions increases mainly because of the increasing switching frequency.

The corresponding experimental results are shown in Figs. 8 to 11. The four waveforms in each figure represent line voltage v_{ab}, NP voltage fluctuation ΔV_{dc}, phase current i_a, modulation voltages v_{ap} and v_{an} from top to bottom.

The experimental results show that with zero-sequence voltage injection, the two control strategies have a promising effect on the suppression of NP voltage fluctuation, which is consistent with the findings of the control domain analysis in Section III. The imbalance and low frequency fluctuation of NP voltage is suppressed, and the output current is sinusoidal. Notably, the switching times increase due to the O level disassembly, thus worsening output current quality.

V. Conclusions

With focus on the NP voltage fluctuation mechanism, the relationship between O level disassembly and NP current is studied comprehensively in this work. A detailed and clear discussion of the O level disassembly phase is presented. Based on such discussion, the essence of the dynamic balance of the NP voltage is proposed. Given the middle zero-sequence injection, an easy method of determining the

disassembly phase is finally proposed. Simulation and experiments are conducted to verify the validity and practicability of the strategies.

The strategies proposed have a certain correlation with the two modified modulation algorithm. Comparatively, the proposed balance algorithms, which are based on the relationship between *O* level disassembly, NP current, and NP voltage, are more direct and clearer. NP voltage fluctuation can be completely compensated without the low-frequency fluctuation of the NP voltage.

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