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DC-Link Capacitor Voltage Balanced Modulation Strategy Based on Three-Level Neutral-Point-Clamped Cascaded Rectifiers

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Abstract

This study proposes a new modulation strategy to deal with unbalanced output voltage that is based on three-level neutral-point-clamped cascaded rectifiers. The fundament idea is to reallocate the value of the voltage levels generated by each of the modules on the basis of space vector pulse width modulation. This proposed modulation strategy can reduce the switching frequency while maintaining the mutual-module voltage balance. First, an analysis of unbalanced output voltage is reflected. Then a new modulation strategy is introduced in detail. Internal module capacitor voltages are balanced by the selection of redundant vectors. Moreover, the voltage balance ability is calculated. Finally, the feasibility of this modulation strategy is verified through experimental results.

Key words: Balance region calculation, Cascaded rectifier, Neutral-point-clamped, Voltage balanced modulation

I. INTRODUCTION

Multilevel convertors are widely used in high-power applications for medium or high voltages due to their structural advantages in terms of high capacity, high output voltage and low voltage rating requirements for the power switches [1], [2]. At present, the power electronic transformers for 15 kV single-phase traction power supply systems in Europe use the cascaded H-bridge rectifier (CHBR) topology [2]. The three-level neutral-point-clamped cascaded rectifier (3LNPC–CR) requires fewer modules, generates more output voltage levels, and has greater superiority in high-voltage and large-capacity conditions than the CHBR. However, an unbalanced capacitance voltage within the individual modules and an unbalanced DC-link voltage between the modules are the main problems of the 3LNPC–CR topology [3].

The phenomenon of unbalanced DC-link capacitor voltages are inevitable in 3LNPC convertors. The authors of [4], [5] researched a hardware voltage sharing circuit and a modulation strategy to deal with the unbalance capacitance voltage within modules [4], [5]. The use of hardware voltage sharing circuits effectively equalizes the capacitance voltage of the DC link. However, it results in the problems of circuit complexity, high costs and large losses. Meanwhile, the modulation strategies are conducted using redundant vectors to control the capacitor voltage and to change the direction of the capacitor current to realize the voltage balance [6]. This design has been widely applied in single-phase NPC convertors to deal with the unbalance problem.

A problem within a module is expected when the loads of a cascaded converter differ or the loads change. Differences appear in the output power, and an unbalanced voltage exists among the modules in practical applications. Control and modulation strategies are generally based on proportional–integral (PI) controllers and phase–shift carriers (PSC). These

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strategies are commonly used to balance the mutual-module voltage in research and various applications [7]. PI-based strategies balance the voltage by adjusting the modulation of each module. However, these strategies are limited, given that modulation waves range from −1 to 1. Hence, these strategies fail when the modulation wave of any module exceeds 1 or −1. To extend the capability in terms of voltage balance, several modulation strategies have been studied [8]-[15]. The authors of [8]-[11] proposed a modulation strategy that is based on CHBR. In [8]-[10], strategies with extended operating regions were researched. These strategies balance the DC-link voltage even with the removal of the load of one module. Although these strategies are effective, the process of switch state change is not considered. A 3-D space modulation is utilized in a three-module CHBR, which has good voltage balance capability [11]. However, the 3-D concept requires smooth operation of the switch state changes in the 3-D cube. A generalized expression of the switching frequency was obtained in [12], where the result was derived on the basis of time-domain current error dynamics, which is applicable at any level of a cascaded multilevel inverter. The balanced modulation strategies in [13]-[15] were proposed for solving the voltage balance of 3LNPC–CRs. These strategies can also balance the DC-link voltage when one module has no load. However, a switch state jump was observed in [13]. The authors of [14] proposed a modulation strategy that can smoothen the switch state using a complex optimism algorithm. The authors of [15] used SPM modulation to simplify the smoothening strategy. However, some of the dynamic character is lost in voltage balance ability. A modulation strategy has been composed of pulse width modulation (PWM) and space vector PWM (SVPWM). PSC–PWM has superiority in terms of its high-power quality and simple implementation of modular and distributed control. Meanwhile, SVPWM has advantages in terms of its feasible physical meaning, high voltage utilization rate and adaptive digital realization [17]-[20].

The DC-link voltage balance control strategies in cascaded inverters have been studied extensively. However, the balancing capability of any of these strategies is limited. Thus, the voltage balance capability of modulation should be calculated to obtain the limit of the unbalance degree [14]-[22]. In CHBR research, most of the voltage balance regions use output power as the result [12]-[15]. However, using output power as the result, changes with the load of the rectifier. The authors of [13]-[15] proposed an unbalance degree that uses the admittance of the load to allow the calculation result to remain unchanged even with changes in the load of the rectifier. The authors of [14] calculated the voltage balance capability of a 3LNPC–CR with different modules. The authors of [17] adopted the PSC-SVPWM into the voltage balance. However, this does not represent the voltage balance capability. This study indicated that the capability increased

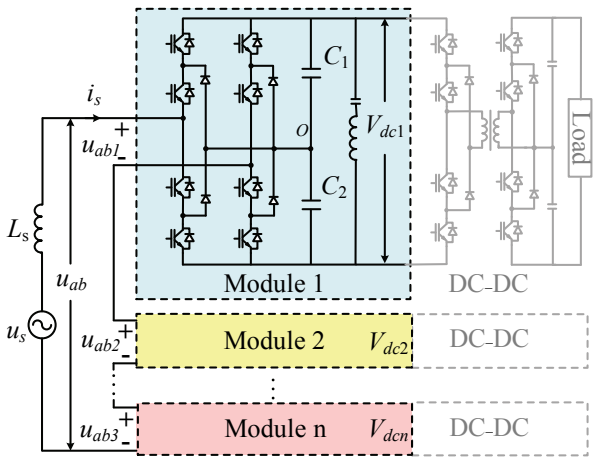

Fig. 1. Structure of a 3LNPC–CR.

when a gain was obtained in the modules of a 3LNPC–CR. The authors of [16] used the PSC-SVPWM modulation strategy to deal with the voltage balance problem in a 3LNPC-CR, which was reported in IPEC 2018. This paper is an improvement of the paper presented in that conference. When compared with the conference paper [16], this paper added an analysis of the basic principle of the modulation strategy and reveal the relationship between the modulation index and the voltage balance capability. It also presents more complete simulation and experimental results.

In PSC–SVPWM, the input voltage level may change rapidly at a given time [18]. Two or more modules change the voltage level simultaneously, and the switching frequency increases. These changes can lead to a rectifier-bridge short. A SVPWM modulation strategy for multimodule 3LNPC–CRs is proposed in this study to reduce the number of the changing modules, to change them to the levels of adjacent modules and to ensure normal operation of the converter. The proposed strategy solves the internal module and mutual-module unbalanced problems as the switching frequency is reduced. Simulation and experiment results verify the feasibility and validity of the proposed strategy.

II. Structure of an NPC–CR

Fig. 1 shows the structure of a multimodule NPC–CR. Each module is made up of two bridges, and each bridge can output three voltage levels: +E, 0, and -E. E is the capacitance voltage in the balanced case.

Control and DC-link capacitor voltage balanced modulation strategies are shown in Fig. 2. Transient current control is applied for the NPC–CR to maintain the sinusoidal structure of the grid current and power factor unity as well as to tract the sum of the reference DC-link voltage. This strategy is composed of a voltage outer loop and a current inner loop, where V_{dci} is the DC-link voltage of each module, and V_{dc}* is the sum of the DC-link voltage references. i_s* is the result of

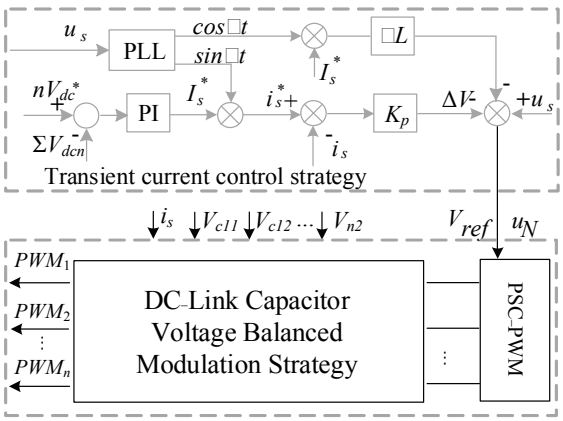

Fig. 2. Transient current control strategy.

TABLE I
VOLTAGE LEVEL STATE OF AN NPC RECTIFIER (i_S>0)

U_{abx}	Mode	V_a	V_b	C_1	C_2
2E	1	E	−E	Charge	Charge
E	2	E	0	Charge	No effect
	3	0	−E	No effect	Charge
0	4	0	0	No effect	No effect
−E	5	−E	0	No effect	Discharge
	6	0	E	Discharge	No effect
−2E	7	−E	0	Discharge	Discharge

the PI controller that obtains the error between V_{dc}* and the sum of V_{dci}.

In this study, u_s is the input AC voltage. The phase and frequency of u_s can be detected using a phase-locked loop, which can be used as the phase and frequency of i_s*. The grid current can track i_s* using the PI controller to maintain the sinusoidal characteristic of i_s. Thus, the system can acquire u_{ref}, which can be predicted as follows:

$$\begin{cases} i_s^* = K_{vp}(V_{dc}^* - \sum V_{dc}) + \int (V_{dc}^* - \sum V_{dci})dt / K_{vi} \\ u_{ref} = u_s - \omega L i_s^* \cos \omega t - K_{ip}[i_s^* \sin \omega t - i_s] \end{cases}, \quad (1)$$

where uS is the sign of the input voltage, V_{dci} is the output voltage of module I, and V_{dc}* is the reference voltage of all the modules. U_s and i_s represent the voltage and current of the grid side, respectively. Table I presents the relationship between the switch states and power flow of a single module when i_s>0.

III. MODULATION STRATEGY OF AN NPC–CR

A. Determination of Working Area

A new modulation strategy is proposed, which is based on a three-module 3LNPC–CR that can generate 13 voltage levels in the overall input terminal. Accordingly, u_{ab}* can be divided into 12 areas on the basis of its instantaneous value. M is the amplitude modulation degree. The mathematical expression of u_{ab}* is presented in equation (2), and the specific area determination rules are presented in equations (3) and (4).

$$u_{ab}^* = 6EM \sin(\omega t), \quad (2)$$

$$|area| = \begin{cases} 6, & 5E < |u_{ab}^*| \\ 5, & 4E < |u_{ab}^*| \le 5E \\ 4, & 3E < |u_{ab}^*| \le 4E \\ 3, & 2E < |u_{ab}^*| \le 3E \\ 2, & E < |u_{ab}^*| \le 2E \\ 1, & 0 < |u_{ab}^*| \le 1E \end{cases}, \quad (3)$$

$$area = \begin{cases} |area|, & u_{ab}^* \ge 0 \\ -|area| + 1, & u_{ab}^* < 0 \end{cases}. \quad (4)$$

B. Determination of the Input Voltage Levels of Each Module

The output voltage is unbalanced with different loads of all the modules since power flows in the direction of the rectifier. The power outflows have the same situation. This new modulation strategy aims to adjust the power distribution and to keep the output voltage balanced by reallocating the input voltage levels of each of the power modules. In particular, when the grid current i_s>0, the output voltage of module i is assumed to be the highest among those of the cascaded modules. When u_{abi}>0, the voltage level should be decreased to decrease the power flow into module i. When u_{abi}<0, the voltage level should also be decreased to increase the outflow power of module i. When the grid current i_s<0, the output voltage of module k is assumed to be the lowest among those of all the cascaded modules. When u_{abk}>0, the voltage level should be increased, which increased the flow of power into module k. When u_{abk}<0, the input voltage level should also be increased to decrease the power outflow of module k. Accordingly, properly reallocating the input voltage levels of each of the modules balances the output voltages.

The reference voltage u_{ab}* is composed of the two nearest voltage vectors V_A [V_{A1},V_{A2},V_{A3}] and V_B[V_{B1},V_{B2},V_{B3}], which represent the input voltages of module1, module2 and module3. $V_{A,sum}$ and $V_{B,sum}$ are the overall input voltage levels when V_A and V_B are operational. The reference voltage u_{ab}* can be expressed using equation (2). The initial value of u_{ab}* is zero. Thus, at the beginning, V_A and V_B are set to [0 0 0]. The relationship between V_A and V_B is shown in Equation (5). When the slope of u_{ab}* is positive, V_A and V_B represent the voltage levels of the lower and upper boundaries in each area, respectively. When the slope of u_{ab}* is negative, V_A and V_B represent the voltage levels of the upper and lower boundaries in each area, where E is the DC-link voltage.

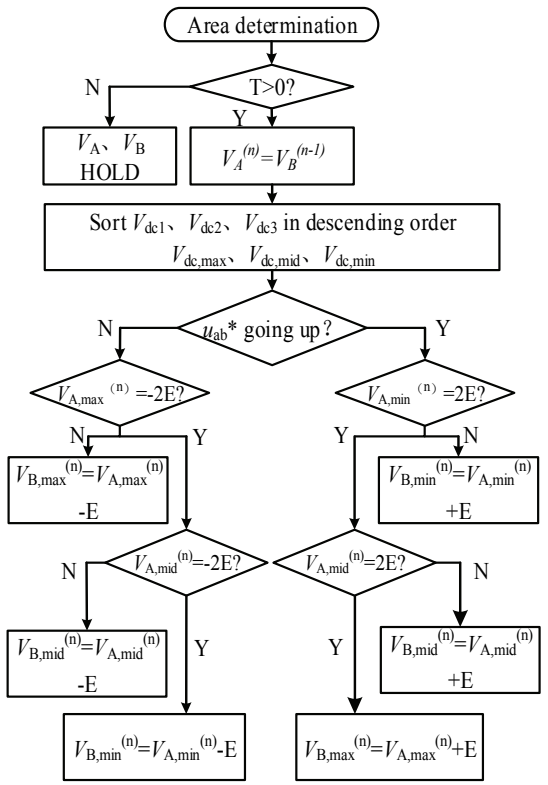

Fig. 3. Flowchart of the voltage vector distribution when i_s>0.

$$\begin{cases} V_{A,sum}-V_{B,sum}=-E,\ u_{ab}^{*} \text{ is going up} \\ V_{A,sum}-V_{B,sum}=E,\ u_{ab}^{*} \text{is going down} \end{cases} \tag{5}$$

The procedure of the proposed modulation strategy is presented when the grid current i_s>0, which is same as when the grid current i_s<0.

1) Determine the area where uab* is working.

2) If the area changes or uab* achieves its maximum and minimum values, it generates the triggering signal T. This signal decided the VA, VB to plus or minus E.

3) Rank Vdc1, Vdc2 and Vdc3 in a descending order, and Vdc,max, Vdc,mid and Vdc,min is the result. Mmax, Mmid and Mmin stand for modules with the maximum, medium, and minimum output voltages, respectively.

4) Determine whether uab* shows a tendency to rise. On the one hand, if it does show a tendency to rise, then the input voltage of Mmin adds E. If the input voltage of Mmin has already reached 2E and it cannot increase anymore, the input voltage of Mmid adds E before its input voltage reaches 2E. Otherwise, the input voltage of Mmin must add E. On the other hand, if uab* does not exhibit the tendency to go up, the input voltage of Mmax subtracts E. If the input voltage of Mmax becomes −2E and it cannot decrease anymore, the input voltage of Mmid subtracts E at the second priority. If the input voltage of Mmid has reached −2E, the last choice is the input voltage of Mmin minus E.

5) The vector of the input voltage before the triggering signal T is allocated to VA, and the input vector of the voltage after T is allocated to VB. Therefore, VB is obtained in the same way as VA. Prior to this procedure, VB obtained in the previous triggering period should be allocated to VA in the early stage of the current triggering period for continuity of the whole process.

For the sake of simplicity, the procedure is similar when i_s<0.

TABLE II
PRINCIPLE FOR CHOOSING REDUNDANT VECTORS

	$V_{C1}>V_{C2}$, $i_s>0$	$V_{C1}>V_{C2}$, $i_s<0$	$V_{C1}<V_{C2}$, $i_s<0$	$V_{C1}<V_{C2}$, $i_s>0$
U_{abx}=E	$[V_a,V_b]$= [0,−E]	$[V_a,V_b]$= [E,0]	$[V_a,V_b]$= [0,−E]	$[V_a,V_b]$= [E,0]
U_{abx}=−E	$[V_a,V_b]$= [−E,0]	$[V_a,V_b]$= [0,E]	$[V_a,V_b]$= [−E,0]	$[V_a,V_b]$= [0,E]

C. On Time Calculation

$V_{A,sum}$ and $V_{B,sum}$ are the overall input voltage levels when V_A and V_B are operational. T_A and T_B refer to the "on" time of the voltage vectors V_A and V_B. The on time calculation can be obtained using the following equation:

$$u_{ab}^{*}=\begin{cases} V_{A,sum}T_A+V_{B,sum}T_B=u_{ab}^{*}T_s \\ T_A+T_B=T_s \end{cases}. \tag{6}$$

D. Internal Module Voltage Balance Strategy

The abovementioned steps are to determine the voltage levels to balance the mutual–module voltage. However, all of these steps should still consider the voltage levels of each of the bridge legs. In this way, the capacitor voltages of each module become balanced. Table I shows that even with the same input voltage, the charging/discharging states of the DC-link capacitors can be obtained differently using the redundant voltage vectors of each of the bridge legs. Considering the power flow direction and the difference between two capacitor voltages, these redundant voltage vectors are selected for obtaining the charging/discharging path for the DC-link capacitors. The detailed selection rules are presented in Table II.

E. Balanced Region Calculation

The balanced region is calculated to determine the balance capability. The DC-link voltage of each of the modules remains balanced when the unbalanced module remains steady. Thus, the capacitor energy of an unbalanced module must be maintained to remain unchanged during one period. The unbalanced load must consume the input energy of an unbalanced module. An experiment is conducted to verify the calculation. In this experiment, a three-module 3LNPC–CR is deduced. Fig. 4 shows that the modulation wave is symmetrical according to the proposed strategy. Thus, only a quarter period of the input energy is needed in the calculation of the

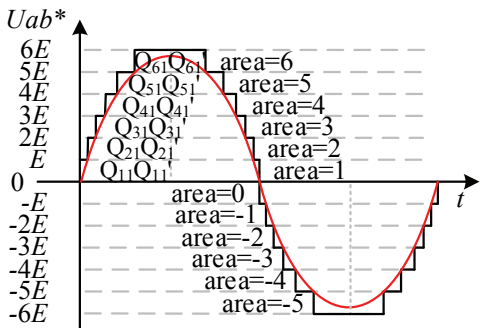

Fig. 4. Region of the proposed strategy.

TABLE III
WORKING TIME OF AN NPC–CR IN EACH AREA

m	Ta	Tb
Area=1	(1−6 Msin(ωt))Ts	(6 Msin(ωt))Ts
Area=2	(2−6 Msin(ωt))Ts	(6 Msin(ωt)−1)Ts
Area=3	(3−6 Msin(ωt))Ts	(6 Msin(ωt)−2)Ts
Area=4	(4−6 Msin(ωt))Ts	(6 Msin(ωt)−3)Ts
Area=5	(5−6 Msin(ωt))Ts	(6 Msin(ωt)−4)Ts
Area=6	(6−6 Msin(ωt))Ts	(6 Msin(ωt)−5)Ts

balanced region. The working times of the NPC–CR in each area are shown in Table III.

The calculation result of the input energy is shown as follows, where Q_{11} to Q_{61} and Q_{11}' to Q_{61}' are the input energies for the high and low levels in the six areas, respectively. Where $\theta = \omega t$.

$$\begin{cases} Q_{11} = -\int_{0}^{\sin^{-1}(\frac{1}{6M})} V_{dc1} i_s (6M\sin\theta) d\theta \\ Q_{21}' = -0.5\int_{\sin^{-1}(\frac{1}{6M})}^{\sin^{-1}(\frac{2}{6M})} V_{dc1} i_s (2-6M\sin\theta) d\theta \\ Q_{21} = -\int_{\sin^{-1}(\frac{1}{6M})}^{\sin^{-1}(\frac{2}{6M})} V_{dc1} i_s (6M\sin\theta-1) d\theta \\ Q_{31}' = -\int_{\sin^{-1}(\frac{2}{6M})}^{\sin^{-1}(\frac{3}{6M})} V_{dc1} i_s (3-6M\sin\theta) d\theta \\ Q_{31} = -0.5\int_{\sin^{-1}(\frac{2}{6M})}^{\sin^{-1}(\frac{3}{6M})} V_{dc1} i_s (6M\sin\theta-2) d\theta \\ Q_{41}' = -0.5\int_{\sin^{-1}(\frac{3}{6M})}^{\sin^{-1}(\frac{4}{6M})} V_{dc1} i_s (4-6M\sin\theta) d\theta \\ Q_{51}' = 0.5\int_{\sin^{-1}(\frac{4}{6M})}^{\sin^{-1}(\frac{5}{6M})} V_{dc1} i_s (6M\sin\theta-4) d\theta \\ Q_{61}' = \int_{\sin^{-1}(\frac{5}{6M})}^{\frac{\pi}{2}} V_{dc1} i_s (6-6M\sin\theta) d\theta \\ Q_{61} = \int_{\sin^{-1}(\frac{5}{6M})}^{\frac{\pi}{2}} V_{dc1} i_s (6M\sin\theta-5) d\theta \\ Q_{11}' = Q_{41} = Q_{51} = 0 \end{cases} \tag{7}$$

According to the energy consumption analysis above, the DC-link voltage of the unbalanced module remains balanced only if the load exhausts the input energy. Thus, the balanced region calculation is defined in equation (8), where Δy refers to the unbalance degree, Y_i is the admittance of the module i,

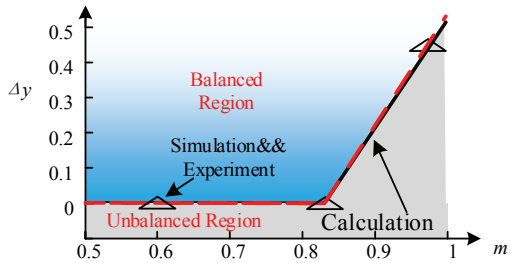

Fig. 5. Balanced region calculation of a three-module 3LNPC–CR.

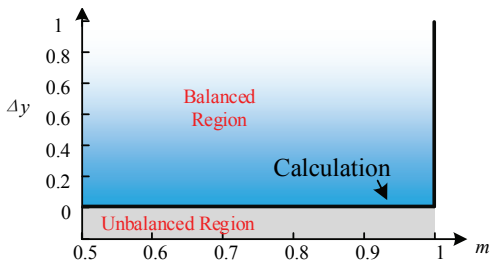

Fig. 6. Balanced region calculation of n-modules.

Y_l is the admittance of the changed load, f is the area of U_{ab}*, and M is the amplitude modulation degree. According to equation (8), the load of the NPC–CR is balanced when Δy is 1. The unbalanced module has no load when Δy is 0. The result of the calculation is illustrated in Fig. 5.

$$\Delta y = \frac{n \cdot Y_l}{\sum_{j=1}^{n} Y_i} \geq \frac{2\sqrt{2} \cdot \sum_{f=1}^{f=6} (Q_{f1} + Q_{f1}')}{\pi \cdot M} \tag{8}$$

To apply the result in n modules, the n modules of a 3LNPC–CR are also calculated using equation (9). When n approaches infinity, $Q_{f(2n-1)1}$, $Q_{f(2n-1)1}'$, $Q_{f(2n)1}$ and $Q_{f(2n)1}'$ approach 0 as their zones decreases to 0. However, the sum of the other zones is negative. Therefore, the proposed strategy can balance the voltage in an n-module 3LNPC–CR, no matter what M is, when one load is removed. The result of this is shown in Fig. 6, which indicates that the voltage balance ability becomes stronger as the module of the 3LNPC–CR increases, as shown in [17].

$$\begin{aligned} \lim_{n\to\infty, Y_l=0} \Delta y &= \lim_{n\to\infty, Y_l=0} \frac{2\sqrt{2} \cdot \sum_{f=1}^{f=2n} (Q_{f1} + Q_{f1}')}{\pi \cdot M} \\ &= \lim_{n\to\infty, Y_l=0} \frac{2\sqrt{2} \cdot \sum_{f=1}^{f=2n-2} (Q_{f1} + Q_{f1}')}{\pi \cdot M} + \\ &\quad \lim_{n\to\infty, Y_l=0} (Q_{f(2n-1)1} + Q_{f(2n-1)1}' + Q_{f(2n)1} + Q_{f(2n)1}') \\ &= \lim_{n\to\infty, Y_l=0} \frac{2\sqrt{2} \cdot \sum_{f=1}^{f=2n-2} (Q_{f1} + Q_{f1}')}{\pi \cdot M} \leq 0 \end{aligned} \tag{9}$$

TABLE III
PARAMETERS OF A THREE-MODULE 3LNPC–CR

Parameter	Value
Grid voltage (u_s)	75 V
Grid inductor	2 mH
Load	30
Modulation index	0.8

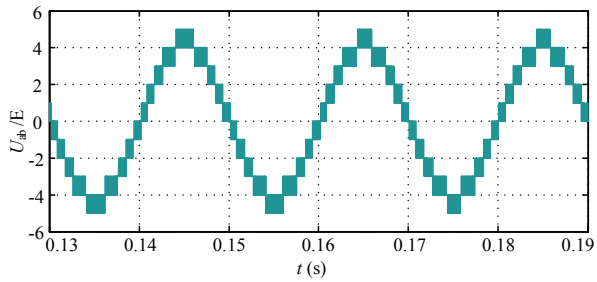

Fig. 7. Waveform of the input voltage levels of a three-module cascaded NPC rectifier.

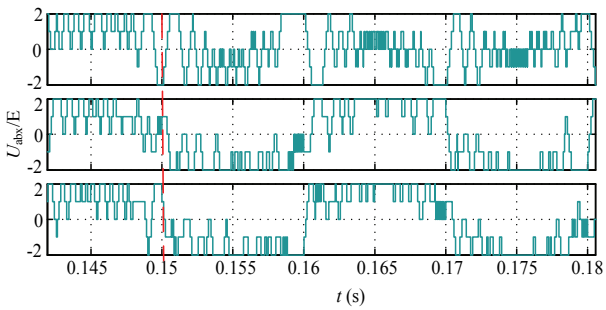

Fig. 8. Level–skip waveforms of module input voltages when the load of module 1 is cut off.

IV. SIMULATION AND EXPERIMENTAL RESULTS

For verifying the correctness of the proposed modulation strategy based on PSC-SVPWM, a simulation model based on a 3LNPC–CR is built using Simulink/MATLAB. Table III lists the parameters.

At 0.15 s, module 1 changed from normal load to no-load. Figs. 7 shows instantaneous waveforms of the overall input terminal voltage, while Fig. 8 illustrates the input voltage of each of the modules. Fig. 7 shows that when the reference voltage u_{ab}* reaches its peak value, it works in area 5 and is made up of 4E and 5E while the modulation index is 0.7. With an increase of modulation index, the working area becomes different. Although the load of module 1 is cut off, overall input voltage is not affected. Fig. 8 shows that the load voltage of module 1 becomes the highest among those of the three cascaded modules while the load of module 1 is cut off at 0.15 s. When the grid current is greater than zero, the input voltage of module1 is lower than those of module 2 and module 3, which indicates that less power flows into module 1. When the grid current is negative, the input voltage of module 1 is higher than those of the other modules, which indicates that more power flows out of module 1.

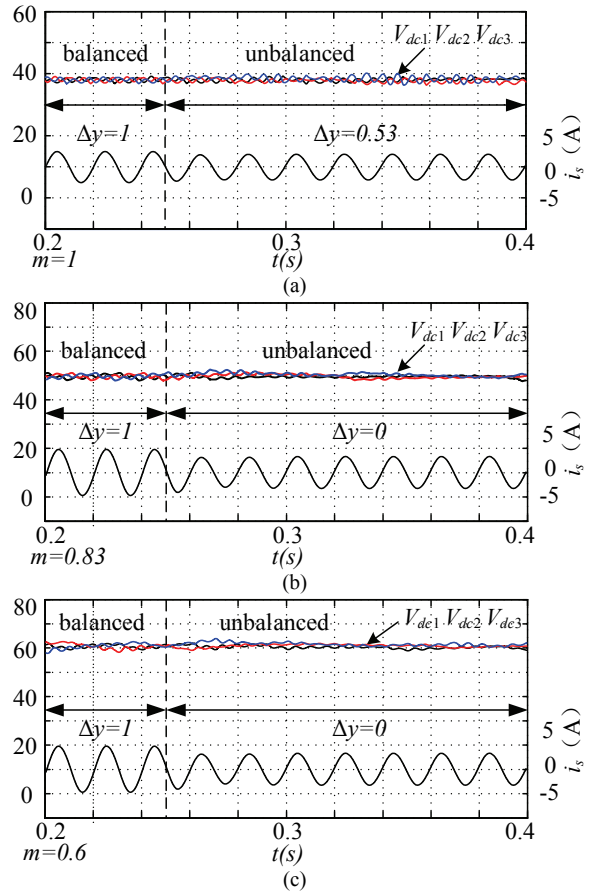

Fig. 9. Voltage and current waveforms when the load of module 1 is removed.

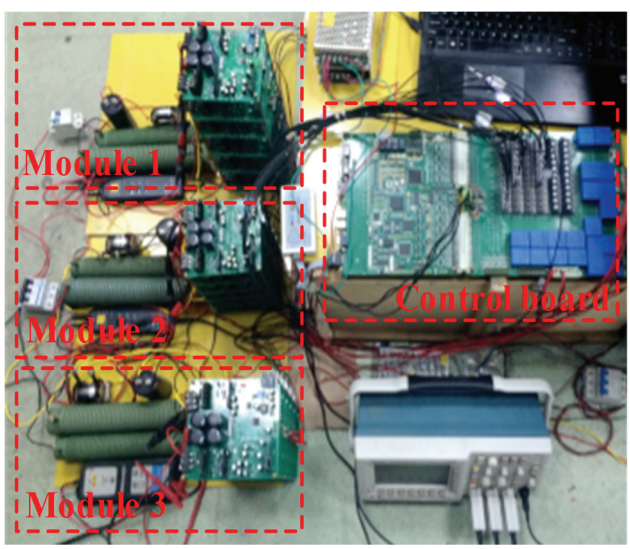

Fig. 10. Prototype of a three-module NPC–CR.

To verify the balanced region calculation, three points in Fig. 5, namely, m=1, m=0.83 and m=0.6, are simulated in Fig. 9. At 0.25 s, the load changes in the calculation, while the DC-link voltage of all the modules is kept balanced.

In order to verify the validly of the modulation strategy, an experimental platform has been built. Fig. 10 shows a picture

TABLE IV
PARAMETERS FOR THE EXPERIMENT

Parameter Names	Parameters	Numbers
Voltage source	75 V/50 Hz	1
IGBT	IHW20N120R	24
FPGA	EP3C55F484C8	
Voltage sensor	LV-25-P	4
Current sensor	LA-25-NP	1
Filter inductance	1 mH	1
DC-link voltage (V_{dc})	38–60 V	3
DC-link capacitor	1880 μF	6
Output power	114–360 W	1
Carrier wave frequency	1500 Hz	-
Inductance of LC	1 mH	3
Capacitance of LC	4700 μF	3
Max switch frequency	2750 Hz	
Number of modules	3	-

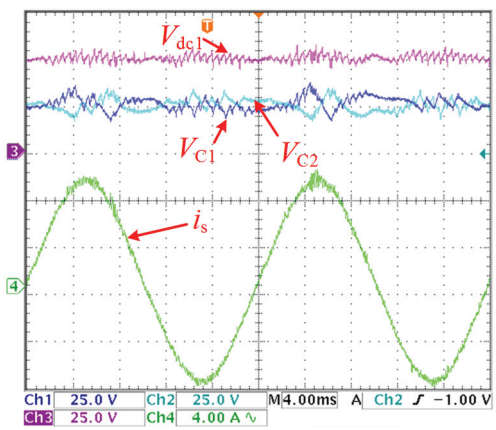

Fig. 11. Voltages of a capacitor in a module.

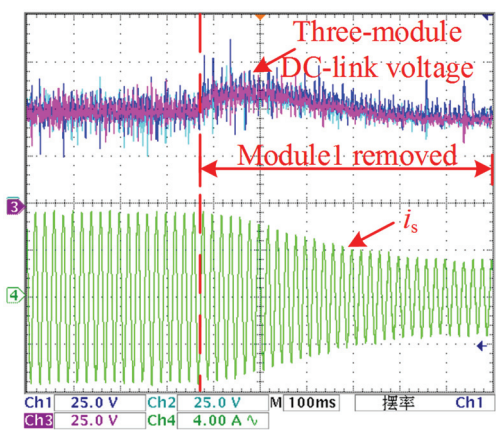

Fig. 12. Voltage and current waveforms when the load of module 1 is removed (m=0.83).

of the prototype. The experimental parameters are identical to those in the simulation, as presented in Table IV.

Fig. 11 shows that the internal capacitor voltage of module1 is balanced and that the rectifier has good static performance.

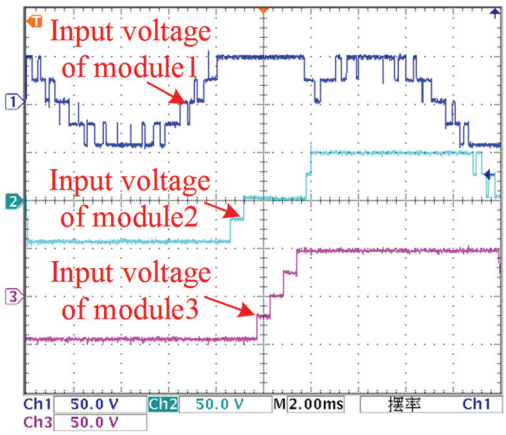

Fig. 13. Level–skip waveforms of the module input voltages when the load of module 1 is removed.

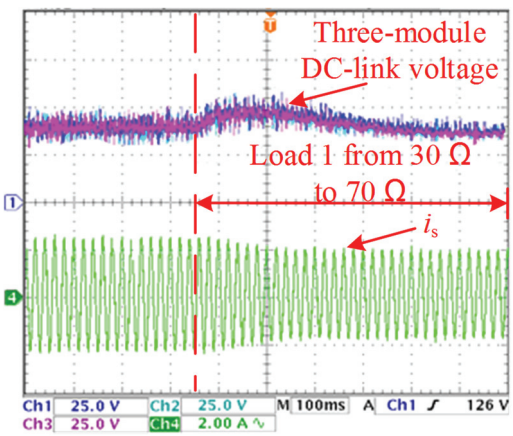

Fig. 14. Voltage and current waveforms when the load of module 1 changed from 30 Ω to 70 Ω (m=1, Δy=0.53).

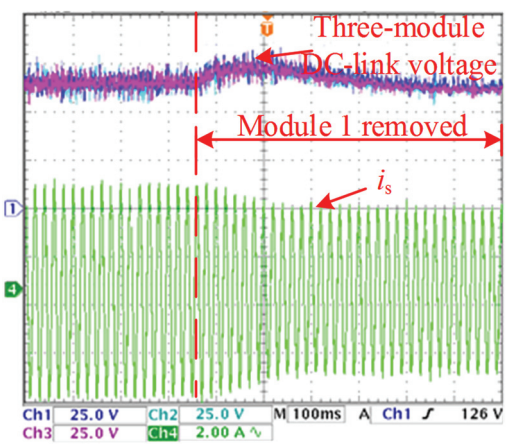

Fig. 15. Voltage and current waveforms when the load of module 1 is removed (m=0.6, Δy=0).

In order to verify the dynamic properties, the load of module 1 is cut off. Fig. 12 shows that the output voltage of each module converges and is kept balanced after approximately 0.26 s. The grid current remains steady except for a reasonable change in its amplitude due to the fact that the load is cut off.

Fig. 13 shows that after the load of module 1 is cut off, the input voltage of module 1 changes rapidly, which balances the output voltages. When the grid current is positive and negative, the input voltage of module 1 becomes lower and higher, respectively. These conditions are consistent with the abovementioned modulation rules.

The experiment also verifies the balanced region calculation. Figs. 12, 14 and 15 match Fig. 9. This further verifies the results of the balanced region calculation.

V. CONCLUSIONS

On the basis of a three-module 3LNPC–CR, a new modulation strategy is proposed for obtaining the internal module and mutual-module voltage balances.

The properties of this new modulation strategy are as follows.

1) Only one module changes its input voltage level at each instant of the total voltage level change. This action effectively decreases the frequency of the switches.
2) The DC-link voltage rapidly converges to the same value even if one of the loads is cut off when the loads are unbalanced.
3) The balanced region of the proposed modulation is calculated and verified by simulation and experimental results. These results show the voltage balance capability of the proposed modulation.

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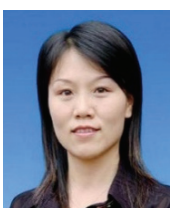

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