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DC-Link Voltage Balance Control Using Fourth-Phase for 3-Phase 3-Level NPC PWM Converters with Common-Mode Voltage Reduction Technique

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Abstract

This paper proposes a DC-link voltage balance controller using the fourth-phase of a three-level neutral-point clamped (NPC) PWM converter with medium vector selection (MVS) PWM for common-mode voltage reduction. MVS PWM makes the voltage reference by synthesizing the voltage vectors that cannot generate common-mode voltage. This PWM method is effective for reducing the EMI noise emitted from converter systems. However, the DC-link voltage imbalance problem is caused by the use of limited voltage vectors. Therefore, in this paper, the effect of MVS PWM on the DC-link voltage of a three-level NPC converter is analyzed. Then a proportional-derivative (PD) controller for the DC-link voltage balance is designed from the DC-link modeling. In addition, feedforward compensation of the neutral point current is included in the proposed PD controller. The effectiveness of the proposed controller is verified by experimental results.

Key words: Common-mode voltage reduction, DC-link voltage balancing control, Three-level NPC converter

I. INTRODUCTION

Power conversion systems using power semiconductors have a high efficiency and good power characteristics. Thus, they have been widely used in the industry in recent years. However, as the use of these power conversion systems increases, EMC/EMI problems are emerging as an important issue [1]-[4]. A power conversion system generates common-mode voltage (CMV) due to the operation of the power semiconductor. The EMI noise caused by CMV is conducted or radiated into other electric systems, which results in malfunctions of nearby equipment. For this reason, research has been conducted to reduce the EMI noise emitted from the power conversion systems [5]-[12].

Research on the reduction of the EMI noise is mainly aimed at reducing the common-mode voltage output in two-level or three-level PWM converter systems. In particular, the three-level NPC PWM converter has a much higher output quality and has a lower dv/dt than the two-level converter [15]-[18]. Among the voltage vectors available in a three-level NPC converter, six medium voltage vectors and one zero voltage vector do not generate common-mode voltage. From these characteristics, a PWM method using only medium voltage vectors and the zero voltage vector is proposed in [10]-[12]. This method has a significant effect on EMI noise reduction. However, it has a low quality output current because these methods do not use the nearest voltage vectors from the reference voltage. In particular, the DC-link voltage imbalance cannot be controlled because the voltage vector for controlling the imbalance between the upper and lower DC voltages is not used.

Since MVS PWM cannot control the DC-link voltage imbalance, the fourth-phase connected to the DC-link is added to solve the problem of the DC-link voltage imbalance [12]. In addition, a three-level NPC converter including a fourth-phase to replace a faulty phase under the fault condition, and to help control the DC-link voltage balance when a fault has not occurred has been proposed in [14]. Although a system

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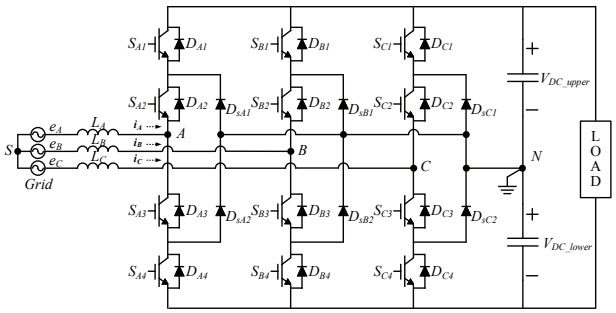

Fig. 1. Circuit configuration of a three-phase three-level NPC PWM converter.

including a fourth-phase for DC-link voltage balance has been proposed, a study on a control system considering the DC-link voltage characteristic has not been proposed.

Therefore, this paper proposes a balance controller for the DC-link voltage using the fourth-phase of a three-phase three-level NPC PWM converter with MVS PWM for the common-mode voltage reduction. The effect of MVS PWM on the DC-link of the three-level NPC converter is analyzed and a PD controller is designed from the modeling of the neutral point of the DC-link including the fourth-phase. In addition, the controller includes feedforward compensation of the current flowing from the converter to the neutral point of the DC-link to improve the performance of the controller according to changes of the input power. The effectiveness of the proposed control method is verified through experimental results.

II. PWM Method for Common-mode Voltage Reduction

Fig. 1 shows a three-phase three-level NPC converter. The switching states and output voltage of a single leg of the three-level NPC converter are presented in Table I. As shown in Table I, a three-phase three-level NPC converter can be operated with 27 switching states and these switching states can be classified into 4 types of voltage vectors depending on the voltage magnitude [19]-[21]. In addition, the converter outputs common-mode voltage according to the switching states, and the common-mode voltage can be defined in (1) [5], [6].

$$V_{CM} = V_{SN} = \frac{V_{AN} + V_{BN} + V_{CN}}{3}$$
$$V_{xN}(x = A, B, C) = \{-\frac{V_{DC}}{2}, 0, \frac{V_{DC}}{2}\} \quad (1)$$

In Fig. 2, a space vector diagram of the three-level NPC converter is described. Three-level NPC systems generally use space vector PWM (SVPWM). SVPWM makes the reference voltage V* by using the nearest three voltage vectors. When SVPWM is used in the converter, common-mode voltage is generated from the converter because the voltage

TABLE I
Amplitude of the Common-Mode Voltage According to the Switching States

Voltage Vectors	Magnitude	Switching States	Common-mode voltage output
Zero Vector	***0***	[PPP]	$V_{DC}/2$
		[OOO]	***0***
		[NNN]	$-V_{DC}/2$
Small Vector	$V_{DC}/3$	[POO], [OPO], [OOP]	$V_{DC}/6$
		[PPO], [POP], [OPP]	$V_{DC}/3$
		[ONN], [NON], [NNO]	$-V_{DC}/3$
		[NOO], [ONO], [OON]	$-V_{DC}/6$
Medium Vector	$V_{DC}/\sqrt{3}$	**[PON], [OPN], [NPO], [NOP], [ONP], [PNO]**	***0***
Large Vector	$2V_{DC}/3$	[PPN], [PNP], [NPP]	$V_{DC}/6$
		[PNN], [NPN], [NNP]	$-V_{DC}/6$

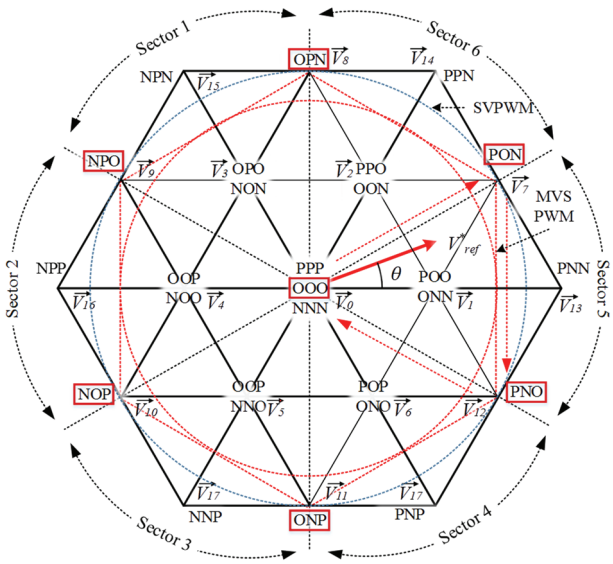

Fig. 2. Space vector diagram of MVS PWM.

vector used in SVPWM has common-mode voltage output in a range between -V_{DC}/3~+V_{DC}/3. However, medium voltage vector selection (MVS) PWM can make zero common-mode voltage output from the converter since the reference voltage of MVS PWM is synthesized by the nearest two medium vectors and a zero vector [OOO] that cannot generate common-mode voltage. Table II explains the sector division criterion of MVS PWM and the voltage vectors used in each of the sectors. Fig. 3 presents the switching sequence of the MVS PWM in sector 5. The switching sequence is started and ended in the zero vector [OOO], and two medium vectors are used as the effective voltage vector. If the effect of dead-time is not considered, the converter can generate zero

TABLE II
DIVISION OF SECTORS AND SWITCHING SEQUENCES

Sector	Theta (θ)	Switching Sequence		
		T_0	T_1	T_2
1	$\frac{\pi}{2} \le \theta < \frac{5\pi}{6}$	$\vec{V}_0$ [OOO]	$\vec{V}_9$ [NPO]	$\vec{V}_8$ [OPN]
2	$\frac{5\pi}{6} \le \theta < \frac{7\pi}{6}$	$\vec{V}_0$ [OOO]	$\vec{V}_9$ [NPO]	$\vec{V}_{10}$ [NOP]
3	$\frac{7\pi}{6} \le \theta < \frac{3\pi}{2}$	$\vec{V}_0$ [OOO]	$\vec{V}_{11}$ [ONP]	$\vec{V}_{10}$ [NOP]
4	$\frac{3\pi}{2} \le \theta < \frac{11\pi}{6}$	$\vec{V}_0$ [OOO]	$\vec{V}_{11}$ [ONP]	$\vec{V}_{12}$ [PNO]
5	$\frac{11\pi}{2} \le \theta$, $\theta < \frac{\pi}{6}$	$\vec{V}_0$ [OOO]	$\vec{V}_7$ [PON]	$\vec{V}_{12}$ [PNO]
6	$\frac{\pi}{6} \le \theta < \frac{\pi}{2}$	$\vec{V}_0$ [OOO]	$\vec{V}_7$ [PON]	$\vec{V}_8$ [OPN]

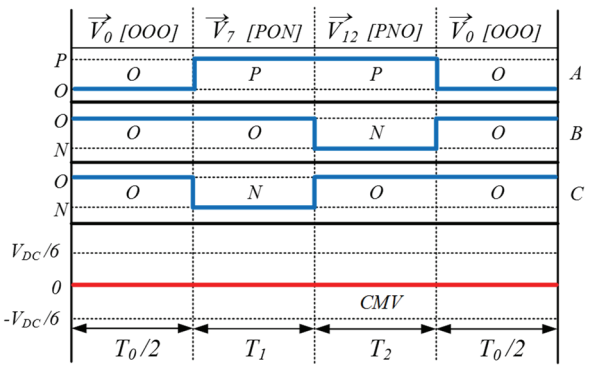

Fig. 3. Switching sequence of MVS PWM (Ex: Sector 5).

common-mode voltage.

Even if MVS PWM can reduce common-mode voltage, the voltage utilization decreases to 86.7% and the ripple of the phase current increases due to the limited use of switching states. In addition, the problem of DC-link voltage imbalance cannot be controlled since MVS PWM only uses medium voltage vectors.

III. EFFECT OF MVS PWM ON DC-LINK VOLTAGE IMBALANCE

Generally, the DC-link voltage imbalance of a three-level NPC PWM converter can be explained by four types of voltage vectors. The zero vector and large vector do not affect the voltage imbalance because no current flows through the capacitors or the same current flows through the upper and lower capacitors. However, the small vector seriously affects the voltage imbalance. The magnitudes of the currents flowing through the upper and lower capacitors are different, and the tendency of the imbalance is reversed depending on the switching type, P-type and N-type. In the case of a medium

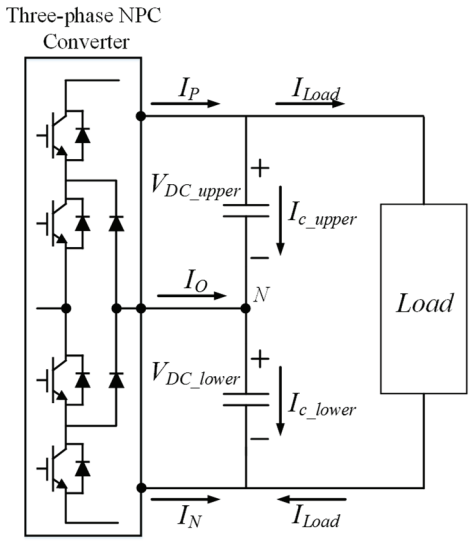

Fig. 4. DC-link equivalent circuit of a three-phase NPC converter with a constant load.

vector, the voltage imbalance is affected by the three-phase input current. However, it does not have a significant effect. Since MVS PWM is applied to the three-level NPC converter in this paper, a detailed analysis of the effect of MVS PWM on the voltage imbalance should be conducted for effective control of the DC-link voltage imbalance. Fig. 4 shows an equivalent circuit of a DC-link connected to a converter and a constant load. I_x (x=P, O, N) means the current flowing through the phase of the x-state. In the case of the [PON] switching state in sector 5 as described in Fig. 3, for example, I_P is the phase A current and I_N is the phase C current. The current flowing through the upper and lower capacitors, I_{c_upper} and I_{c_lower}, can be defined as (2) and (3), respectively.

$$I_{C\_upper} = I_P - I_{Load} \tag{2}$$

$$I_{C\_lower} = -I_N - I_{Load} \tag{3}$$

In addition, the voltage variation of the two capacitors during the duration time of [PON] can be expressed by (4) and (5). From (4) and (5), the voltage difference between the upper and lower capacitors can be formulated as (6) if the upper and lower capacitors have the same capacitance.

$$dV_{DC\_upper} = \frac{1}{C}(I_P - I_{Load})T_1 \tag{4}$$

$$dV_{DC\_lower} = \frac{1}{C}(-I_N - I_{Load})T_1 \tag{5}$$

$$\begin{aligned} dV_{DC\_diff} &= d(V_{DC\_upper} - V_{DC\_lower}) \\ &= \frac{1}{C}(I_P + I_N)T_1 = -\frac{1}{C}I_O T_1 \end{aligned} \tag{6}$$

In (6), the voltage imbalance of the DC-link capacitors is affected by the current flowing through the phase of the O-state I_O. If I_O is positive, the difference between the upper and lower capacitor voltage increases. This means that

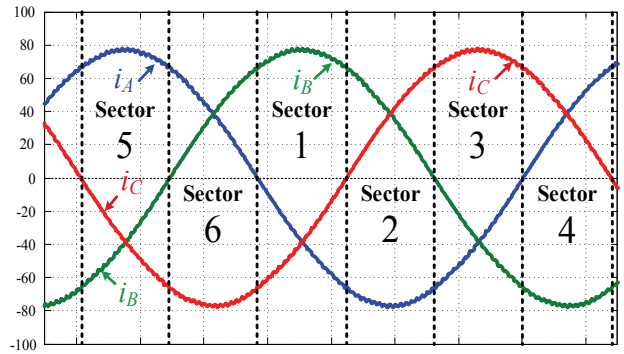

Fig. 5. State of the three-phase currents according to each sector.

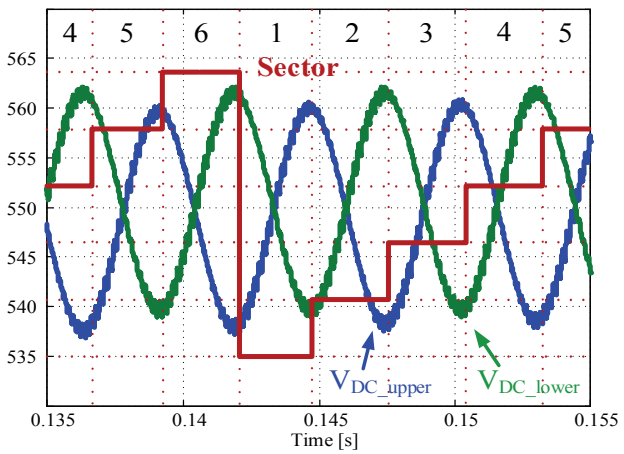

Fig. 6. DC-link voltages of the upper and lower capacitor in each sector of the MVS PWM.

V_{DC_upper} increases and V_{DC_lower} decreases. Under a negative I_O condition, the change of the two voltages occurs as opposed to the case of a positive I_O condition.

As mentioned above, the effect of a medium vector on the DC-link voltages depends on the condition of the current flowing through the O-state. In Fig. 5, the sectors are roughly classified based on the three-phase current waveform to confirm the state of the three-phase current in each sector. In sector 5 as an example, the two medium vectors [PON] and [PNO] are used as an effective vector. In [PON], the current through the phase of the O-state is a phase B current (I_B). In addition, the phase C current (I_C) is equal to I_O in [PNO]. Since both currents are negative in most of sector 5, I_O is also negative. In this case, the upper capacitor voltage V_{DC_upper} rises and the lower capacitor voltage V_{DC_lower} decreases for the duration time of the two medium vectors [PON] and [PNO]. The sector with this characteristic is defined as the P-type sector and the other P-type sectors are sectors 1 and 3.

Compared with the P-type sector including sector 5, the O-state current I_O is positive in sector 2, 4 and 6. Therefore, V_{DC_upper} decreases and V_{DC_lower} increases in these even sectors. These sectors are defined as N-type sectors. Since the reference voltage is rotated by the operation of the converter, the P-type and N-type sectors are altered continuously at an interval of 60°. As a result, the voltage of the upper and lower DC capacitors has third order ripples corresponding to the fundamental frequency (60Hz) and the two voltage ripples are in opposite phases as presented in Fig. 6. Furthermore, there is a voltage imbalance of the DC component. This is caused by the change of the output power and the inherent imbalance of the hardware. Although the DC component is less than the AC component mentioned above, the DC component should be controlled with the AC component since there is a possibility that it may be a bigger problem.

IV. DC-LINK VOLTAGE BALANCING METHOD USING THE FOURTH-PHASE

In general, balance control for the DC-link voltage of a three-level NPC converter utilizes a method of adjusting the switching time of the P-type and N-type small vectors. In addition, several papers have proposed a control method to balance the DC-link voltages in a three-level NPC topology [22]-[27]. However, MVS PWM does not employ small vector due to the common-mode voltage. Therefore, the general method utilizing the small vector cannot be applied to MVS PWM. To solve this problem, a method connecting the fourth-phase to the DC-link was proposed as described in Fig. 7 [12]-[14].

The additional fourth-phase is operated depending on the measured voltage difference between the upper and lower capacitor voltage. In addition, the switching operation of the fourth-phase is implemented independently of the other three phases. The operation principle of the fourth-phase is similar to that of the buck-boost DC/DC converter. For example, if the upper capacitor voltage is larger than the lower capacitor voltage, the fourth-phase outputs positive voltage and it makes the inductor current 'I_{FN}' flow from the upper capacitor to the lower capacitor. This means the energy stored at the upper capacitor is transferred to the lower capacitor by positive current like a boost mode. In the opposite case, a negative voltage is generated from the fourth-phase so that negative current flows. As a result, the voltage difference is reduced because V_{DC_upper} increases and V_{DC_lower} decreases.

In this paper, the dipolar modulation described in Fig. 8 is used to operate the fourth-phase [19]. The general switching method for a three-level NPC system is not suitable to operate the fourth-phase as a DC/DC converter due to the unipolar switching. As a solution used in a previous paper, bipolar modulation is used for the fourth-phase. However, this method carries the risk of a short or voltage breakdown in an IGBT when the switching state is changed. On the other hand, dipolar modulation can produce three switching states in a single period of PWM, and the O-state functions as a dead-time between the P-state and the N-state.

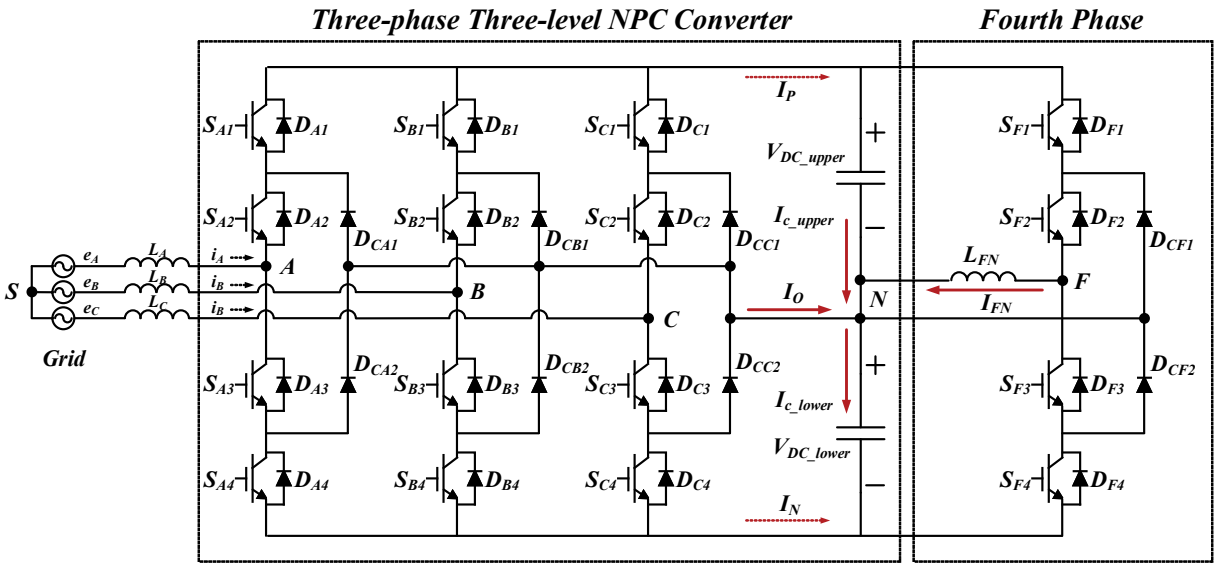

Fig. 7. Grid-connected three-phase three-level NPC converter with a fourth-phase for balancing the DC-link voltage.

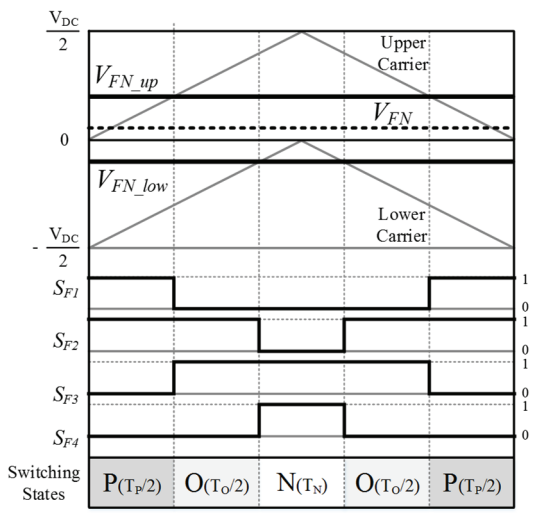

Fig. 8. Dipolar modulation for fourth-phase operation.

V. DC-LINK VOLTAGE BALANCING METHOD USING THE FOURTH-PHASE

As mentioned in previous sections, the DC and AC components of the DC-link voltage imbalance occur due to an use of MVS PWM. This voltage imbalance problem cannot be solved by MVS PWM itself since MVS PWM only uses a medium vector as the effective voltage vector. For this reason, a fourth-phase is required to solve the voltage imbalance problem. Although several papers have discussed the use of a fourth-phase to control voltage imbalance, there is a lack of explanation for the specific control methods and controllers. Thus, this paper proposes a proportional derivative (PD) controller for voltage balance control using a fourth-phase. The PD controller has a fast response to continuously variable errors. Therefore, the voltage imbalance of the AC component can be effectively suppressed [28], [29].

The proposed controller is designed from the modeling of the DC-link. In Fig. 7, the currents flowing in the DC-link circuit, including the fourth-phase, are described. Equation (7) can be acquired by applying the KCL law to the neutral point of the DC-link.

$$I_{c\_upper} - I_{c\_lower} = -(I_O + I_{FN}) \tag{7}$$

In general, the capacitor voltage (V_C) is decided by the current (I_C) flowing through the capacitor (C) as expressed in (8). In addition, (8) can be given as the Laplace transform in (9).

$$V_C = \frac{1}{C}\int I_C dt + V_C(0) \tag{8}$$

$$V_C = \frac{I_C}{sC} \tag{9}$$

Therefore, the current flowing through the upper and lower capacitors can be represented by the derivative of the voltage and the capacitance in (10).

$$C_{upper}\frac{dV_{DC\_upper}}{dt} - C_{lower}\frac{dV_{DC\_lower}}{dt} = -(I_O + I_{LN}) \tag{10}$$

Where, C_{upper} and C_{lower} are the capacitance of the upper and lower capacitors, respectively.

If the upper and lower capacitances are equal to each other as a capacitance C, (10) can be rearranged into (11) with a Laplace transform.

$$sC(V_{DC\_upper} - V_{DC\_lower}) = -(I_O + I_{FN}) \tag{11}$$

The voltage difference between the upper and lower capacitors can be given by:

$$V_{DC\_diff} = V_{DC\_upper} - V_{DC\_lower} = -\frac{I_O + I_{FN}}{sC} \tag{12}$$

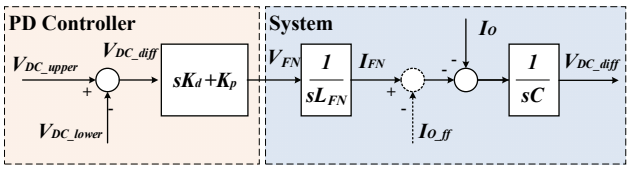

Fig. 9. DC-link voltage balancing control system with a PD controller.

In (12), the voltage imbalance is affected by the current I_O and can be controlled by the current I_{FN} flowing through the fourth-phase inductor L_{FN}. From (12), the control system for balancing the DC-link voltage can be described in Fig. 9. The difference between the measured upper and lower capacitor voltages is used as an error input of the PD controller. In addition, the PD controller outputs the voltage produced from the fourth-phase. The effect of the current I_O can be eliminated by the feedforward compensation using I_{O_ff}.

The transfer function of the PD controller of Fig. 9 is shown in (13).

$$G_{PD}(s) = sK_D + K_P \tag{13}$$

Where K_D is the gain of the derivative control, and K_P is the gain of the proportional controller. The open-loop system of Fig. 9 can be expressed as (14).

$$\begin{aligned} G(s) &= (sK_D + K_P)\frac{1}{sL_{FN}}\frac{1}{sC} \\ &= \frac{sK_D + K_P}{s^2 L_{FN} C} = \frac{K_D(s + K_P/K_D)}{sL_{FN}C} \end{aligned} \tag{14}$$

The transfer function of the closed-loop system is given by:

$$T(s) = \frac{G(s)}{1+G(s)} = \frac{\frac{K_D}{L_{FN}C}s + \frac{K_P}{L_{FN}C}}{s^2 + \frac{K_D}{L_{FN}C}s + \frac{K_P}{L_{FN}C}} \tag{15}$$

The closed loop system has the characteristic polynomial. If the desired characteristic polynomial is assumed as (16), the gains for the PD controller can be obtained by (17) and (18).

$$s^2 + 2\zeta\omega s + \omega^2 \tag{16}$$

$$K_P = L_{FN} C\omega^2 \tag{17}$$

$$K_D = 2\zeta L_{FN} C\omega \tag{18}$$

Where ω is the bandwidth of the controller and ξ is the damping ratio.

Additionally, the proposed controller contains feedforward compensation for the O-state current I_O. When the DC-link voltage balancing is controlled by using the fourth-phase control, the current I_O affects the performance of the controller as a disturbance since I_O is changed when the output power of the converter is fluctuated. Therefore, the response of the controller may be degraded in the transient state. The feedforward compensation can improve the response speed of the controller by reducing the effect of the current I_O.

TABLE III
ESTIMATED I_{O_FF} FOR FEEDFORWARD COMPENSATION ACCORDING TO THE SECTORS

Sectors	Switching states and corresponding current		Estimated current I_{O_ff}
	T_1	T_2	
1	[NPO] I_C	[OPN] I_A	$(I_C T_1 + I_A T_2)/T_s$
2	[NPO] I_C	[NOP] I_B	$(I_C T_1 + I_B T_2)/T_s$
3	[ONP] I_A	[NOP] I_B	$(I_A T_1 + I_B T_2)/T_s$
4	[ONP] I_A	[PNO] I_C	$(I_A T_1 + I_C T_2)/T_s$
5	[PON] I_B	[PNO] I_C	$(I_B T_1 + I_C T_2)/T_s$
6	[PON] I_B	[OPN] I_A	$(I_B T_1 + I_A T_2)/T_s$

In Fig. 9, I_{O_ff} is a feedforward compensation component and can be obtained by estimating the average value for a single period of PWM. During the zero vector [OOO], the current I_O means the sum of the three-phase current and it is generally zero. When two medium vectors are implemented, the current corresponding to the O-state in each of the two medium vectors flows as I_O. Therefore, the average O-state current can be obtained by using the switching time for the medium vector and the phase current corresponding to the O-state of the medium vector. For example, the O-state current is the phase B current in the medium vector [PON] in sector 5 as described in Fig. 5. In the same way, the phase C current is equal to the O-state current when the [PNO] is operated. Using the obtained current value and the switching time for the two medium vectors, the average O-state current in sector 5, as an example, for a single period (T_s) can be given as (18).

$$I_{O\_ff} = (I_B T_1 + I_B T_2)/T_s \tag{18}$$

The estimated I_{O_ff} in all of the sectors is shown in Table III.

The proposed PD controller, including the feedforward compensation and the overall system, is described in Fig. 10.

VI. EXPERIMENTAL RESULTS

The conditions and hardware setup for the experiment to verify the proposed method are presented in Fig. 11 and Table IV. The control board is based on a DSP TMS320c28346 and an FPGA cyclone IV EP4CE40 is used to control the three-level NPC PWM converter and the fourth-phase. The converter system controls the DC-link voltage at 700V with a constant DC voltage control. A resistor is parallel connected to the DC-link as a constant output load and it is capable of step

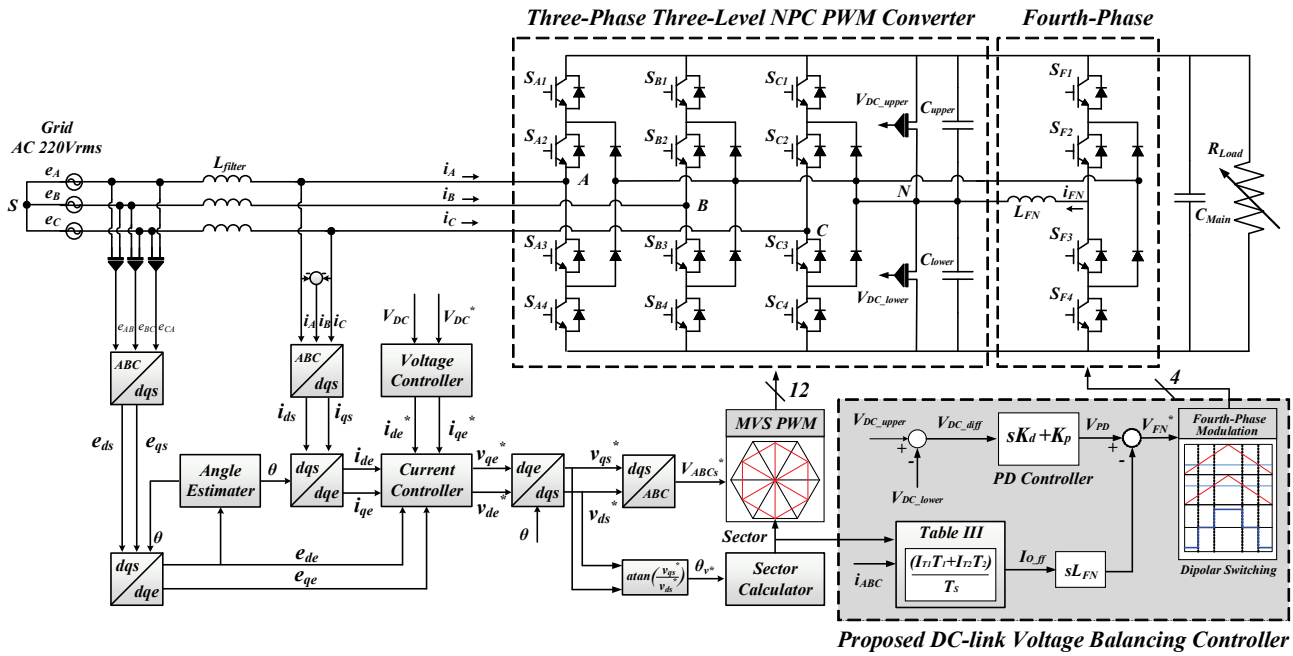

Fig. 10. Grid-connected three-level NPC PWM converter with MVS PWM and a fourth-phase with a DC-link voltage balancing controller.

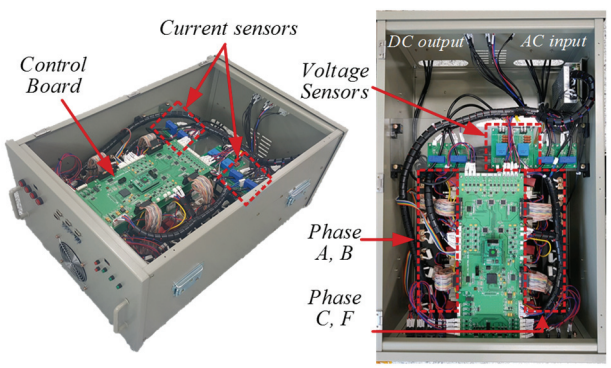

Fig. 11. Fourth-phase three-level NPC converter module prototype.

TABLE IV
CONDITIONS OF THE EXPERIMENT

Input grid voltage (V_{LL})	220 Vrms
Switching frequency	10 kHz
Harmonic filter	L-filter (5mH)
Fourth phase inductor (L_{FN})	5mH
Upper and Lower DC capacitor (C_{Upper}, C_{Lower})	660uF
Main DC capacitor (C_{Main})	1,000uF
Control method for three-phase converter	Constant DC voltage control
Reference DC voltage	700 V
DC load condition (R_{Load})	Resistor load of maximum 6kW under 700V

load changes. In order to stabilize the DC-link voltage, the main DC capacitor is connected to the converter DC output and it is placed between the converter and the resistor load.

In Fig. 12, common-mode voltage V_{SN} and phase voltage output V_{ABCN} waveforms of SVPWM and MVS PWM are presented. As shown in Fig. 12(a), SVPWM produces common-mode voltage such as $-V_{DC}/6$, 0, $V_{DC}/6$ and $V_{DC}/3$. On the other hand, MVS PWM generates almost zero common-mode voltage because MVS PWM only uses voltage vectors that cannot generate common-mode voltage. A little CMV ($V_{DC}/6$) is generated due to the dead-time but this voltage can be reduced by the compensation method proposed in [12].

Although MVS PWM can eliminate the common-mode voltage produced from a three-level NPC converter system, the performance of the input phase current is deteriorated since MVS PWM does not use the nearest three voltage vector from the reference voltage but two medium voltage vectors and a zero vector [OOO]. For this reason, MVS PWM generates a larger harmonic at the switching frequency when compared with SVPWM as shown in Fig. 13.

Fig. 14(a) shows experimental waveforms of the DC-link voltages and the fourth-phase current I_{FN} before and after applying the proposed balance controller. The experiment shown in Fig. 14 is conducted under a 3kW constant load condition. Before applying the controller, as presented in Fig. 14(b), the upper and lower DC voltage are separated up to about 5V and the ripple for each of the voltages is about 2V. After applying the fourth-phase and the proposed controller, the two DC voltages V_{DC_upper} and V_{DC_lower} are controlled to an average of 350V, which corresponds to half of the DC-link voltage. In addition, the voltage ripple of the two capacitors is reduced by 30% from 3.2V to 2.2V. As for the practical

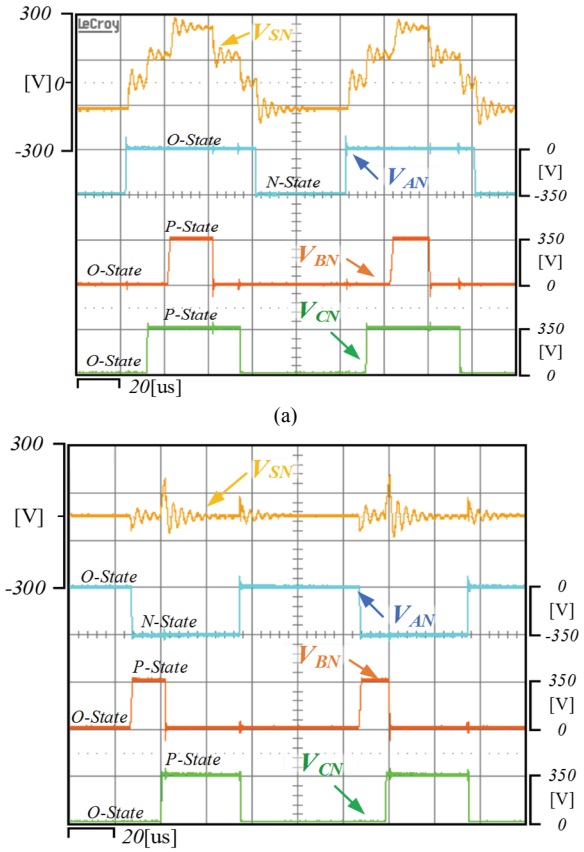

Fig. 12. Common-mode voltage and three-phase voltage output: (a) SVPWM; (b) MVS PWM.

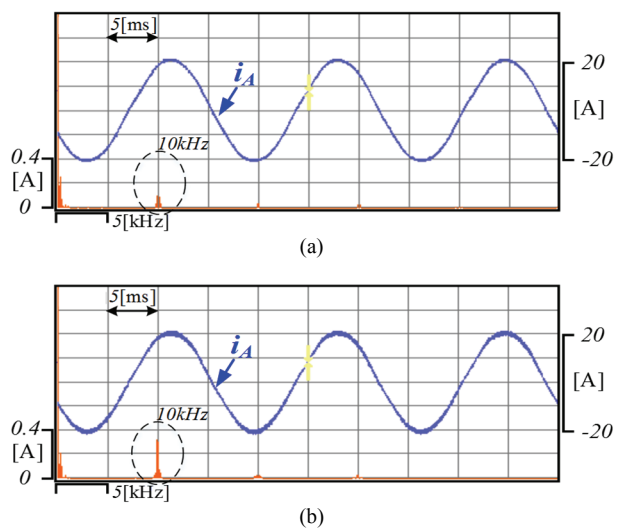

Fig. 13. Input phase current waveform and FFT analysis results under the load condition of 5kW: (a) SVPWM; (b) MVS PWM.

results of the experiments, the DC component of the voltage difference V_{DC_diff} can be reduced by adjusting the gain of the 'P' controller. However, this tends to increase the magnitude of the ripple of the two voltages. In addition, the voltage ripple can be reduced by adjusting the gain of the 'D' controller.

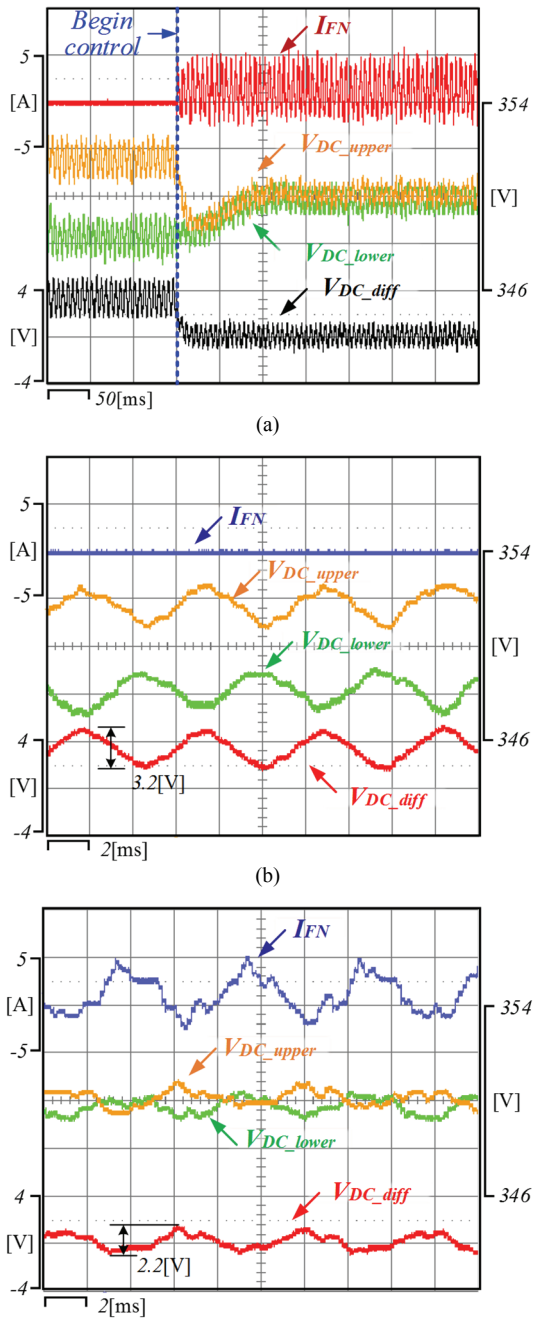

Fig. 14. Experimental results of DC-link voltage balancing: (a) Step control waveform before and after control; (b) Without the controller; (c) With the controller.

Fig. 15 shows control performance according to a step load change. The experiment was conducted under a step load change from 3kW to 5kW. If the controller is not applied, as shown in Fig. 15(a), the difference between V_{DC_upper} and V_{DC_lower} becomes larger due to the change of the load. Moreover, the ripple of the two voltages increases. On the other hand, after applying the proposed controller, as shown in Fig. 15(b), the average difference between the two voltages is kept close to zero. Although the voltage ripple increases

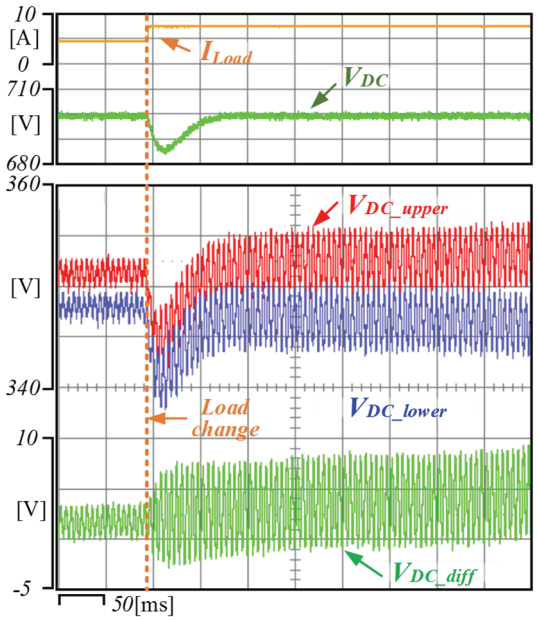

Fig. 15. Experimental results under a step load change: (a) Without the controller; (b) With the controller.

slightly, it is suppressed more than the result shown in Fig. 15(a).

VII. Conclusions

This paper proposed a DC-link balance controller with a fourth-phase for three-phase three-level NPC converters using MVS PWM. The proposed controller is based on the PD controller which has a fast response to variable errors. The effect of MVS PWM on the DC-link voltage was analyzed through an equivalent circuit of the DC-link. It was found that a DC and AC voltage imbalance occur. To solve the imbalance problem, the proposed PD controller was designed from an equivalent circuit of the DC-link and applied to the fourth-phase. Experimental results show that the average differe nce between the upper and lower capacitor voltage was controlled to almost zero and that the voltage ripple was suppressed by about 30%.

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