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Single-Phase Step-Up Five-Level Inverter with Phase-Shifted Pulse Width Modulation

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Abstract

A single-phase step-up five-level inverter topology with a new phase-shifted pulse width modulation (PS-PWM) strategy is proposed in this paper. When compared with conventional single-phase five-level inverter topologies, the proposed topology can realize multilevel inversion with a double step-up ratio, a reduced number of switching devices and self-balanced capacitor voltages. When compared with the conventional PS-PWM strategy, the new PS-PWM strategy can be implemented with one carrier reduced, which makes it much easier to implement in a digital signal processor (DSP) system. Experimental results have been presented to verify the effectiveness of the proposed inverter and the PS-PWM strategy.

Key words: Five-level, PS-PWM, Self-balance, Single-phase, Step-up

I. INTRODUCTION

Single-phase multilevel inverters have received increasing attention due to their interesting features such as low harmonic currents and low voltage stresses across switching devices. As the output voltage level increases, the output harmonic content of inverters decreases, which allows for the use of smaller and less expensive output filters. Single-phase five-level inverters are widely used single-phase multilevel topology. The single-phase five-level inverter was first proposed by cascading two H-bridge inverters (CHB) to produce a five-level waveform [1], [2]. However, eight switches and their corresponding drivers are necessary for the circuit. Moreover, two split dc sources are needed, which can result in voltage-imbalance issues that should be carefully studied [3]. A single-phase full-bridge five-level neutral-point potential clamped (NPC) inverter and an improved version of the inverter have been proposed in [4]. Both of the circuits have only one dc source, which reduces the cost when compared with CHB. An improved modulation strategy has been proposed to achieve voltage-balance control for the two split capacitor voltages in the single-phase active NPC (ANPC) [5]. In [6], a single-phase five-level inverter comprising an asymmetric flying-capacitor H-bridge with a novel PWM scheme was proposed. Although improved output waveforms, a small filter size and low total harmonics distortion (THD) can be achieved by the circuit in [6], a pre-charging problem increases the complexity of the modulation strategy due to the flying-capacitor. To reduce the number of switches, an alternative five-level inverter was proposed in [7] and further studied and improved in [8-10]. Only five switches are needed in these newly proposed inverters, which simplifies the corresponding drive circuits. However, there are four diodes in the circuit of each type of inverter, which is not helpful for improving efficiency.

Single-phase five-level inverter topologies employing a coupled-inductor technique were proposed in [11]-[13]. The drawback of these circuits is that the coupled inductors need to be carefully designed. In addition, the five-level ANPC with coupled inductors in [12] has many switches. A simplified single-phase multistring five-level inverter was proposed in [14], [15]. Although the circuit can have a smaller number of components and can achieve a high efficiency, the two dc link capacitors are not connected in series, which requires two front step-up dc/dc converters or separate input sources. This increases the cost of the whole two-stage dc/ac power conversion system. A five-level inverter consisting of only

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six switches was proposed to achieve five-level PWM operation without clamping diodes or flying capacitors [16]. However, four active switches endure full dc-bus voltage stress with a high frequency in this topology. Recently, an enhanced single-phase step-up five-level inverter was proposed in [17]. This inverter was based on the switched-diode-capacitor cell presented in [18]. When compared with conventional five-level inverters, the inverter in [17] can realize multilevel inversion with a high step-up output voltage and a simple structure, which is mostly attributed to the switched-diode-capacitor cell. However, additional power switches and diodes are necessary and the corresponding modulation strategy is complicated.

A new single-phase five-level inverter topology with a new PS-PWM strategy is proposed in this paper. A self-balanced function for the capacitor voltages and a two-time step-up function are integrated in the new topology with a reduced number of power components. Four switches operate at a high frequency with low voltage stresses, while the other two switches operate at the line frequency (50 Hz) with high voltage stresses. The proposed PS-PWM strategy could use fewer triangular carriers to achieve the same performance as the conventional PS-PWM strategy.

II. Proposed Inverter

Fig. 1 shows the proposed single-phase five-level inverter. As shown in this figure, there are six active switches, two diodes, and one dc source with two separate capacitors. The power switches S_1 and S_2 complement each other; as do the switches S_3 and S_4, and S_5 and S_6. Therefore, there are three independent active switches S_1, S_4 and S_6. In Fig. 1, U_{C1} and U_{C2} represent the two split capacitor voltages, U_{in} represents the input voltage and u_o represents the output voltage. In addition, the two split capacitors have the same capacitance.

$$C_1 = C_2 \tag{1}$$

To some extent, the two capacitor voltages U_{C1} and U_{C2} remain stable. However, they fluctuate frequently due to the charging and discharging of the capacitors. Therefore, Table I gives the charge and discharge states of the two capacitors C_1 and C_2. Due to the symmetry of the sine wave reference, the charging time of C_1 is the same as that of C_2, i.e., the conduction time of S_2 is the same as that of S_1.

For the proposed inverter, the two switches S_5 and S_6 are operated at the line frequency, while the other switches are operated at a high switching frequency. Based on the states of the switches, there are eight valid switching combinations that generate the required five output levels as shown in Table I. The corresponding operation stages of the five-level inverter are given in Fig. 2. For the convenience of the illustration, the switching function of the switches in Table I is defined as follows:

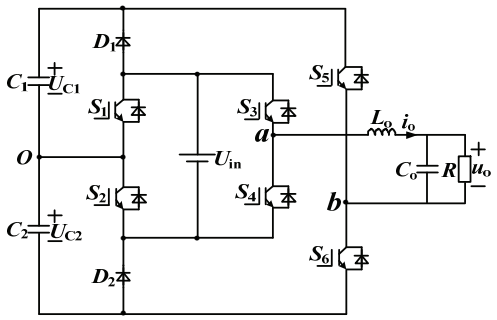


Fig. 1. Proposed single-phase step-up five-level inverter.

TABLE I
Switching Combinations

Stage	S_1	S_2	S_3	S_4	S_5	S_6	u_{ab}
I	0	1	1	0	0	1	$U_{C1}+U_{C2}$
II	0	1	0	1	0	1	U_{C2}
III	1	0	1	0	0	1	U_{in}
IV	1	0	0	1	0	1	0
V	0	1	1	0	1	0	0
VI	0	1	0	1	1	0	$-U_{in}$
VII	1	0	1	0	1	0	$-U_{C1}$
VIII	1	0	0	1	1	0	$-U_{C1}-U_{C2}$

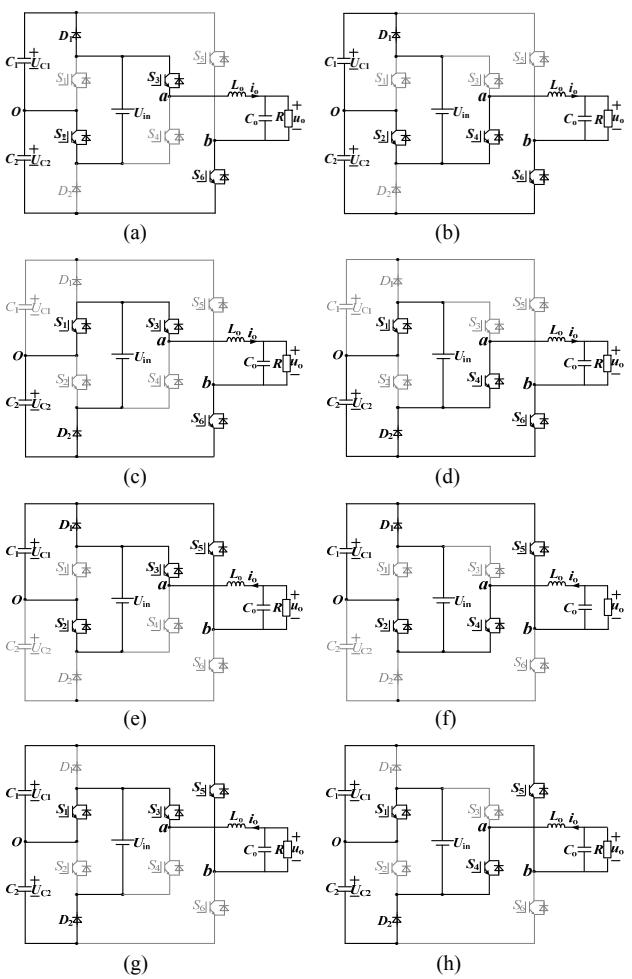


Fig. 2. Operating stages: (a) I; (b) II; (c) III; (d) IV; (e) V; (f) VI; (g) VII; (h) VIII.

$$S_i = \begin{cases} 1 & S_i \text{ is on} \\ 0 & S_i \text{ is off} \end{cases}, \quad i = 1, 2...6 \tag{2}$$

The eight operating stages of the proposed inverter are given in Fig. 2 and described in details as follows.

1) Maximum positive output level (U_{C1}+U_{C2}) (Stage I): in Stage I, the switches S_2, D_1, S_3 and S_6 are ON, and all of the other switches are off. The total voltage (U_{C1}+U_{C2}) is applied to the *LC* output filter, and the capacitor C_1 is charged by the input source U_{in}.
2) Half positive output level U_{in} or U_{C2} (Stages II and III): one switching combination shown in Stage II is such that the switches S_2, D_1, S_4 and S_6 are ON. The other switching combination is such that the switches S_1, D_2, S_3 and S_6 are ON. During Stage II, the voltage U_{C2} is applied to the *LC* output filter and the capacitor C_1 is charged by U_{in} simultaneously. During Stage III, U_{in} is applied to the *LC* filter and charges the capacitor C_2.
3) Zero output level (Stages IV and V): in Stage IV, the switches S_1, D_2, S_4 and S_6 are ON. In Stage V, the switches D_1, S_2, S_3 and S_5 are ON. During these two stages, zero voltage is applied to the *LC* output filter. The capacitor C_2 is charged by U_{in} during Stage IV and the capacitor C_1 is charged by U_{in} during Stage V.
4) Half negative output level U_{in} or -U_{C1} (Stages VI and VII): one switching combination shown in Stage VI is such that the switches D_1, S_2, S_4 and S_5 are ON. The other switching combination shown in Stage VII is such that the switches S_1, D_2, S_3 and S_5 are ON. During Stage VI, -U_{in} is applied to the *LC* output filter and the capacitor C_1 is charged by U_{in} simultaneously. During Stage VII, -U_{C1} is applied to the *LC* output filter and the capacitor C_2 is charged by U_{in} simultaneously.
5) Maximum negative output level -(U_{C1}+U_{C2}) (Stage VIII): in Stage VIII, the switches S_1, D_2, S_4 and S_5 are ON, and the total voltage -(U_{C1}+U_{C2}) is applied to the *LC* output filter. In addition, the capacitor C_2 is charged by the input source U_{in}.

The two split capacitor voltages are self-balanced by the input voltage source U_{in}, i.e.:

$$U_{C1} = U_{C2} = U_{in} \tag{3}$$

III. PS-PWM METHOD

For a multilevel inverter, the logic relationship among the drive signals of the switches, carrier signals and modulation signals should be achieved before selecting a certain modulation strategy. In the proposed inverter, with three pairs of complementary switches, it is only necessary to determine the logic relation among the drive signals of three switches, carrier signals and modulation signals. In this section, the eight switching combinations in Table I are rewritten in Table II with A, B and C to generate a five-level voltage waveform.

TABLE II
TRUTH TABLE

Stages	S_1	S_4	S_6	u_{ab}	A	B	C
I	0	0	1	U_{C1}+U_{C2}=2U_{in}	1	1	1
II	0	1	1	U_{C2}=U_{in}	1	1	0
III	1	0	1	U_{in}	1	0	1
IV	1	1	1	0	1	0	0
V	0	0	0	0	0	0	0
VI	0	1	0	-U_{in}	0	0	1
VII	1	0	0	-U_{C1}=-U_{in}	0	1	0
VIII	1	1	0	-U_{C1}-U_{C2}=-2U_{in}	0	1	1

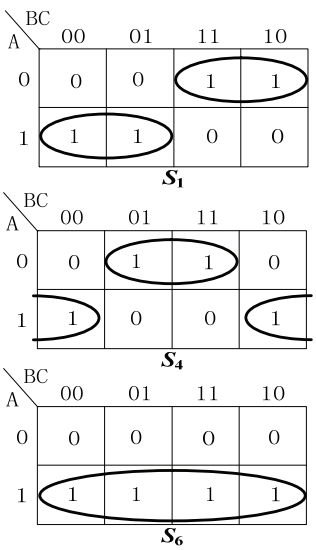


Fig. 3. Karnaugh maps for S_1, S_4 and S_6.

A, B and C represent the outputs of the three comparators, which are also given in Fig. 5.

To determine the relations among A, B and C and S_1, S_4 and S_6, three Karnaugh maps for the switches S_1, S_4 and S_6 are presented in Fig. 3. According to Fig. 3, it is not difficult to obtain the logic relations shown in (4). The next step is to select a modulation strategy for the inverter.

$$\begin{cases} S_1 = A\overline{B} + \overline{A}B = A \oplus B \\ S_4 = A\overline{C} + \overline{A}C = A \oplus C \\ S_6 = A \end{cases} \tag{4}$$

For a multilevel inverter, carrier-based phase disposition pulse width modulation (PD-PWM) is a common strategy. As shown in Fig. 4(a), the PD-PWM strategy is implemented by using four triangular carriers and one reference signal. Four carriers with the same frequency, amplitude and phase angle are disposed as the upper and lower four layers, labelled as $C_1(t)$, $C_2(t)$, $C_3(t)$ and $C_4(t)$, which are symmetrically distributed in the two-side of the horizontal axis, and compared with a sine modulation wave $m(t)$. However, it is difficult to produce so many triangular carriers with the phase disposition in a DSP control board. In addition, a lot of

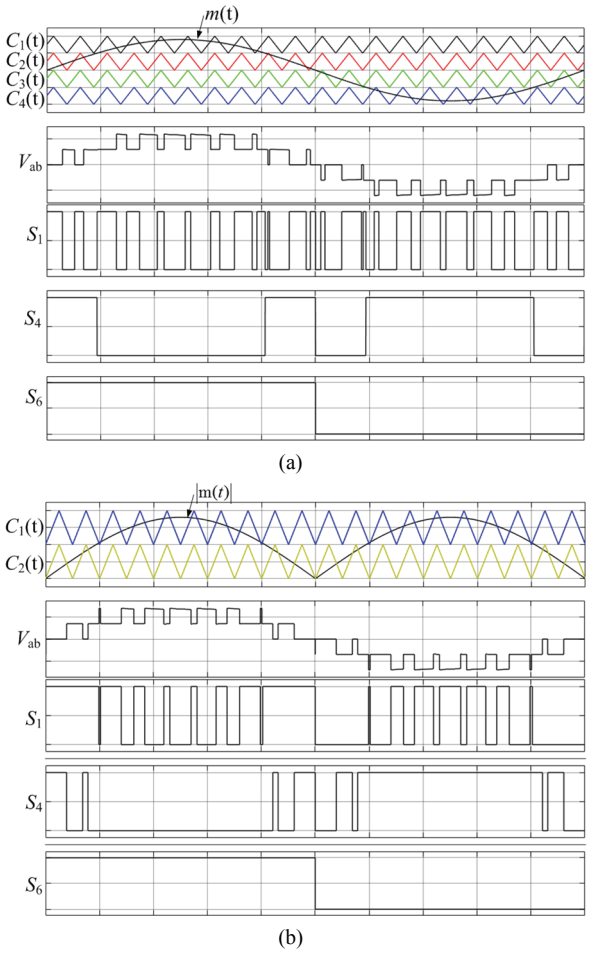


Fig. 4. Switching patterns of PD-PWM strategies: (a) Conventional PD-PWM; (b) Optimal PD-PWM.

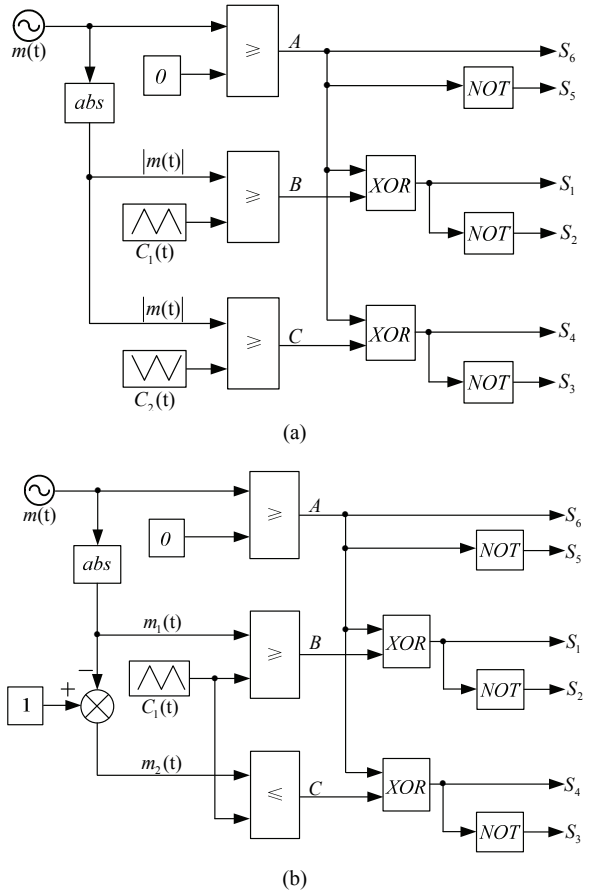


Fig. 5. Modulation logic diagram of PD-PWM strategies: (a) Conventional PS-PWM; (b) Proposed PS-PWM.

triangular carriers drain the computing resources of the DSP. Therefore, it is desirable to take a modulation strategy with a reduced number of triangular carriers that can achieve the same or much better output performance than the conventional PD-PWM strategy.

Referring to the modulation strategy in [17], [21], an optimal PD-PWM strategy with only two triangular carriers can be used to generate switching signals for the proposed inverter. The switching patterns of the inverter with the optimal PD-PWM strategy are presented in Fig. 4(b), where the two triangular carrier signals $C_1(t)$ and $C_2(t)$ have the same frequency, amplitude, and phase angle. The same output performance as the conventional PD-PWM can be achieved. However, it is still difficult to produce two triangular carriers with phase disposition in a DSP control board.

Another interesting strategy is phase-shifted pulse width modulation (PS-PWM) and its logic relation, shown in Fig. 5(a), is similar to that in the optimal PD-PWM. A small difference between them is that the two triangular carriers $C_1(t)$ and $C_2(t)$ in the PS-PWM strategy are phase-shifted 180 degrees instead of phase disposition. In Fig. 5(a), the reference sinewave $m(t)$ is used to compare with zero for zero-crossing detection and for providing the line frequency switching signals for S_5 and S_6. The absolute value of the sinewave $|m(t)|$ is used for comparison with the triangular carrier signals $C_1(t)$ and $C_2(t)$ to provide switching signals for the other four switches S_1-S_4.

Producing two phase-shifted triangular carriers is a lot easier than producing two carriers with phase disposition in a DSP control board system. The switching patterns of an inverter with the conventional PS-PWM strategy was given in Fig. 6. By comparing Fig. 5(a) and Fig. 6(a), it can be found that the equivalent switching frequency of the output voltage using the PS-PWM strategy is two times that using the PD-PWM strategy or the optimal PD-PWM strategy. As a result, the output harmonic component can be largely reduced and the output filter can be designed with a smaller size by using the PS-PWM strategy. That is why the PS-PWM strategy is widely used in power converters.

In this paper, a new PS-PWM strategy is proposed using only one triangular carrier $C_1(t)$ as shown in Fig. 5(b). In addition, its switching patterns are given in Fig. 6(b). Like the conventional PS-PWM strategy, the drive signals of S_1 and S_4 are phase-shifted 180 degrees. The same output performance as the conventional PS-PWM strategy can be achieved with

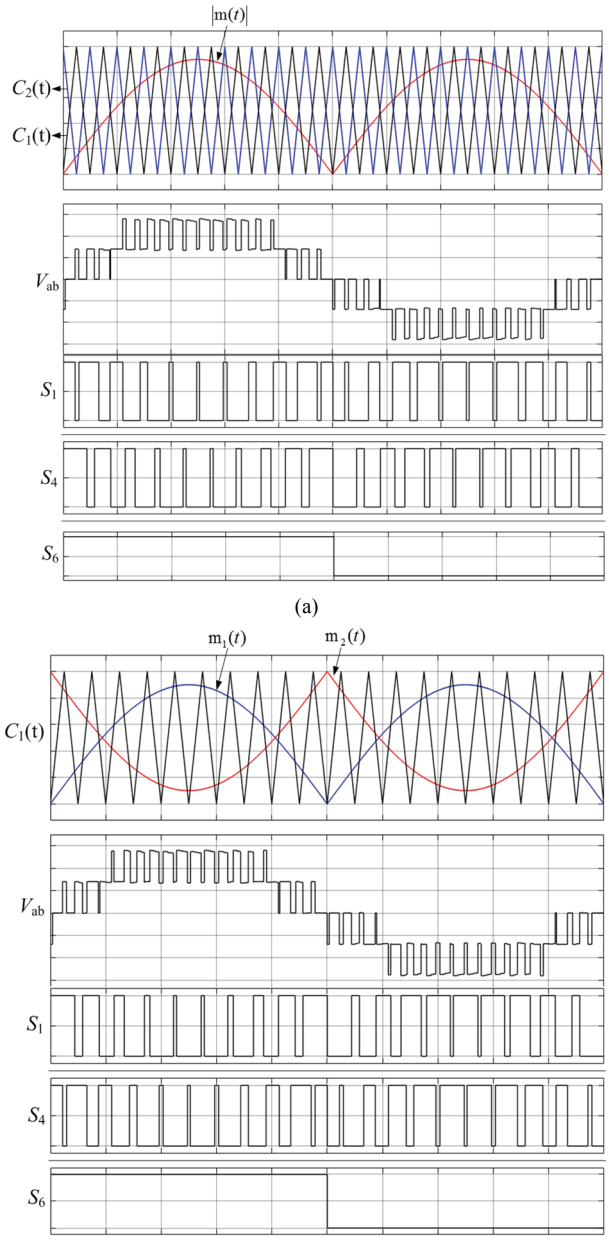


Fig. 6. Switching patterns of PS-PWM strategies: (a) Conventional PS-PWM; (b) Proposed PS-PWM.

one carrier reduced, which makes it a lot easier to implement in a DSP control board system. In the proposed PS-PWM strategy, the two reference waves $m_1(t)$ and $m_2(t)$ given in (5) are needed and it can be considered that $m_2(t)$ is achieved by rotating $m_1(t)$ 180 degrees. It is easy to produce $m_1(t)$ and $m_2(t)$ in a DSP control board.

$$\begin{cases} m_1(t) = |m(t)| \\ m_2(t) = 1 - |m(t)| \end{cases} \tag{5}$$

In the proposed PS-PWM modulation strategy, the triangular carrier $C_1(t)$ is used for comparison with $m_1(t)$ and $m_2(t)$ to generate the switching signals for S_1 and S_4. Unlike the conventional PS-PWM strategy, the comparing logic for obtaining C (i.e., the output of the third comparator in Fig. 5(b)) in the proposed PS-PWM strategy is contrary to that of the conventional PS-PWM strategy. The second triangular carrier $C_2(t)$ is not necessary in the proposed PS-PWM strategy. On the whole, the proposed PS-PWM strategy is easier to implement while guaranteeing the same inverter performance as the conventional PS-PWM strategy.

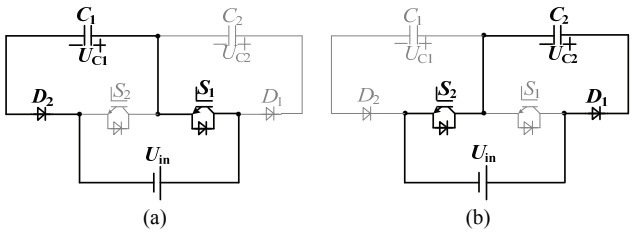


Fig. 7. Equivalent circuits of the switched-diode-capacitor cell: (a) S_1 is on, S_2 is off; (b) S_1 is off, S_2 is on.

IV. Performance Analysis

A. Integration of Self-Balanced and Step-Up Function

It is easy to show that the two capacitors C_1 and C_2 are charged and discharged, as reported in [18]-[20]. Equivalent circuits of the switched-diode-capacitor network are presented in Fig. 7. It can be seen that when the switch S_1 is on, the capacitor C_2 is charged by the input source U_{in} through the diode D_2. It can also be seen that when S_2 is on, the capacitor C_1 is charged by the input source U_{in} through the diode D_1. Considering the voltage drops of the diodes, C_1 is charged at U_{in}-U_{D1} and C_2 is charged at U_{in}-U_{D2}. In the proposed topology, the two diodes D_1 and D_2 have the same characteristics and they are the same kind of diode in the experiment. Thus, the difference between U_{D1} and U_{D2} is very small even when considering practical parasitic parameters. In addition, the difference between C_1 and C_2 only influences their voltage ripples but does not influence their average voltages. Therefore, there is no need to consider the neutral-point potential issue in this five-level inverter. Since there are idle states of the two capacitors, enough capacitance is provided to ensure stable capacitor voltages.

Considering that the reference wave $m(t)$ is equal to $m\sin(2\pi f_m t)$, the output voltage u_o (RMS value) can be expressed as follows:

$$u_o = (U_{C1} + U_{C2}) * m\sin(2\pi f_m t)/\sqrt{2} = \sqrt{2} m U_{in}\sin(2\pi f_m t) \tag{6}$$

Where f_m is the line frequency and m is the modulation index that is expressed by:

$$m = \frac{A_m}{2A_c} \tag{7}$$

Therefore, the step-up ratio of the inverter can be defined as:

$$\frac{u_o}{U_{in}} = \sqrt{2} m\sin(2\pi f_m t) \tag{8}$$

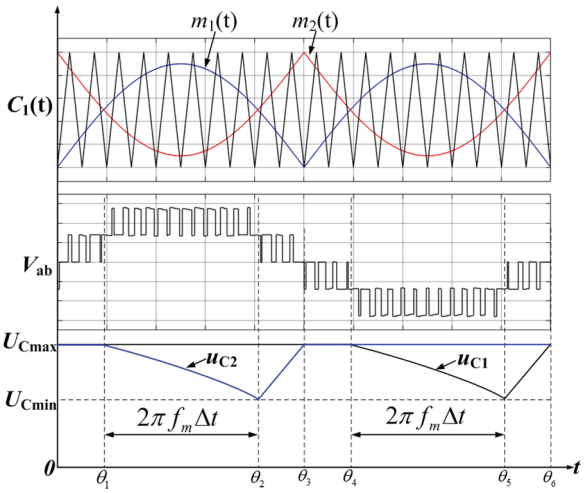


Fig. 8. Capacitor voltages during one fundamental period.

It can be concluded from (8) that the proposed inverter has step-up capacity and that the step-up ratio is two times that of the conventional single-phase two-level inverter.

B. Loss Analysis

According to the theoretical analysis above, the two switches S_5 and S_6 experience voltage stresses equaling to $2U_{in}$ while the other four switches S_1-S_4 experience voltage stresses equal to U_{in}. In addition, a great advantage of the proposed topology is a self-balancing function for capacitor voltages. As shown in Table II and Fig. 2, the two capacitors C_1 and C_2 are charged and discharged for the same period during a whole fundamental switching cycle. As a result, the two capacitor voltages are self-balanced. Meanwhile, a two-time step-up ratio is achieved.

When the modulation index m is less than or equal to 1/2, the inverter outputs three voltage levels while the two capacitors C_1 and C_2 are kept idle under this condition. When m is over 1/2, the capacitor voltage waveform during one fundamental period is presented in Fig. 8, in which there is:

$$\begin{aligned}
\theta_1 &= \sin^{-1}(A_c / A_m) \\
\theta_2 &= \pi - \sin^{-1}(A_c / A_m) \\
\theta_3 &= \pi \\
\theta_4 &= \pi + \sin^{-1}(A_c / A_m) \\
\theta_5 &= 2\pi - \sin^{-1}(A_c / A_m) \\
\theta_6 &= 2\pi
\end{aligned} \tag{9}$$

Thus, the time period Δt in which the voltage of C_1 or C_2 decreases can be expressed as follows:

$$2\pi f_m \Delta t = \theta_2 - \theta_1 \tag{10}$$

According to (7), (9) and (10), Δt can be obtained by:

$$\Delta t = \frac{1}{2f_m} - \frac{\sin^{-1}(1/(2m))}{\pi f_m} \tag{11}$$

Therefore, the voltage across C_1 or C_2 can be obtained by:

$$u_c = U_{C\max}\, e^{-\frac{2t}{RC}}, 0 < t < \Delta t \tag{12}$$

Where R and C are the output load and the capacitance of C_1 and C_2. It can be concluded from Fig. 2 that the capacitor C_1 is charged when S_2 and D_1 are turned on, and that the capacitor C_2 is charged when S_1 and D_2 are turned on. For simplicity, the diodes D_1 and D_2 are assumed to have a voltage drop of U_D. By ignoring the on-state resistance of the power switches and parasitic resistors in the circuit, the maximum capacitor voltage across C_1 and C_2 can be calculated as follows:

$$U_{C\max} = U_{in} - U_D \tag{13}$$

Therefore, as shown in Fig. 9, the capacitor voltages of C_1 and C_2 can be calculated by:

$$u_c = (U_{in} - U_D)\, e^{-\frac{2t}{RC}}, 0 < t < \Delta t \tag{14}$$

In addition, the voltage ripple of C_1 or C_2 can be estimated based on (11) and (14).

$$\Delta u_c = U_{C\max} - U_{C\min} = (U_{in} - U_D)(1 - e^{\frac{2\sin^{-1}(1/(2m))}{\pi f_m RC} - \frac{1}{f_m RC}}) \tag{15}$$

It can be seen from (15) that the voltage variation of the capacitor is related to the fundamental frequency f_m, modulation index m, output load R and capacitance C.

For switched-capacitor inverters, there are three types of power losses, including switching losses, conduction losses and capacitor distribution losses. In capacitor charging or discharging cycles, capacitor distribution losses are produced due to the voltage difference between the capacitors. Reference [22] indicates that the distribution losses are directly proportional to the capacitance and the capacitor voltage ripple. Thus, the capacitor distribution losses can be estimated by:

$$P_{dis} = f_s * \frac{1}{2} C (\frac{\Delta u_c}{2})^2 * 2 = \frac{1}{4} f_s C \Delta u_c{}^2 \tag{16}$$

Where f_s is the switching frequency.

The conduction loss is caused by the parasitic parameters, including the on-state resistances of the switches and the forward voltage drops of the diodes. For the main power circuit with a load R, there are two different conduction paths. Fig. 9 shows the switching states according to their relative position between the modulation signal and the carrier signal during one switching period T_s. Since T_s is much shorter than the fundamental period, the modulation signal can be deemed as a straight horizontal line during T_s. In this way, the on-state ratio k_1 in the operating states of Fig. 2(b)-(g), and the on-state ratio k_2 in the operating states of Fig. 2(a) and Fig. 2(h), can be obtained.

$$\frac{2mA_c \sin\theta}{A_c - 0} = \frac{k_1 T_s}{T_s} \Rightarrow k_1 = 2m\sin\theta \,(0<\theta<\theta_1, \theta_2<\theta<\theta_4, \theta_5<\theta<\theta_6) \tag{17}$$

$$\frac{2mA_c \sin\theta - A_c}{2A_c - A_c} = \frac{k_2 T_s}{T_s} \Rightarrow k_2 = 2m\sin\theta - 1 \,(\theta_1<\theta<\theta_2, \theta_4<\theta<\theta_5) \tag{18}$$

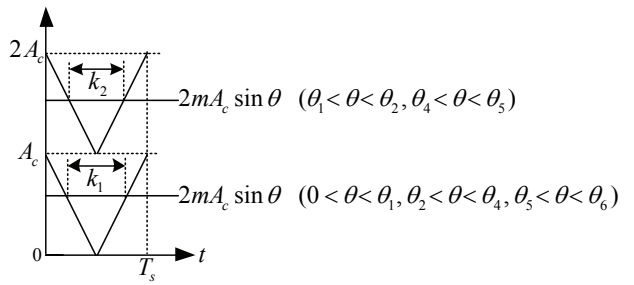


Fig. 9. Switching states according to the relative position between the modulation signal and the carrier signal during T_s.

For the operating states of Fig. 2(b), (c), (f) and (g), three switches are conducted with the conduction loss:

$$P_{con\_1}=\frac{1}{\pi}\left(\int_0^{\theta_1}d\theta+\int_{\theta_2}^{\theta_4}d\theta+\int_{\theta_5}^{\theta_6}d\theta\right)*\left(\frac{U_{in}-u_{ab}}{3r_{on}+R}\right)^2*3r_{on}*k_1 \quad (19)$$

For the operating states of Fig. 2(a) and Fig. 2(h), two switches and one diode are conducted, and the conduction loss can be calculated by:

$$P_{con\_2}=\frac{1}{\pi}\left(\int_{\theta_1}^{\theta_2}d\theta+\int_{\theta_4}^{\theta_5}d\theta\right)*\left[\left(\frac{2U_{in}-u_{ab}}{2r_{on}+R}\right)^2*2r_{on}+\frac{2U_{in}-u_{ab}}{2r_{on}+R}U_D\right]*k_2 \quad (20)$$

According to (17)-(20), the total conduction losses of the proposed inverter can be calculated by:

$$\begin{aligned}P_{con}&=P_{con\_1}+P_{con\_2}=\frac{1}{\pi}\left[\left(\frac{U_{in}-u_{ab}}{3r_{on}+R}\right)^2*24mr_{on}*\left(1-\sqrt{1-\frac{1}{4m^2}}\right)+\right.\\&\left.\left[4m\sqrt{1-\frac{1}{4m^2}}-\pi+2\sin^{-1}\left(\frac{1}{2m}\right)\right]*\left[\left(\frac{2U_{in}-u_{ab}}{2r_{on}+R}\right)^2*4r_{on}+\frac{2U_{in}-u_{ab}}{2r_{on}+R}*U_D\right]\right.\end{aligned} \quad (21)$$

The switching loss can be estimated from the charging and discharging processes of the parasitic capacitance between the drain terminal and the source terminal. Due to the phase-shift modulation, the equivalent switching frequency is doubled. Thus, the switching loss can be estimated by:

$$P_{sw}=2f_s*C_{ds}V_b^2 \quad (22)$$

Where C_{ds} and V_b are the parasitic capacitance and the maximum block voltage of each switch. The block voltages of S_1-S_4 are all equal to U_{in}, and the block voltages of S_5 and S_6 are equal to $2U_{in}$. Therefore, the total switching loss of the proposed inverter can be calculated by:

$$P_{sw}=2[f_s*C_{ds1}*4*U_{in}^2+f_m*C_{ds2}*2*(2U_{in})^2]=(8f_sC_{ds1}+16f_mC_{ds2})U_{in}^2 \quad (23)$$

Where C_{ds1} is the parasitic capacitance of S_1-S_4 and C_{ds2} denotes the parasitic capacitance of S_5-S_6. Finally, the total power losses of the proposed inverter can be calculated by:

$$P_{total}=P_{dis}+P_{con}+P_{sw} \quad (24)$$

C. Comparative Analysis

As previously mentioned, many single-phase five-level inverter topologies have been proposed. In this section, Table III summarizes comparisons between popular five-level inverters and the proposed inverter. In Table III, *S*, *D*, *C* and *L* represent the quantities of the switches, diodes, capacitors, and inductors used in the topologies. It can be observed that only five active switches are needed and that four diodes are added for the inverters reported in [7]-[10], which may increase the conduction losses of the inverters. The topology in [14], [15] has the lowest number of power components. However, two split dc sources are necessary, which greatly limits its application. A new hybrid five-level inverter was developed in [16] without clamped diodes or capacitors. The topology is simple with only six power switches. When compared with the hybrid five-level inverter, two more diodes are needed in the proposed inverter. However, under the same output voltage conditions, only two power switches in the proposed inverter bear a high voltage stress while four power switches in the inverter of [16] bear a high voltage stress. Moreover, only U_{C2} in the topology of [16] helps contribute to achieving the two voltage levels $+0.5U_{in}$ and $-0.5U_{in}$, while U_{C1} remains idle expect for contributing to achieving the two voltage levels U_{in} and $-U_{in}$ together with U_{C2}. This is the basic reason for an imbalanced potential issue, and a voltage-balance control strategy is necessary. However, this issue does not exist in the proposed five-level inverter because both U_{C1} and U_{C2} in the proposed topology help in achieving the two voltage levels $+0.5U_{in}$ and $-0.5U_{in}$. The two capacitor voltages are self-balanced during the modulation process. Therefore, there is no need to consider voltage-balance control strategies for the proposed topology.

All of these topologies, except the topology in [17] and the proposed topology in this paper, have a common neutral-point potential imbalance issue. The modulation strategies of these topologies should accurately balance the charging time for each of the capacitors for realizing the voltage-balance goal. However, this makes the modulation strategies more complicated. On the other hand, neutral-point potential imbalance is not an issue for the topology in [17] or the proposed topology due to the self-balanced function of the switched-diode-capacitor cell. The integration of the front step-up circuit and the back inversion circuit in [17] is a good advantage. However, it results in a complicated modulation scheme since the step-up function and inversion function should be considered simultaneously. Moreover, the proposed inverter in this paper has one less inductor and one less diode when compared with the topology in [17]. The proposed PS-PWM strategy makes it much easier to implement in an actual control system. Hence, the proposed topology is simpler and easier to implement.

On the whole, the double function of dc-dc step-up conversion with a two-time ratio and dc-ac inversion with a simple modulation strategy is realized in the proposed five-level inverter. On the one hand, one dc source with a reduced number of power switches and small voltage stresses are achieved. On the other hand, a new PS-PWM strategy with one carrier is proposed, and it is easy to implement in

TABLE III
COMPARISON ANALYSIS

Topology	S	D	C	L	Source	Step-up	Self-balanced	Modulation	Phase-Shifted
CHB [1, 2]	8	0	0	0	2	No	No	Simple	Yes
NPC [4]	6	2	2	0	1	No	No	Simple	No
ANPC [5]	8	0	3	0	1	No	No	Complicated	No
FC [6]	6	0	3	0	1	No	No	Simple	No
[7-10]	5	4	2	0	1	No	No	Simple	Yes
[14,15]	6	0	0	0	2	No	No	Simple	No
[16]	6	0	2	0	1	No	No	Simple	No
[17]	6	3	2	1	1	Yes	Yes	Complicated	No
Proposed inverter	6	2	2	0	1	Yes	Yes	Very Simple	Yes

DSP control board systems. All of these merits make it superior to existing five-level inverters.

D. Closed-Loop Control

The closed-loop implementation of the inverter is based on a proportional resonant (PR) controller with a resonant peak at the fundamental frequency 50Hz. An overall block diagram of the control scheme is presented in Fig. 10, and the PR controller structure is given as:

$$G(\mathrm{s}) = k_p + \frac{2k_r\omega_c s}{s^2 + 2\omega_c s + \omega_o{}^2} \tag{25}$$

Where k_p is the proportional gain, k_r is the resonant gain, ω_c is the cut-off frequency, and ω_o is the fundamental radian frequency. The resonant gain of the PR controller will only integrate frequencies very close to the fundamental frequency and will not introduce stationary error or phase shift [23], [24]. Using the PR controller, reference tracking performance can be enhanced and the known drawback of a PI controller that the steady-state errors in the single-phase system can be alleviated.

According to the bilinear transformation (9) in [25], the expression (8) could be discretized as (10).

$$s = \frac{2}{T}\frac{1-z^{-1}}{1+z^{-1}} \tag{26}$$

$$G(z) = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{a_0 + a_1 z^{-1} + a_2 z^{-2}} \tag{27}$$

Where 1/T means the control frequency of the PR controller and a_0, a_1, a_2, b_0, b_1 and b_2 are:

$$\begin{cases} a_0 = 1 \\ a_1 = \dfrac{2\omega_0{}^2T^2 - 8}{\omega_0{}^2T^2 + 4\omega_c T + 4} \\ a_2 = \dfrac{\omega_0{}^2T^2 - 4\omega_c T + 4}{\omega_0{}^2T^2 + 4\omega_c T + 4} \\ b_0 = \dfrac{k_p(\omega_0{}^2T^2 + 4\omega_c T + 4) + 4k_r\omega_c T}{\omega_0{}^2T^2 + 4\omega_c T + 4} \\ b_1 = k_p a_1 \\ b_2 = \dfrac{k_p(\omega_0{}^2T^2 - 4\omega_c T + 4) - 4k_r\omega_c T}{\omega_0{}^2T^2 + 4\omega_c T + 4} \end{cases} \tag{28}$$

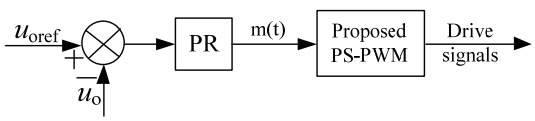


Fig. 10. Overall block diagram of the control scheme.

Therefore, a difference equation is obtained as follows:

$$u(k) = -\frac{a_1}{a_0}u(k-1) - \frac{a_2}{a_0}u(k-2) + \frac{b_0}{a_0}e(k) + \frac{b_1}{a_0}e(k-1) + \frac{b_2}{a_0}e(k-2) \tag{29}$$

In expression (29), $u(k)$, $u(k\text{-}1)$ and $u(k\text{-}2)$ represent the output voltage signals at the moments k, k-1 and k-2. Meanwhile, $e(k)$, $e(k\text{-}1)$ and $e(k\text{-}2)$ represent the corresponding error signals at the moments k, k-1 and k-2, respectively. The expression (29) can then be programmed into the DSP control board system to realize the PR control for stabilizing the output voltage of the proposed inverter.

V. EXPERIMENTAL VERIFICATION

To verify the correctness of the proposed topology and modulation method, an experimental prototype with a 150W output power, as shown in Fig. 11, has been built according to the parameters presented at Table IV. The controller is implemented based on a digital signal processor TMS320F28335.

It should be noted that a three-phase LC filter board and a three-phase voltage-current sensor board are presented in the prototype picture. However, a single-phase LC filter and a single voltage sensor are used in the actual prototype. In the PR controller, k_p is 0.0001, k_r is 1.0, w_c is 5rad/s, and w_o is 314.15. Referring to [26], the inductor L_o is calculated as:

$$L_o = \frac{U_{in}}{4 * f_o * (\frac{\sqrt{2}P_o}{u_o} * \eta)} \tag{30}$$

In (30), f_o means the equivalent switching frequency of the output voltage u_{ab}, P_o means the output power, and η means current ripple percentage. In the experiment, η is selected as 20%. With a switching frequency of 10 kHz, the equivalent switching frequency f_o of the output voltage u_{ab} should be 20 kHz due to the PS-PWM strategy. According to the

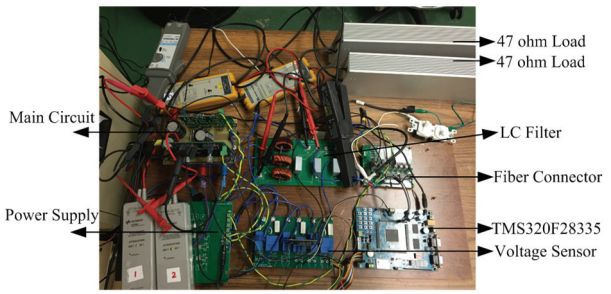


Fig. 11. Experimental prototype.

TABLE IV
EXPERIMENTAL PARAMETERS

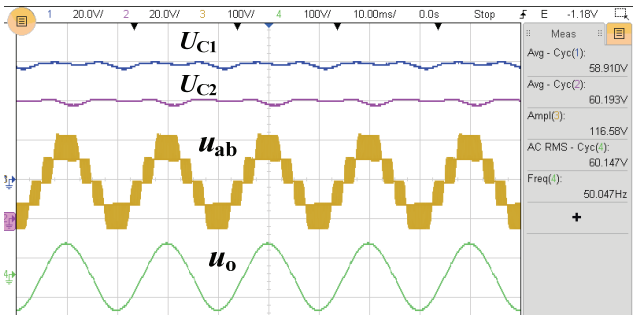
Components	Rated Values
Input voltage U_{in}	60V
Output voltage u_o	60V
Switching frequency f_s	10kHz
Line frequency f_m	50Hz
Capacitors C_1, C_2	470uF
Switches S_1-S_4	IRFP250
Switches S_5, S_6	IRFP450
Diodes D_1, D_2	FFB20UP20STM
Inductor L_o	1.0mH
Output capacitor C_o	6.3uF
Driver	A3120

experimental parameters and (30), the inductor L_o is 1.06mH. In the prototype, the inductor is selected as 1.0mH. On the other hand, the cut-off frequency f_{cut} of the output LC filter is usually regarded as ten percent of the switching frequency of the output voltage V_{ab}, i.e., 2kHz.

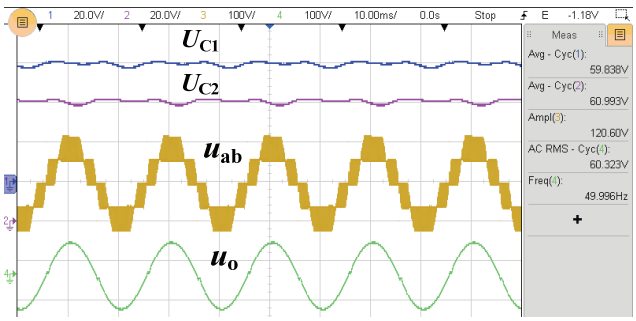
$$f_{cut} = \frac{1}{2\pi\sqrt{L_o C_o}} = 2.0kHz \tag{31}$$

According to (31), the output capacitor C_o can be calculated as 6.3uF. Therefore, the inductance and capacitance of the LC filter are 1.0mH and 6.3uF.

Comparison results of the conventional PS-PWM strategy and the proposed PS-PWM strategy are presented, including the key voltage waveforms in Fig. 12, the drive signals of S_1, S_4 and S_6 in Fig. 13, the terminal voltage waveforms of the switches S_1 and S_4, and the output voltage in Fig. 14. It can be seen from Fig. 12 that the output voltage u_{ab} presents a five-level shape and that the output voltage u_o presents a pure sine waveform. In addition, the two capacitor voltages are both nearly 60V, which is equal to the input voltage 60V. This verifies the correctness of the step-up capability and self-balance function. Low frequency capacitor voltage ripples are inevitable due to the charging and discharging of the capacitors. The drive signals of the switches in Fig. 13 show that the switches S_1 and S_4 have a 180 degrees difference in phase, which verifies the correctness of the proposed PS-PWM strategy. In Fig. 14, the output voltage is composed of a 20 kHz PWM voltage signal, which is two

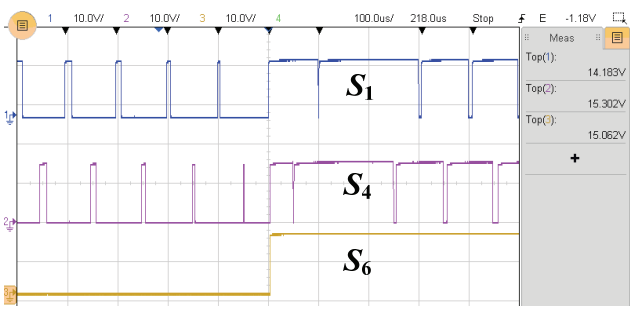


(a)

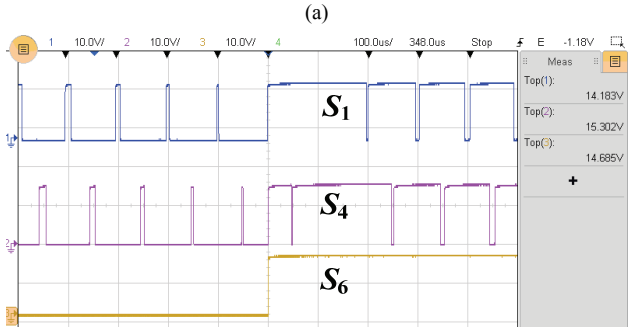


(b)

Fig. 12. Key voltage waveforms: (a) Conventional PS-PWM; (b) Proposed PS-PWM.



(a)

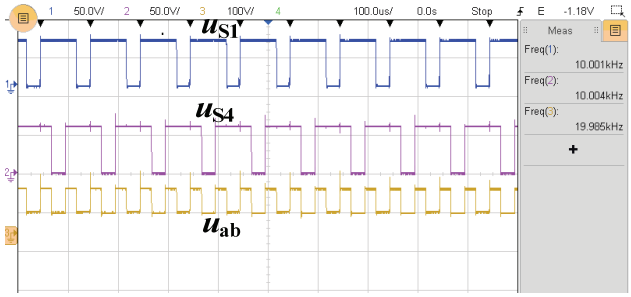


(b)

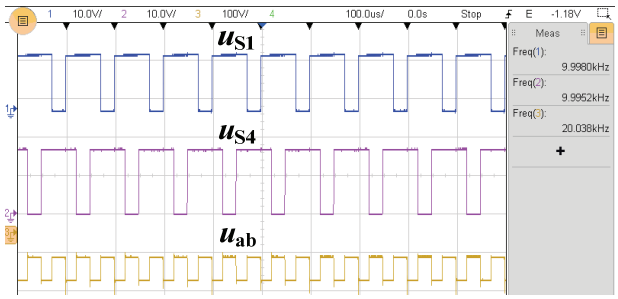
Fig. 13. Drive signals: (a) Conventional PS-PWM; (b) Proposed PS-PWM.

times of the switching frequency of S_1 and S_4. All of the comparison results in Figs. 12-14 verify the proposed PS-PWM strategy.

By comparing experimental results under the two different PS-PWM modulation strategies, it can be concluded that the proposed PS-PWM strategy has output performance equivalent to that of the conventional PS-PWM strategy. Thus, it can be

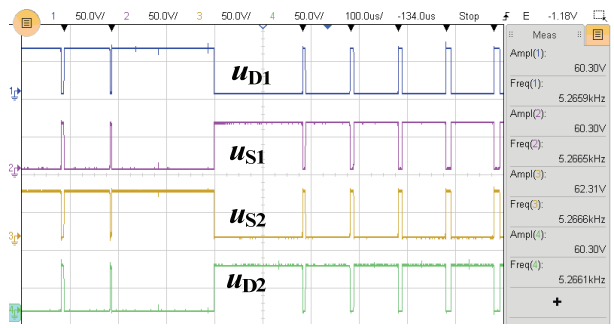


(a)

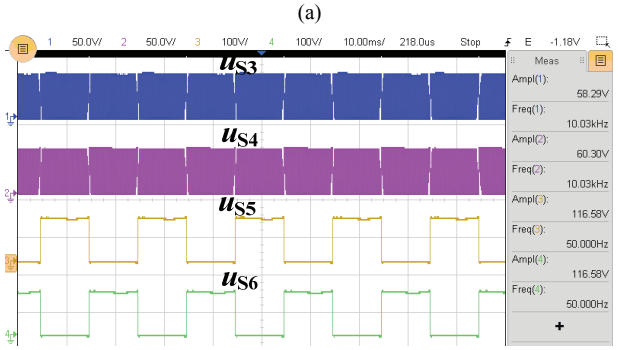


(b)

Fig. 14. Terminal voltage waveforms of S_1, S_4, and the output voltage: (a) Conventional PS-PWM; (b) Proposed PS-PWM.



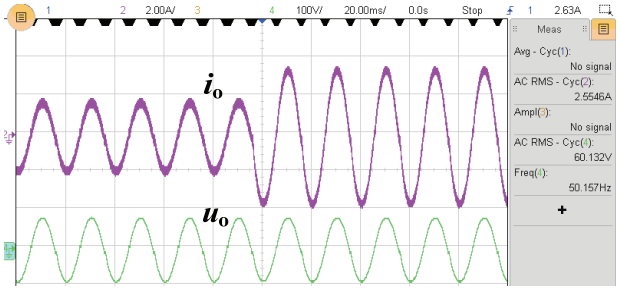
(a)



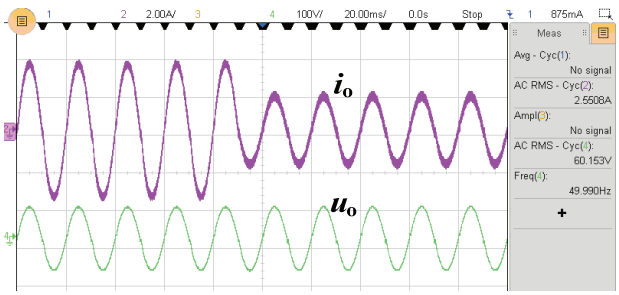
(b)

Fig. 15. Voltage waveforms of switches and diodes under the proposed modulation strategy: (a) D_1, S_1, S_2, D_2; (b) S_3, S_4, S_5, S_6.

claimed that the proposed PS-PWM strategy is equivalent to the conventional PS-PWM strategy in terms of inverter output performance. Since one triangular carrier is reduced, the proposed PS-PWM strategy is better than the conventional PS-PWM strategy in actual implementation. In fact, the proposed PS-PWM strategy can be used or extended to other



(a)



(b)

Fig. 16. Dynamic results under a load step.

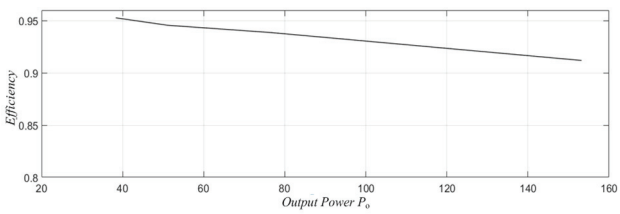


Fig. 17. Conversion efficiency curve.

power converter systems, such as a multi-phase dc/dc converter systems, cascaded multilevel converters, and modular multilevel converters. With the proposed PS-PWM strategy, half carriers can be saved and it becomes a lot easier to implement in a DSP.

Apart from the analysis mentioned above, it can be seen from Fig. 15 that all of the power components besides S_5 and S_6 endure half of the peak value of the output voltage. Although S_5 and S_6 endure the output peak voltage, the switching frequency for each of the switches is equal to the line frequency, which does not cause high switching losses. Moreover, the dynamic results of the inverter under a load step from 47 ohm to 23.5 ohm or vice versa are also given in Fig. 16. It can be seen that the output voltage is kept stable under the load step, and that the output current i_o increases by two times or half of its original value during a very short time, which indicates a very good dynamic response of the inverter.

Finally, the conversion efficiency of the inverter is presented in Fig. 17. The conversion efficiency of the inverter is over 95.27% at a light load and 91.19% at a full load (i.e., 23.5 ohm for the 150W power rating). As shown in Fig. 12, the voltage ripple Δu_c of C_1 or C_2 is around 3.0V. The parasitic capacitance C_{ds1} of the switches S_1-S_4 (IRFP250) is 530pf, and the parasitic capacitance C_{ds2} of the switches S_5-S_6

(IRFP450) is 380pf. In addition, the conduction resistance of S_1-S_4 (IRFP250) is 0.085ohm, and the conduction resistance of S_5-S_6 (IRFP450) is 0.4ohm. The equivalent series resistance of C_1 or C_2 is 0.1ohm. Based on the parameters and the formulas (16), (21) and (23), the capacitor distribution loss, conduction loss and switching loss of the proposed inverter with a full power load are calculated as 8.58W, 4.26W and 0.16W. It can be found that the capacitor distribution loss dominates the total power loss, while the switching loss is the lowest. The conversion efficiency of the proposed inverter with a full load is 91.33%, which basically matches its tested value of 91.19%.

VI. CONCLUSION

A single-phase step-up five-level inverter has been proposed and implemented with a new PS-PWM strategy in this paper. The operating principle and performance analysis show that a double step-up ratio, reduced number of power devices and self-balanced capacitor voltages are achieved in the proposed inverter topology. Furthermore, the proposed PS-PWM strategy is equivalent to the conventional PS-PWM strategy with one less carrier, which makes it much easier to implement in a DSP control board system. The proposed PS-PWM strategy provides a new idea for implementing phase-shifted modulations and can be extended to other power converters. The PR control method was utilized to realize closed loop control for the output voltage of the proposed inverter.

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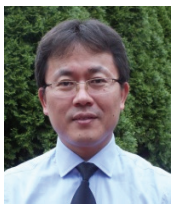

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