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# A Novel Method for Compensating Phase Voltage Based on Online Calculating Compensation Time

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## Abstract

Dead time and the nonideal characteristics of components all lead to phase voltage distortions. In order to eliminate the harmful effects caused by distortion, numerous methods have been proposed. The efficacy of a method mainly depends on two factors, the compensation voltage amplitude and the phase current polarity. Theoretical derivations and experiments are given to explain that both of these key factors can be deduced from the compensation time, which is defined as the error time between the ideal phase voltage duration and the actual phase voltage duration in one Pulse Width Modulation (PWM) period. Based on this regularity, a novel method for compensating phase voltage has been proposed. A simple circuit is constructed to realize the real-time feedback of the phase voltage. Utilizing the actual phase voltage, the compensation time is calculated online. Then the compensation voltage is derived. Simulation and experimental results show the feasibility and effectivity of the proposed method. They also show that the error voltage is decreased and that the waveform is improved.

**Key words:** Compensation time, Dead time, Nonideal characteristics of components, Real-time feedback on phase voltage

## I. INTRODUCTION

The phase voltage produced by a Voltage Source Inverter (VSI) cannot always be measured directly. When this occurs, the actual phase voltage is often replaced by the command phase voltage. However, due to the dead time effect and the nonideal characteristics of components [1], [2], there is a distinct error between the actual phase voltage and the command phase voltage which may result in current distortion and torque ripples. Thus, it is necessary to compensate the error of the phase voltage.

Numerous methods have been studied and proposed to alleviate the distortion of phase voltage. Most of these methods can be sorted into two types, methods based on model observation [3]-[5] and methods based on mechanism analysis [6]-[8].

Methods based on model observation estimate the error voltage caused by the dead-time effect and the nonideal characteristics of components through adopting motor models or observers. In [9], a simple vectorial disturbance estimator is established by transforming the phase voltage, phase current and rotor position. In [10], the sixth harmonic of the integrator output of a synchronous d-axis proportional integral (PI) current regulator is used to compensate output voltage distortion. Usually, the calculation costs of methods based on model observation are fairly high.

Methods based on mechanism analysis quantitively and theoretically analyze and evaluate dead-time effect. The error voltage is drawn by the volt-second principle of PWM. The efficacy of such method depends on amplitude of compensation voltage and the polarity of phase current. The compensation voltage amplitude can be obtained by off-line pointing and on-line testing [11]. With regard to the current polarity, direct A/D sample is used in many papers [12]. However, the accuracy is usually very low because of Direct Current (DC) drift of sensors and high frequency noise. Since the current polarity determines compensation accuracy, the wrong detection results can make the situation worse [13]. In [14], a hardware circuit is applied to detect the current of the freewheeling diode. In [15], [16], terminal voltage of diode is used to judge current polarity, however, the power supply is complex which may increase

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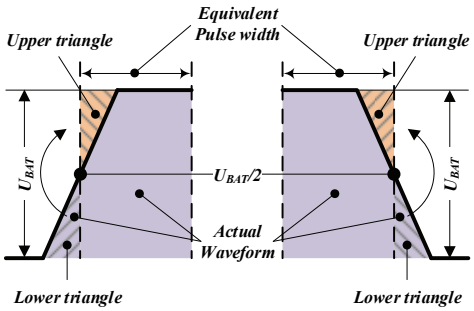


Fig. 1. Slope process of voltage change and the equivalent step process.

costs. The current predictive control in [17] can judge the polarity of current. However, in this method, precise machine parameters are needed.

In this paper, the cause and effect of the error voltage is analyzed, and the change rules of the compensation voltage are determined. Consistency between the compensation time and the phase current is found. On the basis of this new discovery, a novel method for compensating phase voltage is proposed. A simple hardware circuit is designed to realize the real-time feedback of VSI output. Then the compensation time is calculated according to the output. The compensation voltage amplitude and the phase current polarity are both derived from the compensation time. Then the compensation voltage is determined. Simulation and experimental results are presented to verify the effectiveness of the proposed method.

## II. Analysis of Phase Voltage Distortion

### A. Distortion Analysis

In reality, due to the nonideal characteristics of components and the parasitic capacitors of switching devices, voltage changes are not instantaneous. They act as a slope process which is plotted in the heavy line in Fig. 1. For the sake of convenience, the actual slope process can be equivalent to a step process which is plotted in the dashed line in Fig. 1. The transformation process is as follows. Taking $U_{BAT}/2$ as the vertex, shadowed triangles are plotted. Obviously, the upper triangle and the lower triangle have the same area. If the lower triangle is rotated around the $U_{BAT}/2$ vertex, the lower triangle overlaps with the upper triangle and an equivalent pulse width is made.

One arm (phase A) from a VSI is taken as an example to analyze the distortion. Fig. 2 shows the waveform applied to a gate electrode in one PWM period after inserting dead time. Fig. 3 shows the one arm condition when $i_A$>0. The power devices are Insulated Gate Bipolar Transistors (IGBTs). Thus, the current can only flow in one direction.

Analyzing Fig. 2 and Fig. 3, the condition of $i_A$ >0 is discussed here. In the 'a' period of Fig. 2, $Q_L$ is turned on. Since the IGBT can only conduct in one direction, the current flows through $D_L$, and the potential of the output terminal is

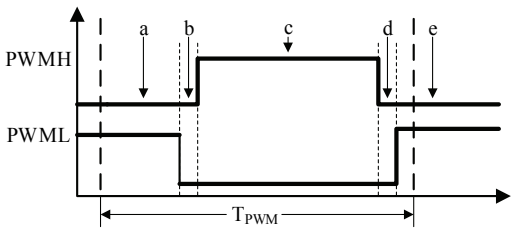


Fig. 2. Waveform applied to a gate electrode.

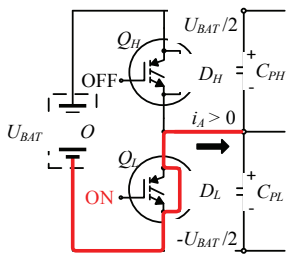


Fig. 3. One arm condition when $i_A$>0.

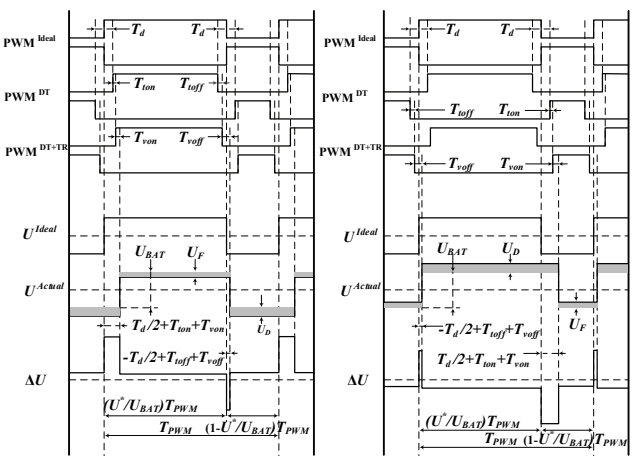


Fig. 4. Waveform distortion process when $i_A$ >0 and $i_A$ <0. (a) $i_A$ >0. (b) $i_A$ <0.

($-U_{BAT}/2-U_D$), where $U_D$ is the voltage drop of the freewheeling diode. In the 'b' period, $Q_L$ and $Q_H$ are both turned off. In this case, the power devices of phase A operate in dead time, and potential of the output terminal is still ($-U_{BAT}/2-U_D$). In the 'c' period, $Q_H$ is turned on and the current flows through $Q_H$. Hence, the potential of the output terminal is ($U_{BAT}/2-U_F$), where $U_F$ represents the forward voltage drop of the IGBT. In the 'd' period, $Q_H$ and $Q_L$ are both turned off, and the power devices are working in the other dead time. Thus, the potential of the output terminal is ($-U_{BAT}/2-U_D$), which is the same as the 'b' period. The condition of $i_A$ <0 is similar to the condition of $i_A$ >0. Therefore, it will not be covered here. It can be concluded that the amplitude and phase of the terminal voltage are both distorted.

The authors of [18] deduced the phase voltage distortion in detail. Fig. 4 shows the whole process of how the phase voltage gets distorted. Take phase A as an example. In Fig. 4, $T_d$ is the

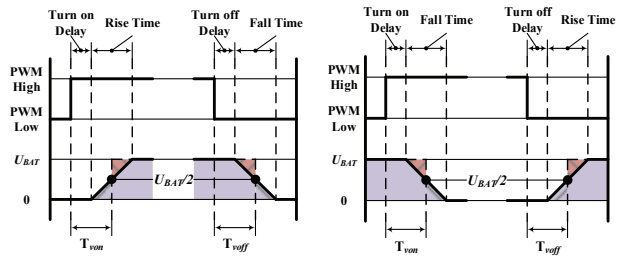


Fig. 5. $T_{von}$ and $T_{voff}$ in two current polarity. (a) $i_A$>0. (b) $i_A$<0.

inserting dead time; $T_{ton}$ and $T_{toff}$ are the total turn on delay and turn off delay of the gate drive circuits; $T_{von}$ is the delay between the gate rising edge and the phase voltage changes, while $T_{voff}$ defines the delay between the gate falling edge and the phase voltage changes. To be sure, $T_{von}$ and $T_{voff}$ both contain two stages.

Fig. 5 shows the two stages of $T_{von}$ and $T_{voff}$ in different current polarities. In Fig. 5, $V_{GE}$ is the switch signals applied to an IGBT gate electrode. Usually, the power devices used in the upper and lower bridge are identical. Therefore, their time-delay characteristics are the same. Taking Fig. 5(a) $i_A$ >0 as example, $T_{von}$ includes two parts. The first part is the device turns on delay, which is the delay time from the rising edge of gate electrode to the breakover of the IGBT. The second part is the delay of the rise time, which is the delay of the charging time of the parasitic capacitor. $T_{voff}$ also includes two parts. The first part is the device turn off delay, which is the delay time from the falling edge of the gate electrode to the shut of the IGBT. The second part is the delay of the fall time. Since the turn on (off) delay is mainly decided by the gate drive circuits, the turn on (off) delay varies little under different conditions. The rise (fall) time is the main factor affecting $T_{von}$ and $T_{voff}$. Fig. 5(b) $i_A$ <0 is similar to Fig. 5(a) $i_A$ >0.

### *B. Distortion Theory*

The distortion process is as follows. ① Inserting dead time changes the $PWM^{Ideal}$ to $PWM^{DT}$. ② Due to the non-ideal characteristics of the parts in the gate drive circuits, the $PWM^{DT}$ changes to $PWM^{DT+TR}$. $PWM^{DT+TR}$ is the exact signal applied to the IGBT gate electrode. In Fig. 4, $U^*$ is the corresponding phase voltage to the outcome of SVPWM. In addition, $U^{Ideal}$ is the ideal output of the VSI, and $U^{Actual}$ is the actual output of the VSI. As a result, $\Delta U=U^{Ideal}-U^{Actual}$ is the error voltage. Obviously, the error voltage $\Delta U$ is the exact compensation voltage.

In Fig. 4, the expression of the compensation voltage ($i_A$ >0) can be derived using the average value principle of PWM:

$$\Delta U=\frac{T_c^+}{T_{PWM}}\cdot\left(U_{BAT}+U_D-U_F\right)+\frac{U^*}{U_{BAT}}\cdot U_F+\left(1-\frac{U^*}{U_{BAT}}\right)\cdot U_D \quad (1)$$

where $T_c^+$ is the compensation time for $i_A$ >0. It can be written as (2).

$$T_c^+=\Delta T_{rise}^+-\Delta T_{fall}^+ \quad (2)$$

$\Delta T_{rise}^+$ and $\Delta T_{fall}^+$ are defined as (3) which are total delay time.

$$\begin{cases}\Delta T_{rise}^+=\dfrac{T_d}{2}+T_{ton}+T_{von}\\ \Delta T_{fall}^+=-\dfrac{T_d}{2}+T_{toff}+T_{voff}\end{cases}\quad(i_A>0) \quad (3)$$

$$T_c^+=T_d+\left(T_{ton}-T_{toff}\right)+\left(T_{von}-T_{voff}\right) \quad (4)$$

Similarly, the compensation voltage and compensation time for $i_A$ <0 can be written in (5) and (6).

$$\Delta U=\frac{T_c^-}{T_{PWM}}\cdot\left(U_{BAT}+U_D-U_F\right)-\frac{U^*}{U_{BAT}}\cdot U_D-\left(1-\frac{U^*}{U_{BAT}}\right)\cdot U_F \quad (5)$$

$$T_c^-=-\left[T_d+\left(T_{ton}-T_{toff}\right)+\left(T_{von}-T_{voff}\right)\right] \quad (6)$$

In (1) and (5), the command voltage $U^*$ varies from 0 to $U_{BAT}$. For the sake of convenience, replace $U^*$ with $\bar{U}^*$, and the range of $\bar{U}^*$ is -$U_{BAT}$ /2 ~ $U_{BAT}$ /2. With the definition of $T_c$ and sgn($i_A$) as (7) and (8), the compensation voltage can be described as (9).

$$T_c=\begin{cases}T_c^+ & (i_A>0)\\ T_c^- & (i_A<0)\end{cases} \quad (7)$$

$$\mathrm{sgn}\left(i_A\right)=\begin{cases}1 & (i_A>0)\\ -1 & (i_A<0)\end{cases} \quad (8)$$

$$\Delta U=\frac{T_c}{T_{PWM}}\cdot\left(U_{BAT}+U_D-U_F\right)+\mathrm{sgn}(i_A)\cdot\frac{U_F+U_D}{2}+\frac{\bar{U}^*}{U_{BAT}}\cdot\left(U_F-U_D\right) \quad (9)$$

## III. PROPOSED COMPENSATION METHOD

From (9), the amplitude of the compensation voltage is decided by $T_c$, $T_{PWM}$, $U_{BAT}$, $U_D$, $U_F$ and $\bar{U}^*$. Among all of the parameters, $\bar{U}^*$, $U_{BAT}$, and $T_{PWM}$ are the easiest to obtain. $U_D$ and $U_F$ can either be obtained online or composed a look-up table offline. From (9), $T_c$ is the key factor that affects the amplitude of the compensation voltage. However, $T_c$ is hard to obtain. From (4) and (6), the parameters that affect $T_c$ are $T_d$, $T_{ton}$, $T_{toff}$, $T_{von}$ and $T_{voff}$. Among them, $T_d$ is given by a program. $T_{ton}$ and $T_{toff}$ are the total delay of the gate drive circuits. Since the circuits work in a simple condition where the power of the circuits is approximately constant, $T_{ton}$ and $T_{toff}$ can be considered as constants. However, it is difficult to get the accurate values of $T_{von}$, $T_{voff}$ by the off-line or prediction method. Aiming at obtaining an accurate compensation time $T_c$, this paper proposed a method that calculates $T_c$ by utilizing online real-time feedback on the rectangular wave of the phase voltage. Fig. 5 illustrates that the compensation time $T_c$ is equal to the high-level duration of $U^{Ideal}$ minus the high-level duration of $U^{Actual}$. Thus, once the high-level duration of $U^{Actual}$ is measured $T_c$ can be calculated.

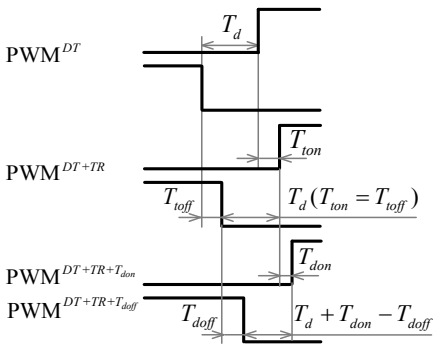


Fig. 6. Analysis of waveform distortions.

Equation (9) implies that the compensation time is mainly affected by the current polarity. Methods using A/D converters to get current in many papers are sensitive to noise. Moreover, a phase shift will be introduced when using filters, therefore, results in judgments are far from accurate. In this paper, the consistency between the compensation time $T_c$ and the phase current is found. With this regularity, the current polarity can be judged by the sign of the compensation time $T_c$.

### *A. Derivation of Rise Time $T_r$ and Fall Time $T_f$*

As shown in Fig. 6, the rise time $T_r$ (fall time $T_f$) is the main factor affecting $T_{von}$ and $T_{voff}$. To verify the consistency between the current polarity and the sign of the compensation time $T_c$, the relationship between $T_r$ ($T_f$) and the current should be derived. The derivation is based on the charging (discharging) time model of the parasitic capacitor.

The terminal voltage $v$ linearly rises after the turn off of the lower switch when $i_r$ is negative, as given by:

$$v = \frac{i_r}{C_p} t \tag{10}$$

where $C_p$ is the parasitic capacitance of one arm.

In Fig. 6, the rising edge of $PWM^{DT+TR+Tdon}$ represents the actual turn on moment of the upper switch, so does $PWM^{DT+TR+Tdoff}$. The transmit delay $T_{ton}$ and $T_{toff}$ of the two gate drive signals are considered to be the same. In addition, taking into consideration the difference between the turn on delay $T_{don}$ and the turn off delay $T_{doff}$, the timespan between these two moments is derived as $T_d + T_{don} - T_{doff}$. When $i_r$ is equal to a critical value $I_c$, the terminal voltage reaches $U_{BAT}$ at the end of $T_d + T_{don} - T_{doff}$. In addition, $I_c$ can be deduced as (11) according to (10).

$$I_c = \frac{U_{BAT} C_p}{T_d + T_{don} - T_{doff}} \tag{11}$$

Fig. 7 shows the variation trend of the terminal voltage $v$ at different currents $i_r$. The dotted line in the figure sets as the equivalent rising time. Suppose the rising edge of terminal voltage is an ideal step signal, and the average value of terminal voltage in a PWM period remains the same after the equivalent processing. The equivalent rising edge represents

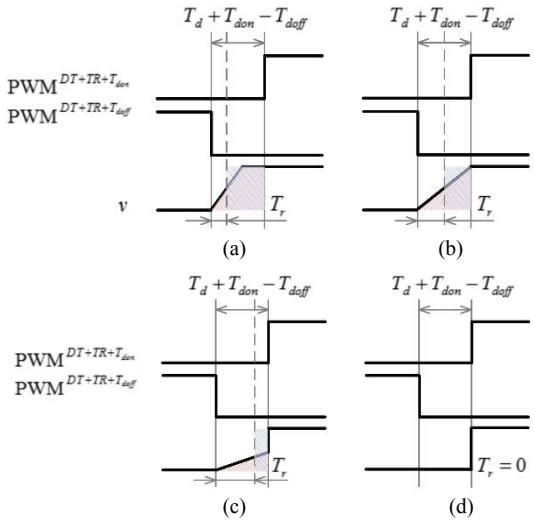


Fig. 7. Variation trends of the terminal voltage $v$ and rise time $T_r$ at different currents. (a) $i_r < -I_c$. (b) $i_r = -I_c$. (c) $-I_c < i_r < 0$. (d) $i_r > 0$.

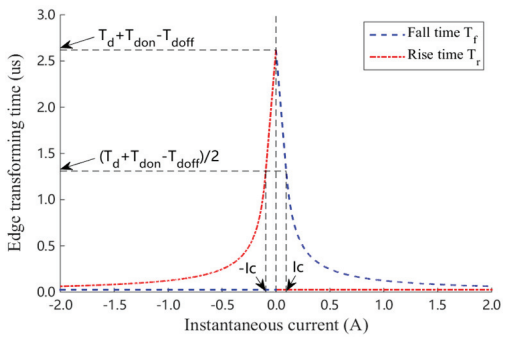


Fig. 8. Characteristics of the rise time and fall time of inverter output voltage for the instantaneous value of phase current.

the actual step moment of the terminal voltage. The blue shaded space and the red shaded space have the same area. According to this rule, the rise time $T_r$ at different values of $i_r$ is derived in (12).

$$T_r = \begin{cases} \dfrac{U_{BAT} C_p}{-2 i_r} & (i_r \le -I_c) \\ (T_d + T_{don} - T_{doff}) + \dfrac{i_r (T_d + T_{don} - T_{doff})^2}{2 U_{BAT} C_p} & (-I_c < i_r < 0) \\ 0 & (i_r > 0) \end{cases} \tag{12}$$

The fall time $T_f$ at different currents is derived as given by expression (13).

$$T_f = \begin{cases} 0 & (i_f < 0) \\ (T_d + T_{don} - T_{doff}) - \dfrac{i_f (T_d + T_{don} - T_{doff})^2}{2 U_{BAT} C_p} & (0 < i_f < I_c) \\ \dfrac{U_{BAT} C_p}{2 i_f} & (i_f \ge I_c) \end{cases} \tag{13}$$

When $i_f$ is negative and the upper switch is turned on, the parasitic capacitor is shorted and the terminal voltage $v$ is pulled down to zero in a very short time. This time is ignored in the analysis of $T_f$. Curves of $T_r$ and $T_f$ are plotted based on equations (12) and (13), as shown in Fig. 8, where $T_d$ =3us,

$T_{don}$=0.12us, $T_{doff}$=0.51us, $U_{BAT}$=248V and $C_p$=1nF.

### B. Demonstration of the Consistency between the Sign of the Compensation Time Tc and the Current Polarity

Before derivation the consistency, some assumptions should be set and some minor factors should be neglected. (1) The switches of one arm is of consistency. (2) The charging time of the parasitic capacitor is zero when connected to the positive pole of battery. (3) The discharging time of the parasitic capacitor is zero after the lower switch is turned on when the current is negative. (4) The transition delays of the rising and falling edge of the gate-drive signals are the same, $T_{ton}$= $T_{toff}$. (5) Ignore the effect of zero-current clamping. The demonstration is divided into 3 conditions according to the polarities of $i_r$ and $i_f$.

*1)* $i_r$ >0 and $i_f$ >0: Under this condition, the rising edge and falling edge of the terminal voltage are caused by the turn on and turn off of the upper switch, respectively. As shown in Fig. 5(a), $T_{von}$ and $T_{voff}$ are:

$$\begin{cases} T_{von} = T_{don} + T_r \\ T_{voff} = T_{doff} + T_f \end{cases} \tag{14}$$

Considering (4), (14) and Fig. 7, when $i_f$ >0, $T_f$ increases with the decrease of $i_f$. When $i_f \to 0+$, $T_f$ reaches its maximum value $T_d + T_{don}$ - $T_{doff}$, and $T_{voff}$ also reaches its maximum value $T_d + T_{don}$. $T_c$ reaches its minimum value $T_r$ according to (15). $T_r$ is supposed to be zero when $i_r$ >0. However, $T_r$ is close to but slightly larger than zero. The minimum value of $T_c$ is bigger than zero. Therefore, $T_c$ >0 when $i_r$ >0 and $i_f$ >0. The derivation process is concluded as follows:

$$\begin{aligned} \lim_{i_f \to 0^+} T_c &= \lim_{i_f \to 0^+} (T_d + (T_{ton} - T_{toff}) + (T_{von} - T_{voff})) \\ &= \lim_{i_f \to 0^+} (T_d + (T_{von} - T_{voff})) \\ &= T_d + (T_{don} + T_r) - (T_{doff} + \lim_{i_f \to 0^+} T_f) \\ &= T_d + (T_{don} + T_r) - (T_{doff} + (T_d + T_{don} - T_{doff})) \\ &= T_r > 0 \end{aligned} \tag{15}$$

*2)* $i_r$ <0 and $i_f$ <0: Under this condition, when $i_r$ <0, $T_r$ increases with the increase of $i_r$. When $i_r \to 0-$, $T_r$ reaches its maximum value $T_d$ + $T_{don}$ - $T_{doff}$, and $T_{voff}$ also reaches its maximum value $T_d + T_{don}$ and $T_c$ reaches its maximum value – $T_f$ according to (16). The maximum value of $T_c$ is negative. Therefore, $T_c$ <0 when $i_r$ <0 and $i_f$ <0. The derivation process is concluded into the following equation.

$$\begin{aligned} \lim_{i_r \to 0^-} T_c &= -\lim_{i_r \to 0^-} (T_d + (T_{ton} - T_{toff}) + (T_{von} - T_{voff})) \\ &= -\lim_{i_r \to 0^-} (T_d + (T_{von} - T_{voff})) \\ &= -(T_d + (T_{don} + T_f) - (T_{doff} + \lim_{i_r \to 0^-} T_r)) \\ &= -(T_d + (T_{don} + T_f) - (T_{doff} + (T_d + T_{don} - T_{doff}))) \\ &= -T_f < 0 \end{aligned} \tag{16}$$

*3)* $i_r$ <0 and $i_f$ >0: The compensation time $T_c$ in this condition is:

$$T_c = \Delta T_{rise}^- - \Delta T_{fall}^+ = T_r - T_f \tag{17}$$

As in Fig. 8, when $|i_r|$<$|i_f|$, $T_r$ >$T_f$. Therefore, $T_c$ > 0 according to equation (17). Similarly, when $|i_r|$=$|i_f|$ and $|i_r|$>$|i_f|$, the conclusions $T_c$ = 0 and $T_c$ < 0 can be derived respectively.

Summarizing the relation between $T_c$, $i_r$ and $i_f$ under the three conditions, the following expression is obtained.

$$\mathrm{sgn}(T_c) = \begin{cases} +1 & i_r + i_f > 0 \\ 0 & i_r + i_f = 0 \\ -1 & i_r + i_f < 0 \end{cases} \tag{18}$$

Define the equivalent phase current polarity $i_{ep}$:

$$i_{ep} = \mathrm{sgn}(i_r + i_f) \tag{19}$$

Introduce $i_{ep}$ into expression (18). Then expression (20) is derived as:

$$i_{ep} = \mathrm{sgn}(T_c) \tag{20}$$

It has been theoretically verified that the sign of the compensation time $T_c$ is consistent with the equivalent phase current polarity.

### C. Experiment Verification of the Demonstration

Fig. 9 shows the variation trend of the terminal voltage in 6 consecutive cycles when the phase current increases from negative to positive in experiments. Fig. 10 shows the variation trend of the phase current, the equivalent phase current polarity $i_{ep}$ and the compensation time $T_c$ of the 6 consecutive cycles in Fig. 8. In Fig. 9(a), the rise time is long and the fall time is short, which indicates that current at the rising edge $i_r$ and falling edge $i_f$ are both negative, as shown in Fig. 9(a). In Fig. 9(b) and Fig. 9(c), the rise time and fall time both increase when compared with Fig. 9(a). The rise time increases when the current is negative since if the amplitude of the current decreases, the charging time of the parasitic capacitor increases and then the rise time increases. The fall time increases since the current at the falling edge if it has changed from negative in Fig. 9(a) to positive in Fig. 9(b) and Fig. 9(c), as shown in Fig. 10. The fall time in Fig. 9(c) is shorter than that in Fig. 9(b) because current at the falling edge if it increases and the parasitic capacitor discharges faster. In Fig. 9(a), (b), (c), (d) and (e), the rise time remains long which means that the current at the rising edge $i_r$ is still negative, and the rising time becomes longer and longer since $i_r$ becomes smaller and smaller and the parasitic capacitor charges slower and slower. When the absolute value of $i_r$ is smaller than $I_c$, the charging time of the parasitic capacitor is limited by $T_d$ + $T_{don}$ - $T_{doff}$. Therefore, the slope of the rising edge changes sharply in Fig. 9(e). In Fig. 9(f), the rise time is short and the fall time is long, which indicates that the current is positive at both the rising edge and the falling edge. To summarize, the current finishes the change from negative to positive in 6 consecutive cycles, and the phase current is oscillating in this process. In particular, in Fig. 9(d), the current amplitude at the rising edge and the

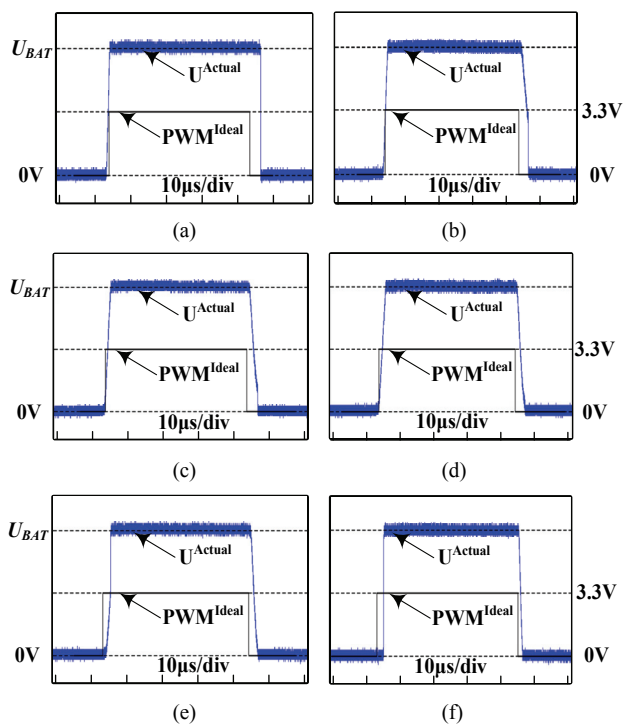


Fig. 9. Trend of the terminal voltage in 6 consecutive cycles when the phase current increases from negative to positive in experiments.

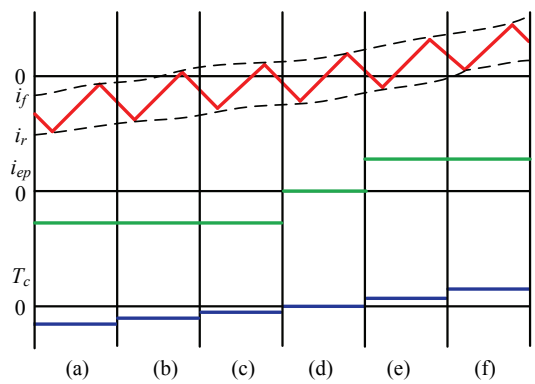


Fig. 10. Variation trend of the phase current, equivalent phase current polarity $i_{ep}$ and compensation time $T_c$ of the 6 consecutive cycles in Fig. 9.

falling edge are about equal but the polarities are opposite. This is the condition where the equivalent phase current polarity $i_{ep}$ is equal to zero. It can be seen roughly that $T_c$=0 in the figure. It is experimentally verified that the compensation time $T_c$ has the same sign as the equivalent phase current. The variation trend of the phase voltage in 6 consecutive cycles when the phase current decreases from positive to negative in experiments will not be repeated here.

Taken together, the amplitude and polarity of the compensation voltage can be derived from the compensation time $T_c$. Thus, the compensation method is simplified. The key factor turns into accurately measuring the compensation time $T_c$. Since the change rule of $T_c$ is complicated, the online measurement of $T_c$ is implemented in this paper. As defined above, the compensation

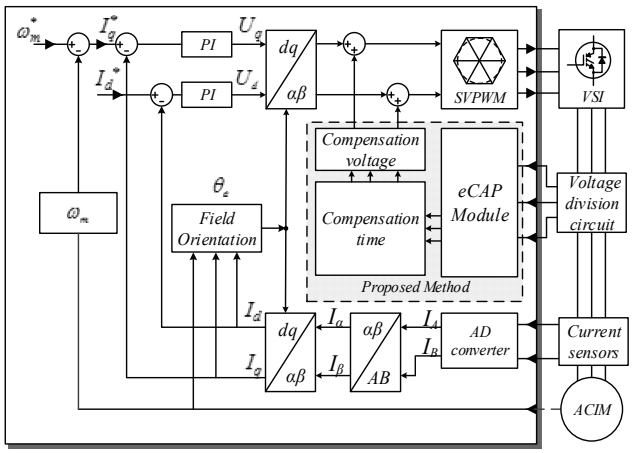


Fig. 11. Control-model with the proposed compensation method.

TABLE I
SIMULATION PARAMETERS

| Variables | Quantities | Units |
|---|---|---|
| Battery voltage $U_{BAT}$ | 248 | V |
| PWM period | 100 | μs |
| Dead time | 3 | μs |
| Forward voltage drop $U_F$ | 1.6 | V |
| Diode voltage drop $U_D$ | 1.5 | V |
| Electric time constant | 2.979 | ms |
| Stator phase resistance $R_s$ | 2.35 | ohm |

time $T_c$ is equal to the high-level duration of $U^{Ideal}$ minus the high-level duration of $U^{Actual}$. The high-level duration of $U^{Ideal}$ is given by $PWM^{Ideal}$, and the high-level duration of $U^{Actual}$ can be measured by real-time feedback of the terminal voltage. The actual terminal voltage is a periodic rectangular wave. Thus, the event capture unit can be used to obtain the high-level duration of $U^{Actual}$. In addition, since the actual terminal voltage is digital signal, it is easy to catch and interference-free. As a result, isolation is not required for the hardware feedback circuit, and a high-speed comparator for voltage comparison is used to get the high-level duration of $U^{Actual}$ precisely and quickly. Fig. 11 shows a control-model with the proposed compensation method.

## IV. SIMULATION RESULTS

A simulation model is established to verify the proposed method. The simulation parameters are shown in Table I.

The conventional open-loop fixed compensation is a simple and relatively effective compensation solution. The compensation time $T_c$ equals to dead-time $T_d$. The compensation phase voltage can be defined in (21).

$$\Delta U_A^{conv} = \mathrm{sgn}(i_A) \cdot \frac{T_d}{T_{PWM}} \cdot U_{BAT} \tag{21}$$

Fig. 12 is a voltage waveform of the α axis and β axis in actual situations without compensation. In actual situations,

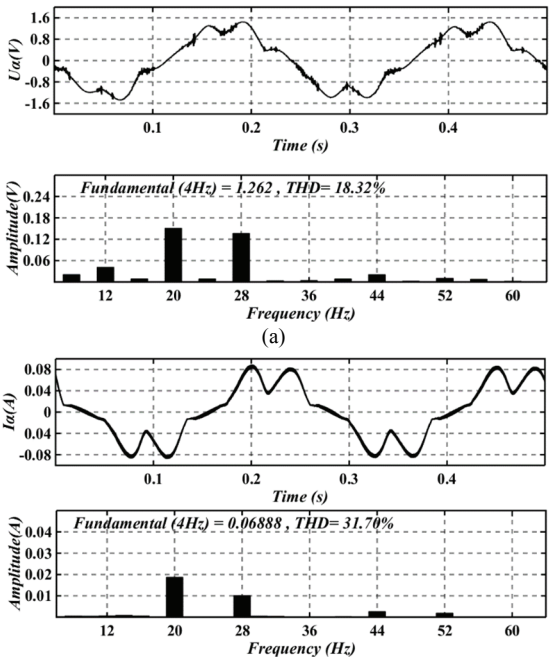


Fig. 12. Voltage waveforms of the α axis and β axis with FFT results in actual situations without compensation. (a) α axis voltage waveform and FFT results. (b) β axis voltage waveform and FFT results.

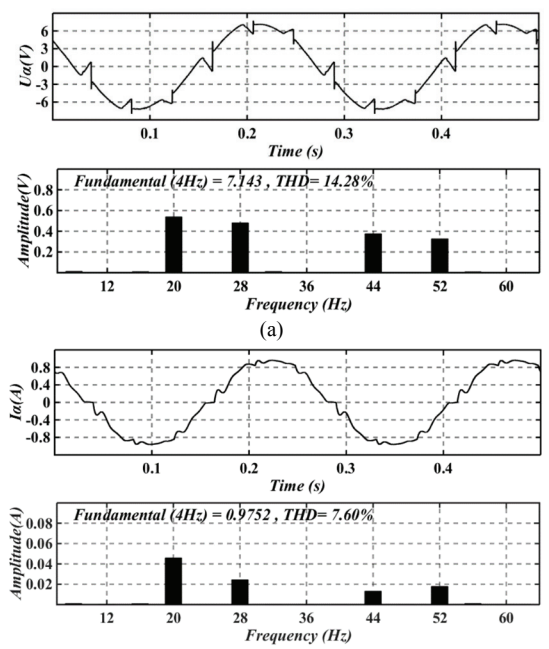


Fig. 13. Voltage waveforms of the α axis and β axis with FFT results in actual situations adopting the conventional compensation scheme. (a) α axis voltage waveform and FFT results. (b) β axis voltage waveform and FFT results.

the voltage and current are severely distorted especially by the 5th and 7th harmonics.

Fig. 13 is a voltage waveform of the α axis and β axis in actual situations adopting the conventional compensation scheme. It

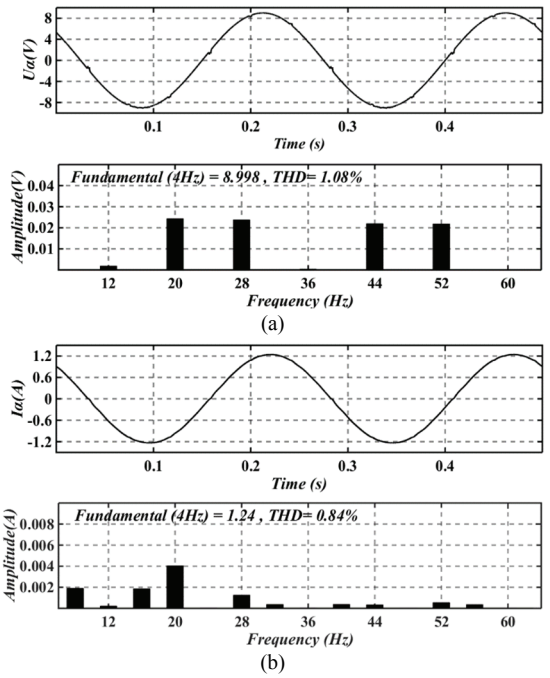


Fig. 14. Voltage waveforms of the α axis and β axis with FFT results in actual situations adopting the proposed compensation method. (a) α axis voltage waveform and FFT results. (b) β axis voltage waveform and FFT results.

can be seen in Fig. 13 that the conventional scheme does reduce the distortion effect. However, the distortion in the zero-crossing region is still serious. This is because in the conventional scheme, the compensation time is fixed to $T_d$. However, as shown above, the compensation time is approximately equal to $T_d$ only when the current amplitude is large and it varies a lot when the current amplitude is close to zero. Therefore, the conventional scheme can alleviate distortion when the current amplitude is large. However, it has no effect when the current amplitude is close to zero.

Fig. 14 shows voltage waveforms of the α axis and β axis in actual situations by adopting the proposed compensation method. Fig. 14 verifies that the proposed method can make the voltage and current waveforms approach to a sine wave. The THD value is near 1%, and the proposed method behaves much better when current is close to zero.

## V. Experiment Results

An experimental platform is set up with a TMS320F28335. The load motor is an 184W induction motor. The experimental platform set up is shown in Fig. 15. The parameters of the experimental platform are listed in Table II.

Fig. 16 shows waveforms of DSP feedback signal and the output signal of the VSI. As shown in Fig. 16, $U^{tActual}$ has a distinct phase error and the feedback signal mirrors the actual pulse width quite well. In addition, when the rise time or fall time is long, the feedback signal reflects the equivalent pulse width defined in Fig. 1.

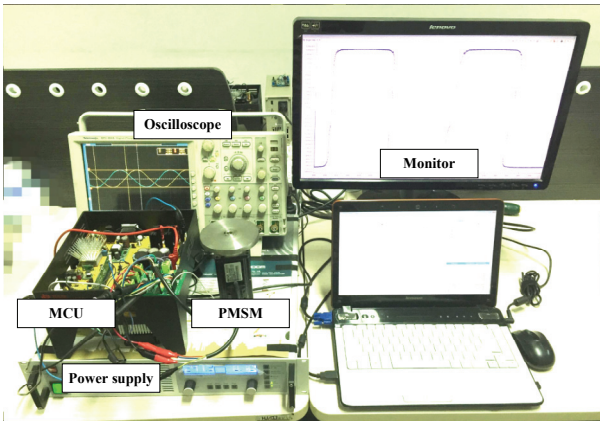


Fig. 15. Experimental platform.

TABLE II
EXPERIMENTAL PARAMETERS

| Variables | Quantities | Units |
|---|---|---|
| Battery voltage $U_{BAT}$ | 248 | V |
| Motor rated voltage | 200 | V |
| Motor rated current | 1.3 | A |
| Motor rated speed | 1725 | rpm |
| Power module | PS21765 | -- |

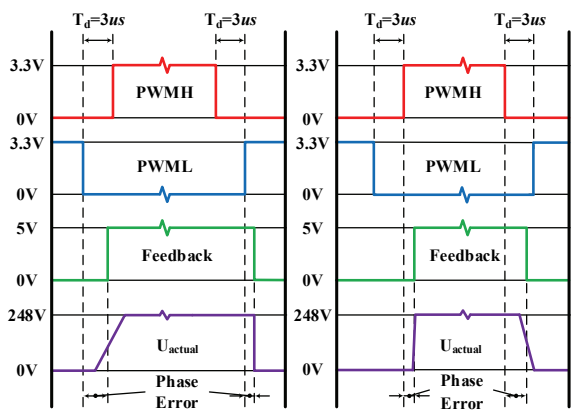


Fig. 16. DSP output signal, feedback signal and VSI output signal. (a) Phase current is negative. (b) Phase current is positive.

### A. Comparison of the Compensation Error

Fig. 17 shows a contrast of the compensation voltage between the conventional scheme and the proposed scheme. It is clear that after compensation, the error voltage with the proposed scheme is much less than the error voltage with the conventional scheme. Moreover, the compensation voltages of the two schemes differ greatly at the zero-crossing regions.

### B. Compensation Effects at Low Speed

Fig. 18 and Fig. 19 show current and voltage waveforms at an ultra-low speed of 3r/min. As can be seen in the figures, the voltage and current are seriously distorted and the motor jitters violently. The actual voltage is almost the same as the command

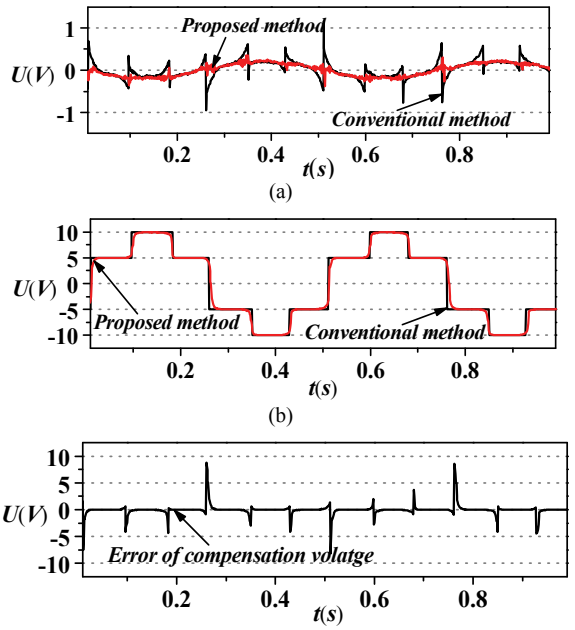


Fig. 17. Comparison of compensation voltages between the conventional method and proposed method. (a) Error voltage after compensation. (b) Compensation voltage. (c) Errors of the two compensation methods.

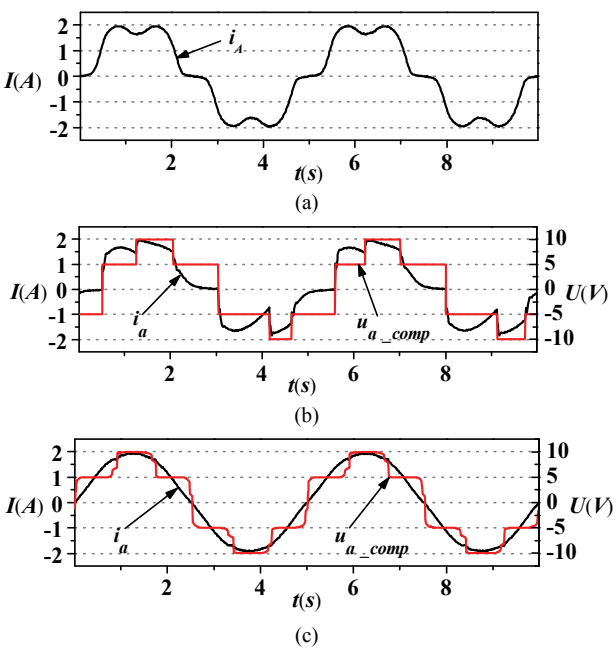


Fig. 18. α axis current and α axis compensation voltage at 3r/min. (a) Phase current without compensation. (b) Phase current with the conventional compensation. (c) Phase current with the proposed compensation.

voltage when applying the proposed method. However, the effect of the conventional scheme is not satisfying. The compensation voltage of the conventional method consists of straight lines. However, the compensation voltage of the proposed method has more rounded edges.

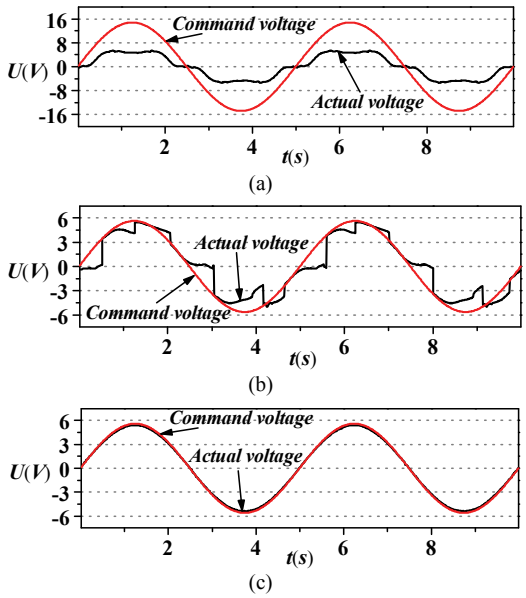


Fig. 19. α axis current and α axis compensation voltage at 3r/min. (a) Phase voltage without compensation. (b) Phase voltage with the conventional compensation. (c) Phase voltage with the proposed compensation.

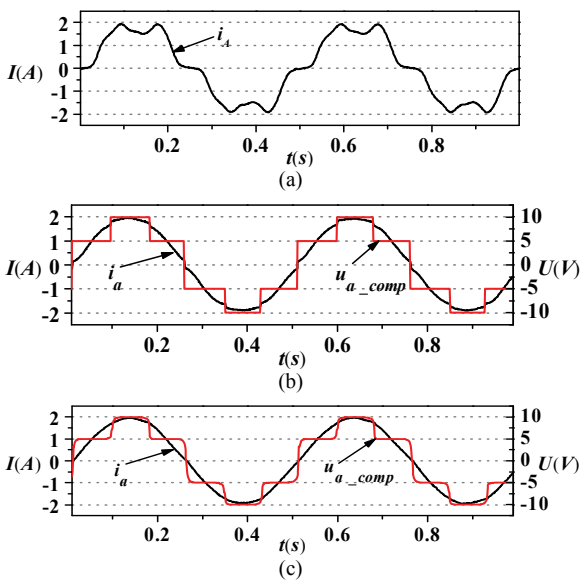


Fig. 20. α axis current and α axis compensation voltage at 30r/min. (a) Phase current without compensation. (b) Phase current with the conventional compensation. (c) Phase current with the proposed compensation.

Fig. 20 and Fig. 21 show current and voltage waveforms at a speed of 30r/min. The conventional method has a negative effect on the zero-crossing regions while the proposed method compensates the voltage almost perfectly during the whole process.

### C. Compensation Effects When the Speed Varies

Fig. 22 shows that the compensation time always changes with the phase current. Therefore, this regularity has been verified by theoretical derivation, simulations and experiments.

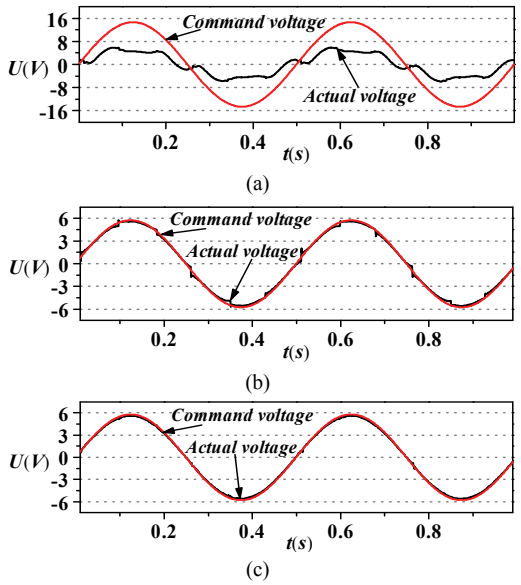


Fig. 21. α axis current and α axis compensation voltage at 30r/min. (a) Phase voltage without compensation. (b) Phase voltage with the conventional compensation. (c) Phase voltage with the proposed compensation.

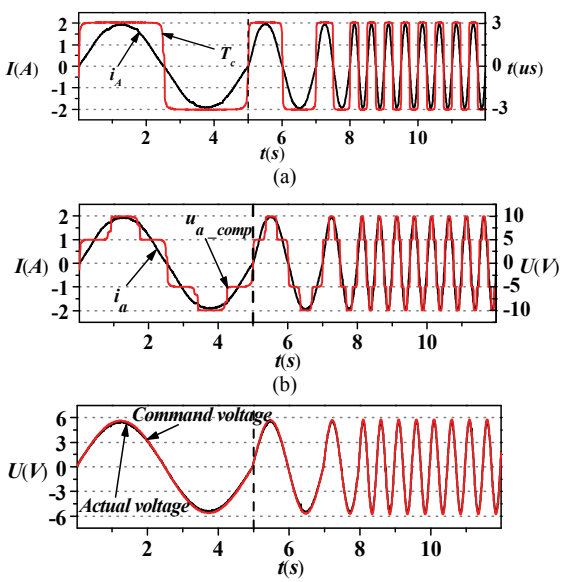


Fig. 22. Waveforms when the rotor speed leaps from 3r/min to 30r/min. (a) α axis current and compensation time Tc. (b) α axis current and compensation voltage. (c) α axis actual voltage and command voltage.

In addition, in Fig. 22(c), the experiment with speed varies from 3r/min to 30r/min is carried out and the compensation time still follows the current perfectly.

Fig. 23 shows compensation results at a relatively high frequency with the proposed method in experiments. The FFT analysis indicates that the proposed method is effective in suppressing voltage harmonics at a high frequency. As can be seen in Fig. 24, with an increase of frequency, the voltage harmonics decrease to a low level even without compensation. Instead of suppressing

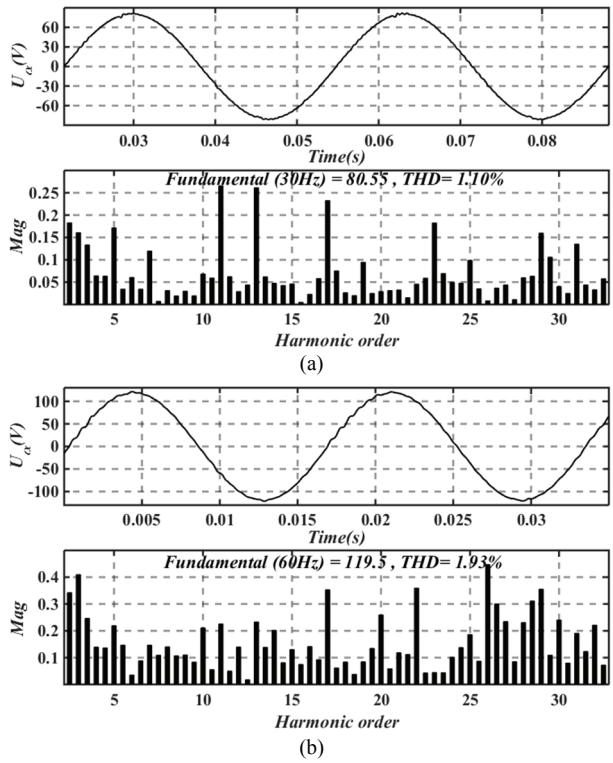


Fig. 23. α axis voltage and FFT analysis at a relatively high frequency with the proposed method. (a) 30Hz. (b) 60Hz.

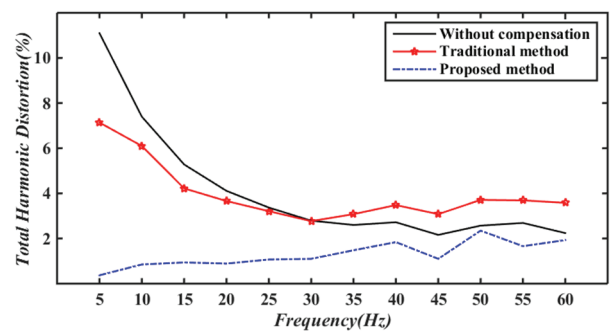


Fig. 24. Voltage THD at various frequencies.

voltage harmonics, the traditional method aggravates voltage distortion, while the proposed compensation method alleviates voltage distortion under all measured frequencies.

## VI. Conclusions

The voltage distortion caused by the dead time and nonideal characteristics of components has a negative effect on the performance of motors. Therefore, compensation of the voltage is necessary in high precision control systems. The distortions in the entire driving unit are synthetically considered in the proposed method, and the feedback control of a VSI is realized. This paper theoretically and experimentally demonstrates the consistency between the compensation time and the corresponding phase current in one PWM cycle. Finally, it is concluded that the amplitude and polarity of compensation voltage can both be derived from the compensation time. Simulation and experimental results show that the proposed method can achieve a satisfactory effect under various conditions. When compared with conventional methods, the proposed method doesn't need high-precision current sensing. Thus, it has broader application prospects.

## Acknowledgment

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