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Analysis and Implementation of LC Series Resonant Converter with Secondary Side Clamp Diodes under DCM Operation for High Step-Up Applications

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Abstract

Resonant converters have attracted a lot of attention because of their high efficiency due to the soft-switching performance. An isolated high step-up converter with secondary-side resonant loops is proposed and analyzed in this paper. By placing the resonant loops on the secondary side, the current stress for the resonant capacitors is greatly reduced. The power loss caused by the equivalent series resistance of the resonant capacitor is also decreased. Clamp diodes in parallel with the resonant capacitors ensure a unique discontinuous current mode in the converter. Under this mode, the active switches can realize soft-switching during both turn-on and turn-off transitions. Meanwhile, the reverse-recovery problems of diodes are also alleviated by the leakage inductor. The converter is essentially a step-up converter. Therefore, it is helpful for decreasing the transformer turn-ratio when it is applied as a high step-up converter. The steady-state operation principle is analyzed in detail and design considerations are presented in this paper. Theoretical conclusions are verified by experimental results obtained from a 500W prototype with a 35V-42V input and a 400V output.

Key words: DC/DC converter, Diode clamping, High voltage gain, LC resonant converter, Low voltage input

I. INTRODUCTION

Step-up converters with a high voltage gain and good efficiency have been widely developed in many applications, such as renewable energy (photovoltaic arrays and fuel cell stacks), automobile electrical systems, uninterruptible power systems and electrostatic precipitator systems [1]-[5], [7]-[20], [24]-[27]. For the sake of safety, isolation is usually required in high step-up converters. However, for a single hard-switching isolated converter, such as a full-bridge converter or a flyback converter, it is hard to achieve a very high voltage gain especially under high power conditions. On one hand, the switching loss and the output diode reverse-recovery loss are huge due to the hard switching status. On the other hand, the leakage inductance of a transformer would lead to high voltage spikes during the switching process and increases the voltage stress of the switches.

A high voltage gain can be realized by the cascaded connection of two step-up converters [4]-[6]. Hence, the requirement of the voltage gain can be distributed into two converters. In [4], a cascaded system consisting of a boost pre-regulated converter and an LLC converter with constant switching frequency is proposed. The final output voltage is only regulated by the duty-ratio of the boost converter. As a result, the control system can be easily designed. Similar ideas can be found in [5], [6]. However, due to the hard-switching operation in the pre-regulated stage, the efficiency is limited and it is hard to be highly promoted. In addition, the stability problems of cascaded systems also need special attention during the design process of closed-loop systems.

A high step-up function can be also achieved by the combined converters with Input Parallel Output Series (IPOS) architectures [7]-[9]. By this means, the components in each converter unit can be selected with low current and voltage ratings to achieve better characteristics because of the power distribution in the IPOS system. The conduction voltage drops of the diodes and active switches can be reduced when

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compared with high voltage rating components. However, input current sharing and output voltage sharing must be taken care of during the design process. The cost and circuit size are increased and the reliability is decreased with an increase in the number of modules.

In [10]-[13], coupled-inductors were introduced into converters to realize the high step-up function. However, the leakage inductance must be controlled in a minor range, which makes the design process of the magnetic component complex, especially under high turn-ratio situations. The energy stored in the leakage would also result in high spikes. Therefore, active clamp circuits [7], [12], [13] or non-dissipative snubbers [10], [11] need to be applied in order to recycle leakage energy and to suppress voltage spikes, which increase the design complexity of the circuit.

Voltage-multiplier technology has been widely employed in the secondary rectifier circuits of isolated converters in order to obtain a high voltage gain [14]-[16]. When compared with conventional rectifier circuits such as half-wave and full-wave rectifiers, the turn-ratio of the transformer or coupled-inductors can be significantly decreased when the voltage-multiplier order increases. Therefore, it is an effective method to level up the voltage gain. However, high-order voltage-multiplier circuits result in increases in cost, circuit size and power loss [27]. In addition, the dynamic response of the converter is also degraded in high-order voltage-multiplier circuits.

Resonant converters are also widely applied to achieve a high voltage gain, since the parasitic capacitor or leakage inductor in high turn-ratio transformers can be fully utilized to participate in the resonant process in order to achieve soft-switching. Hence, Zero Current Switching (ZCS) or Zero Voltage Switching (ZVS) can be easily realized during switching transitions [17]-[19]. Therefore, no active clamp circuit or non-dissipative snubber circuit is needed in the converters. As a result, resonant converters usually have simple structures with high power density. However, different resonant converters have different merits and drawbacks. For example, the LC Series Resonant Converter (SRC) has a variety of Continues Current Modes (CCMs) and Discontinues Current Modes (DCMs), and the control system must be carefully designed in order to make sure the converter operates properly in the predetermined mode [19], [28], [29]. In addition, the SRC is hard to regulate the output voltage under light load conditions while the LC Parallel Resonant Converter (PRC) is hard to regulate the output voltage under heavy load conditions [30]. The LLC resonant converter is attractive and shows a lot of unique improvements. However, the design process of an LLC transformer needs a lot of attention to obtain a satisfactory compromise between the leakage and magnetizing inductance [17], [20]. In addition, since the magnetizing inductance is restricted by the inductance ratio and its value is usually not very large, the power loss caused by the circulating current associated with magnetizing inductance takes up a large proportion, especially when the switching frequency is far from the resonant frequency [21]-[23]. Furthermore, under low input voltage situations, there is always a large resonant current through the series resonant capacitor on the primary side of the transformers in SRC, LCC and LLC converters, where more bulky resonant capacitors need to be placed in parallel to reduce the Equivalent Series Resistance (ESR) in order to improve efficiency.

An improved half-bridge LC resonant converter with clamp diodes on the primary side was proposed in [24]. This converter is called a "**LC-DP**" here for the sake of simplicity, which means "**LC** resonant converter with clamp **Diodes** on the **Primary** side". The converter can achieve a high efficiency by setting the converter operating in the DCM. Correspondingly, all of the active switches can realize ZCS during both turn-on and turn-off transitions. The reverse-recovery problems of diodes are also alleviated by the leakage inductor. Using IPOS architectures, modular systems are widely applied in industrial applications for a high voltage output [8], [25], [26]. However, the converter is not very suitable as a high step-up converter, especially under low input voltage conditions. This is due to the fact that the converter is essentially a step-down converter when the turn-ratio is equal to 1. Moreover, the power level of the converter is mainly affected by the input voltage.

For the purpose of finding a high efficiency galvanic step-up converter suitable for the low input voltage field, an improved step-up converter derived from the **LC-DP** converter is proposed in this paper. The proposed converter maintains the advantages of the **LC-DP** and has the following features.

1) By moving resonant loops to the secondary side of the transformer, the current stresses of the resonant capacitors and the clamp diodes are significantly decreased. As a result, the power losses caused by the resonant capacitor ESR and the clamp diodes are decreased.
2) There are no extra power components on the primary side except for the active switches. Therefore, the power loss caused by a large primary-side current can be controlled in the minor range.
3) The active switches can achieve ZCS during both turn-on and turn-off transitions. The reverse-recovery problem of the diodes can be also alleviated by the leakage inductor.
4) There is only one magnetic component in the converter. As a result, the circuit structure is relatively simple.

The rest of this paper is organized as follows. A brief review of the LC-DP converter presented in [8], [24]-[26] is given in Section II. The derivation of the proposed step-up converter and its basic operation principle are presented in Section III. The steady-state operation principle is analyzed in Section IV. The design considerations of the proposed converter are shown in detail in Section V. In Section VI, a prototype with a 35V-42V input and a 400V output is built and experimental results

demonstrating the operation behavior are presented. Some conclusions are given in Section VII.

II. Review of the LC-DP Converter

A schematic of the LC-DP converter is shown in Fig. 1. It can be considered to be an improved LC series resonant converter that has a unique DCM status [8], [24]-[26]. With the clamp diodes D_1 and D_2, the high-order DCM status in the SRC is avoided [28], [29]. Therefore, the control system under the DCM is relatively simple. Meanwhile, the unique DCM status can guarantee that the active switches work under soft-switching conditions during both turn-on and turn-off transitions. The current decline rates for all of the diodes are restricted by the leakage inductor. Therefore, the reverse-recovery problem is significantly alleviated.

The detailed operation principle can be found in [8], [24]-[26]. For the sake of simplicity, only some conclusions and equations are summarized. The capacitors C_1 and C_2 are equal to each other, and C_r denotes their values. They form an equivalent series resonant capacitor with the value $2C_r$. The capacitor C_o is large enough to supply a low impedance path and to filter the output ripple. Therefore, the angular resonant frequency ω_r depends on the leakage inductor L, and the capacitors C_1 and C_2. In the equations that follow, f_s is the switching frequency and f_m is the normalized frequency. V_g is the input voltage. M is the voltage gain. N is the turn-ratio of the step-up transformer. R_0 is the characteristics impedance, and R_L is the load resistor. Q is the quality factor.

$$\omega_r = 2\pi f_r = \frac{1}{\sqrt{2C_r L}} \tag{1}$$

$$R_0 = \sqrt{\frac{L}{2C_r}} \tag{2}$$

$$f_m = \frac{f_s}{f_r} \tag{3}$$

$$Q = \frac{R_L}{R_0} \tag{4}$$

The output voltage is regulated by f_s under a unique DCM. This operation mode requires that f_s must be less than f_r, and that f_s must satisfy the constraint in (5).

$$f_s \le \frac{1}{\frac{2N}{\omega_r M}\sqrt{1-\frac{2M}{N}} + \frac{2}{\omega_r}\arccos\left(\frac{M}{M-N}\right)} \tag{5}$$

Correspondingly, the output power and voltage gain are shown in (6) and (7).

$$P = \frac{1}{2}(C_1 + C_2)V_g^2(2f_s) = 2C_r f_s V_g^2 \tag{6}$$

$$M = \sqrt{2C_r f_s R_L} = \sqrt{\frac{f_m Q}{2\pi}} \tag{7}$$

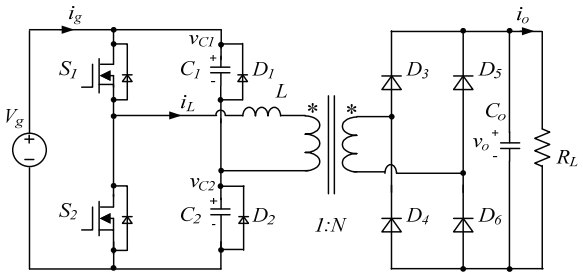


Fig. 1. Main circuit diagram of an LC-DP converter presented in [8], [24]-[26].

The LC-DP converter has the following drawbacks as a high step-up converter.

1) *The Power Loss of the Primary-side Components is High when it Operates under a High Power and a Low Input Voltage:*

In the steady-state operation mode, there are currents flowing through the clamp diodes every switching period. Under the condition of a high power and a low input voltage, the primary-side current is very large, which results in high power loss on the clamp diodes, circuit wire resistance and the ESR of the resonant capacitors.

2) *A Large Turn-ratio is Needed in the LC-DP Converter when it is Applied as a High Step-up Converter:*

The maximum voltage gain for the LC-DP converter is equal to $N/2$. Therefore, the LC-DP is essentially a step-down converter. To realize a high voltage gain, a large turn-ratio is needed, which usually brings a lot of difficulty to the transformer design process. One of the major drawbacks of a high turn-ratio step-up transformer is the high value of the parasitic capacitor on the secondary side. This value reflected to the primary side gives rise to a N^2 times value, which can affect the basic operation principle of the converter [18]. For this reason, the LC resonant process in the LC-DP can be transformed into an LCC resonant process as shown in Fig. 2, where the resonant components are marked with colors.

3) *The Input Voltage V_g Predominantly Affects the Power Level for the LC-DP. Under a Low Input Voltage Situation, the Converter is Hard to Realize a High-power Level Due to the Constraint in (5), Especially as a High Step-up Converter:*

Typical operation regions are illustrated in Fig. 3. Although the LC-DP converter can be considered as a constant power source according to (6), increasing the turn-ratio N can enlarge the possible range of the switching frequency f_s. In addition, the maximum voltage gain is equal to $N/2$. Therefore, the LC-DP needs a high turn-ratio if it works as a high step-up converter. However, as the turn-ratio increases, the operation boundary gradually moves up to the high value range, as shown in Fig. 3. Therefore, the lowest Q value under a certain f_m is also increased. Correspondingly, the lowest R_L value shifts to the high value range because R_0 is fixed in the

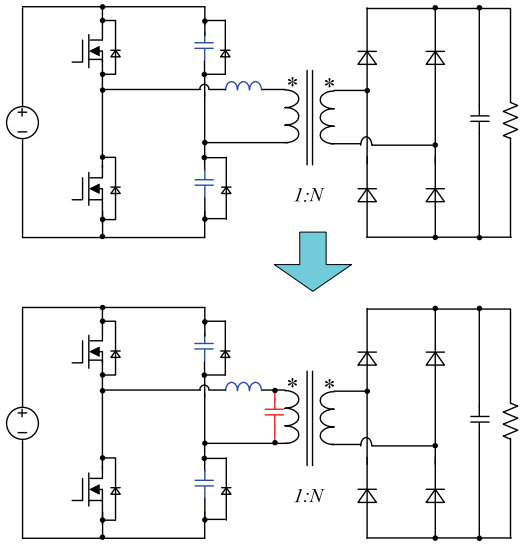


Fig. 2. Parasitic capacitance effects on an LC-DP caused by a high turn-ratio transformer.

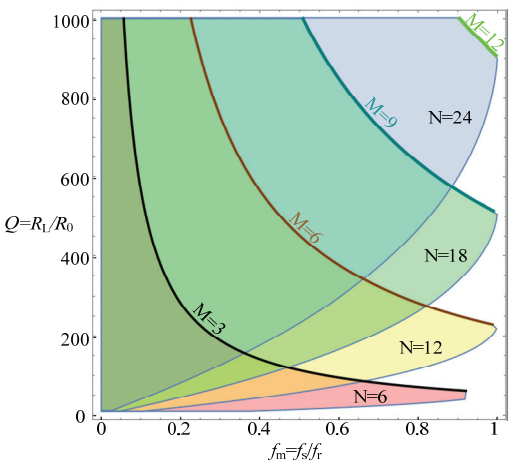


Fig. 3. Typical operation region of an LC-DP converter.

established converter. As a result, if an LC-DP is used to generate an invariable output voltage, the power level under the high turn-ratio condition is lower than that in the low turn-ratio condition. Therefore, the power level for the LC-DP converter is sufficiently decreased by the low input voltage. This situation becomes more and more serious with an increase of the turn-ratio N.

III. Improved Topology and Its Corresponding Operation Principle

A schematic of the proposed converter with clamp diodes on the secondary side is shown in Fig. 4. It can be considered as a derivation from the converter in Fig. 1, which changes the direction of the power flow. For the sake of simplicity, the converter is called "**LC-DS**", which means "**LC** resonant converter with clamp **Diodes** on the **Secondary** side". Therefore, the LC-DS is symmetrical to the LC-DP.

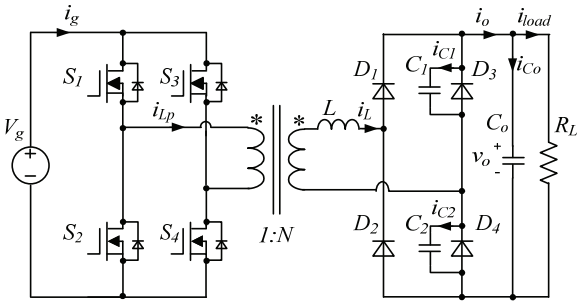


Fig. 4. Main circuit diagram for the proposed LC-DS converter.

The input structure consists of four active switches (S_1-S_4), which forms a full-bridge configuration to fully utilize the input voltage. On the secondary side of the transformer, two rectifier diodes (D_1 and D_2) and two clamp diodes (D_3 and D_4) with paralleled resonant capacitors (C_1 and C_2) form the rectifier stage. The leakage inductor L is illustrated on the secondary side. R_L denotes the load resistor. A large capacitor C_o is placed at the output. As a result, the output voltage contains negligible harmonics of the switching frequency. The resonant process can be determined by the leakage inductor and the two resonant capacitors. N denotes the transformer turn-ratio. The magnetizing inductor is assumed to be large enough. Thus, it is not shown in Fig. 4.

In order to clearly clarify the illustration and analysis, three assumptions are made.

1) All of the component models are ideal and the parasitic parameters are not considered here.
2) The switching dead-time is neglected.
3) The magnetizing inductor L_m is large enough and the magnetizing current is neglected.

The operation modes of the LC-DS converter are illustrated in Fig. 5. The corresponding positive directions are given in Fig. 4. Key waveforms of the converter during steady-state operation are shown in Fig. 6. S_1 and S_2 operate in opposite phases with duty-ratios of 0.5. S_4 operates synchronously with S_1, while S_3 works synchronously with S_2. Here, T_s denotes the switching period.

There are ten operation modes during one switching period as shown in Fig. 6. Only five of the modes are discussed here for the sake of simplicity since the operation process is symmetrical.

Mode I ($t_0<t<t_1$): S_1 and S_4 are switched on, while S_2 and S_3 are switched off. At this time, D_1 conducts. The input of the primary side is V_g. Thus, the equivalent voltage ahead of the leakage inductor L on the secondary side is equal to NV_g. During this stage, the leakage inductor L along with the capacitors C_1 and C_2 participate in the resonant process. The inductor current i_L increases with a sinusoidal shape from zero and flows through D_1. The corresponding current i_{Lp} of the transformer primary side also increases from zero and flows through S_1 and S_4. Therefore, S_1 and S_4 realize the ZCS turn-on process at the instant t_0.

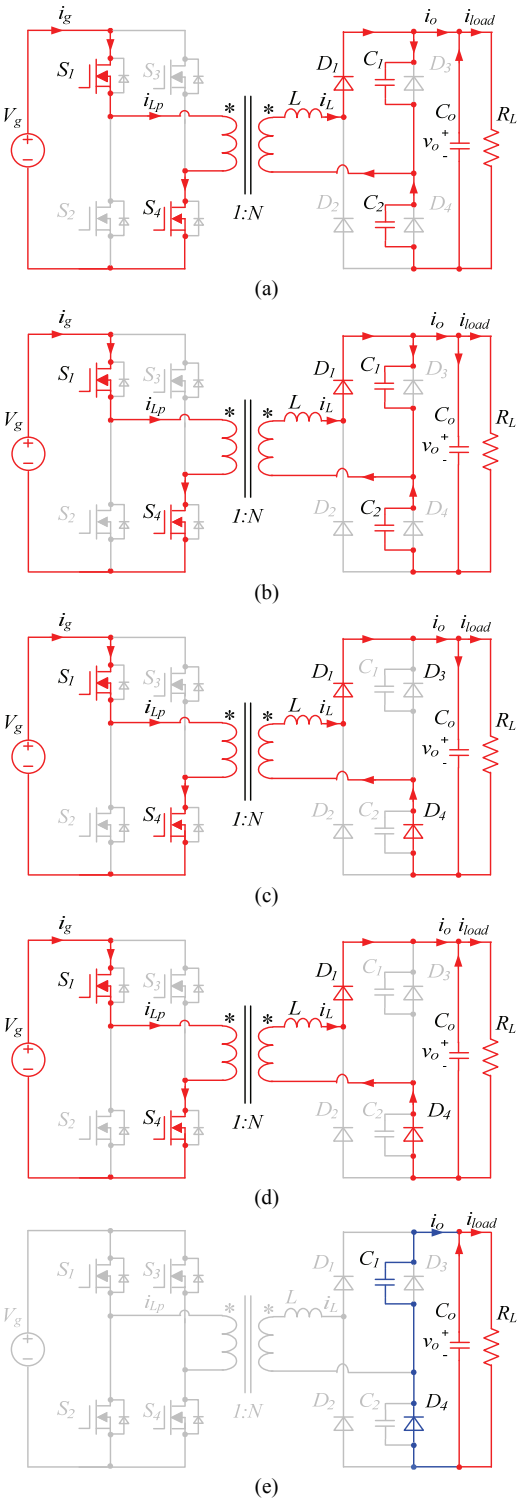


Fig. 5. Equivalent circuits of an LC-DS converter under different operation stages. (a) Mode I (t_0<t<t_1). (b) Mode II (t_1<t<t_2). (c) Mode III (t_2<t<t_3). (d) Mode IV (t_3<t<t_4). (e) Mode V (t_4<t<t_5).

Due to the sufficiently large capacitor C_o, the output port of the converter can be considered as a short circuit during the resonant process. Therefore, the angular resonant frequency ω_r can be defined as (1), where C_r means the value of the resonant capacitors C_1 and C_2. Meanwhile, i_{C1} and i_{C2} can be shown as (8) and (9), where i_o denotes the output current as shown in Fig.4. The absolute values of i_{C1} and i_{C2} are equal to each other. In this stage, this value is always less than the load current i_{load}. Therefore, the output voltage v_o decreases. At the instant t_1, $|i_{C1}|$ and $|i_{C2}|$ are equal to i_{load}. Therefore, v_o gets the minimum value. The characteristic impedance R_0 is still defined as shown in (2). The corresponding stage of Mode I is illustrated in Fig. 5(a).

$$i_{C1} = C_1 \frac{dv_{C1}}{dt} = \frac{1}{2} i_L \tag{8}$$

$$i_{C2} = -i_o = C_2 \frac{dv_{C2}}{dt} = -\frac{1}{2} i_L \tag{9}$$

Mode II (t_1<t<t_2): The inductor current i_L along with the capacitor voltages v_{C1} and v_{C2} remain in the resonant process. Since $|i_{C1}|$ and $|i_{C2}|$ are greater than i_{load}, v_o increases. At instant t_2, v_{C2} decreases to zero, v_{C1} becomes equal to v_o, and the resonant process is suspended. The corresponding stage of Mode II is illustrated in Fig. 5(b).

In both Mode I and Mode II, the converter operates in the resonant process. Therefore, v_{C1}, v_{C2} and i_L can be expressed as follows, where V_o means the DC value of the output voltage:

$$v_{C1}(t) = NV_g(1-\cos(\omega_r t)) \tag{10}$$

$$v_{C2}(t) = V_o - NV_g(1-\cos(\omega_r t)) \tag{11}$$

$$i_L(t) = \frac{NV_g}{R_0}\sin(\omega_r t) \tag{12}$$

$$i_o(t) = \frac{1}{2} i_L(t) \tag{13}$$

Mode III (t_2<t<t_3): At the instant t_2, v_{C2} decreases to zero and the clamp diode D_4 conducts. The capacitor voltage v_{C1} is clamped by the output voltage v_o. Therefore, the inductor current i_L flows through D_4 and D_1 simultaneously. Under the effect of the output voltage v_o, the inductor current i_L decreases linearly. The decline rates of i_L, i_{D1} and i_{D4} are restricted by the leakage inductor. Before the instant t_3, i_L is greater than i_{load}. As a result, v_o continues increasing. At the instant t_3, i_L is equal to i_{load}. Therefore, v_o reaches the maximum value. The corresponding stage of Mode III is illustrated in Fig. 5(c).

Mode IV (t_3<t<t_4): i_L continues decreasing linearly. Since i_L is less than the load current i_{load}, C_o is discharged and v_o decreases. At the instant t_4, i_L decreases to zero and D_1 turns off. The corresponding stage of Mode IV is illustrated in Fig. 5(d).

In both Mode III and Mode IV, the inductor current decreases linearly. The diodes D_1 and D_4 conduct simultaneously. Therefore, the following equations can be obtained:

$$v_{C1}(t) = v_o \tag{14}$$

$$v_{C2}(t) = 0 \tag{15}$$

$$i_L(t) = i_L(t_2) + \frac{1}{L}(NV_g - V_o)(t - t_2) \tag{16}$$

$$i_o(t) = i_L(t) \tag{17}$$

Mode V ($t_4<t<t_5$): S_1 and S_4 are still switched on. However, there is no current flowing through the transformers in both the primary side and the secondary side. Because the output capacitor C_o supplies the load resistor, v_o decreases. Due to the diode D_4, v_{C1} is clamped by the output voltage v_o, Therefore, in theory, there is still a tiny current flowing through D_4 to supply the load. However, it is important to point out that the output capacitor C_o is much larger than the resonant capacitor C_1. Hence, almost a full load current is supplied by the output capacitor C_o. The current through D_4 and C_1 is much smaller than that through C_o. As a result, it can be neglected. The path of the tiny current is illustrated by a blue line in Fig. 5(e). At the instant t_5, S_1 and S_4 are switched off under ZCS while S_2 and S_3 turn on under ZCS since there is no current on the primary side of the transformer. The inductor current i_L begins to increase inversely and C_2 starts to be charged. D_4 turns off with a very tiny current. The corresponding stage of Mode V is illustrated in Fig. 5(e).

From t_5 to t_{10}, the operation process is symmetrical. Therefore, it is not discussed in this paper.

IV. Steady-State Analysis of the LC-DS Converter Under the DCM

Under the operation principle mentioned above, a steady-state analysis of the LC-DS is discussed. From t_0 to t_2 (Mode I and Mode II), the inductor current integration A_1 can be expressed as (18), where t_0 is set equal to zero.

$$\begin{aligned} A_1 &= \int_{t0}^{t2} i_L dt \\ &= \int_{t0}^{t2} \frac{NV_g}{R_0}\sin(\omega_r t)dt \\ &= \frac{NV_g}{\omega_r R_0}(1-\cos(\omega_r t_2)) \end{aligned} \tag{18}$$

From t_2 to t_4 (Mode III and Mode IV), the inductor current integration A_2 is given as (19).

$$\begin{aligned} A_2 &= \int_{t2}^{t4} i_L dt \\ &= \frac{1}{2}\times(t_4-t_2)\times\frac{NV_g}{R_0}\sin(\omega_r t_2) \end{aligned} \tag{19}$$

Since v_{C1} is equal to v_o at the instant t_2, equation (20) can be derived from (10). Here the DC value V_o is used under the assumption of a large output capacitor.

$$v_{C1}(t_2) = NV_g(1-\cos(\omega_r t_2)) = V_o \tag{20}$$

Therefore, A_1 can be simplified as follows:

$$A_1 = \frac{V_o}{\omega_r R_0} \tag{21}$$

In addition, $i_L(t_4)$ is equal to zero. Therefore, equation (22) can be derived from (16).

$$i_L(t_4) = i_L(t_2) + \frac{1}{L}(NV_g - V_o)(t_4 - t_2) = 0 \tag{22}$$

According to equation (20) and (22), A_2 can be simplified as follows:

$$\begin{aligned} A_2 &= \frac{1}{2}\times\frac{L}{V_o - NV_g}\times\left(\frac{NV_g}{R_0}\right)^2\times(1-\cos^2(\omega_r t_2)) \\ &= \frac{1}{2}\times\frac{L}{V_o - NV_g}\times\frac{V_o}{R_0^2}(2NV_g - V_o) \end{aligned} \tag{23}$$

Therefore, the average inductor current I_{Lavg} from t_0 to t_5 can be expressed as follows:

$$\begin{aligned} I_{Lavg} &= \frac{2}{T_s}(A_1 + A_2) \\ &= \frac{2V_o f_s}{\omega_r R_0} + \frac{L}{V_o - NV_g}\times\frac{V_o}{R_0^2}(2NV_g - V_o)f_s \end{aligned} \tag{24}$$

From t_0 to t_5, which is equal to half of a switching period ($T_s/2$), the following equations can be derived, where M is the voltage gain V_o/V_g.

$$NV_g I_{Lavg} = \frac{V_o^2}{R_L} \tag{25}$$

$$\frac{2f_s}{\omega_r R_0} + \frac{Lf_s(2N-M)}{R_0^2(M-N)} = \frac{M}{NR_L} \tag{26}$$

Finally, the voltage gain M and the power P can be given as follows, where the quality factor Q is still defined as (4) and the normalized frequency f_m is defined as (3).

$$\begin{aligned} M &= \frac{V_o}{V_g} \\ &= N\left(2C_r R_L f_s + 1\right) \\ &= \frac{N}{2\pi}\left(f_m Q + 2\pi\right) \end{aligned} \tag{27}$$

$$\begin{aligned} P &= \frac{N^2 V_g^2 (2C_r R_L f_s + 1)^2}{R_L} \\ &= \frac{N^2 V_g^2}{R_L}\left(\frac{1}{2\pi} f_m Q + 1\right)^2 \end{aligned} \tag{28}$$

As shown in Fig. 6, the LC-DS operates in the DCM. All of the active switches (S_1~S_4) guarantee ZCS during both turn-on and turn-off transitions. The current decline rate of the rectifier diodes (D_1 and D_2) and the clamp diodes (D_3 and D_4) are limited by the leakage inductor. Hence, the reverse-recovery problems are sufficiently alleviated. Under this mode, the voltage gain M has a linear relationship with the normalized frequency f_m as shown in (27). Therefore, the output voltage V_o can be linearly regulated through f_s under the DCM.

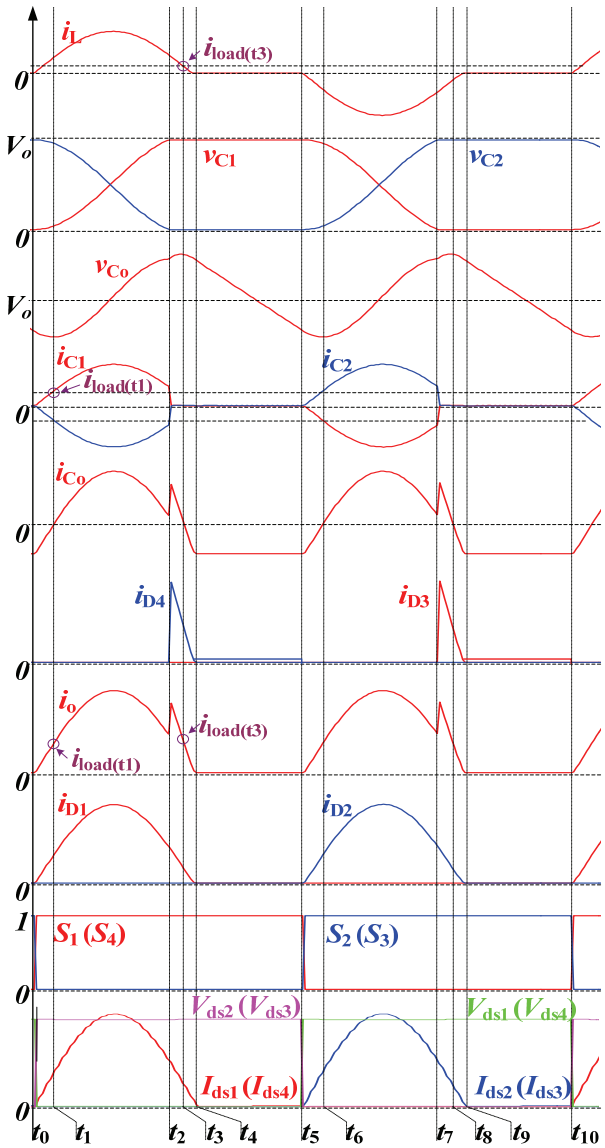


Fig. 6. Waveforms of an LC-DS converter.

V. Design Considerations for the LC-DS Converter

A. Design Principle for the DCM and Soft-switching

From Fig. 6 it is clear that the LC-DS converter operates in the DCM. In addition, all of the MOSFETs naturally realize the ZCS characteristics during both turn-on and turn-off transitions. In this case, the switching frequency f_s must be lower than the resonant frequency f_r. Moreover, the duration from t_0 to t_4 must be less than half of a switching period, to ensure that the inductor current i_L can totally decrease to zero before S_2 and S_3 are switched on. Therefore, the following inequality must be satisfied as the constraint.

$$\frac{T_s}{2} > t_4 - t_0 \tag{29}$$

If t_0 is set equal to zero, t_2 can be found as shown in (30) according to (20).

$$t_2 = \frac{1}{\omega_r}\arccos\left(1-\frac{M}{N}\right) \tag{30}$$

From (12), (22) and (30), the instant t_4 can be simplified as follows:

$$\begin{aligned} t_4 &= \frac{L}{(V_o - NV_g)}\frac{NV_g}{R_0}\sin(\omega_r t_2) + \frac{1}{\omega_r}\arccos\left(1-\frac{V_o}{NV_g}\right) \\ &= \frac{1}{\omega_r\left(\frac{M}{N}-1\right)}\sqrt{1-\cos^2(\omega_r t_2)} + \frac{1}{\omega_r}\arccos\left(1-\frac{M}{N}\right) \\ &= \frac{\sqrt{M(2N-M)}}{\omega_r(M-N)} + \frac{1}{\omega_r}\arccos\left(1-\frac{M}{N}\right) \end{aligned} \tag{31}$$

According to (29), the following inequality must be satisfied.

$$\frac{T_s}{2} > \frac{\sqrt{M(2N-M)}}{\omega_r(M-N)} + \frac{1}{\omega_r}\arccos\left(1-\frac{M}{N}\right) \tag{32}$$

Inequality (32) can be further simplified as (33), where the left part of the inequality is defined as the first constraint $g_1(f_m)$.

$$g_1(f_m) = \frac{2}{Q}\sqrt{1-\left(\frac{1}{2\pi}f_m Q\right)^2} + \frac{f_m}{\pi}\arccos\left(-\frac{1}{2\pi}f_m Q\right) < 1 \tag{33}$$

In addition, the square root in (33) must be a real number. As a result, (34) must be satisfied. This is the second constraint, which is defined as $g_2(f_m)$.

$$g_2(f_m) = \frac{1}{2\pi}f_m Q < 1 \tag{34}$$

Inequality (34) can be transformed into another expression according to (27) as follows:

$$2C_r f_s V_o^2 < \frac{V_o^2}{R_L} \tag{35}$$

The left part of (35) can be considered as the exchanging power in the equivalent resonant capacitor $2C_r$ during half of a switching period and it is defined as P_{Cr}. The right part of (35) is equal to the output power P of the converter. Thus, (36) is equivalent to (35) and (34). Therefore, $g_2(f_m)$ is actually the ratio of P_{Cr} to P. According to (27), $g_2(f_m)$ can be shown in another expression, which is given in (37). It is clear that if the voltage gain is fixed, $g_2(f_m)$ is simultaneously fixed.

$$P_{Cr} < P \tag{36}$$

$$\begin{aligned} g_2(f_m) &= \frac{P_{Cr}}{P} \\ &= \frac{M}{N} - 1 \end{aligned} \tag{37}$$

From (35) and (37), it is clear that the exchanging power of the resonant capacitors needs to be totally transferred to the load as shown in Fig. 6. This process coincides with the

duration from t_0 to t_2. After that, v_{C1} and v_{C2} maintain constant values, and the energy stored in the inductor L is transferred to the load until t_4. From t_4 to t_5, the load is supplied entirely by the filter capacitor C_o.

If $g_2(f_m)$ is equal to 1, the duration from t_2 to t_4 is null according to (31) and (37). Under this condition, the clamp diodes (D_3 and D_4) have no chance to conduct and the converter works as the equivalent series resonant converter. Therefore, the converter is equivalent to a traditional LC series resonant converter, which operates in the "type 1" of odd discontinuous current modes defined in [28], [29]. The output voltage cannot be regulated and is always equal to $2NV_g$. For the purpose of regulating the output, the LC-DS converter should be designed under the conditions that $g_1(f_m)$ and $g_2(f_m)$ are both less than 1.

According to (27) and (34), the maximum output voltage is equal to $2Vg$ if N is equal to 1. Therefore, the LC-DS converter is essentially a step-up converter.

It should be pointed out that MOSFETs can naturally obtain ZCS turn-on and turn-off when the converter operates under the DCM, as described in Fig. 5 and Fig. 6. Therefore, the sufficient and necessary conditions for the realization of soft-switching are the same as the conditions for the realization of DCM, as given in (33) and (34), which means that $g_1(f_m)$ and $g_2(f_m)$ must be simultaneously less than one.

B. Voltage and Current Stress of the Diodes D_1-D_4

From Fig. 4, it is concluded that the voltage stress of the rectifier diodes D_1 and D_2 is equal to V_o. The voltage applied across D_3 and D_4 is also equal to V_o.

According to Fig. 6 and (12), the current stress of the diodes D_1 and D_2 can be expressed as shown in (38). The current stress of the diodes D_3 and D_4 is equal to $i_L(t_2)$, which is expressed in (39) according to (12) and (20).

$$i_{D1,D2\_\max} = \frac{NV_g}{R_0} \tag{38}$$

$$\begin{aligned} i_{D3,D4\_\max} &= i_L(t_2) \\ &= \frac{NV_g}{R_0}\sin(\omega_r t_2) \\ &= \frac{NV_g}{R_0}\sqrt{1-(1-\frac{M}{N})^2} \end{aligned} \tag{39}$$

C. Voltage and Current Stress of the Active Switches S_1-S_4

From the illustrations in Section III, it is clear that all of the active switches (S_1- S_4) have the same voltage and current stress. The voltage stress is equal to the input voltage V_g. The current stress is equal to N^2V_g/R_0 according to (12) and Fig. 6.

D. Voltage and Current Stress of the Resonant Capacitors C_1-C_2

According to Fig. 6, it can be concluded that the voltage stress of the resonant capacitors is equal to the output voltage V_o. Meanwhile, the current stress of the resonant capacitors can be given as follows:

$$i_{C1,C2\_\max} = \frac{NV_g}{2R_0} \tag{40}$$

E. Design Considerations for the Transformer Turn-ratio

According to (27) and (34), the maximum voltage gain M is equal to $2N$. However, voltage gain M must be designed to be less than $2N$ so the output voltage can be regulated by the switching frequency f_s. Hence, in the practical design process, the transformer turn-ratio N can be selected close to $M/2$, which means that $g_2(f_m)$ is close to one and the value of $i_L(t_2)$ approaches zero. Therefore, the conduction loss of the diodes D_3 and D_4 can be decreased significantly according to (39).

F. Restrictions of the Switching Frequency f_s and Selection of the Resonant Components

As shown in (1) and (2), the leakage inductor L and the resonant capacitors C_1 and C_2 determine the value of the resonant frequency f_r and the characteristic impedance R_0. In order to set the converter operating under the DCM, the constraints functions $g_1(f_m)$ and $g_2(f_m)$ must be less than 1. Therefore, there exist boundary conditions to restrict the normalized frequency f_m and the selection of the resonant parameters. Analytic solutions for the restriction of f_m are hard to obtain because $g_1(f_m)$ contains a square root part and an inverse trigonometric part. Therefore, the iteration method and illustration are presented here in order to find the boundary conditions. A flowchart of the iteration method is shown in Fig. 7.

G. Selection of the Output Capacitor C_o

The output capacitor C_o is used as the filter capacitor and its value must be large enough to supply a low impedance path during the resonant process. Under this assumption, it can be considered that all of the ac components of the output current i_o are filtered by the output capacitor. Therefore, the load current i_{load} can be considered as a constant value.

However, as shown in Fig. 6, the output capacitor current i_{Co} has the characteristics of piecewise polynomial functions, which bring a lot of difficulty to ripple calculations. As discussed above, in order to reduce the conduction loss of D_3 and D_4, the voltage gain M can be designed close to $2N$. In this way, the current waveform of i_{Co} can be considered to be sinusoidal in shape from t_2 to t_4 as shown in Fig.8. The output voltage ripple can be calculated based on waveforms from t_0 to t_5, which is equal to half of a switching period. Therefore, the piecewise polynomial functions for i_{Co} can be simplified as shown in (41), where I_{load} means the DC value of the load current.

$$i_{Co}(t) = \begin{cases} \dfrac{NV_g}{2R_0}\sin(\omega_r t) - I_{load} & (t_0 < t < t_4) \\ -I_{load} & (t_4 < t < t_5) \end{cases} \tag{41}$$

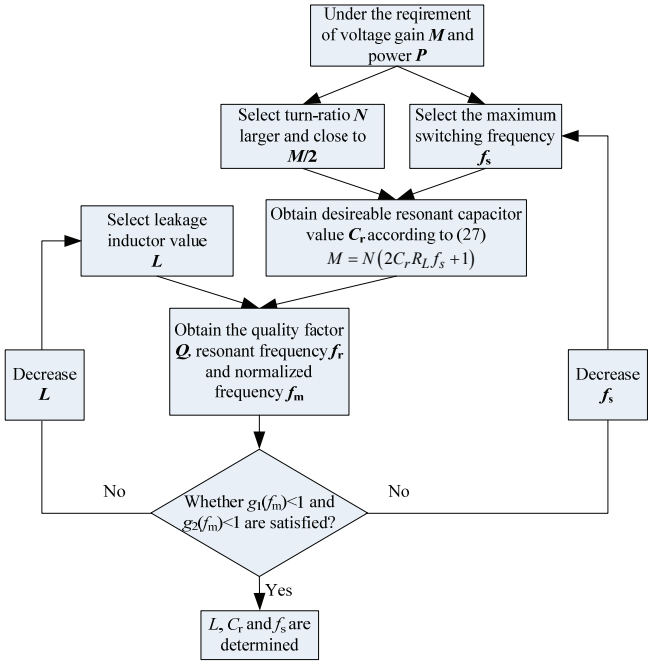


Fig. 7. Iteration method for the design process of L, C_r and f_s.

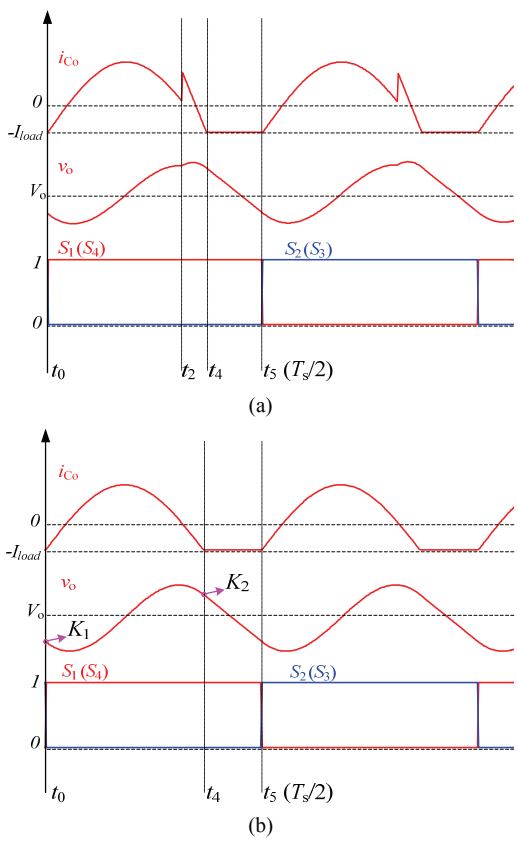


Fig. 8. Waveform approximation process when M is close to $2N$. (a) Key waveforms. (b) Approximate key waveforms.

Hence, the capacitor voltage v_o can be expressed as shown in (42). K_1 and K_2 denote different initial values corresponding to Fig. 8. The output voltage ripple can be expressed as shown in (43). Therefore, the output capacitor C_o can be selected under a desirable ripple range.

$$v_o(t)=\begin{cases}\dfrac{NV_gC_r}{C_o}(1-\cos(\omega_r t))-\dfrac{I_{load}}{C_o}t+K_1 & (t_0<t<t_4)\\ -\dfrac{I_{load}}{C_o}t+K_2 & (t_4<t<t_5)\end{cases} \tag{42}$$

$$v_{o\_ripple}=\frac{2NV_gC_r}{C_o}\cos(\arcsin\frac{2I_{load}R_0}{NV_g})+\frac{I_{load}}{C_o}(\frac{2}{\omega_r}\arcsin\frac{2I_{load}R_0}{NV_g}-\frac{1}{\omega_r}\pi) \tag{43}$$

Due to the possibility that an electrolytic capacitor is used as the output capacitor, ESR is considered here and it is denoted by R_{ESR}. Therefore, the maximum ripple range can be estimated by equation (44).

$$v_{o\_ripple}=\frac{2NV_gC_r}{C_o}\cos(\arcsin\frac{2I_{load}R_0}{NV_g})+\frac{I_{load}}{C_o}(\frac{2}{\omega_r}\arcsin\frac{2I_{load}R_0}{NV_g}-\frac{1}{\omega_r}\pi)+\frac{NV_gR_{ESR}}{2R_0} \tag{44}$$

H. Performance Comparisons

When compared with (3), the LC-DS converter has two more freedom-degrees to extend the power level, i.e. R_L and N. From (28) it is clear that although the numerator and denominator both contain R_L, the power P is always larger than $(NV_g)^2/R_L$. Therefore, with a decrease of R_L (the load becomes heavier), the power level can be increased. In addition, the power level can be increased by selecting a large turn-ratio N. As explained in Section II, increasing the turn-ratio N will decrease the power level in the LC-DP. However, this phenomenon is avoided in the proposed LC-DS converter, because the constraint inequalities (33) and (34) have no relationship with the turn-ratio N. Therefore, when compared with the LC-DP, the power level can be extended by the LC-DS in high step-up applications.

As explained in Section II, the parasitic capacitance of a step-up transformer reflected to the primary side increases with the growth of the turn-ratio N. This large value may affect the basic operation principle in an LC-DP under high turn-ratio conditions. However, this phenomenon is sufficiently alleviated in the LC-DS by moving the resonant loops to the secondary side. When compared with the LC-DP, the transformer parasitic capacitance has little effect on the LC resonant process because the value reflected to the secondary side is much less than that reflected to the primary side.

Moreover, in the high step-up condition, the secondary-side resonant loops withstand less current stress when compared with primary-side resonant loops. Therefore, the power loss caused by the clamp diodes and ESR of the resonant capacitors in an LC-DS converter is less than that in an LC-DP converter.

TABLE I
PERFORMANCE COMPARISON

	LC-DS	Converter in [20]	Converter in [11]	Converter in [16]
Active switch number	4	4	1	6
Diode number	4	2	7	2
Capacitor number	3	4	6	5
Inductor number	Transformer leakage inductor	2 (1 can be integrated in transformer)	Transformer leakage inductor	3 (1 can be integrated in transformer)
Transformer number	1	1	1	1
Minimum number of main circuit components	12	12	15	16
Pulse modulation mode	PFM	PFM	PWM	PWM
Driver position	Primary-side	Primary-side	Primary-side	Primary and Secondary sides
Voltage stress of primary-side switches	S_1-S_4:V_g	S_1- S_4:V_g	S_1, D_1, D_2: >V_g	S_1- S_4: >V_g
Voltage stress of secondary-side switches	D_1-D_4:V_o	D_1, D_2:V_o	D_3-D_7: <V_o/2	D_1, D_2, S_5, S_6: V_o/2
Peak/RMS value of transformer current	High	High	Middle	Low
Soft-switching realization	S_1-S_4: ZCS on&off D_1-D_4: ZCS off	S_1-S_4: ZVS on D_1, D_2: ZCS off	S_1:ZCS on & ZVS off D_1-D_3, D_6: ZCS off	S_1-S_6: ZVS on D_1, D_2: ZCS off
Transformer complexity	Low	High	High	Low

In addition, the parasitic capacitance of the transformer is mainly composed of interlayer capacitance and inter-turn capacitance in the windings. To realize the same voltage gain, the turn-ratio N can be significantly reduced in the LC-DS when compared with the LC-DP. Therefore, the parasitic capacitance in the LC-DS is much smaller than that in the LC-DP. Therefore, the LC-DS converter is suitable as a step-up converter for low input applications.

In order to make design trade-off and topology selection in engineering applications, the LC-DS is compared with some other state-of-the-art topologies. Comparison results are summarized in Table I.

The LC-DS and the converter in [20] have higher Peak/RMS values of the transformer current than PWM type converters because of the resonant operation mode. Nevertheless, due to the easy realization of soft-switching under the PFM control, they need fewer components than PWM type converters, where active clamp circuits or a non-dissipative snubber need to be implemented into the PWM type converters in order to realize soft-switching. In addition, the converter in [16] needs both primary-side and secondary-side drivers, which increase the complexity of the circuit design. Meanwhile, the voltage stresses of the primary-side switches in the LC-DS are also lower than those in [11] and [16]. When compared with the converter in [20], the transformer of the LC-DS is very simple because there is no constraint relationship between the leakage inductance and the magnetizing inductance. Therefore, the LC-DS is easy to implement.

VI. EXPERIMENTAL VERIFICATION

A 500W prototype of the LC-DS converter is built to verify the theoretical analysis. The input voltage range is from 35V to 42V and the output voltage is 400V. The voltage gain varies from 11.43 to 9.52. The output ripple is designed to be less than 1% of the nominal value of the output voltage.

TABLE II
MAIN CIRCUIT PARAMETERS OF THE LC-DS

Parameter	Symbol	Specification
Input voltage	V_g	35V-42V
Output voltage	V_o	400V
Leakage inductor	L	69.2μH
Magnetizing inductor	L_m	57.4mH
Resonant capacitor value	C_1, C_2	30nF
Resonant capacitor ESR	R_{C1_ESR}, R_{C2_ESR}	33.3mΩ
Resonant frequency	f_r	78.1kHz
Output capacitor	C_o	530μF
Output capacitor ESR	R_{o_ESR}	210mΩ
Transformer turn-ratio	1:N	10:60

To reduce the conduction loss of the clamp diodes according to (39), the maximum voltage gain M is designed close to 2N. Hence, N is selected to be equal to 6. Therefore, $g_2(f_m)$ is equal to 90% under a 35V input. Meanwhile, it is equal to 59% under a 42V input, according to (37).

The main circuit parameters of the LC-DS prototype are determined as shown in Table II corresponding to Fig. 4. The transformer is made up by combining two EE55 ferrite cores to guarantee a large magnetizing inductor. The leakage inductor L is 69.2μH and the magnetizing inductor is 57.4mH. Both of them are measured on the secondary side. The magnetizing inductor is sufficiently large when compared with the leakage inductor. So the magnetizing current can be

TABLE III
Q-F_M RANGE UNDER THE CONSTRAINTS OF G_1 AND G_2 WITH A 400V OUTPUT

P(W)	Q	$R_L(\Omega)$	f_m
500	9.42	320	0-0.666
450	10.47	356	0-0.599
400	11.78	400	0-0.533
350	13.46	457	0-0.466
300	15.70	533	0-0.400
250	18.85	640	0-0.333
200	23.56	800	0-0.266

neglected. IRFP4568 MOSFETs are applied as the active switches, and DSEI60-06A diodes are used for both the rectifier and clamp diodes. Multiple Panasonic 10-nF/1600-Vdc film capacitors are employed in parallel as resonant capacitors, the ESR of which is 100mΩ according to the manufacture's datasheet. A 560-μF/450-Vdc aluminum electrolytic capacitor is employed as the output capacitor. To be more accurate, the aluminum electrolytic capacitor is measured by an LCR meter. The equivalent capacitor value of aluminum electrolytic capacitor is denoted by C_o, while its ESR is denoted by R_{o_ESR}.

In order to fully demonstrate the theoretical analysis, a prototype with power range from 200W to 500W was designed in the DCM presented in Section III. The output voltage is regulated by the switching frequency based on (27). Table III presents the possible range of the normalized frequency f_m under the condition of (33) and (34) corresponding to different Q values. As discussed in Section V, the constraints $g_1(f_m)$ and $g_2(f_m)$ must be less than 1. In order to find the boundary conditions between f_m and Q, the operation region based on the parameters in Table II is illustrated in Fig. 9, where the colorful lines correspond to different gain values.

Corresponding to power range from 200W to 500W with a 400V output, the load resistor R_L varies from 800Ω to 320Ω. According to (2), R_0 is 33.96. From (4) it can be concluded that quality factor Q varies from 23.56 to 9.42.

On the basis of (27), the relationship between M and f_m is illustrated in Fig. 10, where the colorful lines correspond to different quality factors. Under the requirement of a 400V output, the desirable voltage gain is 11.43 (35V input) and 9.52 (42V input), respectively.

Therefore, two operation tracks for the LC-DS ranging from 200W to 500W are illustrated by arrow lines, which correspond to voltage gains of 11.43 and 9.52, respectively.

There are four operation points (A~D) marked in Fig. 10, which determine the operation region (covered in light blue) for the LC-DS prototype. Point A stands for the operation point with a 35V input and 200W of power, while B stands for the operation point with a 35V input and 500W of power. Similarly, C corresponds to a 42V input and 200W of power, while D corresponds to a 42V input and 500W of power.

On one hand, if the converter is operating under closed-loop control and a load step occurs, that means the quality factor Q

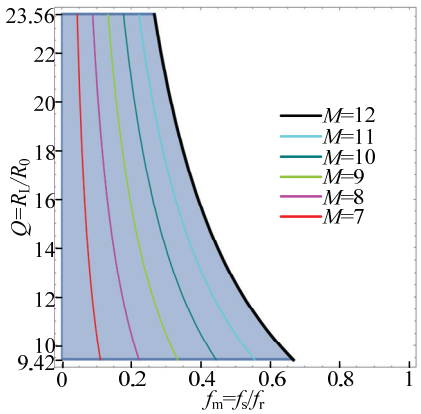


Fig. 9. Restriction region of Q-f_m.

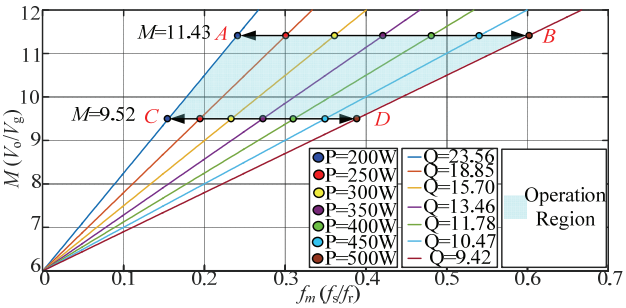


Fig. 10. Operation region of the prototype and a plot diagram of M-f_m.

changes and the voltage gain is kept constant, the steady-state operation point of Fig. 10 moves horizontally. For example, under the 35V input and 400V output condition, if a load step from 200W to 500W occurs, the operation point moves from A to B.

On the other hand, if the converter is operating under closed-loop control and the input voltage varies, that means the quality factor is kept constant but voltage gain changes. Thus, operation point moves along with a certain color line. For example, under the 200W power condition, if the input voltage varies from 35V to 42V, the operation point moves from A to C along with the blue line, which corresponds to a Q value of 23.56.

According to Fig. 10, the theoretical normalized frequency f_m varies from 0.24 to 0.60 under a 35V input. Meanwhile, it varies from 0.16 to 0.39 under a 42V input. Therefore, the theoretical switching frequency varies from 12.2kHz to 47.1kHz. In practical operation, the switching frequency is higher than the theoretical result due to power loss. Below this frequency range, the converter can operate with a simple PWM control at a constant switching frequency. The output is regulated by decreasing the duty-ratio when the load resistor further increases. However, this is not the main purpose of this paper and it is not discussed here.

Experimental waveforms are shown in Fig. 11-Fig. 15. All of the MOSFETs guarantee ZCS during both turn-on and turn-off transitions. The diode reverse-recovery problems are significantly alleviated because the current decline rate is

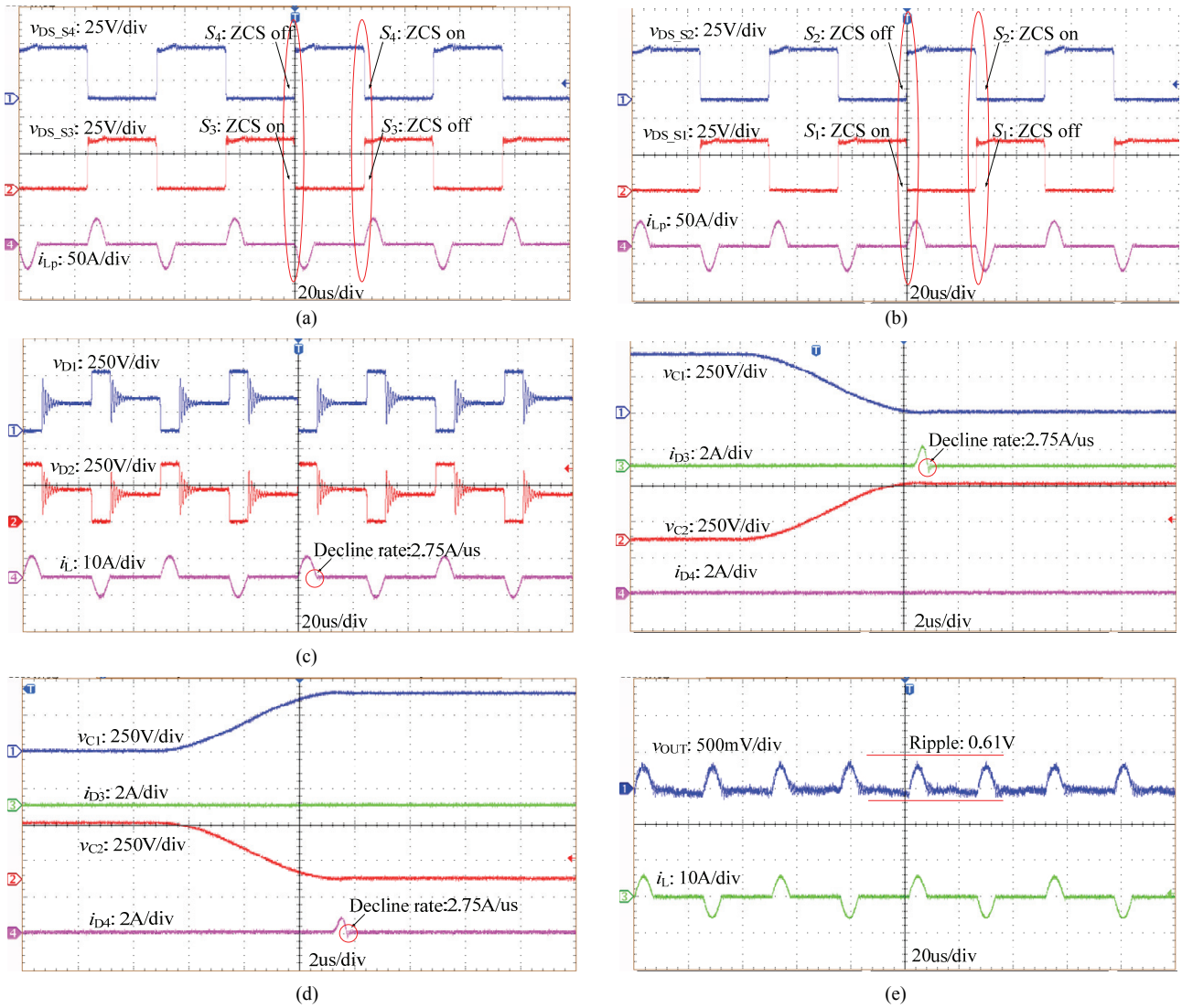


Fig. 11. Light load experimental waveforms (V_g=35V, V_o=400V, P=200W). (a) Drain-source voltage of S_3 and S_4, and the primary-side current i_{Lp}. (b) Drain-source voltage of S_1 and S_2, and the primary-side current i_{Lp}. (c) Voltage of D_1 and D_2, and the secondary-side current i_L. (d) Current of D_3 and D_4, and the voltage of C_1 and C_2. (e) Output voltage ripple, and the secondary-side current i_L.

TABLE IV
VOLTAGE RIPPLE OF THEORETICAL AND MEASURED RESULTS

Operation conditions	Theoretical ripple	Measured ripple
V_g=35V, P=200W	0.67V	0.61V
V_g=35V, P=500W	0.66V	0.6V
V_g=42V, P=200W	0.8V	1V
V_g=42V, P=500W	0.8V	1.1V

restricted by the leakage inductor. According to (22), the theoretical decline rate is 2.75A/μs under a 35V input, and 2.14A/μs under a 42V input, respectively. The output ripple is also measured and shown in Table IV. It is clear that the practical and computed values have good accordance with each other when the input voltage is 35V, and the voltage gain M is close to 2N. Ripple estimation error increases when M is far away from 2N.

It should be noted that there is a high-frequency ringing in the v_{D1} and v_{D2} waveforms as shown in Fig. 11(c)-Fig. 14(c). This is caused by the parasitic capacitance in the diodes D_1 and D_2. When the current i_L decreases to zero, the leakage inductor and parasitic capacitance of the rectifier diodes (D_1 and D_2) form high-frequency resonant loops. As a result, the ringing appears. In addition, there is a high-frequency ringing in i_{D3} and i_{D4} as shown in Fig. 13(d)-Fig. 14(d). This is caused by the parasitic inductance of the wire in series with the clamp diodes, where the wire length must be enough for a current probe to measure i_{D3} and i_{D4}. In addition, experimental results on the dynamic response of the prototype are given in Fig. 15. A simple proportional-integral controller is applied to achieve the closed-loop system. This is based on the relationship between f_s and v_o given in (27).

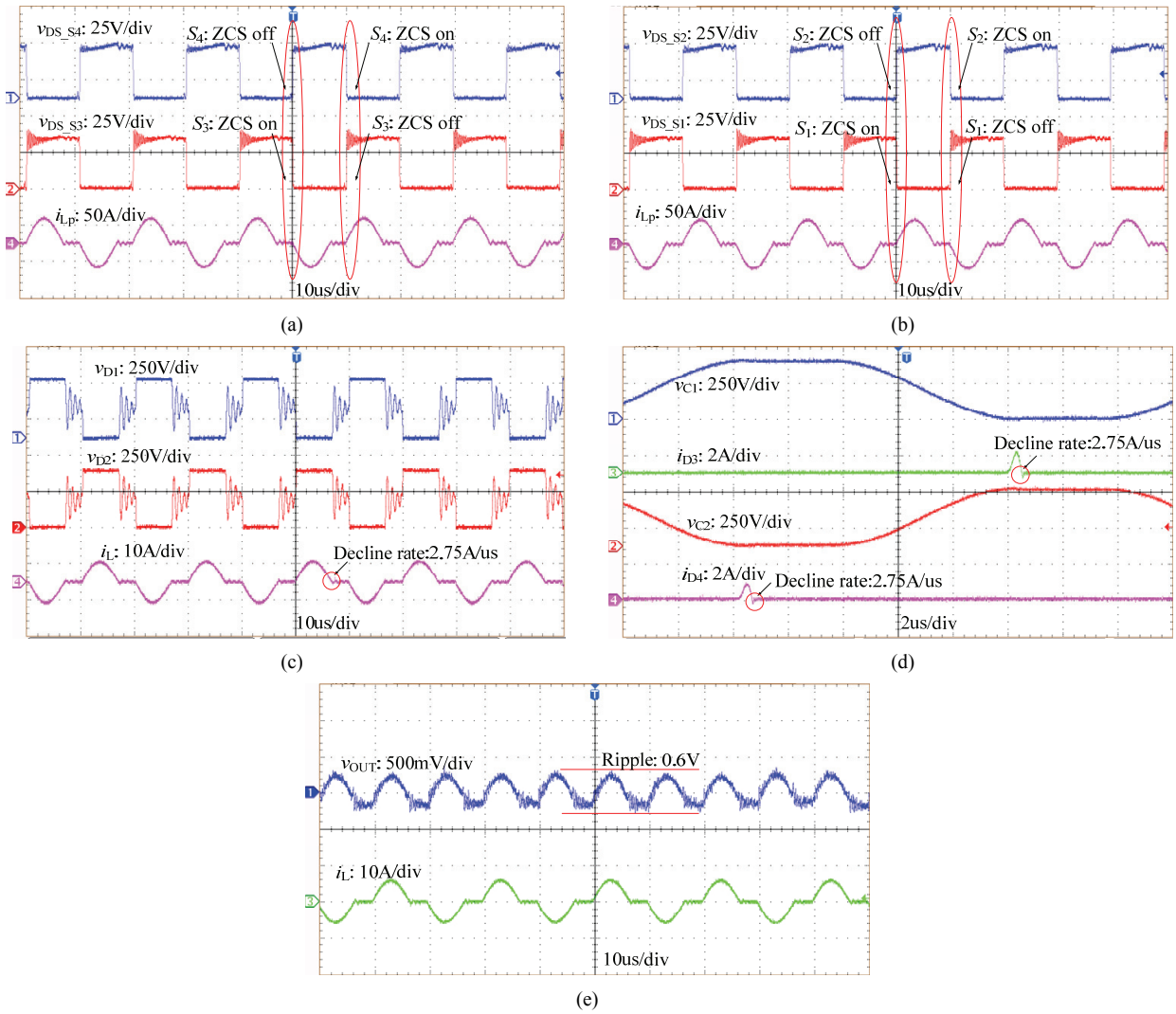


Fig. 12. Nominal power experimental waveforms (V_g=35V, V_o=400V, P=500W). (a) Drain-source voltage of S_3 and S_4, and the primary-side current i_{Lp}. (b) Drain-source voltage of S_1 and S_2, and the primary-side current i_{Lp}. (c) Voltage of D_1 and D_2, and the secondary-side current i_L. (d) Current of D_3 and D_4, and the voltage of C_1 and C_2. (e) Output voltage ripple, and the secondary-side current i_L.

It should be pointed out that there is always a trade-off between the transformer volume and the magnetizing inductor value. As discussed before, the magnetizing current can be omitted if the magnetizing inductor is large enough. However, there is always some magnetizing current in the transformer. If a small transformer is selected to save space, a large magnetizing current induces more power loss in the transformer and decreases efficiency. Meanwhile, the turn-off transitions of the MOSFETs can no longer be considered as a ZCS turn-off process. Therefore, the maximum value of the magnetizing current must be controlled.

This value can be computed according to equation (45). Here, L_m denotes the secondary-side magnetizing inductor, i_{Lm} denotes secondary-side magnetizing current, and i_{Lmp} denotes the primary-side magnetizing current.

$$i_{Lmp\_\max} = N i_{Lm\_\max} = \frac{N^2 V_g}{4 f_s L_m} \tag{45}$$

In the prototype, the maximum value of i_{Lmp} is designed to be less than 600mA. The theoretical minimum value of L_m is 51.6mH according to (45). Therefore, two EE55 ferrite cores are selected in parallel to provide the magnetizing inductor.

Practical efficiency curves of the LC-DS prototype are given in Fig. 17. Breakdown illustrations of the power loss are shown in Fig. 18. A full-bridge LLC converter is selected for a comparison in the efficiency test due to the primary-side resonant tank. In order to make a fair comparison, only the transformer and resonant capacitors are different in the two prototypes. The transformer core size of the LLC converter is the same as that of the LC-DS converter. Photographs of these two prototypes are shown in Fig. 16. Efficiency curves of the prototypes are illustrated in Fig. 17. Moreover, the maximum temperatures of the components are recorded under the 500W power condition, as shown in Table V. It is obvious that the temperatures of the resonant capacitors in the LLC are much

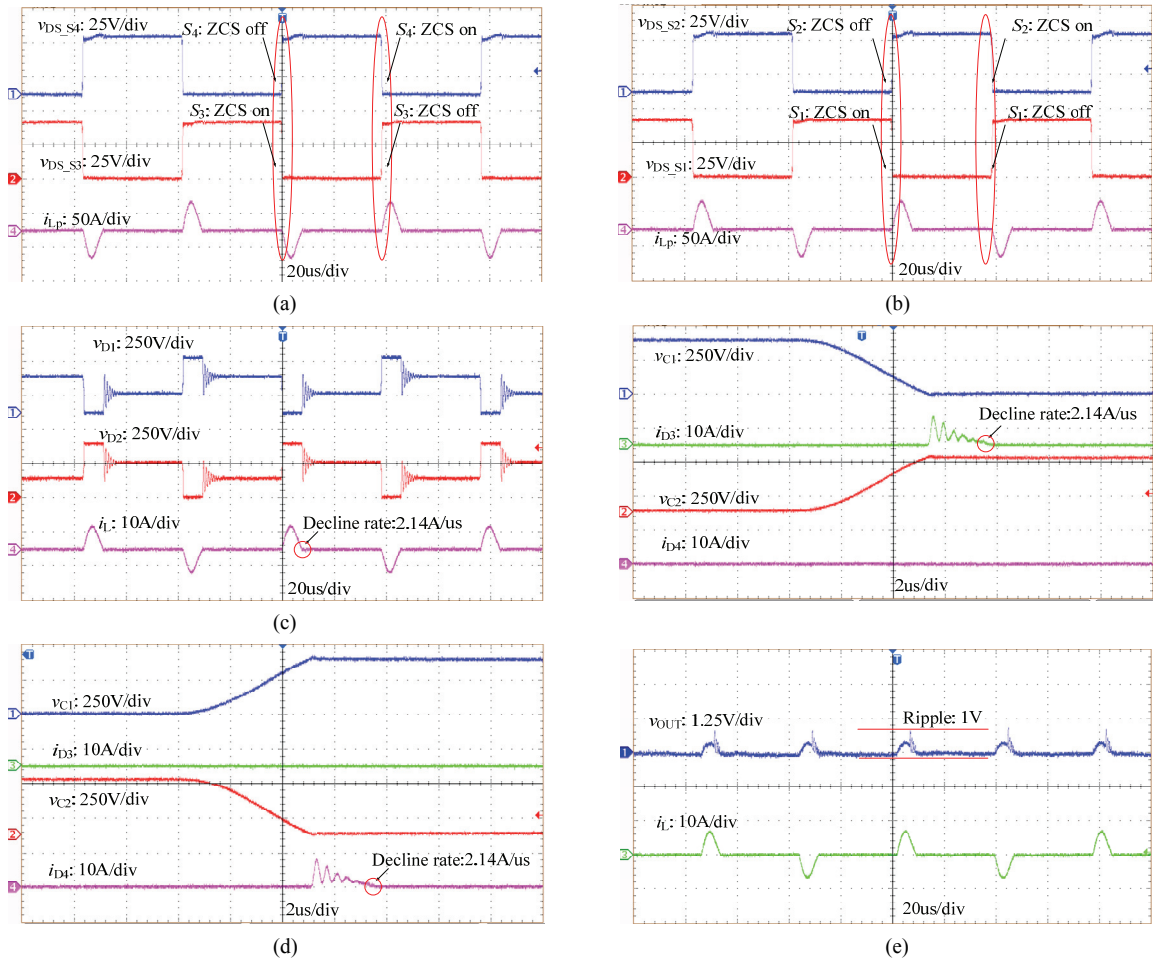
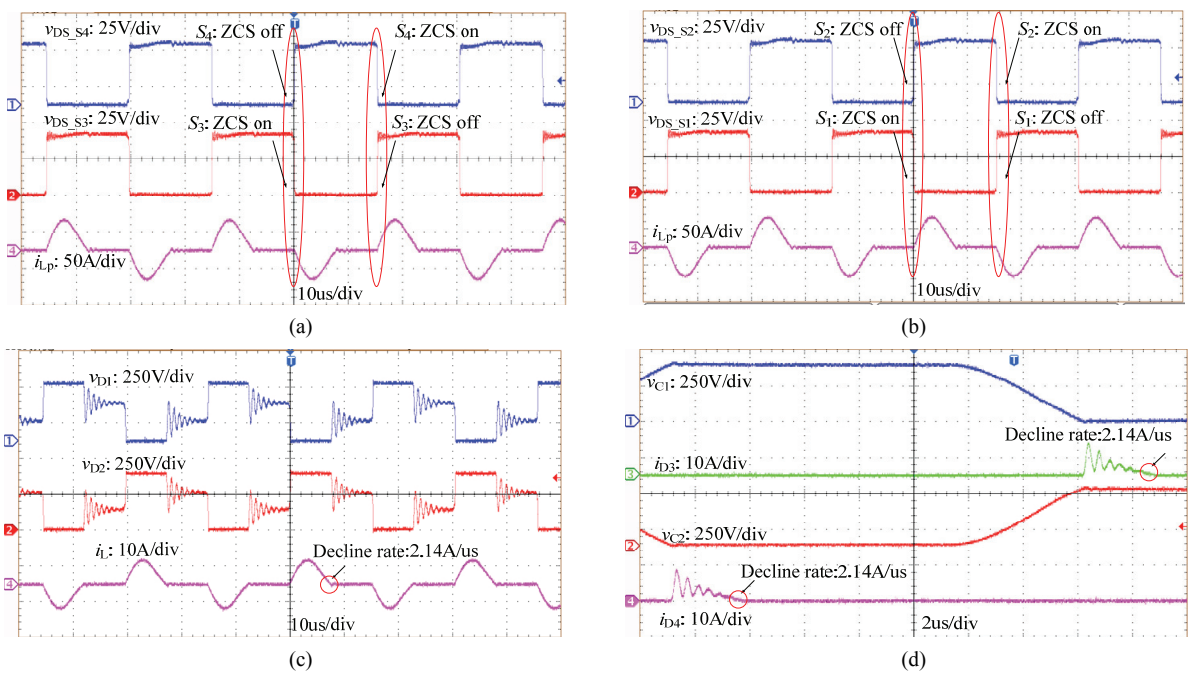
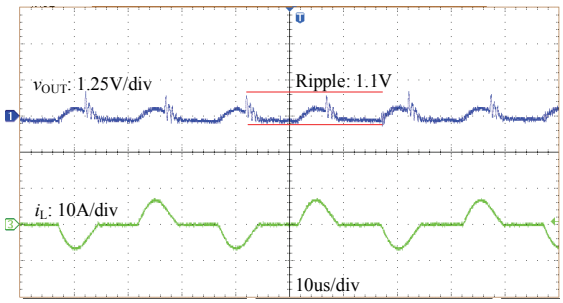


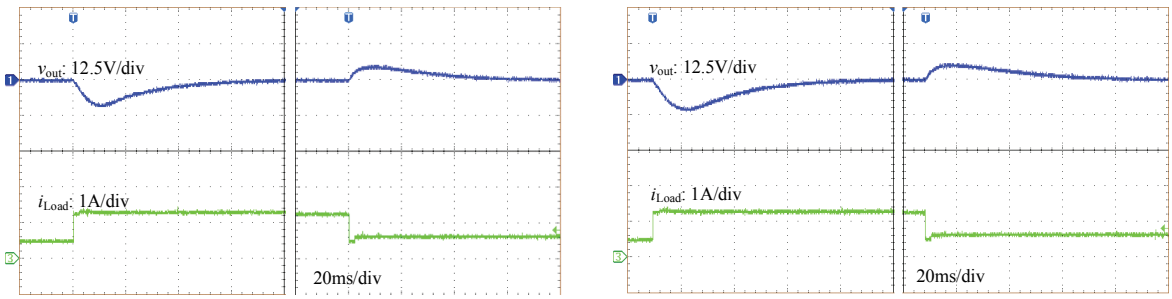
Fig. 13. Light load experimental waveforms (V_g=42V, V_o=400V, P=200W). (a) Drain-source voltage of S_3 and S_4, and the primary-side current i_{Lp}. (b) Drain-source voltage of S_1 and S_2, and the primary-side current i_{Lp}. (c) Voltage of D_1 and D_2, and the secondary-side current i_L. (d) Current of D_3 and D_4, and the voltage of C_1 and C_2. (e) Output voltage ripple, and the secondary-side current i_L.





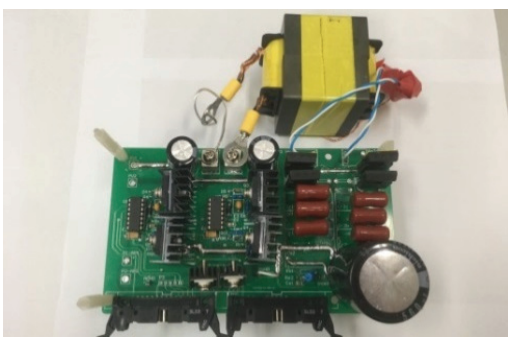
(e)

Fig. 14. Nominal power experimental waveforms (V_g=42V, V_o=400V, P=500W). (a) Drain-source voltage of S_3 and S_4, and the primary-side current i_{Lp}. (b) Drain-source voltage of S_1 and S_2, and the primary-side current i_{Lp}. (c) Voltage of D_1 and D_2, and the secondary-side current i_L. (d) Current of D_3 and D_4, and the voltage of C_1 and C_2. (e) Output voltage ripple, and the secondary-side current i_L.

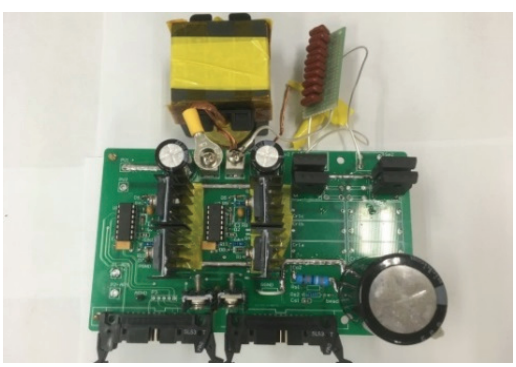


(a) (b)

Fig. 15. Experimental dynamic response of an LC-DS prototype. (a) 200W-500W load step under a 35V input. (b) 200W-500W load step under a 42V input.



(a)



(b)

(C_r=1μF, L_{rp}=14.3μH, L_{mp}=55μH, transformer turn-ratio is 1/3)

Fig. 16. Photographs of LC-DS and LLC prototypes. (a) LC-DS prototype. (b) LLC prototype.

TABLE V
MAXIMUM TEMPERATURES OF THE COMPONENTS IN A 500W POWER TEST

	LLC	LC-DS
MOSFETs	78.3° C@35V input 78.0° C@42V input	79.8° C@35V input 78.5° C@42V input
Diodes	50.2° C@35V input 51.1° C@42V input	52.3° C@35V input 51.5° C@42V input
Resonant capacitors	75.8° C@35V input 73.8° C@42V input	35.5° C@35V input 34.2° C@42V input
Transformer	60.5° C@35V input 61.7° C@42V input	62.7° C@35V input 61.2° C@42V input

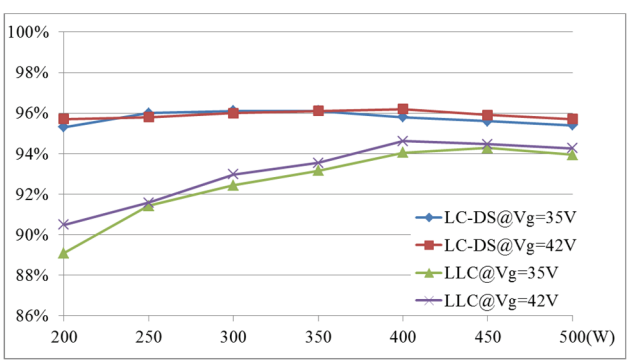
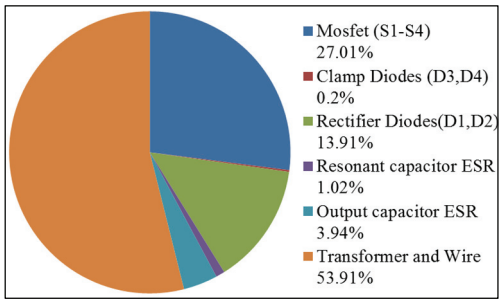
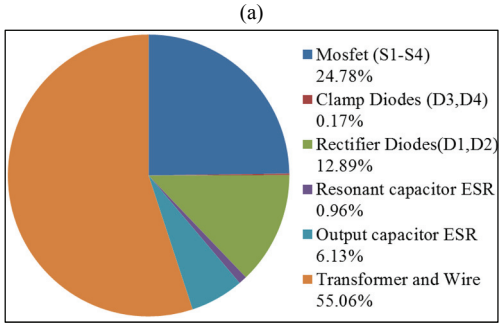


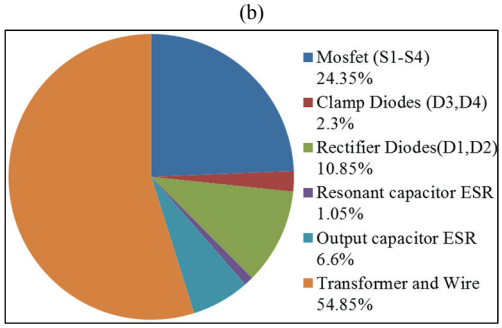
Fig. 17. Measured efficiency curves.



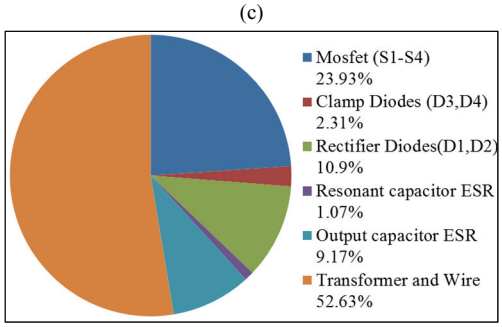
(a)



(b)



(c)



(d)

Fig. 18. Breakdown illustrations of power loss. (a) V_g=35V, P=500W. (b) V_g=35V, P=200W. (c) V_g=42V, P=500W. (d) V_g=42V, P=200W.

higher than those in the LC-DS converter. This is due to the fact that the large primary-side resonant current induces a non-negligible power loss. Hence, the efficiency performance of the LLC converter is not satisfactory when compared with the LC-DS converter.

VII. Conclusions

An LC resonant converter with clamp diodes on the secondary side (LC-DS) is proposed in this paper. The operation principle is analyzed in detail and the design considerations are also presented.

The LC-DS has simple circuit and transformer structures. It is derived from the LC-DP converter presented in [8], [24]-[26]. When compared with the LC-DP, the power level of the LC-DS can be extended by two more design freedom-degrees especially under a low input voltage. When the transformer turn-ratio is equal to 1, the LC-DS is essentially a step-up converter. Therefore, it is suitable to realize a high step-up function and it is helpful for decreasing the transformer turn-ratio.

By placing resonant loops on the secondary side of a step-up transformer, the current stress of the resonant capacitors is significantly decreased. Therefore, the power loss caused by the ESR of the resonant capacitors is decreased. Meanwhile, the power loss caused by the clamp diodes is noticeably reduced.

A full-bridge structure is applied on the primary side so there are only active switches without other extra power components. Therefore, the power loss caused by a large primary-side current can be controlled in a minor range.

All of the active switches operate under ZCS during both turn-on and turn-off transitions. The reverse-recovery problems of the diodes are significantly alleviated because the current decline rate is limited by the leakage inductor.

A 500W prototype with a 35V-42V input and a 400V output has been built. Experimental results obtained with the prototype show good agreements with the theoretical analysis.

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