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Analytical and Experimental Validation of Parasitic Components Influence in SiC MOSFET Three-Phase Grid-connected Inverter

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Abstract

With the development of renewable energy, grid-connected inverter technology has become an important research area. When compared with traditional silicon IGBT power devices, the silicon carbide (SiC) MOSFET shows obvious advantages in terms of its high-power density, low power loss and high-efficiency power supply system. It is suggested that this technology is highly suitable for three-phase AC motors, renewable energy vehicles, aerospace and military power supplies, etc. This paper focuses on the SiC MOSFET behaviors that concern the parasitic component influence throughout the whole working process, which is based on a three-phase grid-connected inverter. A high-speed model of power switch devices is built and theoretically analyzed. Then the power loss is determined through experimental validation.

Key words: Gate driver, Modeling, Parasitic components, SiC MOSFET, Three-phase grid inverter

I. INTRODUCTION

Over the past several years, people have been focused on the application of wide band-gap (WBG) semiconductor power devices as high blocking voltage and large power supplies [1], [2]. The SiC MOSFET is the most representative of the switch devices that are widely used in three-phase AC motors, renewable energy vehicles, aerospace and military power supplies, and so forth [3]-[6]. In these research fields, power loss and the noise caused by current and voltage oscillations are problems that cannot be neglected when the switching frequency is increased [7]-[11]. Traditionally, determining the influence of a SiC MOSFET at a high switching frequency is accomplished by using mathematical or physical modeling. The modeling approach for SiC MOSFET switch devices uses a datasheet, which is obtained from the manufacturer's handbook, to predict the performance influence of the parasitic components. However, the feasibility of this method is worth discussing since the influence of the parasitic components is nonlinear. Furthermore, the method of using temperature to describe the average power consumption can affect the analysis of the specified device. In addition, a Q3D Extractor and IMPACT software shed light on the internal physical structure of the device. Nevertheless, the process is complicated and greatly influenced by the subjective knowledge of researchers. Additionally, with respect to experiments, the previous works mainly focused on the test results of SiC MOSFETs using the double pulse test (DPT) and neglect the actual effects in a specific experimental platform [12]. In this paper, as shown in Fig. 1, the physical modeling of a SiC MOSFET working process with parasitic components is analyzed. In addition, the influence of the switch device on three-phase grid-connected inverters under a variety of switching frequencies is discussed.

The rest of the paper is organized as follows. In Section II,

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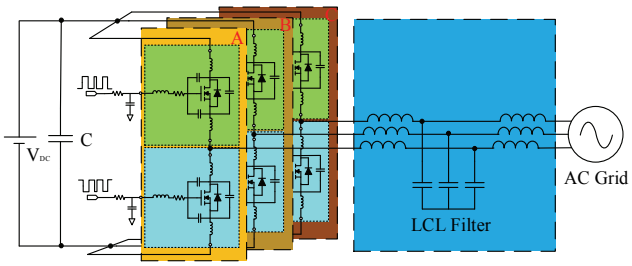


Fig. 1. System diagram of a three-phase grid-connected inverter with SiC MOSFET parasitic parameters under SPWM control.

SiC MOSFET high-speed small-signal modeling is analyzed and discussed. In Section III, the current and voltage oscillations in transistors during the working process are derived. Section IV discusses the reasons for power loss. In Section V, experimental details are introduced with the gate driver design. In addition, drive waveforms of different external gate resistances and parasitic gate-source capacitances are presented and used to validate the discussion on the influence of SiC MOSFET inverters. Finally, Section VI summarizes the main conclusions of this work.

II. Physical Modeling and Theoretical Analysis of a SiC MOSFET

As shown in Fig. 2, it is easy to build-up an intrinsic structural model of a SiC MOSFET with parasitic parameters through an analysis of physical characteristics, such as the I-V curve and the C_{iss}-V_{ds} curve [13], [14]. The parasitic components can exist in the same or different structural layers, which plays an important role in the turning-on, conducting and turning-off phenomena of power switching devices. Moreover, the inversion layer experiences a high blocking voltage (> 1200 V) for the super-junction structure, which produces a transverse electric field between the P-N junction when the bias of the device is reversed. Due to the high doping content of the drift layer when compared to that of the traditional Si-based layer, the conducting resistance of the SiC MOSFET decreases drastically. Bypassing the intrinsic parasitic body-diode between the drain-source layers is indispensable for regulating high-voltage changes when the transistors are computed in switching transients. All of these properties manifest the SiC MOSFET as an ideal rectifier when used in high power density, low power loss and high blocking voltage applications. Moreover, an analytical timing diagram of the SiC MOSFET working process in a three-phase grid-connected inverter is shown in Fig. 3.

The working process is analyzed based on the driving voltage, V_{dc} and the internal structure of the MOSFET. Then the transistor structure model is built in detail, the parasitic components are obtained from a datasheet, and the working region of the transistor is analyzed according to the changed driving voltage and the operating voltage [15]-[17]. It is clear

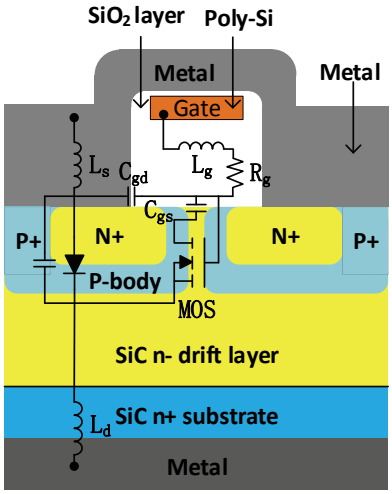


Fig. 2. Intrinsic structural diagram of a SiC MOSFET with parasitic components.

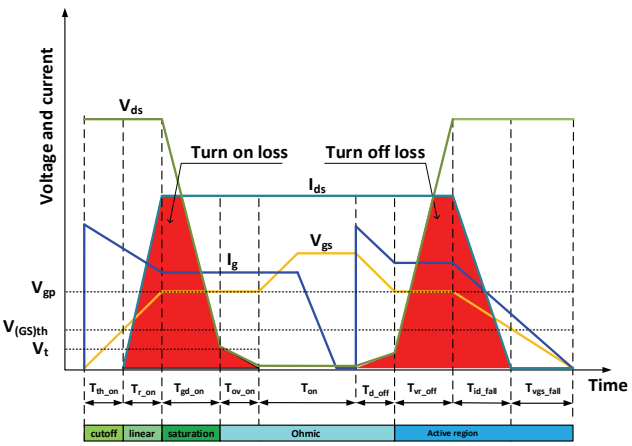


Fig. 3. Timing diagram of the working process of a SiC MOSFET in a three-phase grid-connected inverter.

that the working region of the SiC MOSFET, which is driven by the gate driver, can be divided into five parts, such as the cutoff region, linear region, saturation region and so on, that are introduced by high-speed small-signal modeling.

A. Modeling of the Cut-Off Region

To operate a SiC MOSFET in a three-phase inverter, the gate current must charge the input capacitor C_{iss} to approximately 950 pF for the SiC MOSFET (C2M0080120D), as is given by Equ. (1). When the gate voltage V_{gs} reaches a gate threshold voltage $V_{GS(th)}$ of approximately 2.1 V between the SiO_2 inversion layer and the channel, the working stage of the switch device transitions from the cutoff regime to the linear regime. Under ordinary conditions, it is necessary to prevent the device from opening in the cutoff regime, since the damage to the device increases with the cut-off time. Increasing the gate resistance can decrease the cut-off time. However, it can also aggravate the current spiking. Fig. 4(a) shows the corresponding high-speed small-signal model.

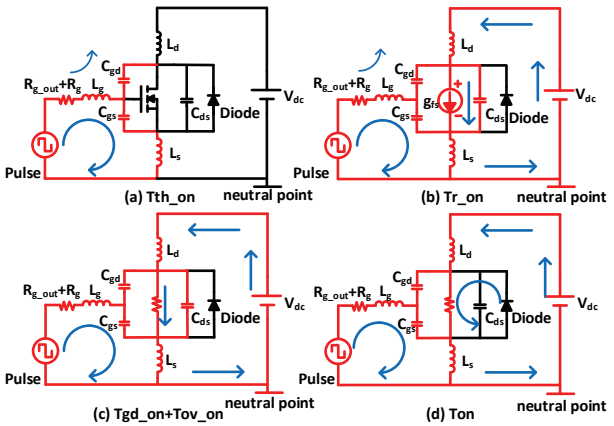


Fig. 4. Turning-on and conducting processes of the intrinsic current of a SiC MOSFET.

$$\begin{cases} C_{iss} = C_{gs} + C_{gd} \\ C_{oss} = C_{gd} + C_{ds} \\ C_{rss} = C_{gd} \end{cases} \tag{1}$$

where C_{oss} is the capacitance of the output capacitor (approximately 80 pF), which works in the output circuit of the SiC MOSFET, and C_{rss} is the capacitance of the reverse transfer capacitor (approximately 7.6 pF), which branches the high-frequency signals. Additionally, the lower the value of C_{rss}, the higher the upper limit of the switching frequency that is suitable for high-power density applications. In addition, the cutoff time is calculated as:

$$T_{th\_on} = (R_{g\_out} + R_g) C_{iss} \ln\left(\frac{1}{1 - \frac{V_{GS(th)}}{V_{Rg}}}\right) \tag{2}$$

where R_{g_out} is the outside driven resistance of the PCB layout, and V_{Rg} is the voltage value across the intrinsic parasitic gate resistor.

B. Modeling of the Linear Region

As shown in Fig. 4(b), at this stage, the SiC MOSFET works as a voltage-controlled current source until V_{gs} arrives at the Miller plateau. Thus, the drain-source current I_{ds} rises linearly when adjusted under the condition of $V_{gs} \geq V_{GS(th)} \,\&\, V_{ds} > V_{gs} - V_{GS(th)}$, which is illustrated as:

$$I_{ds} = g_{fs} \frac{W}{L}\left(V_{gs} - V_{GS(th)} - \frac{V_{ds}}{2}\right) \cdot V_{ds}\left(1 + \lambda V_{ds}\right) \tag{3}$$

Where g_{fs} is the transconductance of the SiC MOSFET, which is approximately 8 S; W and L are the channel width and length, which are approximately 10 μm; and λ represents the channel length modulation parameter.

Additionally, the rise time T_{r_on} is calculated as:

$$T_{r\_on} = (R_g + R_{g\_out}) C_{iss} \ln\left(\frac{g_{fs}\left(V_{Rg} - V_{GS(th)}\right)}{g_{fs}\left(V_{Rg} - V_{GS(th)}\right) - I_{ds}}\right) \tag{4}$$

C. Modeling of the Saturation Region

In Fig. 4(c), when V_{gs} remains unchanged when influenced by the Miller effect, I_{ds} rises up to the maximum value, and V_{ds} begins to clearly fall at the same time. This stage of the SiC MOSFET is frequently called the saturation region, since I_{ds} does not increase in proportion to the drive current changes. When I_{gs} is saturated, the main gate current I_{gs} charges C_{gd} until it arrives at an electric charge Q_{gd} of 23 nC, according to the datasheet. It should be noted that the time of the saturation region is derived as:

$$T_{gd\_on} = \frac{Q_{gd}(R_g + R_{g\_out})}{V_{Rg} - V_{gp}} \tag{5}$$

The drain-source current is given by Equ. (6) when satisfying the condition of $V_{gs} \geq V_{GS(th)} \,\&\, V_{ds} \leq V_{gs} - V_{GS(th)}$.

$$I_{ds} = \frac{g_{fs}}{2} \cdot \frac{W}{L}\left(V_{gs} - V_{GS(th)}\right)^2 \cdot \left(1 + \lambda V_{ds}\right) \tag{6}$$

D. Modeling of the Ohmic Region

This state of the SiC MOSFET is comprised of the end of the Miller plateau, the beginning stage of the Q_{gd} discharge and the whole time of conduction. Since the third part occupies the main process, this stage of the SiC MOSFET is typically modeled as a resistor when the intrinsic body-diode functions as a freewheeling diode, as shown in Fig. 4(d). In addition, the conduction time T_{on} is D/f_{sw} for the upper SiC MOSFET, and I_{ds} is calculated as:

$$I_{ds} = g_{fs} \frac{W}{L}\left[\left(V_{gs} - V_{GS(th)}\right) V_{ds} - \frac{1}{2} V_{ds}^{\,2}\right] \tag{7}$$

where the current I_{ds} remains a constant value. However, its value increases in experiments to accommodate decreasing conduction resistance R_{ds} values.

E. Modeling of the Active Region

This region is the opposite of the turning-on stage since Q_{gd} discharges during the whole process until the drain-source current decreases to a nearly zero state. In addition, this region is composed of three time transitions, which are described as T_{vr_off}, T_{id_fall} and T_{vgs_fall}. Furthermore, this stage represents the beginning of the release of the stored charge of Q_{gd} when the driven current gradually decreases. Therefore, I_{ds} begins to be reduced by the Miller effect and arrives at nearly zero. The details of this region are shown in Fig. 5, which sheds light on the turning-off process of the internal current of the SiC MOSFET.

For the part of this stage shown in Fig. 5(a), V_{gs} is clamped to the value of the Miller voltage $V_{GS(th)}$, and the drain-source voltage rises linearly. The corresponding time of this state is given by:

$$T_{vr\_off} = \frac{Q_{gd}(R_g + R_{g\_out})}{V_{gp}} \tag{8}$$

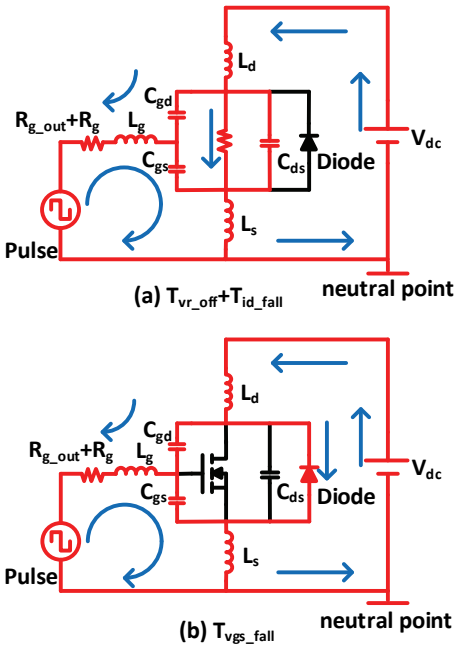


Fig. 5. Turning-off process of the intrinsic current of a SiC MOSFET.

In the second process of this stage, I_{ds} decreases noticeably at the end of the Miller plateau, and V_{ds} maintains the same value for the transistor entering the cut-off state, which can produce a power loss during transients. It is noted that the time of this transition is given by:

$$T_{id\_fall} = (R_g + R_{g\_out}) C_{iss} \ln\left(\frac{V_{gp}}{V_{gs\_th}}\right) \tag{9}$$

As shown in Fig. 5(b), in this stage, the reverse recovery effect of the parasitic body-diode of the MOSFET results in a current oscillation to decrease the P-N junction, which increases the power loss at this time.

III. Influence of the Parasitic Parameters on the Transistor Curve Oscillation

The influence of the intrinsic parasitic components of a SiC MOSFET is mainly reflected in the changes of *di/dt* at the moment of the turn-on transient and in the changes of *dv/dt* at the moment of the turn-off transient. This is traditionally illustrated as electromagnetic interference (EMI) that overshoots the expected value and forms unnecessary damage to high-speed signals.

A. Oscillation During the Turning-On Stage

During the turning-on stage, the drain-source current changes from the linear region to the saturation region, which can produce an overshoot in the release of the charge of C_{ds} and is influenced by the parasitic inductance. The overshoot performance can be analyzed by modeling a simplified equivalent circuit of the RCL, as shown Fig. 6. The calculation

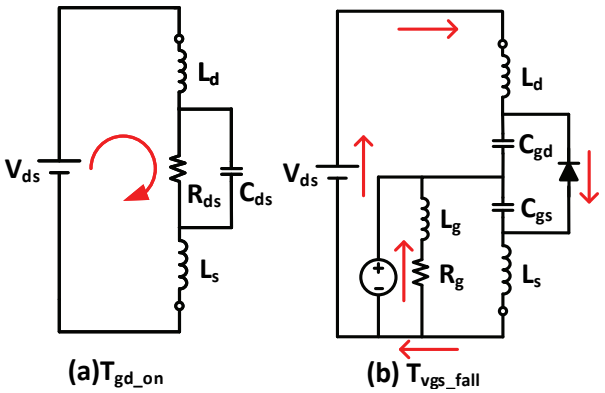


Fig. 6. MOSFET equivalent circuits at transients. (a) Turning-on process. (b) Turning-off process.

of the peak value of I_{ds} is proposed in (10). Additionally, the sinusoidal part of the calculation is the reason for the oscillation, which is expressed as a ringing:

$$I_{peak} = I_0\left(1 - \frac{e^{(-\pi/\omega)}\sin(\pi+\beta)}{\omega\sqrt{(L_s+L_d)C_{ds}}}\right) \tag{10}$$

where ω is the concussion angle frequency, which is calculated as Equ. (11). In addition, β is given by Equ. (12):

$$\omega = \sqrt{\frac{1}{(L_s+L_d)C_{ds}} - \left(\frac{R}{2(L_s+L_d)}\right)^2} \tag{11}$$

$$\beta = \arctan\left(\frac{\omega}{\alpha}\right) \tag{12}$$

Where α is R/2L, and R is less than $2\sqrt{(L_s+L_d)/C_{ds}}$. The resonant frequency of I_{ds} is the same as the gate current, which is given by:

$$F_{req} = \frac{1}{2\pi\sqrt{(L_s+L_d)C_{ds}}} \tag{13}$$

Based on the above theoretical analysis, an effective method to decrease the current overshoot is to improve the resonant frequency to reduce the influence of the second-order system instability. This is done to mitigate the amplitude of the sinusoidal part of I_{peak}. However, a high resonant frequency may increase the risk of self-oscillation.

B. Oscillation During the Turning-Off Stage

As shown in Fig. 6, V_{ds} can produce a ringing during the reverse recovery of the intrinsic body-diode, which informs the current oscillation. The corresponding *dv/dt* capability is given by:

$$\begin{cases} \dfrac{dV_{ds}}{dt} = \dfrac{V_{GS(th)}}{Z_{gs}C_{gd}} \\ Z_{gs} = \sqrt{R_g^2 - \left(\dfrac{1}{\omega C_{gs}} - \omega\left(L_g + L_s + L_d\right)\right)^2} \end{cases} \tag{14}$$

A method for reducing ringing is to increase the gate-drain capacitor and resistor values. However, the switching loss increases when the holding C_{gd} of the high-capacity capacitor and the large value of the gate resistance. Therefore, a balance exists between the EMI and the switching power loss of SiC MOSFETs.

IV. Theoretical Analysis of the Power Loss Calculation

The primary power loss is derived during the process of inverter energy transformation, which includes the conduction loss, switching loss, and body-diode reverse-recovery-related loss of a SiC MOSFET. In addition, the power loss of an LCL filter needs to be considered, especially the core loss and winding loss in three-level inverters.

A. Conduction and Switching Losses

The drain-source resistance R_{ds} can be regarded as a constant in the ohmic region of a SiC MOSFET in the linear amplification area of this period. Since the voltages and currents of the transistors in the same bridge perform periodic variations, which are shown in Fig. 7, it is simple to calculate the conduction loss, including the forward conduction loss and reverse conduction loss, which are calculated by Eqns. (15) and (16), respectively.

$$P_{con\_for}=\frac{\sum_{i=1}^{n}E_i}{\sum_{i=1}^{n}T_i}=\frac{\sum_{i=1}^{n}P_{con}^{i}t_{con}^{i}}{\sum_{i=1}^{n}T_i}=\frac{T_{on}P}{T_{cycle}}=DP \tag{15}$$

$$P_{con\_rever}=\frac{\sum_{j=1}^{n}E_j}{\sum_{j=1}^{n}T_j}=\frac{\sum_{j=1}^{n}P_{con}^{j}t_{con}^{j}}{\sum_{j=1}^{n}T_j}=\frac{T_{off}P'}{T_{cycle}}=(1\text{-}D)P' \tag{16}$$

where P and P' are the calculated variations of the forward conduction loss and reverse conduction loss given by Equ. (17). In addition, n is the frequency modulation ratio, which is calculated by $n=f_{sw}/f_0$.

$$\begin{cases} P=6I_{rms}^{2}R_{ds}\left(\frac{1}{8}+\frac{m_a\cos\phi}{3\pi}\right) \\ P'=6I_{rms}^{2}R_{ds}\left(\frac{1}{8}-\frac{m_a\cos\phi}{3\pi}\right) \end{cases} \tag{17}$$

where the current I_{rms} is defined by (18), m_a is a constant (~0.8), and the $\cos\phi$ is between 0.8-1[18].

$$I_{rms}=\frac{4P_{out}}{3\sqrt{2}m_a\cos\phi V_{dc}} \tag{18}$$

In theory, the turning-on power loss decreases as a function of the turn-on period t_r, which is defined as the time from I_{ds} reaching 10% of the steady-state current to V_{ds} falling to 10% of V_{dc}. The turning-off period t_{off} is defined from V_{ds} rising to 10% of V_{dc} to I_{ds} falling to 10% of the inductive load current [14]. There is no crossing area between V_{ds} and I_{ds} in the reverse conduction process of the switching device. Therefore, the switching loss of the bridge only exists in the first and second quadrants of Fig. 7. According to the authors of [19], the switching loss of a switch can be simplified as the two red regions shown in Fig. 3. Therefore, the theoretically derived process of the switching loss in the $\sum_{i=1}^{n}T_i$ period is given as:

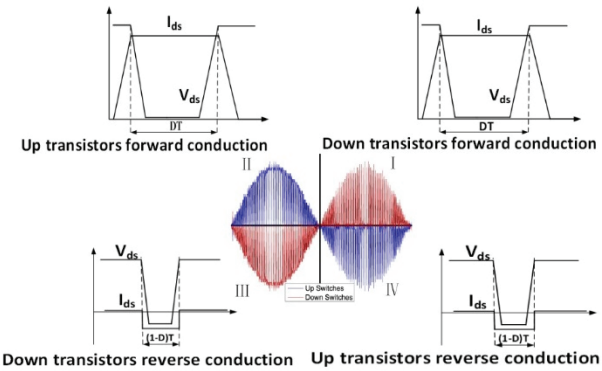


Fig. 7. Conduction losses of transistors in the same bridge.

$$\begin{cases} P_{sw\_on}=\dfrac{\sum_{i=1}^{n}E_{turn\_i}^{on}}{\sum_{i=1}^{n}T_i}=f_{sw}P_{on}\left(T_{r\_on}+T_{gd\_on}+T_{ov\_on}\right) \\ P_{sw\_off}=\dfrac{\sum_{i=1}^{n}E_{turn\_i}^{off}}{\sum_{i=1}^{n}T_i}=f_{sw}P_{off}\left(T_{d\_off}+T_{vr\_off}+T_{id\_off}\right) \end{cases} \tag{19}$$

where P_{on} and P_{off} are the effective turning-on and turning-off power losses during a cycle period, which is defined as:

$$P_{on}=P_{off}=I_{rms}V_{rms}=\frac{V_{peak}I_{peak}}{2} \tag{20}$$

where V_{peak} and I_{peak} are the maximum absolute values of the shut-down voltage and the conduction current of the device.

It is apparent that the switching power loss must be taken into consideration when the switching frequency rapidly increases. In addition, it can reduce the turning-on time and turning-off time by decreasing the value of R_{g_out}. However, this results in the problem of a low-driven capability, which can result in C_{gd} being shaken by the reduction of the two-order system damping at the same time. Therefore, there is a balance between the power loss and EMI problems, and the R_{g_out} value is usually chosen to be no less than the parasitic gate resistance of the SiC MOSFET for a low Q_g and high switching speeds [19].

B. Gate Driver Loss

There is energy dissipation in the gate driver when the gate current charges C_{iss} until it can conduct the SiC MOSFET. Then the loss calculation is given by:

$$P_{\text{gate}} = Q_g V_{gs\_\max} f_{\text{sw}} \tag{21}$$

Moreover, the gate driver energy is the criterion for designing the driver PCB layout. When the switching frequency increases, the voltage supplied for the SiC MOSFET should decrease to a suitable level in order to keep the energy balanced, which reduces the risk of a breakdown in the P-N junction between the gate and source terminals.

C. Reverse-Recovery-Related Losses of the Intrinsic Body-Diode

During the turning-off transient, the parasitic body-diode of a SiC MOSFET functions as a freewheeling diode, which leads the current flow through the drain-source terminals in Fig. 5(b). This usually appears as downward-shocking at the end of the turning-off period. The loss is introduced by:

$$P_{\text{body\_diode}} = \frac{1}{2} Q_{rr} V_{ds} f_{sw} \tag{22}$$

where Q_{rr} is the reverse-recovery-charge. This must be taken into consideration when the switching frequency increases to a high level, which is usually at 200 kHz.

D. Winding Loss and Core Loss of the LCL Filter

In theory, the losses in an LCL filter can be calculated by:

$$P_{lcl} = P_{winding} + P_{core} \tag{23}$$

where the first part of Equ. (23) is the winding loss that approximately depends on the current flow through the inboard inductor. In addition, the core loss is given as:

$$\begin{cases} P_{winding} = I_{rms}^2 \left(R_o + \alpha \left(T - T_o \right) \right) \\ P_{core} = P_{fundamental} + P_{harmonic} \end{cases} \tag{24}$$

where, I_{rms} is the RMS of the current flow through the filter, R_0 is the resistance of copper at T_0 (approximately 25°C), α is the temperature coefficient of copper, and T is the radiation temperature of the LCL filter. Additionally, the core power loss depends on the fundamental and harmonic currents when the filtering effect is not apparent [20].

V. Experiment Results and Analysis

Fig. 8 shows the experimental set-up. The device with a SiC MOSFET is operated as a 2 kW DC-AC inverter with its switching frequency changed from 20 kHz to 100 kHz. The micro-controller RT box is to collect the analog signal, which is from the current sensor, and to internally process the closed-loop.

A diver logic schematic is shown in Fig. 9(a). In detail, the resistor and capacitor low-pass filter (RC LPF) intercept the PWM digital signal, as expected. The IC (ACPL-P345) is chosen as the core of the gate driver, since it consists of a gate drive optocoupler that isolates the high working voltage and the low driver voltage, a relay module that functions as a

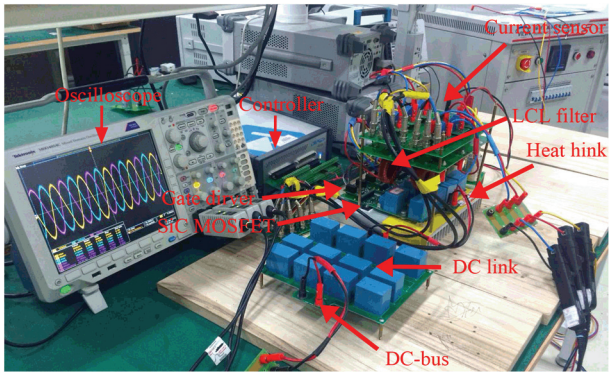
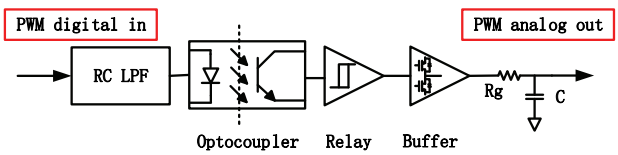
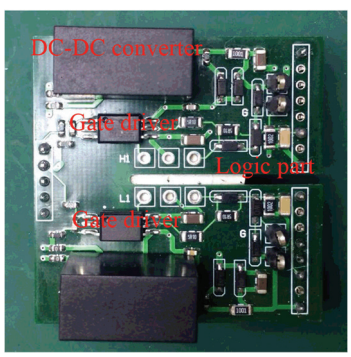


Fig. 8. Prototype of a 2000 W three-phase grid-connected inverter.



(a)

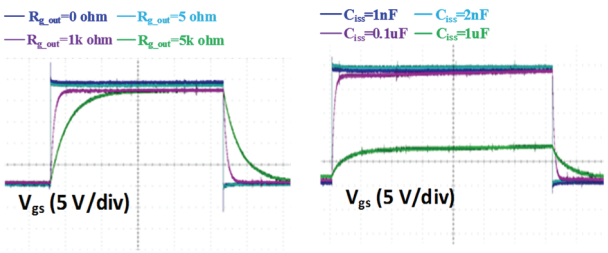


(b)

Fig. 9. Driver logic schematic and the circuit board. (a) Schematic of the gate driver. (b) 3D space model.

hysteresis comparator for threshold control, and a buffer that is the output gate current needed to increase the driving capability. Then the gate current from the buffer times R_{g} is used to drive the switch devices when C functions as another RC LPF.

The two SiC MOSFETs of the bridge are placed face to face on the circuit board, and the inter-distance of the components must be greater than the electrical-security-distance of approximately 2.5 mm. Furthermore, the different PCB lines should have a distance of 2 mm, since the maximum rated voltage is 750 V according to the criteria of the security creepage-distance. Two different film capacitances are chosen for filtering the current of the voltage source power supply. 400 μF large-capacity buffer capacitors are formed by paralleling multiple capacitors, which can suppress input DC voltage spikes. It should be noted that 1μF, which parallels the DC bus bar, is further used to decouple the stray inductance and to diminish the influence of high frequency signals [21], [22]. The up and down MOSFET test line is to test the current that conventionally flows through the SiC MOSFET.



(a) (b)

Fig. 10. Gate-source driving waveforms of a SiC MOSFET. (a) At different external gate resistances when C_{iss} is 1nF. (b) At different input capacitances when R_{g_out} is 5 ohms.

A. Influence of the Driven Waveforms of a SiC MOSFET Under the Influence of Parasitic Components

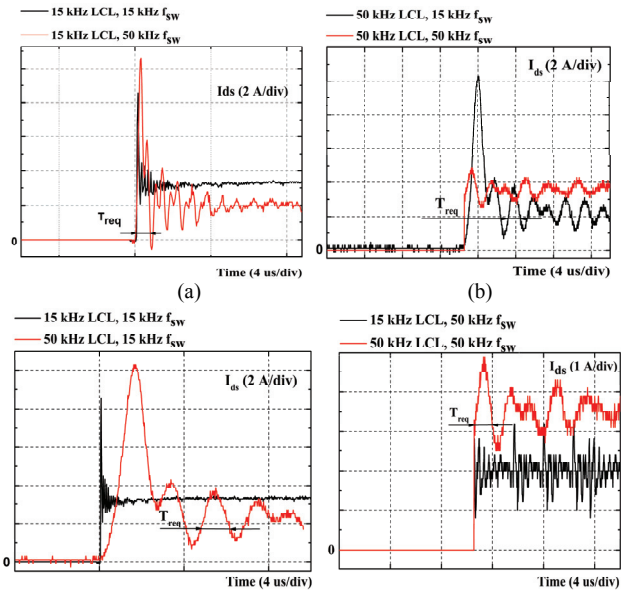
In terms of the above discussions, the driven waveforms of SiC power switch devices drivers are different when the influences of the parasitic components vary. In Section II, the issues that pronouncedly affect the driven waveforms are the external gate resistance and the input capacitances. Additionally, the switching frequency also serves as an important variable in mastering the validation result. To intuitively validate the discussions, an experimental platform is chosen where the inductances are based on a 100 kHz switching frequency to design for a reduction of the influence of the series inductance. In addition, the impact of the parasitic components can be fitted by adding an external RCL circuit.

Therefore, the impact of different external gate resistances on driven waveforms is presented as Fig. 10(a) when C_{iss} is 1nF. It is clear that the slope of V_{gs} can be slowed down, which affects the driving capability of the gate driver in the SiC MOSFET. Then the turn-on time is increased when the external gate resistance increases according to Eqns. (2) and (4). In theory, the rising time of the conducting transient is 1ns which is about 0.01% of the conduction time. For example, the rising time is about 1.7ns when the driver is tested under the condition of R_{g_out} being 5 ohms and C_{iss} being 1nF as shown in Fig. 10(a). This also increases the turn-off time with less waveform oscillation when compared with a low gate resistance. According to the discussion in Section II, C_{iss} can be affected by the driven waveform of the gate driver, which is shown in Fig. 10(b). Apparently, the influence of increasing the input capacitor is similar to that of raising the external gate resistance, as can be seen by the curve trends interpreted by Eqns. (2)-(9).

B. Curve Oscillation of a SiC MOSFET

In this part, an LCL filter with different switching frequencies is tested in the 750 V(DC) input voltage-source to validate the discussion of the curve oscillation of a SiC MOSFET during switch transients.

As shown in Fig. 11, the turning-on transient of a SiC MOSFET is presented. It is clear that ΔI_{ds} increases with an increase of the higher switching frequency. The main reason



(a) (b)

(c) (d)

Fig. 11. Comparison of experimental switching characteristics under different LCL filter conditions and switching frequencies.

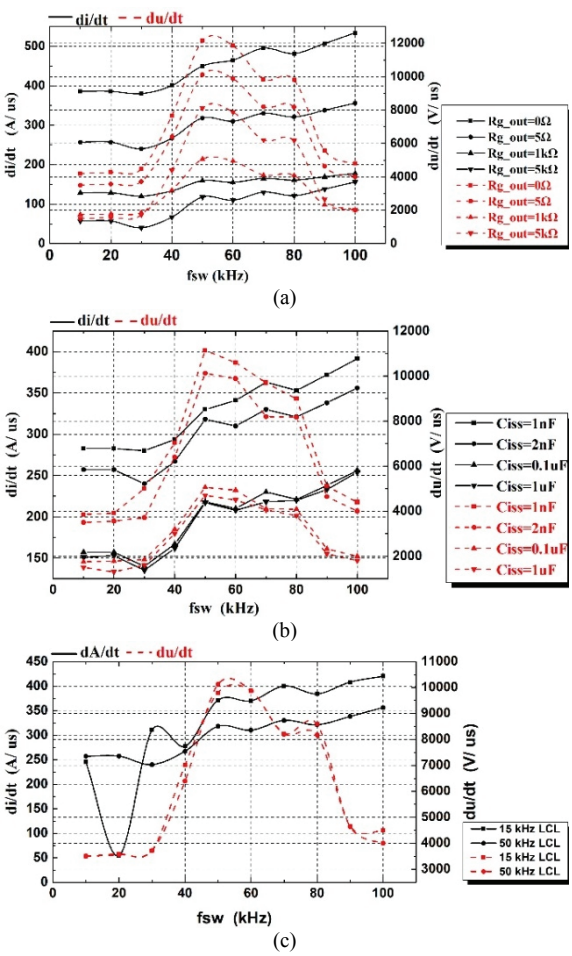


Fig. 12. Current and voltage oscillations with the influence of parasitic components under a series of test frequencies. (a) Influence of the parasitic resistance. (b) Influence of the parasitic capacitance. (c) Influence of different filter inductances.

for this is that the amplitude of the sinusoidal part decreases in Equ. (10) when the switching frequency increases. The synchronization between the resonant frequency and the switching frequency increases the impact of the concussion angle, which is calculated by $\omega=2\pi f_{req}$, when the switching frequency increases. Moreover, Fig. 11(c) and Fig. 11(d) address the LCL filter influence when the decreased inductance value of the LCL filter raises the value of I_{peak}. This is similar to adding an external parasitic inductance between the drain and source of a SiC MOSFET with a larger filter inductor according to Equ. (13).

It should be noted that the parasitic RCL components can influence the curve oscillation on the basis of the theoretical discussion. Therefore, the influences of the external gate resistance, gate-source capacitance and drain-source inductance on the inverter, which were tested under a series of switching frequencies, are shown in Fig. 12.

It is clear that *di/dt* and *dv/dt* decrease when increasing the external gate resistances and gate-source capacitances. At the same time, *di/dt* increases when the switching frequency varies to a high level, since the turning-on time is reduced by the fast open transient of the SiC MOSFET. In addition, *dv/dt* is increased at first. Then it is restored to the original level, as the wheeling diode causes the current to change smoothly and the function of drain-source capacitor, which slows the acceleration. Therefore, the voltage ringing of the turning-off transient is the same for switching frequencies over 60 kHz.

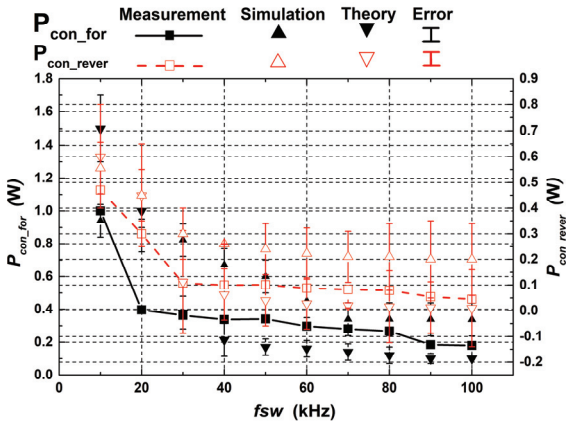
C. Power Loss and Temperature Results

In terms of the discussion in section IV, the conduction loss and switching loss of a SiC MOSFET, which mainly depend on the gate driver capability in the same experimental environment, are depicted in Fig. 13(a).

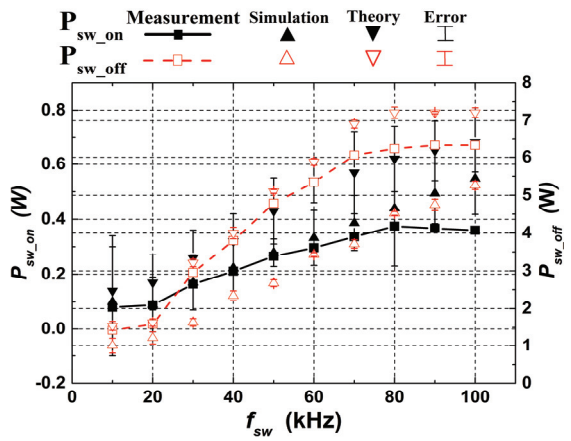
Apparently, the measured data curves validate that the conduction loss of the SiC MOSFET decreases and then maintains a steady state when the switching frequency increases up to 100 kHz. By analyzing the theoretical derivation, the conduction loss is cut by an output power reduction, which is affected by increasing the switching frequency according to the design formula. Furthermore, the switching power loss of the SiC MOSFET is shown in Fig. 13(b). It is evident that the switching loss dissipates slowly under the high switching frequency condition until the system comes into the steady-state.

These results can be derived from the gate driven capacity. Therefore, the gate power loss must be taken into consideration, which is presented in Fig. 14. This figure shows that the increasing switching frequency promotes a gate driver power loss when the current of the gate terminal changes significantly.

In addition, the parasitic body-diode reverse-recovery related loss is an important issue that needs to be taken into consideration. As shown in Fig. 15(a), the P-N junction can release the stored charge, which forms the reverse-recovery



(a)



(b)

Fig. 13. Comparison of the switching conduction loss and the switching loss under a series of switching frequencies. (a) Forward conduction loss and reverse conduction loss. (b) Turning-on switching loss and turning-off switching loss.

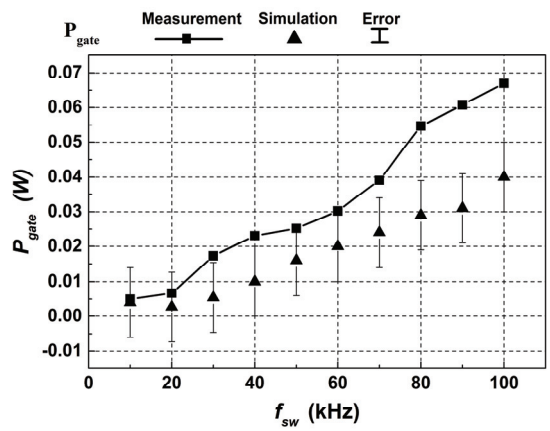
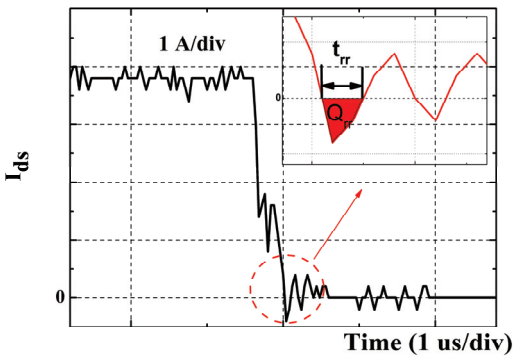


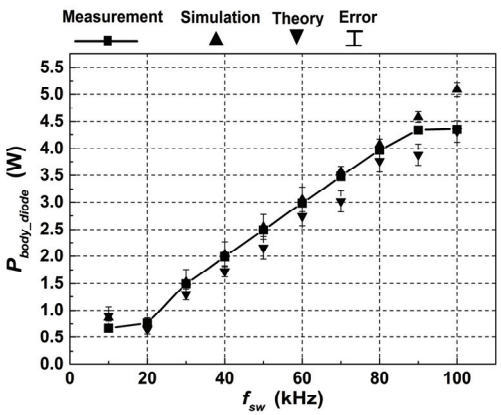
Fig. 14. Gate driver power loss when R_{g_out} is 5 Ω and C_{iss} is 2 nF.

current, when the D-S voltage is too high. The reverse-recovery charge of a C2M0080120D is 165 nC. It is too high which is why steps should be taken to alleviate the problem.

According to the above analysis, the current flow through the SiC MOSFET demonstrates a large downward spike that aggravates the reverse-recovery-related loss when the switching

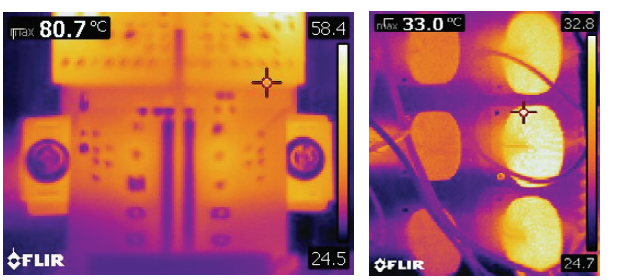


(a)

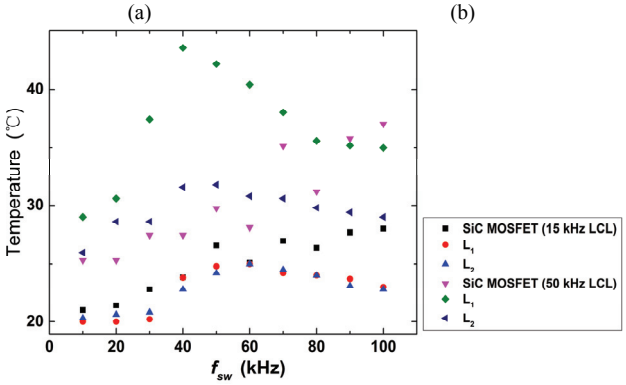


(b)

Fig. 15. Body-diode reverse-recovery-related phenomena. (a) Current curve of the SiC MOSFET at a turning-off transient. (b) Reverse-recovery-related loss statistical curve.



(a) (b)



(c)

Fig. 16. Temperature rise situation. (a) Thermal imaging of a SiC MOSFET in a single bridge under a 50 kHz switching frequency. (b) Corresponding LCL filter thermal imaging. (c) Temperature trend of the devices for a series of switching frequencies and conditions.

frequency is seriously increased, as shown in Fig. 15(b). The surplus power loss is caused by the parasitic inductance between the drain and source terminals when the frequency magnifies the influence of the current oscillation during the turning-off period.

In addition, as shown in Fig. 16(a) and Fig. 16(b), the intuitive phenomenon of power loss is the temperature, which releases energy in the form of heat radiation. Therefore, the heat sink under the switches accelerates the process in order to prevent thermal damage due to overheating. However, the cooling system cannot prevent temperature increases from higher switching frequencies due to power loss, as previously discussed. In addition, the LCL filter radiates more heat energy, and the issues that decide the curve distribution lie in the LCL design. In Fig. 16(c), $L_{1,2}$ was designed based on 50 kHz to produce more heat radiation when compared to 15 kHz. In detail, the temperatures of the devices rapidly increase by nearly 1.2~1.6 times when the frequency increases.

VI. Conclusion

This paper demonstrated the influence of parasitic components in the driving waveforms, curve oscillations and power loss with a switching frequency increase. Unlike previous analyses of parasitic parameters in DPT, this paper focus on a three-phase inverter design with the consideration of parasitic parameters influence. The drain-source of the SiC MOSFET is controlled by the DC-bus, and the model of the working process is not a current source. The operating state of the transistor is affected by both the external operating voltage and the degree of influence of the driving voltage on the parasitic parameters. Therefore, the decisive factor in the influence of the SiC MOSFET on three-phase grid-connected inverters is the gate driver design. Through an analysis of the working process during the switch turning-on and turning-off periods, it is practical to eliminate the current spikes and voltage oscillations by increasing the external gate resistance or by paralleling the bypass capacitor between the gate and the source node. This can prevent overshoots of the transients in the bridge. However, it also increases the power loss, which is reflected intuitively in the thermal image of the switching transfer stage at the same time. Then the influence of the SiC MOSFET on the three-phase grid-connected inverter is reflected by different LCL filters and switching frequencies. Based on experimental verification, the lower the LCL filter with a switching frequency increased from 15 kHz to 100 kHz, the greater the effect of the parasitic components on the ripple current.

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REFERENCES

[1] J. Millan, P. Godignon, X. Perpina, A. Perez-Tomas, and J. Rebollo, "A survey of wide bandgap power semiconductor devices," *IEEE Trans. Power Electron.,* Vol. 29, No. 5, pp. 2155-2163, May 2014.

[2] W. L. Erdman, J. Keller, D. Grider, and E. Van Brunt, "A 2.3-MW medium-voltage, three-level wind energy inverter applying a unique bus structure and 4.5-kV Si/SiC hybrid isolated power modules," in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 1282-1289, 2005.

[3] S. D. Caro, S. Foti, T. Scimone, A. Testa, G. Scelba, M. Pulvirenti, and S. Russo, "Over-voltage mitigation on SiC based motor drives through an open end winding configuration," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 4332-4337, 2017.

[4] K. Hamada, M. Nagao, M. Ajioka, and F. Kawai, "SiC emerging power device technology for next-generation electrically powered environmentally friendly vehicles," *IEEE Trans. Electron. Devices,* Vol. 62, No. 2, pp. 278-285, Feb. 2015.

[5] S. Jahdi, O. Alatise, C. Fisher, L. Ran, and P. Mawby, "An evaluation of silicon carbide unipolar technologies for electric vehicle drive-trains," *IEEE J. Emerg. Sel. Topics Power Electron.,* Vol. 2, No. 3, pp. 517-528, Sep. 2014.

[6] C. Gammeter, F. Krismer, and J. W. Kolar, "Comprehensive conceptualization, design, and experimental verification of a weight-optimized all-SiC 2 kV/700 V DAB for an airborne wind turbine," *IEEE J. Emerg. Sel. Topics Power Electron.,* Vol. 4, No. 2, pp. 638-656, Jun. 2016.

[7] J. V. P. S. Chennu, R. Maheshwari, and H. Li, "New resonant gate driver circuit for high-frequency application of silicon carbide MOSFETs," *IEEE Trans. Ind. Electron.,* Vol. 64, No. 10, pp. 8277-8287, Oct. 2017.

[8] D. Han, C. T. Morris, W. Lee, and B. Sarlioglu, "Comparison between output CM chokes for SiC drive operating at 20- and 200-kHz switching frequencies," *IEEE Trans. Ind. Appl.,* Vol. 53, No. 3, pp. 2178-2188, May 2017.

[9] X. Li, J. Jiang, A. Q. Huang, S. Guo, X. Deng, B. Zhang, and X. She, "A SiC power MOSFET loss model suitable for high-frequency applications," *IEEE Trans. Ind. Electron.,* Vol. 64, No. 10, pp. 8268-8276, Oct. 2017.

[10] H. Akagi, T. Yamagishi, N. M. L. Tan, S. i. Kinouchi, Y. Miyazaki, and M. Koyama, "Power-loss breakdown of a 750-V, 100-kW, 20-kHz bidirectional isolated DC-DC converter using SiC-MOSFET/SBD dual modules," in *2014 International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE ASIA)*, pp. 750-757, 2014.

[11] N. Oswald, P. Anthony, N. McNeill, and B. H. Stark, "An experimental investigation of the tradeoff between switching losses and EMI generation with hard-switched all-Si, Si-SiC, and all-SiC device combinations," *IEEE Trans. Power Electron.,* Vol. 29, No. 5, pp. 2393-2407, May 2014.

[12] X. Wang, C. Jiang, B. Lei, H. Teng, H. K. Bai, and J. L. Kirtley, "Power-loss analysis and efficiency maximization of a silicon-carbide MOSFET-based three-phase 10-kW bidirectional EV charger using variable-DC-bus control," *IEEE J. Emerg. Sel. Topics Power Electron.,* Vol. 4, No. 3, pp. 880-892, Sep. 2016.

[13] G. Kampitsis, M. Antivachis, S. Kokosis, S. Papathanassiou, and S. Manias, "An accurate Matlab/Simulink based SiC MOSFET model for power converter applications," in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 1058-1064, 2015.

[14] Z. Chen, "Characterization and modeling of high-switching-speed behavior of SiC active devices," Virginia Tech, 2009.

[15] J. Wang, X. Zhou, J. Li, T. Zhao, A. Q. Huang, R. Callanan, F. Husna, and A. Agarwal, "10-kV SiC MOSFET-based boost converter," *IEEE Trans. Ind. Appl.,* Vol. 45, No. 6, pp. 2056-2063, Nov. 2009.

[16] Y. Zhou, H. Liu, T. Yang, and B. Wang, "SPICE modeling of SiC MOSFET considering interface-trap influence," *CPSS Trans. Power Electron. Appl.,* Vol. 3, No. 1, pp. 56-64, Mar. 2018.

[17] J. Wang, T. Zhao, J. Li, A. Q. Huang, R. Callanan, F. Husna, and A. Agarwal, "Characterization, modeling, and application of 10-kV SiC MOSFET," *IEEE Trans. Electron. Devices* Vol. 55, No. 8, pp. 1798-1806, Aug. 2008.

[18] S. Yin, K. J. Tseng, C. F. Tong, R. Simanjorang, Y. Liu, A. Nawawi, and A. K. Gupta, "Evaluation of power loss and efficiency for 50 kW SiC high power density converter," in *2016 Asian Conference on Energy, Power and Transportation Electrification (ACEPT)*, pp. 1-6, 2016.

[19] Y. Liu, Z. Song, H. Wang, G. Wang, J. Peng, and S. Yin, "Comparative evaluation of WBG and Si power devices for the flyback converter," in *IECON 2017 - 43rd Annual Conference of the IEEE Industrial Electronics Society*, pp. 964-969, 2017.

[20] W. Fu, "Design and Comparison of Si-based and SiC-based Three-Phase PV Inverters," University of Wisconsin-Milwaukee, 2015.

[21] G. Zou, Z. Zhao, and L. Yuan, "Study on DC busbar structure considering stray inductance for the back-to-back IGBT-based converter," in *2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 1213-1218, 2013.

[22] F. Zare and G. F. Ledwich, "Reduced layer planar busbar for voltage source inverters," *IEEE Trans. Power Electron.,* Vol. 17, No. 4, pp. 508-516, Jul. 2002.

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