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Interleaved High Step-Up Boost Converter

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Abstract

Renewable energy based on photovoltaic systems is beginning to play an important role to supply power to remote areas all over the world. Owing to the lower output voltage of photovoltaic arrays, high gain DC-DC converters with a high efficiency are required in practice. This paper presents a novel interleaved DC-DC boost converter with a high voltage gain, where the input terminal is interlaced in parallel and the output terminal is staggered in series (IPOSB). The IPOSB configuration can reduce input current ripples because two inductors are interlaced in parallel. The double output capacitors are charged in staggered parallel and discharged in series for the load. Therefore, IPOSB can attain a high step-up conversion and a lower output voltage ripple. In addtion, the output voltage can be automatically divided by two capacitors, without the need for extra sharing control methods. At the same time, the voltage stress of the power devices is lowered. The inrush current problem of capacitors is restrained by the inductor when compared with high gain converters with a switching-capacitor structure. The working principle and steady-state characteristics of the converter are analyzed in detail. The correctness of the theoretical analysis is verified by experimental results.

Key words: Efficiency analysis, High step-up, Low input current ripple, Low output voltage ripple, Voltage balance

I. INTRODUCTION

Traditional fossil fuel resources are being rapidly depleted, and their continued use will further aggravate environmental degradation. The development of clean energy systems is crucial. Photovoltaic power generation, wind power generation and fuel cell power generation are important clean energy technologies. Systems using photovoltaic cells and batteries to provide clean power have become increasingly common. Therefore, in order to transfer the energy from traditional photovoltaic cells (12-48V) to a traditional 110V/220V AC power grid, it is necessary to use a DC-DC converter to improve the voltage. To achieve a high voltage gain, a cascaded boost converter had been presented in [1]-[4]. Although a large conversion ratio can be achieved, the voltage stress on the active switch is equivalent to the value of a high output voltage. Some converters employ the switched-capacitor technique to a conventional boost converter for a high conversion ratio [5]-[8]. Although the voltage stress of the power switch is reduced when the gain is increased, the efficiency of the converter is reduced since more power switch devices are used. In addition, the use of multiple switched capacitor modules brings a great deal of impulse current, which greatly reduces the stability of the converter. Switched-inductor technology has been combined with basic boost converters to obtain a high voltage [9]-[11], and the reverse recovery of the output diode is effectively suppressed. However, there are larger ripples on both the high input current and the output voltage, which is harmful to photovoltaic cells and the load.

Considering the low ripple of the interleaved structures for high power applications, several interleaved Boost converters were proposed in [12]-[15]. However, the voltage gain was not high enough to be suitable for low voltage renewing energy generated systems. In [16], [17], transformer technology is used to improve the voltage gain. However, this increases the volume of the converter, and reduces both the power density and efficiency. Coupled-inductors were used in [18]-[21]. However, this resulted in hysteresis loss and eddies current loss, which reduce the efficiency of the converter. In addition, the leakage inductance can easily cause voltage spikes across the switches, and voltage clamping techniques are required to limit the voltage stresses on the switches. Consequently, this increases both the design cost and the control difficulty.

In this paper, a new interleaved boost converter is proposed

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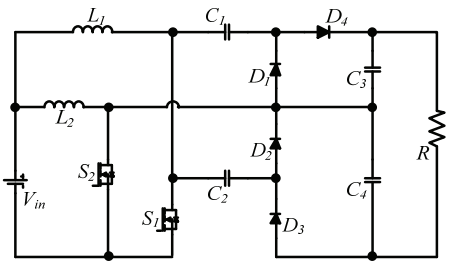

Fig. 1. Topology of the proposed converter.

to achieve a high gain and a high efficiency. The topology of proposed converter is shown in Fig. 1. The converter has the following characteristics. (a) It has a higher step-up ratio with same duty cycles. (b) The voltage stresses of the main switches are very low. (c) It is beneficial for reducing the input current ripple and output voltage ripple. (d) The voltage of output capacitance can be automatically shared without an extra control strategy.

II. Operating Principles of the Proposed Converter

To simplify the circuit analysis, the following assumptions are made.

(a) All of the power semiconductors and energy storage components are ideal, which means the on-state resistance of power semiconductors, the forward voltage drop of the diodes, and the equivalent series resistance (ESR) of the inductors and capacitors are ignored.

(b) All of the capacitances are large enough that each of the capacitor voltages can be treated as constant.

(c) The relationship between d_1 and d_2 can be written as $d_1=d_2=d$, where d_1 and d_2 are the duty cycles of S_1 and S_2, respectively.

(d) The phase difference between the gate driving signals of S_1 and S_2 is 180°.

In the circuit analysis, it is assumed that the converter operates in the continuous conduction mode (CCM) and that the duty ratio of the switches is greater than 0.5. Fig. 2 illustrates operational waveforms of the proposed converter in the CCM during one switching cycle. According to Fig. 2, four operation modes exist in each switching cycle of the proposed converter. Fig. 3 shows an equivalent circuit of the converter in different modes.

Mode *I* and Mode *III*: In this mode, the switches S_1 and S_2 are switched on. The diodes D_1, D_2, D_3 and D_4 are off. The current flow path is shown in Fig. 3 (a). At this time, the inductances L_1 and L_2 are charged by the power, and the currents of the inductances L_1 and L_2 are gradually increased. The capacitances C_3 and C_4 in series are combined to supply the load R. When the switch S_2 is off, the converter operates in the next mode.

Mode *II*: In this mode, the switch S_1 is still in the open

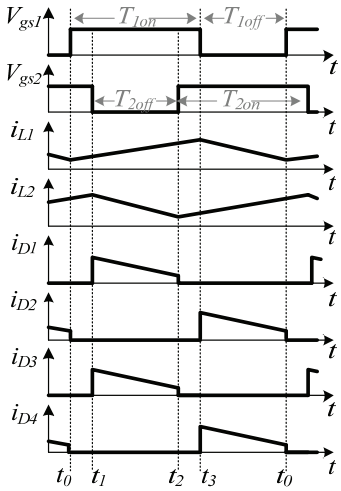

Fig. 2. Key waveforms of one cycle during CCM operation.

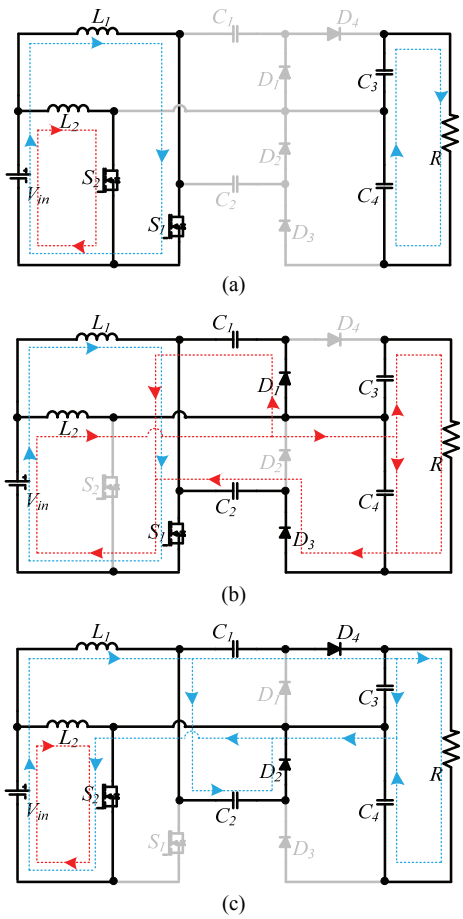

Fig. 3. Equivalent circuit of each mode in the CCM mode. (a) Mode *I* and *III*. (b) Mode *II*. (c) Mode *IV*.

state, and the switch S_2 is closed. The diodes D_1 and D_3 are on, and D_2 and D_4 are off. The current flow path is shown in Fig. 3 (b). At this point, the inductance of L_1 is still being charged, and the current of L_1 continues to increase. The capacitor C_1 is charged by the input power. The input power, the inductor L_2 and the capacitor C_2 are connected in series to provide

energy to the capacitor C_4 and the load R. The capacitor C_3 releases energy to load R at the same time, and the inductor current i_{L2} on L_2 is decreased. When the switch S_2 is switched, the converter operates in mode *III*. Then the converter operates in mode *IV* after the switch S_1 is closed.

Mode *IV*: In this mode, the switch S_1 is still closed, and the switch S_2 is still opened. The diodes D_1 and D_3 are turned off, and the diodes D_2 and D_4 are turned on. The current flow path is shown in Fig. 3 (c). At this point, the inductance of L_1 is still being charged, and the current of L_1 continues to increase. The capacitance C_2 is charged by the input power. The input power, the inductance L_1 and the capacitance C_1 are combined to supply energy to the capacitance C_4 and the load R. The capacitance C_4 also releases energy to the load R, and the inductor current i_{L1} on L_1 continue to decrease. The inductance L_2 is still charged and the current on L_2 continues to increase. When the switch tube S_1 is opened, the converter operates in mode *I* again.

III. Steady-State Performance of the Proposed Converter

A. Voltage Gain and Device Stress in the CCM Mode

The charge is transferred progressively from the input to the output by charging the voltage multiplier stage capacitors. For a converter with three modes (Fig. 3), the voltage gain can be obtained by applying the volt-second equilibrium principle of the boost inductor in a complete working week.

When the switch S_1 is opened, for the inductance L_1:

$$V_{L1}^{I} * T_{1on} = V_{L1}^{II} * T_{1off} \tag{1}$$

Where T_{1on} is the opening time in one cycle S_1, and T_{1off} is the turn off time in one cycle.

From Mode *I* to Mode *III*, it can be seen that:

$$V_{L1}^{I} = V_{in} \tag{2}$$

By (1) and (2), it can be found that:

$$V_{L1}^{II} = \frac{T_{1on}}{T_{1off}} V_{L1}^{I} = \frac{d_1}{1-d_1} V_{L1}^{I} = \frac{d_1}{1-d_1} V_{in} \tag{3}$$

Where d_1 is the switching duty cycle for S_1.

When the switch S_2 is opened, for the inductance L_2:

$$V_{L2}^{I} * T_{2on} = V_{L2}^{II} * T_{2off} \tag{4}$$

Where T_{2on} is the opening time in one cycle for S_2, and T_{2off} is the turn off time in one cycle.

From Modes *I*, *III* and *IV*, it can be seen that:

$$V_{L2}^{I} = V_{in} \tag{5}$$

By (4) and (5), it can be found that:

$$V_{L2}^{II} = \frac{T_{2on}}{T_{2off}} V_{L2}^{I} = \frac{d_2}{1-d_2} V_{L2}^{I} = \frac{d_2}{1-d_2} V_{in} \tag{6}$$

Where d_2 is the switching duty cycle for S_2.

By Mode *II*, it can be seen that the voltage on C_1 is:

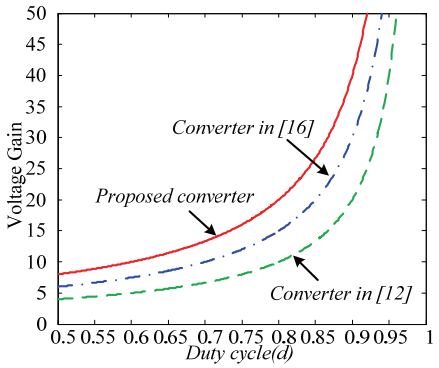

Fig. 4. Voltage gain comparison.

$$V_{C1} = V_{in} + V_{L2}^{II} = V_{in} + \frac{d_2}{1-d_2} V_{in} = \frac{1}{1-d_2} V_{in} \tag{7}$$

Similarly, the expression of the voltage on the capacitor C_2 can be obtained by Mode *IV* as:

$$V_{C2} = V_{in} + V_{L1}^{II} = V_{in} - \frac{d_1}{1-d_1} V_{in} = \frac{1}{1-d_1} V_{in} \tag{8}$$

By mode *IV*, the expression of the voltage on the capacitor C_3 can be obtained as:

$$V_{C3} = V_{in} + V_{L1}^{II} + V_{C1} = V_{in} + \frac{d_1}{1-d_1} V_{in} + \frac{1}{1-d_2} V_{in} \tag{9}$$

In the same way, the expression of the voltage on the capacitor C_4 can be obtained by mode *II* as:

$$V_{C4} = V_{in} + V_{L2}^{II} + V_{C2} = V_{in} + \frac{d_2}{1-d_2} V_{in} + \frac{1}{1-d_1} V_{in} \tag{10}$$

Order $d_1=d_2=d$:

$$V_{C3} = V_{C4} = \frac{2}{1-d} V_{in} \tag{11}$$

According to mode I and mode III, it can be found that the expression of the output voltage is as follows:

$$V_O = V_{C3} + V_{C4} \tag{12}$$

Take formula (11) into the front of the formula:

$$V_O = \frac{4}{1-d} V_{in} \tag{13}$$

Therefore, when the proposed converter operates in the current continuous mode of inductance, the voltage gain is:

$$M_{CCM} = \frac{V_O}{V_{in}} = \frac{4}{1-d} \tag{14}$$

Fig. 4 shows the voltage gain of the proposed converter in the CCM compared with the converters proposed in [16] (n=1) and in [12] under different duty cycles.

During CCM operation, the voltage stresses across S_1, S_2 and D_1~D_4 are written as:

$$V_{S1} = V_{S2} = V_{C1} = V_{C2} = \frac{V_O}{4} \tag{15}$$

$$V_{D1} = V_{D2} = V_{D3} = V_{D4} = V_{C3} = V_{C4} = \frac{V_O}{2} \tag{16}$$

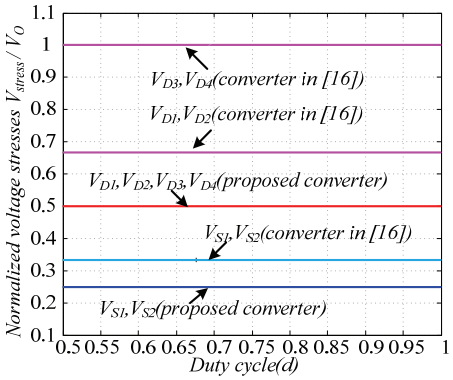

Fig. 5. Normalized voltage stresses of the power components.

Fig. 5 shows a comparison of the normalized voltage stresses of the power components with the converter in [16]. It is concluded that the voltage stress values of the power devices are always lower than the high output voltage. Thus, high-performance power devices, including diodes and switches, can be employed to increase efficiency.

According to the working principle, the current ripples of the inductor can be derived as:

$$\Delta I_{Lm} = \frac{V_{in} dT_S}{L_m} \tag{17}$$

The average currents of I_{C1}, I_{C2}, I_{C3} and I_{CO} are zero in the steady-state. Thus, the average currents of the diodes D_1 and D_3 (I_{D1} and I_{D2}) are equal to $I_{L2,avg}/2$; and the average currents of the diodes D_2 and D_4 (I_{D3} and I_{D4}) are equal to $I_{L1,avg}/2$. The current stresses on S and D_1~D_4 are expressed as:

$$I_{D1(peak)} = I_{D3(peak)} = \frac{\Delta I_{Lm}}{2} + \frac{I_{L2,avg}}{2} \tag{18}$$

$$I_{D2(peak)} = I_{D4(peak)} = \frac{\Delta I_{Lm}}{2} + \frac{I_{L1,avg}}{2} \tag{19}$$

B. Analysis of the Input Current Ripple under the CCM

As shown in Fig. 6(a), at time t_1, the inductance current and the input current can be expressed as:

$$i_{L1}(t_1) = I_{L1,avg} - \frac{(1-d)\Delta i_{L1}}{2d} = \frac{2I_O}{1-d} - \frac{V_{in}(1-d)T_S}{2L_1} \tag{20}$$

$$i_{L2}(t_1) = I_{L2,avg} + \frac{\Delta i_{L2}}{2} = \frac{2I_O}{1-d} + \frac{V_{in} dT_S}{2L_2} \tag{21}$$

$$i_{in}(t_1) = i_{L1}(t_1) + i_{L2}(t_1) = \frac{4I_O}{1-d} + \left(\frac{d}{2L_2} - \frac{1-d}{2L_1}\right) V_{in} T_S \tag{22}$$

The expression of the input current ripple is obtained as:

$$\Delta i_{in} = \left| \left(\frac{d}{2L_2} - \frac{1-d}{2L_1}\right) \right| V_{in} T_S \tag{23}$$

Assuming L_2=nL_1:

$$\Delta i_{in} = \left| \frac{(n+1)d}{n} - 1 \right| \frac{V_{in} T_S}{2L_1} \tag{24}$$

The relationship between the input current ripple and the duty cycle d is given in Fig. 6(b). It can be seen that the inductance value of the converter is designed according to the duty cycle of the converter, and that the zero ripples of the input current can be theoretically realized.

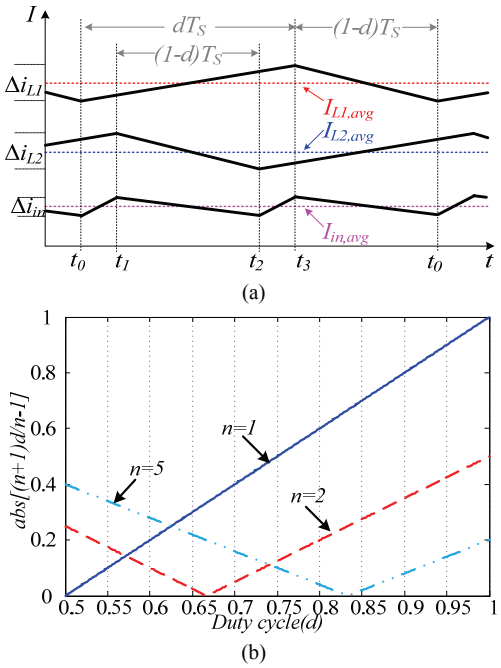

Fig. 6. Input current ripple analysis diagrams.

C. Performance Analysis of the Automatic Balance of the Output Voltage of Two Branches

Assuming the duty cycle of the main switch S_1 is d_1, the duty cycle of the main switch S_2 is d_2, and $d_1 \neq d_2$. In addition, the MOSFET and power diode usually have some voltage drops which should be considered in practical circuit designs. Assuming V_d to be the voltage drops, by applying the voltage-second balance to the inductance, the discharging voltages of L_1 and L_2 can be obtained as:

$$V_{L1}^{disc} = \frac{d_1}{1-d_1}(V_{in} - V_d) \tag{25}$$

$$V_{L2}^{disc} = \frac{d_2}{1-d_2}(V_{in} - V_d) \tag{26}$$

Two voltage-second equations can be rewritten as:

$$d_2 T_S (V_{in} - V_d) + (1-d_2) T_S (V_{in} - V_{C1} - 2V_d) = 0 \tag{27}$$

$$d_1 T_S (V_{in} - V_d) + (1-d_1) T_S (V_{in} - V_{C2} - 2V_d) = 0 \tag{28}$$

The voltages across C_1 and C_2 can be derived as:

$$V_{C1} = \frac{1}{1-d_2} V_{in} - \frac{2-d_2}{1-d_2} V_d \tag{29}$$

$$V_{C2} = \frac{1}{1-d_1} V_{in} - \frac{2-d_1}{1-d_1} V_d \tag{30}$$

When the main switch S_1 is turned off, the output voltage of branch 1 can be derived as:

$$V_{O1} = V_{C3} = V_{in} + V_{L1}^{disc} + V_{C1} - 2V_d = \left(\frac{1}{1-d_1} + \frac{1}{1-d_2}\right)V_{in} - \left(\frac{1}{1-d_1} + \frac{3-2d_2}{1-d_2}\right)V_d \quad (31)$$

Analogously, when the main switch S_2 is turned off, the output voltage of branch 2 can be derived as:

$$V_{O2} = V_{C4} = V_{in} + V_{L2}^{disc} + V_{C2} - 2V_d = \left(\frac{1}{1-d_2} + \frac{1}{1-d_1}\right)V_{in} - \left(\frac{1}{1-d_2} + \frac{3-2d_1}{1-d_1}\right)V_d \quad (32)$$

The output voltage difference between the two branches is:

$$V_{O1} - V_{O2} = 0 \quad (33)$$

According to the voltage–second balance, when the main switches in each branch of the conventional interleaved boost converter have different duty cycles, the branch with the larger duty cycle can output a higher voltage and operates in the continuous current mode. Meanwhile the other branch automatically operates in the discontinuous current mode.

However, since the two branches of the proposed converter have the cross coupling structure of the capacitors C_1 and C_2, the voltage on the output capacitors series C_3 and C_4 can be automatically adjusted according to the duty cycle of the main switch to achieve a new balance. Therefore, the voltage gain of each branch is equal, which effectively suppresses the ripple of the output voltage.

D. Performance Analysis of the Automatic Suppression of Output Voltage Ripple

In order to facilitate analysis and calculation, the change process of the output capacitances of the two branches can be simplified as a linear change as shown in Fig. 7.

At time t_2, the voltage of capacitance and the output voltage can be expressed as:

$$V_{C3}(t_2) = V_{C3,avg} - \frac{(1-d)\Delta V_{C3}}{2d} = \frac{2V_{in}}{1-d} - \frac{I_O(1-d)T_S}{2C_3} \quad (34)$$

$$V_{C4}(t_2) = V_{C4,avg} + \frac{\Delta V_{C4}}{2} = \frac{2V_{in}}{1-d} + \frac{I_O dT_S}{2C_4} \quad (35)$$

$$V_O(t_2) = V_{C3}(t_2) + V_{C4}(t_2) = \frac{4V_{in}}{1-d} + \left(\frac{d}{2C_4} - \frac{1-d}{2C_3}\right)I_O T_S \quad (36)$$

The expression of the output voltage ripple can be obtained by:

$$\Delta V_O = \left|\left(\frac{d}{2C_4} - \frac{1-d}{2C_3}\right)\right| I_O T_S \quad (37)$$

E. Analysis of Soft-Start

At first, the converter is started in the open-loop state with an interleaved duty cycle of 0.5 as shown in Fig. 8. When starting the converter, the output logic value of the timer is 0, and the closed-loop is invalid during this time. In this process,

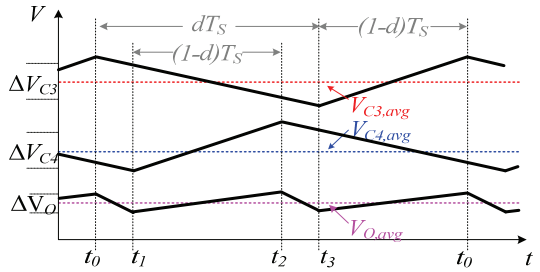

Fig. 7. Output voltage ripple analysis diagram.

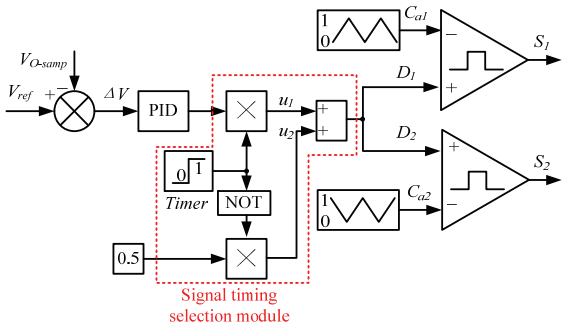

Fig. 8. Soft start control.

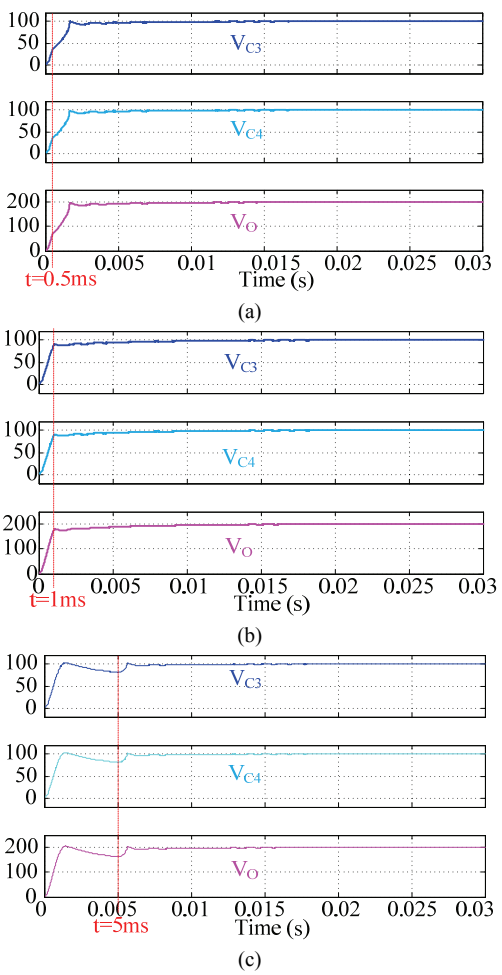

Fig. 9. Simulated waveforms at start-up with different delay times.

the capacitors C_1 and C_4 or C_2 and C_3 are charged like a basic boost converter, and there is no inrush current due to the input inductors. After a certain delay time, which can be designed freely, the output logic value of the timer is 1, and the converter is only operated at the closed-loop as shown in Fig. 8. In addition, there are no inrush currents for the capacitors $C_{1\text{-}4}$ due to the input inductors.

Considering the effect of different delay times, simulated start-up waveforms under different delay times are added as shown in Fig. 9. It can be seen that the capacitors are pre-charged when the duty cycle is 0.5, and that the inrush current can be restrained to a certain extent due to the existence of inductance.

F. Small-Signal Model for Stability Analysis

In order to facilitate modeling analysis, the following assumptions are made. First, the converter works in the CCM. Second, the two inductors are consistent which means inductance L_1=L_2.

The state variables are selected as:

$$x^T=\begin{bmatrix} i_{L1} & i_{L2} & V_{C1} & V_{C2} & V_{C3} & V_{C4}\end{bmatrix},\quad v=\begin{bmatrix}V_{in}\end{bmatrix}.$$

One cycle of the converter can be divided into three states. In each mode of operation, the circuit is linear and its behavior can easily be described by the state-space model given by:

$$\begin{cases}\dot{x}=A_i x+B_i v\\ y=C_i x\end{cases}\qquad i=1,2,3 \tag{38}$$

$$A_1=\begin{bmatrix} \frac{-r_{L1}}{L_1} & 0 & 0 & 0 & 0 & 0\\ 0 & \frac{-r_{L2}}{L_2} & 0 & 0 & 0 & 0\\ 0 & 0 & 0 & 0 & 0 & 0\\ 0 & 0 & 0 & 0 & 0 & 0\\ 0 & 0 & 0 & 0 & \frac{-1}{(R+r_{c3}+r_{c4})C_3} & \frac{-1}{(R+r_{c3}+r_{c4})C_3}\\ 0 & 0 & 0 & 0 & \frac{-1}{(R+r_{c3}+r_{c4})C_4} & \frac{-1}{(R+r_{c3}+r_{c4})C_4}\end{bmatrix}$$

$$B_1^T=\begin{bmatrix}1/L_{m1} & 1/L_{m2} & 0 & 0 & 0 & 0\end{bmatrix} \tag{39}$$

$$C_1=\begin{bmatrix}0 & 0 & 0 & 0 & 1 & 1\end{bmatrix}$$

$$A_2=\begin{bmatrix} \frac{-r_{L1}}{L_1} & 0 & 0 & 0 & 0 & 0\\ 0 & \frac{2r_{L2}+r_{c1}}{2L_2} & \frac{1}{L_2} & 0 & 0 & 0\\ 0 & \frac{1}{2C_1} & 0 & 0 & 0 & 0\\ 0 & \frac{-1}{2C_2} & 0 & 0 & 0 & 0\\ 0 & \frac{-r_{c4}}{2(R+r_{c3}+r_{c4})C_3} & 0 & 0 & \frac{-1}{(R+r_{c3}+r_{c4})C_3} & \frac{-1}{(R+r_{c3}+r_{c4})C_3}\\ 0 & \frac{R+r_{c3}}{2(R+r_{c3}+r_{c4})C_4} & 0 & 0 & \frac{-1}{(R+r_{c3}+r_{c4})C_4} & \frac{-1}{(R+r_{c3}+r_{c4})C_4}\end{bmatrix}$$

$$B_2^T=\begin{bmatrix}1/L_1 & 1/L_2 & 0 & 0 & 0 & 0\end{bmatrix} \tag{40}$$

$$C_2=\begin{bmatrix}0 & 0 & 0 & 0 & 1 & 1\end{bmatrix}$$

$$A_3=\begin{bmatrix} \frac{2r_{L1}+r_{c2}}{2L_1} & 0 & 0 & \frac{-1}{L_1} & 0 & 0\\ 0 & \frac{-r_{L2}}{L_2} & 0 & 0 & 0 & 0\\ \frac{-1}{2C_1} & 0 & 0 & 0 & 0 & 0\\ \frac{1}{2C_2} & 0 & 0 & 0 & 0 & 0\\ \frac{R+r_{c4}}{2(R+r_{c3}+r_{c4})C_3} & 0 & 0 & 0 & \frac{-1}{(R+r_{c3}+r_{c4})C_3} & \frac{-1}{(R+r_{c3}+r_{c4})C_3}\\ \frac{-r_{c3}}{2(R+r_{c3}+r_{c4})C_4} & 0 & 0 & 0 & \frac{-1}{(R+r_{c3}+r_{c4})C_4} & \frac{-1}{(R+r_{c3}+r_{c4})C_4}\end{bmatrix}$$

$$B_3^T=\begin{bmatrix}1/L_1 & 1/L_2 & 0 & 0 & 0 & 0\end{bmatrix} \tag{41}$$

$$C_3=\begin{bmatrix}0 & 0 & 0 & 0 & 1 & 1\end{bmatrix}$$

In the expressions, r_{L1}, r_{L2}, r_{C1} ~ r_{C4} are the parasitic resistors for the inductors (L_1 and L_2) and capacitors (C_1 ~ C_4), respectively. When S_1 and S_2 are switched on, the state-space equation can be expressed as equation (39). After the main switch S_2 is turned off, S_1 is still on, and the state-space equation is expressed as equation (40). When S_1 is turned off, S_2 is on, and the state-space equation is expressed as equation (41).

According to the duty ratios of the three switching states, the following operations are performed.

$$\begin{cases}A=(2d-1)A_1+(1-d)A_2+(1-d)A_3\\ B=(2d-1)B_1+(1-d)B_2+(1-d)B_3\\ C=(2d-1)C_1+(1-d)C_2+(1-d)C_3\end{cases} \tag{42}$$

The state-space averaging equations are obtained as equation (43).

$$A=\begin{bmatrix} \frac{(2-4d)r_{L1}+(1-d)r_{c2}}{2L_1} & 0 & 0 & \frac{1-d}{L_1} & 0 & 0\\ 0 & \frac{(2-4d)r_{L2}+(1-d)r_{c1}}{2L_2} & \frac{1-d}{L_2} & 0 & 0 & 0\\ \frac{d-1}{2C_1} & \frac{1-d}{2C_1} & 0 & 0 & 0 & 0\\ \frac{1-d}{2C_2} & \frac{d-1}{2C_2} & 0 & 0 & 0 & 0\\ \frac{(1-d)(R+r_{c4})}{2(R+r_{c3}+r_{c4})C_3} & \frac{(d-1)r_{c4}}{2(R+r_{c3}+r_{c4})C_4} & 0 & 0 & \frac{-1}{(R+r_{c3}+r_{c4})C_3} & \frac{-1}{(R+r_{c3}+r_{c4})C_3}\\ \frac{(d-1)r_{c3}}{2(R+r_{c3}+r_{c4})C_4} & \frac{(1-d)(R+r_{c3})}{2(R+r_{c3}+r_{c4})C_3} & 0 & 0 & \frac{-1}{(R+r_{c3}+r_{c4})C_4} & \frac{-1}{(R+r_{c3}+r_{c4})C_4}\end{bmatrix} \tag{43}$$

$$B=\begin{bmatrix}1/L_1 & 1/L_2 & 0 & 0 & 0 & 0\end{bmatrix}$$

$$C=\begin{bmatrix}0 & 0 & 0 & 0 & 1 & 1\end{bmatrix}$$

By adding small signal perturbations, that is $X=x+\hat{x}$, $V=v+\hat{v}$, $D=d+\hat{d}$, $Y=y+\hat{y}$ and $\hat{x}\ll x$, $\hat{d}\ll d$, $\hat{v}\ll v$, $\hat{y}\ll y$, the small-signal state-space expression of the converter can be obtained by eliminating the DC terms.

$$\begin{cases}\dot{X}=AX+BX+ED\\ Y=CX\end{cases} \tag{44}$$

Where $E=(2A_1-A_2-A_3)x+(2B_1-B_2-B_3)v$.

The main design parameters of the converter are: input voltage V_{in}=24V, output voltage V_o=200V, output power P_o=200W, switching frequency f=100kHz, duty cycle d=0.6, coupling inductance turn ratio n=1, excitation inductor L_1=L_2=100uH, and capacitances C_1=C_2=47uF, C_3= C_4= 100uF.

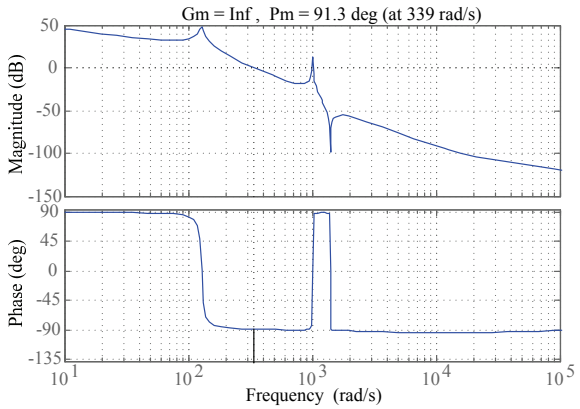

Fig. 10. Bode diagram of a system without compensation.

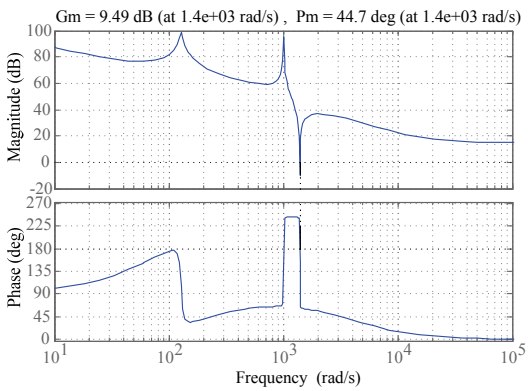

Fig. 11. Bode diagram of a system with compensation.

The expression of the open loop transfer function is:

$$T_v(s)=\frac{0.102(s-1.159\times10^4)(s+1.375\times10^4)}{(s^2+7.84s+1.65\times10^4)}\times\frac{(s^2-1.317s+1.97\times10^6)}{(s^2-3.35s+1.019\times10^6)} \quad (45)$$

A frequency response bode plot is obtained from (45) as shown in Fig. 10.

If the compensator is not introduced into a system, it can be seen from Fig. 10 that the amplitude margin of the system is infinity, the phase angle margin is 91.3° and the cut-off frequency is 339Hz. The system has a positive phase margin, indicating that the system is stable. However, the phase margin is smaller and the stability is poor.

After the compensator was added, the expression of closed-loop transfer function is as follows:

$$T_v(s)=\frac{12.24(0.01s+1)(0.0131s+1)(s-1.159\times10^4)}{s(0.25\times10^{-3}s+1)(s^2+7.84s+1.65\times10^4)}\times\frac{(s+1.375\times10^4)(s^2-1.317s+1.97\times10^6)}{(s^2-3.35s+1.019\times10^6)} \quad (46)$$

The frequency response bode plot is obtained from (46) as shown in Fig. 11.

It can be seen from Fig. 11 that the phase margin of the system is increased to 44.7, the amplitude margin is 9.49 dB and the cut-off frequency is 1.4 kHz after the PID compensator is added. From the above parameters, it can be seen that the stability of the system is improved after adding the PID compensator, and the gain margin is kept within the appropriate range. At the same time, the ability of the system to resist input voltage disturbances and load disturbances is greatly enhanced.

TABLE I
PERFORMANCE COMPARISON OF DIFFERENT CONVERTERS

Topology	Converter in [12]	Converter in [19]	Proposed Converter
Numbers of switches	2	4	2
Numbers of diodes	3	4	4
Number of capacitors	3	5	4
Number of windings	2	5	2
Voltage gain	$\frac{2}{1-d}$	$\frac{2+2n}{1-d}$	$\frac{4}{1-d}$
Voltage stress of switches	$\frac{V_O}{2}$	$\frac{1}{2+2n}V_O$	$\frac{V_O}{4}$
The maximum voltage stress on diodes	$\frac{V_O}{2}$	V_O	$\frac{V_O}{2}$
Ripples of input current	low	low	low
Ripples of output voltage (with same output capacitor)	lower	high	lowest

IV. PERFORMANCE OF COMPARISON

A performance of comparison among the interleaved converters published in [12], [16], [19] and the proposed converter is shown in Table I.

When compared with the converter in [12], the proposed converter doubles the gain while only adding one diode and one capacitor. It also has lower voltage stress and output voltage ripple than the converter in [12]. The converter in [19] achieved a higher voltage gain and soft switching through a coupled inductance technology. However, active or passive clamping circuits are needed to reduce the voltage spikes caused by leakage inductance. The large number of devices reduces the efficiency and is not conducive to improving the power density of the converter. In comparison, the proposed converter has a similar voltage gain, voltage stress and low output voltage ripple while using fewer devices. It is favorable in terms of reliability, circuit volume and cost. Therefore, the proposed converter is a good alternative for applications that require an ultra-step-up voltage gain and a high reliability.

V. DESIGN CONSIDERATIONS

A. Inductor Design

The inductors L_1 and L_2 can be obtained by:

$$L_B=\frac{d(1-d)^2R}{8f_S} \quad (47)$$

TABLE II
PROTOTYPE COMPONENTS AND PARAMETERS

Components	Parameters
Input voltage V_{in}	20~25V
Output voltage V_O	200V
Maximum output power P	200W
Switching frequency f_s	100kHz
Inductor L_1, L_2	100uH
Power switch S_1,S_2	IRFP260N
Diode D_1~ D_4	DSEI30-06A
Capacitors C_1 and C_2	47uF/100V
Capacitor C_3 and C_4	100uF/250V

If the converter is operated in the CCM operation, the inductors L_1 and L_2 should be larger than L_B.

B. Capacitor Design

The capacitor design mainly aims to keep the voltage stresses and fluctuations of the voltage at both ends of the capacitor to within a certain range. The capacitance can be selected by the following formula as:

$$C \geq \frac{P_{\max}}{2 \bullet V_O \bullet \Delta V_C \bullet f_s} \tag{48}$$

VI. EXPERIMENTAL RESULTS

An experimental prototype circuit of the presented converter is built and tested in the laboratory in order to verify the validity of the theoretical analysis. The components used in the converter are shown in Table II.

Figs. 12(a) and 12(b) show waveforms of the currents of the inductors L_1 and L_2 and the input current i_{in}. It can be seen that the currents i_{L1} and i_{L2} are nearly same, and that the input current ripples are very low (ripple rate about 7%) due to the interleaved operation. The theoretical current ripple rate of i_{in} is 5%, which agrees with the experimental result.

Fig. 13 shows the currents of the main switches S_1 and S_2 and the diodes D_1~D_4. Fig. 13(c) shows that the current waveforms and the peak values of the two switches are basically equal. Combined with the current waveforms of the inductors L_1 and L_2 in Fig. 12, it can be concluded that the proposed converter has a better automatic current sharing function.

Figs. 14(a) and 14(b) show waveforms of the voltage stress and current stress of the switches S_1 and S_2 at an output voltage of 200V. Thus, MOSFETs with low on-resistance and low voltage levels can be used. It is useful to reduce the switching losses and to improve efficiency.

Fig. 15(a) and 15(b) show the voltage stresses on the diodes D_1, D_2, D_3 and D_4. It can be seen that the voltage stresses of the diodes D_1, D_2, D_3 and D_4 are approximately 100 V, which is equal to half of the output voltage in the steady-state period.

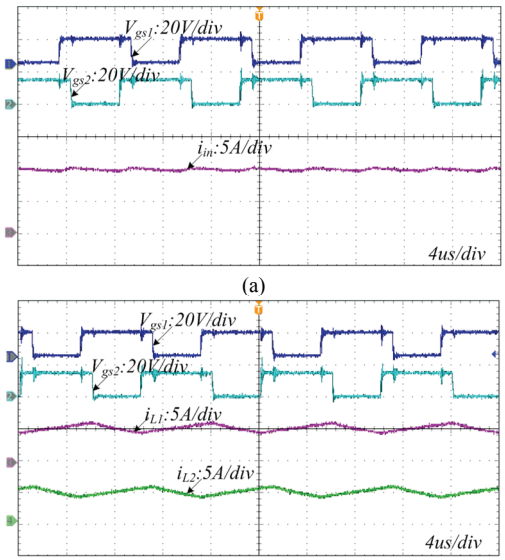

Fig. 12. Waveforms of the currents of inductors.

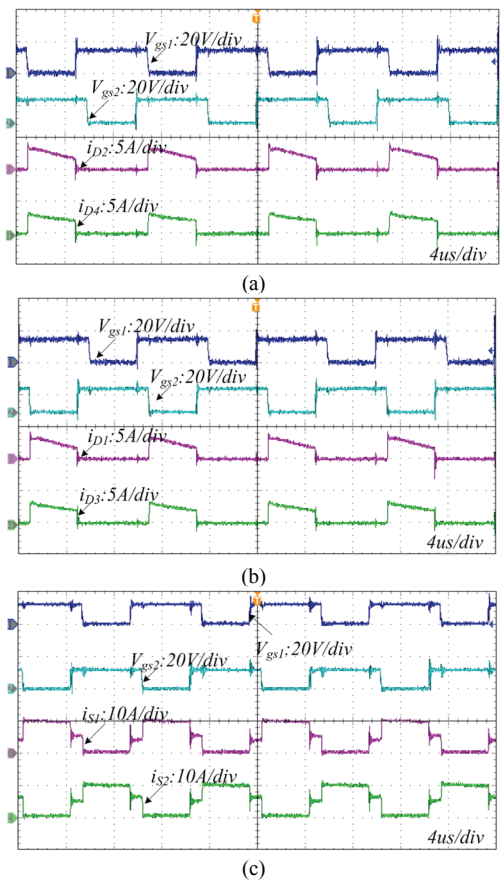

Fig. 13. Current waveforms of the main switches and diodes.

Fig. 16(a) shows the output voltages of the two branches when the main switch duty cycles are d_1=0.65 and d_2=0.6. Fig. 16(b) shows the output voltages of the two branches when the duty cycles are d_1=0.7 and d_2=0.6. According to the Fig. 16(a) and 16(b) it can be found that the output voltages of the two

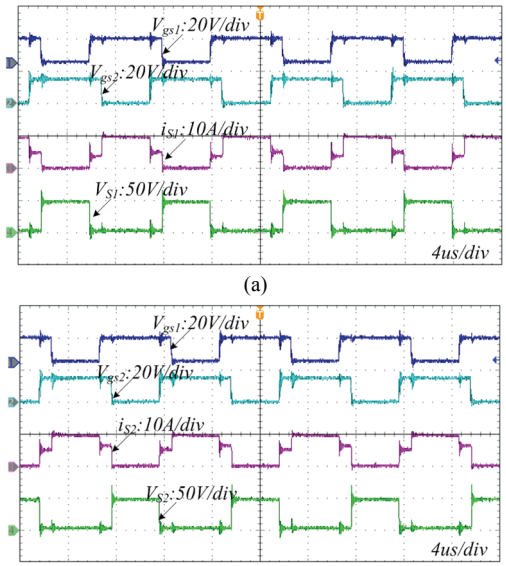

Fig. 14. Waveforms of the voltage current stress of switches.

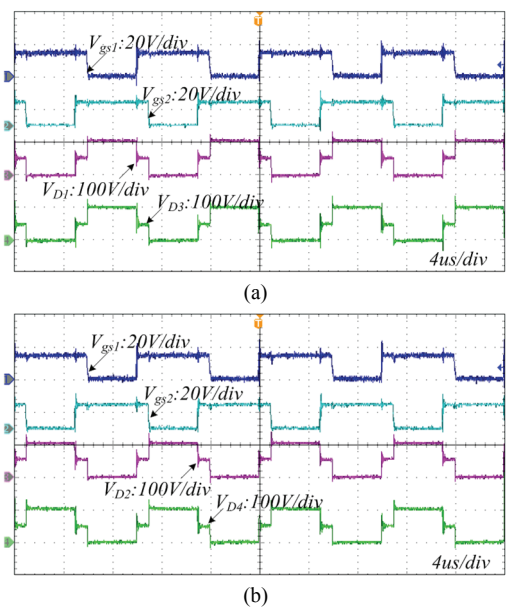

Fig. 15. Waveforms of the voltage stress on diodes.

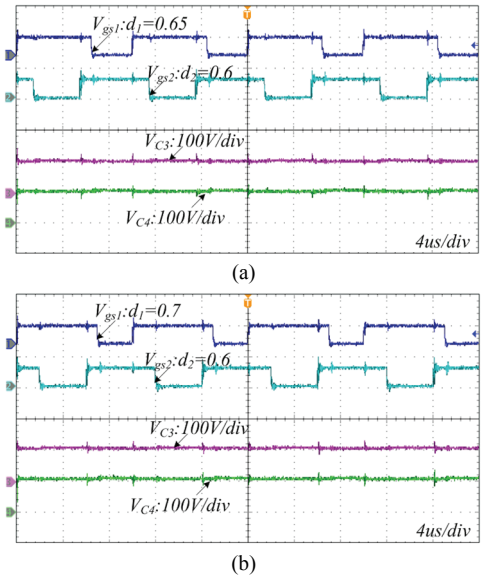

Fig. 16. Output voltages of the two branches at different duty cycles.

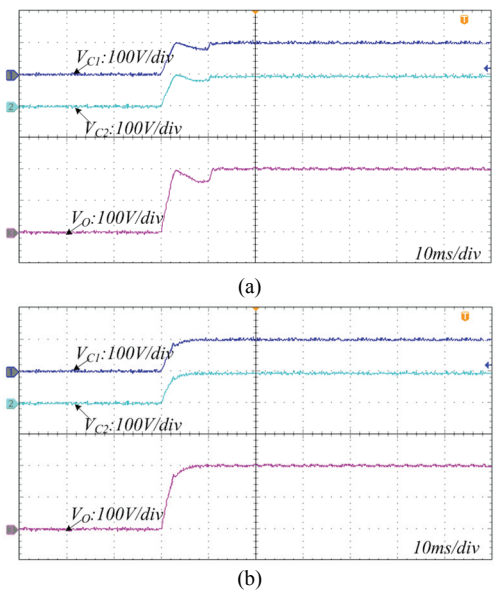

Fig. 17. Waveforms at start-up with different delay times.

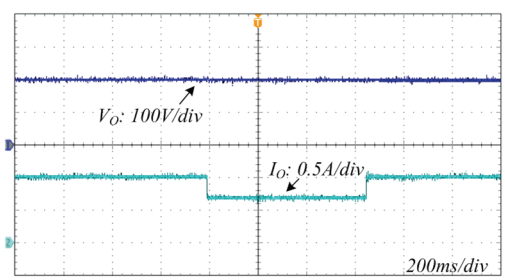

Fig. 18. Experimental waveforms of a step load.

branches are always equal, even if the main switch duty ratios are different. The correctness of the theoretical analysis of the automatic balancing of the two branch output voltages is verified.

Fig. 17(a) shows a soft-start with a too long delay time. Fig. 17(b) shows a soft-start with an appropriate delay time. It can be seen that the different delay times have an obvious influence on the soft-start performance. When the setting of the delay time is appropriate, it can achieve a better soft start effect.

Fig. 18 shows a dynamic response between 200 W and 135 W due to a (200Ω-300Ω-200Ω) step load variation, and the output voltage is maintained at 200V.

Fig. 19 shows the experimental conversion efficiency of the proposed converter when the switching frequency is 100k. The measured maximum efficiency is about 94.37% at half load. When the output power is low, the decrease in efficiency is due to wire loss, drive loss and constant loss.

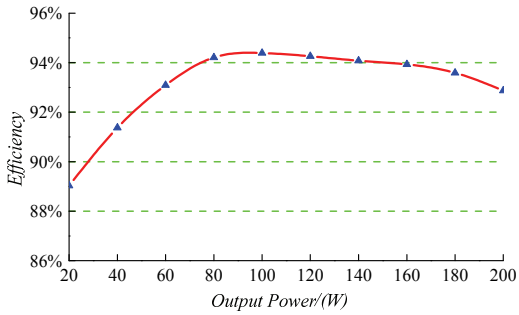

Fig. 19. Efficiency of the proposed converter.

VII. Conclusion

This paper has successfully developed a novel high voltage gain DC–DC converter for low voltage renewable energy systems such as photovoltaic applications. The working principle and steady-state characteristics of the converter are analyzed in detail, and an experimental platform has been developed and tested. The measured maximum efficiency is about 95.7% at half load.

The proposed converter can achieve a high step-up voltage gain and reduce the voltage stress of both the active switches and the diodes, which allows for the use of lower voltage rating MOSFETs and diodes to reduce both the switching and conduction losses. Other characteristics of the converter are: a low output-voltage ripple and a low input-current ripple, which can prevent accelerated reductions it the lifetime of a photovoltaic cell and load. In addition, due to the charge balance of the blocking capacitor, the converter features automatic voltage sharing between C_3 and C_4 without adding any extra circuitry or complex control methods.

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