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Switched Capacitor Based High Gain DC-DC Converter Topology for Multiple Voltage Conversion Ratios with Reduced Output Impedance

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Abstract

This paper presents a switched capacitor (SC) based bidirectional dc-dc converter topology for high voltage gain applications. The proposed converter is able to operate with multiple integral voltage conversion ratios based on user input. The architecture of a user-friendly, inductor-less multi-voltage-gain bidirectional dc-dc converter is proposed in this study. The inductor-less or magnetic-less design of the proposed converter makes it effective in higher temperature applications. Furthermore, the proposed converter has a reduced component count and lower voltage stress across its switches and capacitors when compared to existing SC converters. An output impedance analysis of the proposed converter is presented and compared with popular existing SC converters. The proposed converter is simulated in the OrCAD PSpice environment and the obtained results are presented. A 200 W hardware prototype of the proposed SC converter has been developed. Experimental results are presented to validate the efficacy of the proposed converter.

Key words: Bidirectional, High gain dc-dc converter, Inductor-less, Multi-voltage-gain, Switched capacitor (SC) circuits

I. INTRODUCTION

High voltage gain dc-dc converters are required in many applications such as fuel cells, residential grid connected photovoltaic (PV) systems, high intensity discharge (HID) lamps, electrolyzer (EL) units in hydrogen energy applications, and thermo-electric generators (TEGs). Over the past few decades, residential grid connected PV power systems have become a rapidly growing segment across the globe [1]. However, the voltage level of PV modules is very low when compared to the required voltage level for the dc bus voltage in grid connected PV systems. In order to meet this requirement, the PV series-connected configuration is generally used. However, in this configuration, there is a significant reduction in the generated power due to partial shading conditions and mismatches in the characteristics of PV modules [2]. Therefore, the PV parallel-connected configuration is a more efficient solution when compared to the series-connected configuration in terms of maximizing PV power harvesting [3], [4]. In addition, the low voltage level in the parallel configuration is suitable for meeting the safety standards in residential applications [1]. Since low voltage is generated in the parallel-connected configuration of PVs, step-up dc-dc converters with a high voltage conversion ratio are needed for its integration into the grid. In case of automotive systems, the 12 V battery needs to be boosted up to 100 V to meet the start-up voltage requirements of HID lamps [5]. The electrolyzers used in solar-hydrogen systems to produce hydrogen energy need a dc-dc converter to interface with the dc bus [6]. The front-end converters used in telecom and computer industries make use of 48 V batteries which have to be boosted up to 400 V for the dc bus voltage [7], [8]. In the aforementioned applications, high efficiency high step-up voltage conversion is essential.

Theoretically, the conventional boost converter can attain an infinite voltage gain. However, this is not possible in practice. At a higher duty ratio, the effects of parasitic elements are dominant. Therefore, the voltage gain is sharply reduced as the duty cycle approaches one [9], [10]. To alleviate this, the traditional boost converter is modified by incorporating it

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with additional components such as an inbuilt transformer, coupled inductor or interleaved inductor [11]-[13]. However, this is not suitable for high-power applications since the efficiency decreases considerably at high-power levels. Transformer based isolated converters were presented in [14], [15] to attain a high voltage conversion ratio while maintaining the optimized range of the duty cycle. The high voltage conversion ratio can be attained by increasing the turns ratio of the transformers. However, the energy loss associated with the leakage inductance leads to the reduced efficiency of such converters. The energy loss associated with the leakage inductance can be recycled by using active clamp circuits [16]-[18]. However, these converters have a complicated startup operation and use costly components. In addition, the efficiency is constrained due to the high conduction loss in the active clamp switch.

Furthermore, converters with magnetic elements are bulky and not suitable for high temperature applications. At high temperatures, the magnetic elements are likely to get saturated which brings nonlinearity to the voltage transfer ratio and hence complexity in the control [19], [20]. For these reasons, it is advantageous to use inductor-less converters due to their advantageous properties such as light-weight, high-efficiency and suitability in high temperature applications. The inductor-less converter is commonly referred as a switched capacitor (SC) converter since it consists of only switches and capacitors. Various SC converter topologies have been presented in the literature. The magnetic-less, 42/14 V flying capacitor converter was introduced in [21]. In this converter, the losses associated with the switches and capacitors increased greatly with the voltage conversion ratio. In addition, the control complexity of the converter increases with the voltage gain. Due to these limitations, this is not a suitable candidate for high voltage gain applications. The series-parallel and ladder type SC converters presented in [22], [23], are of high-efficiency and low input current ripple. However, a large number of components is required to obtain a high voltage gain. The Fibonacci SC converter [24], [25] uses fewer components when compared to other SC converters. However, the components of this converter experience a high voltage stress and it requires complex driver circuits. In addition, all of the SC converter topologies found in the literature are for a fixed voltage gain, which limits their applications where multiple voltage gains are required. The switched-capacitor voltage accumulator (SCVA) [26] and switched-diode-capacitor voltage accumulator (SDCVA) [27] can achieve a high voltage gain. However, they both have a low efficiency. An SC converter employing an interleaving feature to decrease the voltage ripple was proposed in [28]. However, the number of required components goes up as the gain increases. A symmetrical modular SC converter, which consists of only two active switches, is reported in [29]. This converter can achieve a high voltage gain with low capacitance requirements. However, its unidirectional property limits its application. Several hybrid SC converters consisting of additional inductors have been proposed to address the above issues [30], [31]. Based on this hybrid configuration, resonance [32] and phase-shift [33] SC converters have been proposed. These converters have higher power densities and improved voltage regulation when compared to traditional magnetic based converters. Nevertheless, they need extra circuitry and a complex control method.

In this study, a multi-stage conversion technique to achieve a high voltage gain is proposed. Based on the proposed technique, a user-friendly, variable voltage gain dc-dc SC converter having five discrete voltage conversion ratios is developed. The main contribution of this paper is the introduction of multiple voltage gains and soft transitions from one voltage level to another voltage level. Its bidirectional power flow capability makes it suitable for battery integrated systems such as telecom applications, hybrid electric vehicles, and fuel cell systems. The presented converter makes use of the basic SC modules used in many SC converter topologies such as multilevel converters, ac-ac converters, and ladder type SC converters [34]-[36].

A steady-state model of a SC converter with a transformer and an equivalent resistance is presented in [37], [38]. In this model, the transformer turns ratio represents the voltage gain of the converter and all of the losses are manifested by the equivalent resistance. The SC converter presented in [39] utilizes the traditional method based on solving differential equations corresponding to different switching states. This method is applicable for analyzing simple SC circuits. A generic method based on the average current model to analyze the dynamic and static performance of an SC converter is proposed in [40]. This method is useful in two-phase SC converters. In [41], the output impedance is calculated in terms of the loop matrix. However, this method requires the solving of a large number of matrix equations. The output impedance of an SC converter decides the output voltage drop and power loss for a given load current [42]. In this paper, a mathematical formulation of output impedance of the proposed converter in terms of the charge multiplier vectors is presented. The remainder of this paper is organized as follows. In section II, the structure and operation of the basic SC module are described. An output impedance analysis of the proposed converter and a comparison with existing SC converters are presented in section III. Section IV introduces the architecture of the proposed user-friendly multi-voltage-gain SC converter. Simulation results are illustrated in section V, and experimental results are presented in section VI to validate the efficacy of a hardware prototype of the converter. Finally, conclusions are drawn in section VII. This paper is the extended version of a prior conference publication [43].

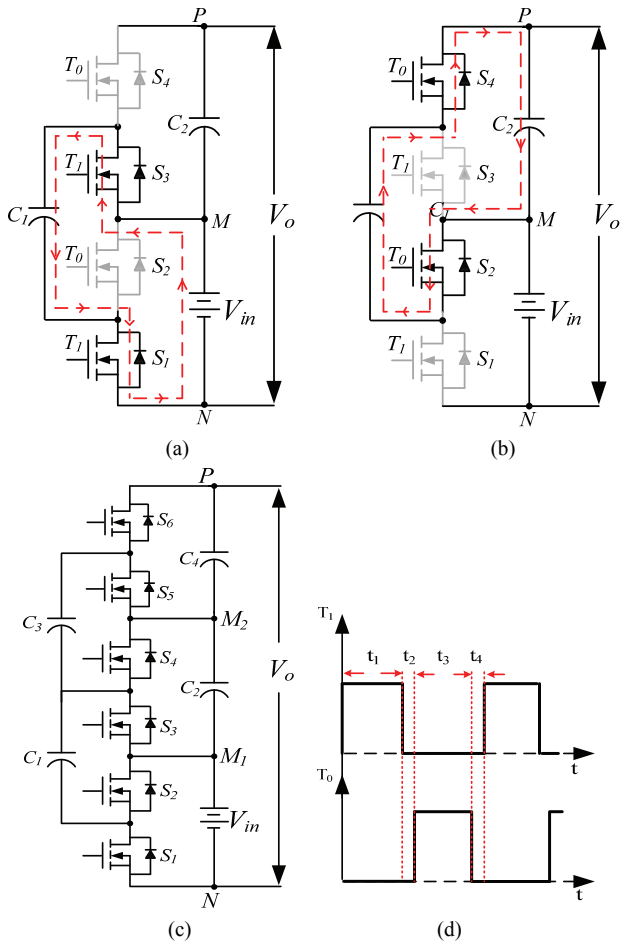

Fig. 1. Diagrams. (a) Current flow path in state-I of a two-times basic SC module. (b) Current flow path in state-II of a two-times basic SC module. (c) Three-times basic module. (d) Complementary PWM switching signals.

II. Basic Modules of the Proposed SC Converter

The two-times and three-times basic SC modules used in the proposed converter, which are extensively used in SC converters [44], [45], are shown in Fig. 1(a) and 1(c), respectively. The voltage gains obtained by the two-times and three-times basic modules are 2 and 3 in the step-up mode; and 1/2 and 1/3 in the step-down mode, respectively.

A. Working of Basic SC Modules

In the step-up mode, the input voltage source is connected between the M and N terminals and the output load is connected between the P and N terminals. Complementary PWM switching signals are depicted in Fig. 1(d). Complementary switching signals are given to alternate switches for the charging and discharging of capacitors. The current flow paths corresponding to the switching sequences are shown in Fig. 1(a) and 1(b). For the time interval t_1, State-I is active, and State-II is active over the time interval of t_3. The time intervals t_2 and t_4 are dead band states, which are introduced to avoid a short circuit of the input voltage source through the switches. In State-I, the switching signal T_1 is 'high' and the signal T_0 is 'low'. In this state the capacitor C_1 is connected in parallel with the input voltage V_{in} and charged by it during the time interval t_1 as illustrated in Fig. 1(a). By the end of this time period, the voltage across the capacitor C_1 becomes equal to the input voltage, i.e.:

$$V_{C_1} = V_{in} \tag{1}$$

In State-II, the switching signal T_1 is 'low' and the signal T_0 is 'high'. In this state, the capacitor C_1 is connected in parallel with the capacitor C_2 as illustrated in Fig. 1(b). During this interval, the capacitor C_1 is discharged to the capacitor C_2 causing the voltage of C_2 to be equal to that of C_1 i.e.:

$$V_{C_2} = V_{C_1} \tag{2}$$

Thus, from (1) and (2):

$$V_{C_2} = V_{in} \tag{3}$$

The output voltage can be expressed as follows:

$$V_{out} = V_{c_2} + V_{in} \tag{4}$$

Therefore, substituting equation (3) into equation (4) yields:

$$V_{out} = 2 \cdot V_{in} \tag{5}$$

Thus, the voltage gain attained by the two-times SC module is 2 in the step-up mode. For the voltage step-down operation, the input voltage is connected between the P and N terminals and the output load is connected between the M and N terminals. Therefore:

$$V_{out} = \left(1/2\right) \cdot V_{in} \tag{6}$$

Hence, the voltage gain of the two-times SC module is $\frac{1}{2}$ in the step-down mode. Similarly, the voltage gains of the three-times SC module, as depicted in Fig. 1(c), are 3 and $\frac{1}{3}$ in the step-up and step-down modes, respectively.

B. Multi-Stage Conversion Technique for a High Voltage Gain

In the proposed technique, two or three basic SC modules are connected back to back to achieve a high gain as shown in Fig. 2. In the subsequent analysis, the two-times and three-times basic SC modules are denoted by the numbers 2 and 3, respectively. For two-stage conversion, there are four possible combinations: 2-2, 2-3, 3-2 and 3-3, where the first number indicates the structure of the first basic SC module and the second number indicates the structure of the second basic SC module in the proposed converter. Similarly, for three-stage conversion, there are eight possible combinations: 2-2-2, 3-2-2, 2-3-2, 2-2-3, 3-3-2, 3-2-3, 2-3-3 and 3-3-3. The input to a constituent basic SC module can be a combination of the capacitor voltages of the previous module. Figure 2(a), 2(b)

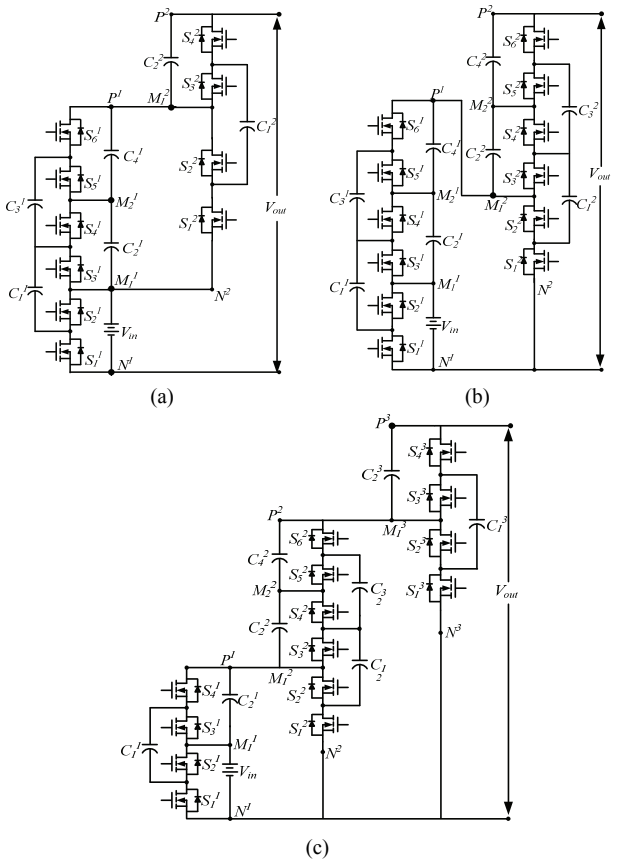

Fig. 2. Diagrams. (a) Two module structure of a 5-times (3-2 configuration) SC converter. (b) Two module structure of a 9-times (3-3 configuration) SC converter. (c) Three module structure of a 12-times (2-3-2 configuration) SC converter.

and 2(c) illustrate the realization of the six-times, nine-times and twelve-times voltage gain SC converters for the 3-2, 3-3 and 2-3-2 configurations, respectively. The converters based on the proposed multi-stage conversion technique can achieve a high voltage conversion ratio and still requires fewer components. In addition, the voltage stress on the switches and capacitors are lower when compared with other SC converters.

C. Comparison of Proposed SC Converter with Basic SC Topologies

The proposed converters are compared with three basic SC topologies: the ladder, series-parallel and Fibonacci SC type converters. As illustrated in Fig. 3(a) and 3(b), the voltage stress experienced by the switches of the proposed converter is somewhat higher than that of ladder-type SC converters. However, the number of power switches required for the proposed SC converter is much lower when compared to the other converters. A comparison of the number of capacitors and the voltage stress of the capacitors with respect to the voltage conversion ratio is illustrated in Fig. 3(c) and 3(d). The Fibonacci SC converter uses a lower number of capacitors than the proposed converter. However, it experiences a very

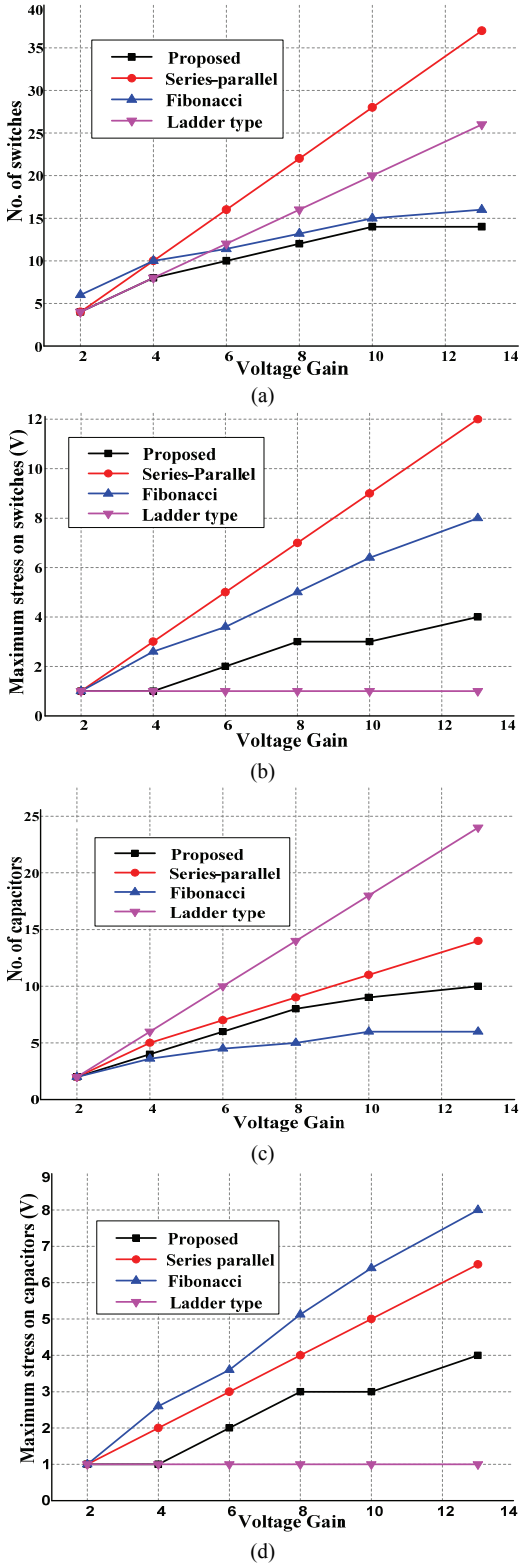

Fig. 3. Comparison graphs. (a) Number of switches. (b) Maximum voltage stress on switches. (c) Number of capacitors. (d) Maximum voltage stress on capacitors vs. voltage gain.

high voltage stress. Thus, from the graphical illustration, it can be inferred that the proposed SC converters are of low cost and light-weight when compared to existing SC topologies.

III. Output Impedance Analysis of the Proposed SC Converter

The output voltage drop and power loss in a switched capacitor circuit are quantified by the output impedance parameter [22], [46].

The definition of the output impedance and its optimization are presented briefly in this paper for the sake of completeness. The output impedance of the proposed converter is derived and compared with the existing SC converters to show its merits.

The output impedance is calculated by the charge flow through each of the components. The charge flows through the capacitors and switches are expressed in terms of output charge as follows:

$$q_c = a_c \cdot q_{out} \qquad q_s = a_s \cdot q_{out} \tag{7}$$

Where a_c and a_s are the capacitor and switch charge multiplier vectors, respectively. The resistive output impedance is a function of the frequency. It has two asymptotic limits, named as the slow switching limit (SSL) and the fast switching limit (FSL).

1) Slow Switching Limit Output Impedance (R_{SSL}): In the SSL, the time duration in each phase is sufficient to fully equilibrate the charge on each of the capacitors. The R_{SSL} is inversely proportional to the switching frequency f_{sw} since the transfer of energy is limited by the capacitive reactance. The R_{SSL} is derived as a function of the capacitor charge multiplier vector [22]. Thus, the average output impedance for the asymptotic limit is given by:

$$R_{SSL} = \frac{V_{out}}{I_{out}} = \sum_i \frac{(a_{ci})^2}{C_i f_{sw}} \tag{8}$$

Where C_i is the capacitance, and a_{ci} is the charge multiplier factor for the i^{th} capacitor.

Output Impedance Optimization in SSL: The optimization of the R_{SSL} is related to the optimized value of the capacitor. Consider the constraint that the summation of the total energy storage capacity of all capacitors is set to E_{total}. This can be expressed as:

$$\sum_i \frac{1}{2}\left(V_{ci,rated}\right)^2 C_i = E_{total} \tag{9}$$

Where $V_{ci,rated}$ is the rated voltage of the i^{th} capacitor.

To minimize the SSL output impedance in (8) by incorporating the constraint (9), the optimization function F is defined as:

$$F = \sum_i \frac{(a_{ci})^2}{C_i f_{sw}} + \lambda\left(\sum_i \frac{1}{2}\left(V_{ci,rated}\right)^2 C_i - E_{total}\right) \tag{10}$$

By minimizing the objective function (10) for C_i, and substituting the value of C_i into (8), the optimized value of the output impedance (R_{SSL}) can be obtained as follows:

$$R^*_{SSL} = \frac{1}{2E_{total} f_{sw}}\left(\sum_i \left|a_{ci} V_{ci,rated}\right|\right)^2 \tag{11}$$

If the converter utilizes the same voltage rating for all of the capacitors, the optimized SSL output impedance of equation (11) is simplified to:

$$R^*_{SSL} = \frac{1}{C_{total} f_{sw}}\left(\sum_i |a_{ci}|\right)^2 \tag{12}$$

2) Fast Switching Limit Output Impedance (R_{FSL}): In the FSL, the 'ON' state resistance of the switches and the other resistances in the circuits dominate. In this asymptotic limit, the time duration in each of the phases is not sufficient to fully equilibrate the capacitors. R_{FSL} is frequency-independent since the energy transfer is limited by the circuit resistance. R_{FSL} is expressed as a function of the switch charge multiplier vector:

$$R_{FSL} = \sum_i \frac{R_i (a_{si})^2}{D_i} \tag{13}$$

Where R_i is the 'ON' state resistance, a_{si} is the charge multiplier factor, and D_i is the duty ratio for the i^{th} switch. If the duty ratio for each of the switches is 0.5, equation (13) is simplified as:

$$R_{FSL} = 2\sum_i R_i (a_{si})^2 = 2\sum_i \frac{(a_{si})^2}{G_i} \tag{14}$$

Where G_i is the conductance of the i^{th} switch.

3) Output Impedance Optimization in FSL: The optimization of the R_{FSL} is related to the switch optimization, which increases the performance of SC converters. The area required for a switch with a blocking voltage of V and a conductance of G is $A_{sw} = GV^2$ [46]. Thus, the total area constraint (A_{total}), related to the cost of the switch, can be expressed as:

$$A_{total} = \sum_i G_i \left(V_{si,rated}\right)^2 \tag{15}$$

Where $V_{si,rated}$ is the rated voltage of the i^{th} switch. With the constraint in equation (15), an optimization function F to minimize the FSL output impedance is defined as:

$$F = \sum_i \frac{2(a_{si})^2}{G_i} + \lambda\left(\sum_i G_i \left(V_{si,rated}\right)^2 - A_{total}\right) \tag{16}$$

By solving equation (16) for the optimized value of G_i, the optimized R_{FSL} can be obtained as:

$$R^*_{FSL} = \frac{2}{A_{total}}\left(\sum_i \left|a_{si} V_{si,rated}\right|\right)^2 \tag{17}$$

If all of the switches have identical voltage ratings, the optimized value of R_{FSL} (from equation (17)) is further simplifies to:

$$R^*_{FSL} = \frac{2}{G_{total}}\left(\sum_i |a_{si}|\right)^2 \tag{18}$$

These parameters give good insight into the performance

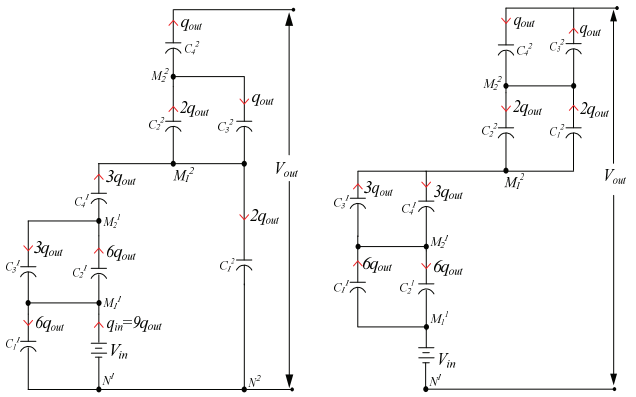

Fig. 4. Charge flow through the capacitors of the proposed SC converter. (a) In phase 1. (b) In phase 2.

of SC converters. Based on the output impedance parameter, a comparison of SC converters with the proposed converter is presented in the next section.

A. Output Impedances of the Proposed SC Converter

The output impedance of the proposed SC converter, operated in the nine-times voltage gain mode (Fig. 2(b)), is obtained in terms of the capacitor and switch charge multiplier vectors. The switches of the converter operate with two phases corresponding to the pair of complimentary gate pulses as shown in Fig. 1(d). The charge multiplier vectors are determined by the flow of the charge using KCL in each phase. The capacitor charge multiplier vector (a_c) is calculated by considering all of the 'ON' state switches and 'OFF' state switches as short-circuited and open-circuited, respectively. Thus, for Fig. 2(b), equivalent circuits showing the flow of the charge through the capacitors in each phase are shown in Fig. 4.

For the nine-times conversion ratio of the proposed converter, $q_{in} = 9q_{out}$. Thus, from Fig. 4(a), the capacitor charge flow vector (q_c) is given by:

$$q_c = \left[-q_{out}\ \ q_{out}-2q_{out}\ \ 2q_{out}-3q_{out}\ \ 3q_{out}-6q_{out}\ \ 6q_{out}\right] \tag{19}$$

Therefore, the capacitor charge multiplier vector (a_c) can be obtained by comparing (19) with (7) as follows:

$$a_c = \left[-1\ \ 1\ -2\ \ 2\ -3\ \ 3\ -6\ \ 6\right] \tag{20}$$

Thus,

$$\sum_i |a_{ci}| = 24 \tag{21}$$

Similarly, the switch charge flow vector (q_s) can be calculated by re-incorporating the switches into the above circuit, which is given by:

$$q_s = \left[-q_{out}\ \ -q_{out}-q_{out}-q_{out}\ \ 2q_{out}\ \ 2q_{out}\ \ -3q_{out}-3q_{out}-3q_{out}-3q_{out}\ \ 6q_{out}\ \ 6q_{out}\right] \tag{22}$$

TABLE I
OUTPUT IMPEDANCE COMPARISON

	Slow Switching limit Impedance (R_{SSL})	Fast Switching limit Impedance (R_{FSL})
MMSCC	$\frac{N^4}{C_{total} f_{sw}}$	$\frac{8(3N-2)^2}{G_{total}}$
SMSCC	$\frac{(N(N-1))^2}{4C_{total} f_{sw}}$	$\frac{8(3N-2)^2}{G_{total}}$
BMSCC	$\frac{(N(N-1))^2}{4C_{total} f_{sw}}$	$\frac{8(3N-2)^2}{G_{total}}$
Proposed converter	$\frac{4\left(\sum_j x^j(2G^j-3)\right)^2}{C_{total} f_{sw}}$	$\frac{32(N-1)^2}{G_{total}}$

N = voltage conversion ratio; G^j = gain of the j^{th} module; x^j = gain product of the subsequent modules.

Thus, the switch charge multiplier vector (a_s) can be obtained by comparing (23) with (7) as follows:

$$a_s = \left[-1\ -1\ -1\ -1\ \ 2\ \ 2\ -3\ \ -3\ -3\ -3\ \ 6\ \ 6\right] \tag{23}$$

Therefore:

$$\sum_i |a_{si}| = 32 \tag{24}$$

Substituting the values of $|a_{ci}|$ and $|a_{si}|$ into (12) and (18), the optimized values of R_{SSL} and R_{FSL} of the proposed SC converter, for the nine-time voltage gain, are obtained as:

$$\begin{cases} R_{SSL} = \dfrac{576}{C_{total} f_{sw}} \\ R_{FSL} = \dfrac{2048}{G_{total}} \end{cases} \tag{25}$$

The generalized expressions for the output impedance of the proposed converter, in terms of the voltage conversion ratio (N), are derived and presented in Table I. In this table, G^j is the gain of the j^{th} module and x^j is the gain product of the subsequent modules of the proposed converter, e.g., for the proposed converter with a 3-3 configuration for a 9-times voltage gain (Fig. 2(b)), $G^1 = 3$, $G^2 = 3$; and $x^1 = 3$, $x^2 = 1$.

A number of SC converter topologies such as the multilevel modular switched-capacitor converter (MMSCC), the symmetric modular switched capacitor converter (SMSCC), and the bridge modular switched capacitor converter (BMSCC) have been reported in the literature [47], [48] and [49], respectively. The output impedances of these converters are listed in Table I.

From the expressions listed in Table I, the output impedances of the above mentioned SC converters are calculated as follows:

$$MMCCC\ (for\ N=8) \begin{cases} R_{SSL} = \dfrac{4096}{C_{total} f_{sw}} \\ R_{FSL} = \dfrac{3872}{G_{total}} \end{cases} \tag{26}$$

TABLE II
COMPONENT COMPARISON FOR SC CONVERTERS

For Gain (N) = 12	No. of capacitors		No. of switch		Total capacitor voltage rating		TDPR	
MMCCC	N (N=1, 2, 3...)	12	$3N$-2	34	$N(N+1)V_{in}/2$	$78V_{in}$	$8(N-1)Pin/N$	$7.33P_{in}$
SMCCC	N (N=2, 4, 6...)	12	$2N$	24	$N(1+N/2)V_{in}/2$	$42V_{in}$	$8(N-1)Pin/N$	$7.33P_{in}$
BMSCC	N (N=4, 8, 12...)	12	N+4	16	$N(1+N/2)V_{in}/2$	$42V_{in}$	$8(N-1)Pin/N$	$7.33P_{in}$
Proposed Converter	$2\sum_j\left(G^j-1\right)$	8	$2\sum_j G^j$	14	$2\sum_j\left(G^j-1\right)V_{in}^j$	$22V_{in}$	$2\sum_j G^jV_{in}^jI_{out}^j$	$12P_{in}$

G^j= gain of the j^{th} module; V_{in}^j= input voltage to the j^{th} module; I_{out}^j = output current of the j^{th} module.

$$SMCCC\ (for\ N=8)\begin{cases}R_{SSL}=\dfrac{784}{C_{total}f_{sw}}\\ R_{FSL}=\dfrac{3872}{G_{total}}\end{cases} \tag{27}$$

$$BMCCC\ (for\ N=8)\begin{cases}R_{SSL}=\dfrac{784}{C_{total}f_{sw}}\\ R_{FSL}=\dfrac{3872}{G_{total}}\end{cases} \tag{28}$$

Thus, the proposed converter has a lower output impedance when compared to the other SC converters, as calculated in (25)-(28). A lower output impedance is evidence of better voltage regulation and efficiency.

The output impedance comparison shows that the proposed converter performs reasonably well in both the SSL and the FSL.

B. Component Comparison with Existing SC Converter Topologies

Table II provides comparisons among the number of capacitors, switch number, total capacitor voltage rating and total device power rating (TDPR) of the proposed converter in terms of voltage gain. The TDPR gives an indication of the semiconductor area required for devices. It depends on the product of the average current flowing through the devices in the 'ON' state and the maximum voltage stress. In this table, N is the voltage conversion ratio, G^j is the gain of the j^{th} module, V_{in}^j is the input voltage to the j^{th} module and I_{out}^j is the output current of the j^{th} module of the proposed converter. Thus, for the 12-times proposed SC converter with a 2-3-2 configuration (Fig. 2(c)), $G^1 = 2$, $G^2 = 3$, $G^3 = 1$; $V_{in}^1 = V_{in}$, $V_{in}^2 = 2V_{in}$, $V_{in}^3 = 6V_{in}$; and $I_{out}^1 = I_{in}/2/2$, $I_{out}^2 = I_{in}/6$, $I_{out}^3 = I_{in}/9$. The comparison shows that the proposed converters require fewer components and lower capacitor voltage ratings when compared to the other SC converters for the same voltage gain. It requires a higher TDPR when compared to three of the SC converters since the current flowing through a constituent module is the input current to the next module. However, in terms of the number of components and the capacitor voltage rating, it is a lot better than the existing converters.

IV. ARCHITECTURE OF THE PROPOSED MULTI VOLTAGE GAIN SC CONVERTER

A user-friendly SC converter, which can produce multiple discrete gains, has been developed as a part of this study. The proposed converter is enabled with five user inputs 'g_n', where 'n' indicates the voltage gain of the converter. For a desired voltage gain, the user has to turn on the corresponding user input g_n. Turning-on and turning-off the user input sets the logic level to '1' ('high') and '0' ('low') at the terminal g_n, respectively. The architecture of the proposed SC converter consists of a power circuit and a control logic circuit as shown in Fig. 5. The power circuit is composed of two three-times basic SC modules, which are connected back to back by means of the bypass switches A, B, C, D and E. The control logic circuit is realized by logic gates, which translates the user inputs into control logic for the bypass switches. The bypass switches enter into the 'ON' state and the 'OFF' state in accordance with the logic levels '1' and '0' at their control terminals, respectively. The user input decides the logic signal level at the control terminal of the bypass switches. A set of logical expressions (29) has been derived to map the user inputs into logic signal levels for the bypass switches. The user inputs and the states of the bypass switches corresponding to desired voltage gains of the converter are presented in Table III.

$$\begin{cases}A &= \left(g_5\cdot\overline{g_6}\right)+g_7+g_9\\ B &= \left(\overline{g_7}\cdot\overline{g_9}\right)\left(g_4\cdot\overline{g_5}+g_6\right)\\ C &= g_5\cdot\overline{g_6}\cdot\overline{g_7}\cdot\overline{g_9}\\ D &= \overline{g_9}\cdot\left(g_7+g_4\cdot\overline{g_5}\cdot\overline{g_6}\right)\\ E &= g_9+\left(g_6\cdot\overline{g_7}\right)\end{cases} \tag{29}$$

In accordance with the user inputs (g_n), the control signal for the bypass switches is automatically generated by logical expressions. The logical expressions are also capable of handling any ambiguity that arises due to the simultaneous selection of more than one user inputs. In this case, the user input, which corresponds to a higher voltage gain, is considered over the other user inputs. For example, if the user inputs g_5, g_6 and g_9 are simultaneously selected (i.e., $g_5 = g_6 = g_9$ = '1'), the converter produces the voltage gain of the nine-

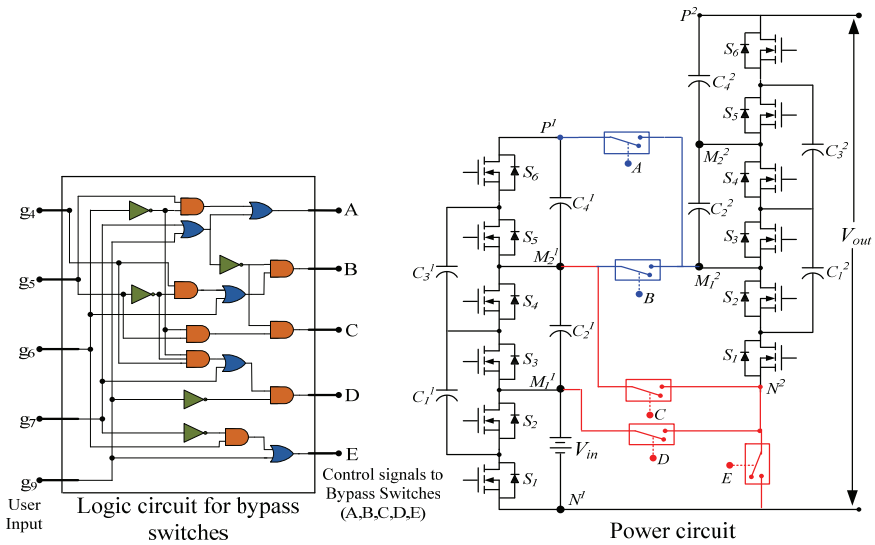

Fig. 5. Architecture of the proposed user-friendly multi-gain SC converter.

TABLE III
USER INPUT AND STATE OF THE BYPASS SWITCHES CORRESPONDING TO THE DESIRED GAINS OF A CONVERTER

Desired gain of the converter	User input	Switches in 'ON' state	Switches in 'OFF' state
4	g4	B and D	A, C, and E
5	g5	A and C	B, D, and E
6	g6	B and E	A, C, and D
7	g7	A and D	B, C, and E
9	g9	A and E	B, C, and D

times the input voltage. Therefore, according to the logic circuit as shown in Fig. 5, A = E = '1' and B = C = D = '0'. Thus, the bypass switches A and E are turned 'ON' and B, C and D are turned 'OFF' to obtain the nine-times voltage gain.

Therefore, the logic circuit enables the proposed converter to operate in the variable voltage conversion mode. The proposed converter can operate in five discrete voltage gain modes: four-times, five-times, six-times, seven-times and nine-times. Basically, the state of the bypass switches decides the input voltage applied to the second module of the converter. Meanwhile, the input voltage applied to the first module of the converter is always equal to V_{in}. Therefore, $V_{C_4^1} = V_{C_2^1} = V_{in}$ and $V_{C_4^2} = V_{C_2^2} =$ input voltage applied to the second module (across the M_1^2 and N^2 terminals). The five modes of operation are briefly explained as follows.

Four-times mode: When the user input g_4 is 'ON' and g_5, g_6, g_7 and g_9 are 'OFF', the converter operates in the four-times mode. According to the logical expressions as mentioned above, the bypass switches B and D are turned 'ON' while A, C and E are turned 'OFF'. Therefore, the capacitor voltage $V_{C_2^1}$ acts as an input to the second module. The equivalent circuit of this mode is shown in Fig. 6. From this circuit, the output voltage of the converter in this mode is equal to:

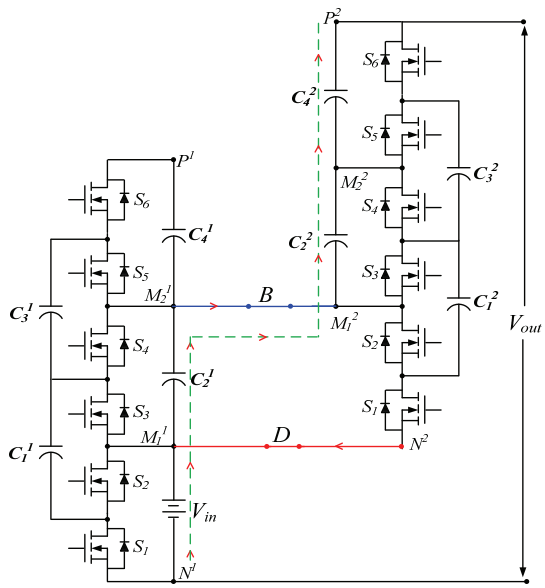

Fig. 6. Equivalent circuit of a converter in the four-times mode of operation.

$$V_{out} = V_{in} + V_{c_2^1} + V_{c_2^2} + V_{c_4^2} \tag{30}$$

In this case, $V_{C_4^2} = V_{C_2^2} = V_{C_2^1} = V_{in}$. Therefore:

$$V_{out} = 4 \cdot V_{in} \tag{31}$$

Five-times mode: When the user input g_5 is 'ON' and g_6, g_7 and g_9 are 'OFF', the converter operates in the five-times mode. It is worth noting that the state of g_4 does not matter since g_5 is already selected. In this case, the bypass switches A and C enter the 'ON' state while B, D and E enter the 'OFF' state. Therefore, the capacitor voltage $V_{C_4^1}$ acts as an input to the second module. The equivalent circuit of this mode is shown in Fig. 7. From this circuit, the output voltage of the converter in this mode is equal to:

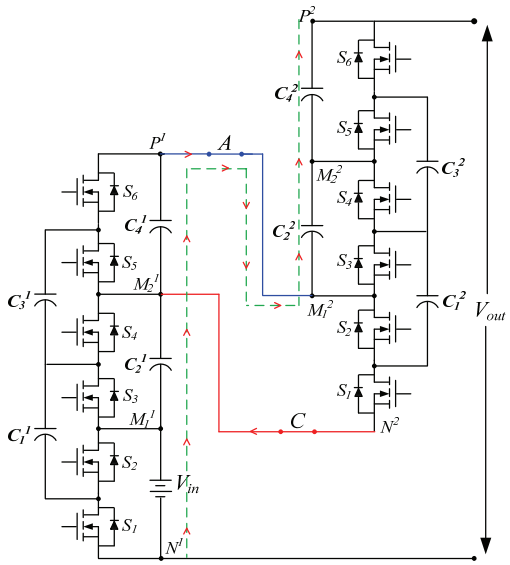

Fig. 7. Equivalent circuit of the converter in the five-times mode of operation.

$$V_{out} = V_{in} + V_{c_2^1} + V_{c_4^1} + V_{c_2^2} + V_{c_4^2} \tag{32}$$

In this case, $V_{C_4^2} = V_{C_2^2} = V_{C_4^1} = V_{C_2^1} = V_{in}$. Therefore:

$$V_{out} = 5 \cdot V_{in} \tag{33}$$

Six-times mode: When the user input g_6 is 'ON' and g_7 and g_9 are 'OFF', the converter operates in the six-times mode. When g_6 is already selected, the states of g_4 and g_5 do not matter. In this mode, the bypass switches B and E are turned 'ON' while A, C and D are turned 'OFF'.

Therefore, the capacitor voltage $V_{C_2^1}$ together with the input voltage V_{in} (i.e., $2V_{in}$) acts as an input to the second module. The equivalent circuit of this mode is shown in Fig. 8. The output voltage of the converter in this mode is equal to:

$$V_{out} = V_{in} + V_{c_2^1} + V_{c_2^2} + V_{c_4^2} \tag{34}$$

In this case, $V_{C_4^2} = V_{C_2^2} = 2V_{in}$, and $V_{C_2^1} = V_{in}$. Therefore:

$$V_{out} = 6 \cdot V_{in} \tag{35}$$

Seven-times mode: When the user input g_7 is 'ON' and g_9 is 'OFF', the converter operates in the seven-times mode. When g_7 is already selected, the states of g_4, g_5 and g_6 do not matter. In this mode, the bypass switches A and D enter into the 'ON' state while B, C and E enter the 'OFF' state. Therefore, the capacitor voltages $V_{C_2^1}$ and $V_{C_4^1}$ together (i.e., $2V_{in}$) act as an input to the second module. The equivalent circuit of this mode is shown in Fig. 9. The output voltage of the converter in this mode is equal to:

$$V_{out} = V_{in} + V_{c_2^1} + V_{c_4^1} + V_{c_2^2} + V_{c_4^2} \tag{36}$$

In this case, $V_{C_4^2} = V_{C_2^2} = 2V_{in}$, and $V_{C_4^1} = V_{C_2^1} = 2V_{in}$. Therefore:

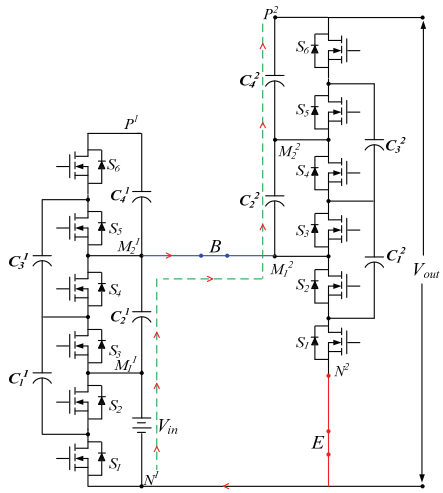

Fig. 8. Equivalent circuit of the converter in the six-times mode of operation.

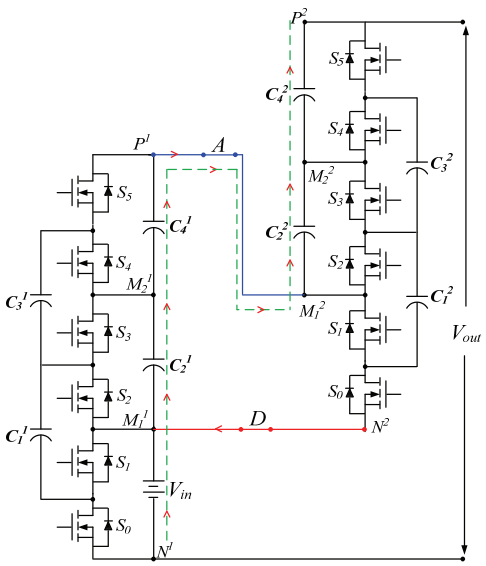

Fig. 9. Equivalent circuit of the converter in the seven-times mode of operation.

$$V_{out} = 7 \cdot V_{in} \tag{37}$$

Nine-times mode: When the user input g_9 is 'ON', the converter operates in the nine-times mode irrespective of the state of the other inputs. In this case, the bypass switches A and E are closed ('ON') while B, C and D are open ('OFF').

Therefore, the capacitor voltages $V_{C_2^1}$, $V_{C_4^1}$ and the input voltage V_{in} combined (i.e., $3V_{in}$) act as the input to the second module. An equivalent circuit of this mode is shown in Fig. 10. From this circuit, the output voltage of the converter in this mode is equal to:

$$V_{out} = V_{in} + V_{c_2^1} + V_{c_4^1} + V_{c_2^2} + V_{c_4^2} \tag{38}$$

In this case, $V_{C_4^2} = V_{C_2^2} = 3V_{in}$ and $V_{C_4^1} = V_{C_2^1} = V_{in}$. Therefore:

$$V_{out} = 9 \cdot V_{in} \tag{39}$$

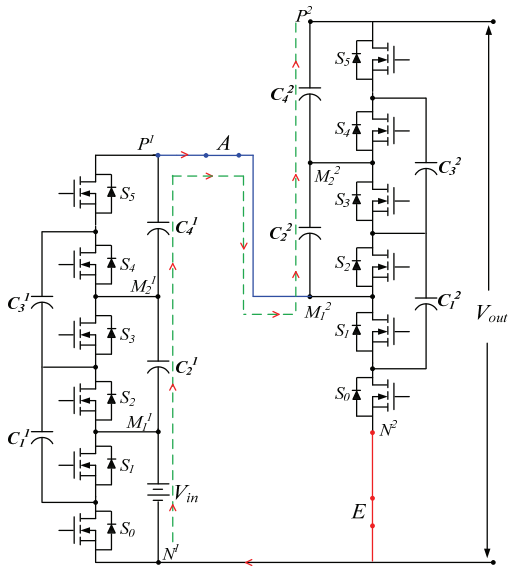

Fig. 10. Equivalent circuit of the converter in the nine-times mode of operation.

V. Simulation Results

The proposed multi-voltage-gain SC converter has been simulated in the OrCAD PSpice environment. A 200 W load was considered for the simulation. Square pulses of 50-kHz frequency at a 50% duty ratio were generated by a 555 Timer IC. Each of the capacitors was 60 μF. For the step-up mode of operation, a 30 V input voltage source is connected between the terminals M_1^1 and N^1 (low voltage side terminals) while output is taken across the terminals P^2 and N^1 (high voltage side terminals). Various voltage waveforms of the converter, when operated in the step-up mode of operation, are shown in Fig. 11(a)-(c). The transition of the output voltage from one voltage level to another, in accordance with the user input, can be observed in Fig. 11(a).

As illustrated in Fig. 11(a), the user input g_4 is selected (i.e., 'ON') at $t = 0$.

Thus, the converter enters into four-times mode, which results in the voltage conversion ratio of the four-times the input voltage. Similarly, at 2 sec., 4 sec., 6 sec. and 8 sec., the user inputs g_5, g_6, g_7 and g_9 are triggered for the five-times, six-times, seven-times and nine-times voltage conversion ratios, respectively. Fig. 11(b) and 11(c) show the voltage stress across the switches and capacitors of the constituent modules of the converter in different modes of operation. From Fig. 11(b), it can be seen that the voltage stress across the switches and capacitors of the first constituent module of the converter is equal to the source voltage (V_{in}), irrespective of the mode of operation. Meanwhile, Fig. 11(c) indicates that the maximum voltage stress across the components of the second constituent module is three-times the source voltage when it is operated in the nine-times voltage gain mode. Similarly, for the step-down mode of operation, a 270 V input source is connected between the high voltage side terminals

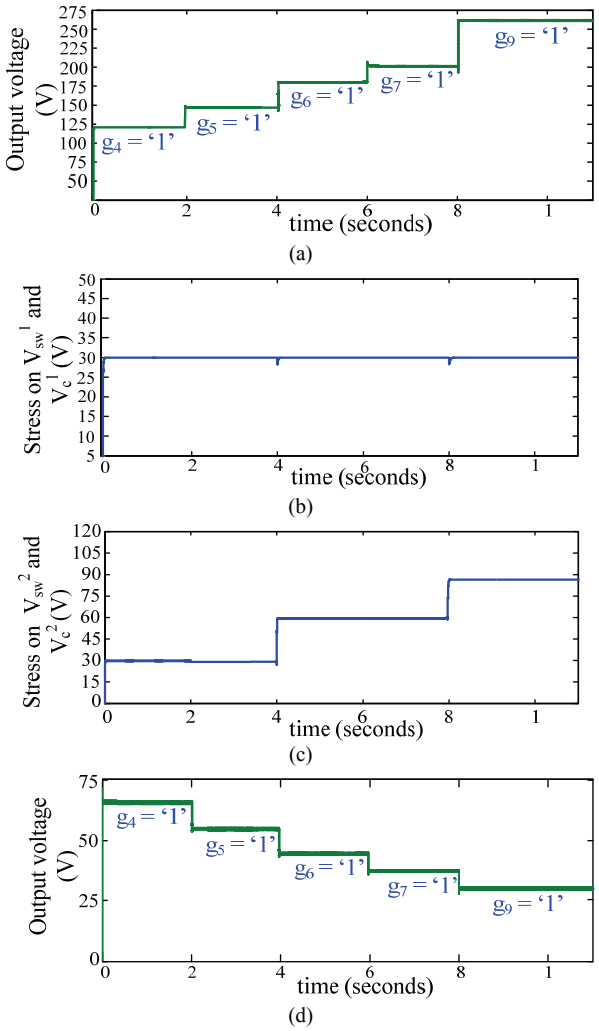

Fig. 11. Voltage waveforms in different mode of operation. (a) Output voltage in the step-up mode. (b) Switch voltage and capacitor voltage of the first constituent module. (c) Switch voltage and capacitor voltage of the second constituent module. (d) Output voltage in the step-down mode.

while the output is taken across the low voltage side terminals. Fig. 11(d) shows the transitions of the voltage levels in accordance with the user input when the converter is operated in the step-down mode of operation. As shown in this figure, the user inputs g_4, g_5, g_6, g_7 and g_9 are enabled for the voltage gains of 1/4, 1/5, 1/6, 1/7 and 1/9, respectively.

In order to analyze the dynamic response performance of the proposed converter, the load is varied between full load and no load, and the obtained output voltage waveform is presented in Fig. 12. The dynamic response shows that the response time of the converter is less than 5 ms.

Fig. 13 shows the responses of different converters when the load is varied between no load to full load. From the waveform, it can be seen that the output voltage drop from no load to full load is lower in the proposed converter when compared to the other SC converters. Thus, the proposed converter provides better voltage regulation.

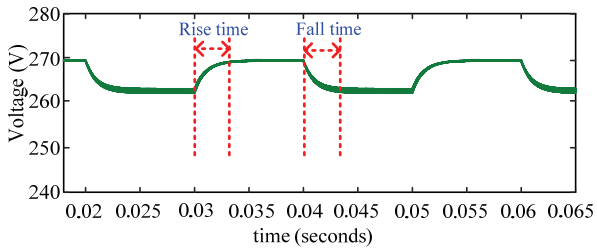

Fig. 12. Dynamic response of the proposed converter.

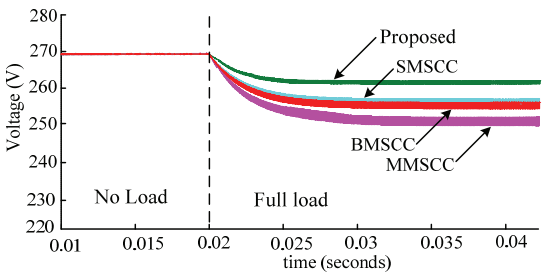

Fig. 13. Drop in output voltage when the load changes from no load to full load.

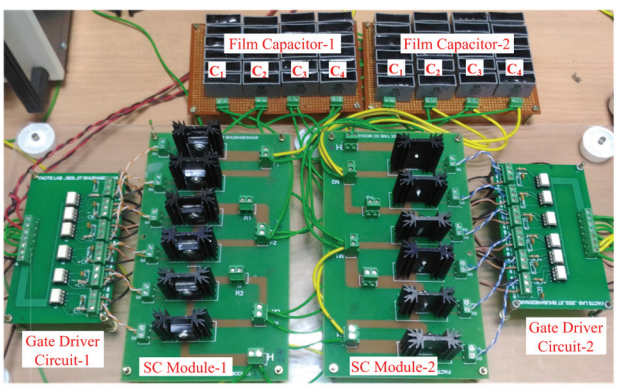

Fig. 14. 200 W hardware prototype of the proposed converter.

VI. Experimental Results

A 200 W laboratory prototype of the proposed converter has been built, and experiments were carried out to verify its performance. A photograph of the prototype is shown in Fig. 14.

A. Capacitor Design

The load is supplied by the series output capacitors of the second constituent module of the converter. The average current supplied to the load by the output capacitors is I_{out}, where I_{out} is the load current. The voltage ripples of the capacitors are given by:

$$\Delta V_C = \frac{I_{out} T_s}{C} \tag{40}$$

Where, $T_s = \frac{1}{f_s}$, and f_s is the switching frequency. Since, $I_{out} = \frac{P_{out}}{V_{out}}$, the value of the capacitance can be expressed as:

$$C = \frac{P_{out}}{V_{out} f_s \Delta V_C} \tag{41}$$

In the prototype, the input voltage is taken as 30 V, the operating frequency is 50 kHz, and the ripple voltage is set to 0.5 % of the output voltage. Therefore, from (41), the required value of the capacitance, when the converter is operated in the four-times mode is found to be 55.5 μF. In the prototype, each of the capacitors C_1, C_2, C_3 and C_4 of the converter is composed of six paralleled 10 μF film capacitors (MPERRB 10.0/K/100). The MOSFETs used in the proposed converter are SiHG20N50C. The ICs (TLP250H) are used for the gate driver circuits of the MOSFETs. Voltage regulators ICs (L7812) are used for the driver power supply. The converter operates at a 50 kHz switching frequency. This requires a pair of complementary pulses of a 50 % duty ratio, which are generated by a C2000 microcontroller. Various voltage waveforms of the experimental results are shown in Fig. 15 with a 30 V input voltage. Waveforms of the input-output voltage and the voltage stress across the capacitors are shown in Fig. 15(a) - 15(e), for different modes of operation. In the figures, V_{in}, V_{out}, V_c^1 and V_c^2 indicate the input voltage, output voltage, voltage stress on the capacitors of the first module and voltage stress on the capacitors of the second module of the converter, respectively. Figure 15(a), 15(b), 15(c), 15(d) and 15(e) represent various voltage waveforms of the proposed converter in four-times, five-times, six-times, seven-times and nine-times voltage gain modes, respectively. These experimental results indicate that the maximum voltage stress across the capacitor is equal to the input voltage, when it is operated in the four-times and five-times modes; twice the input voltage when it is operated in the six-times and seven-times modes; and thrice the input voltage when it is operated in the nine-times mode.

The input and output currents of the converter for a 200 W load, are shown in Fig. 15(f). In this figure, V_{gs} is the gate drive signal, I_{in} is the input current, and I_{out} is the output current of the converter. The converter is made to operate in the nine-times mode. The average input current drawn by the converter is 6.75 A for an average load current of 0.75 A. The dynamic response of the proposed converter showing the rising time and falling time is depicted in Fig. 16. The waveform shows that the response time of the proposed converter is around 5 ms.

Fig. 17 shows experimental waveforms of the transition of voltage levels when the converter operates in different voltage gain modes, in accordance with user inputs. Voltage transitions in the step-up and step-down operation are shown in Fig. 17(a) and 17(b), respectively.

The measured voltage regulation and overall efficiency of the converter for different voltage gain modes of operation are shown in Fig. 18. It can be seen from the curve that the proposed converter has maximum efficiency when it is operated in the six-times mode. In addition, it has minimum

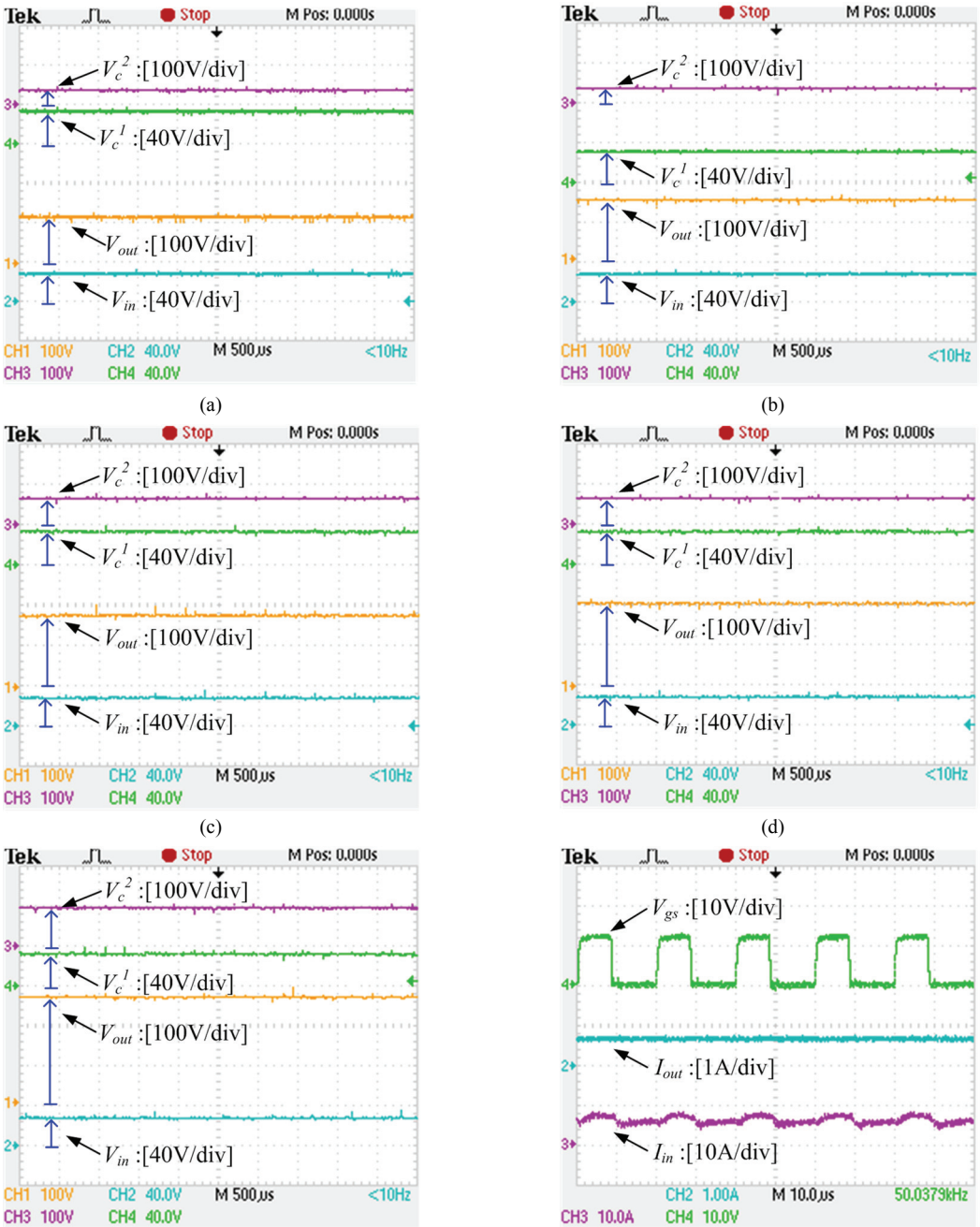

Fig. 15. Voltage waveforms of the converter at a 50-kHz switching frequency and a 30 V input voltage. (a) In four-times mode. (b) In five-times mode. (c) In six-times mode. (d) In seven-times mode. (e) In nine-times mode. (f) Gate drive voltage and current waveforms of the converter.

efficiency when it is operated in the four-times mode. If ON-state voltage drops of the switches are taken into account, there is a net voltage drop in the output capacitor voltages. Since the output capacitor voltages of the first module act as a voltage source to the second module of the proposed converter, the cumulative effect of the switch voltage drop is reflected in the output voltage of the proposed converter. The per unit voltage drop of the proposed converter is calculated by the equivalent circuit in each mode of operation. It is found that the per unit voltage drop of the proposed converter is minimum when operated in the six-times mode, and maximum in the four-times mode when compared to the other modes of operation. This can be seen by the voltage regulation curve of the proposed converter in Fig. 18. In addition, there is power loss associated with the per unit voltage drop due to the cumulative voltage drops of the switches. Therefore, the efficiency curve follows the voltage regulation curve. This curve shows that the overall achievable

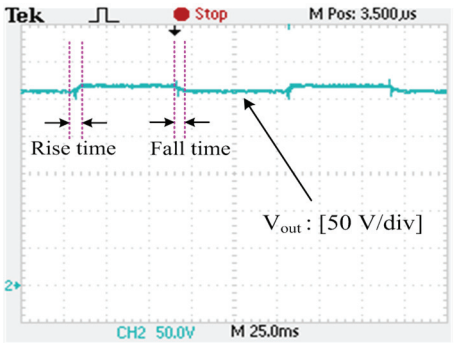

Fig. 16. Experimental waveform showing the dynamic response of the converter in the nine-times mode at a 30 V input.

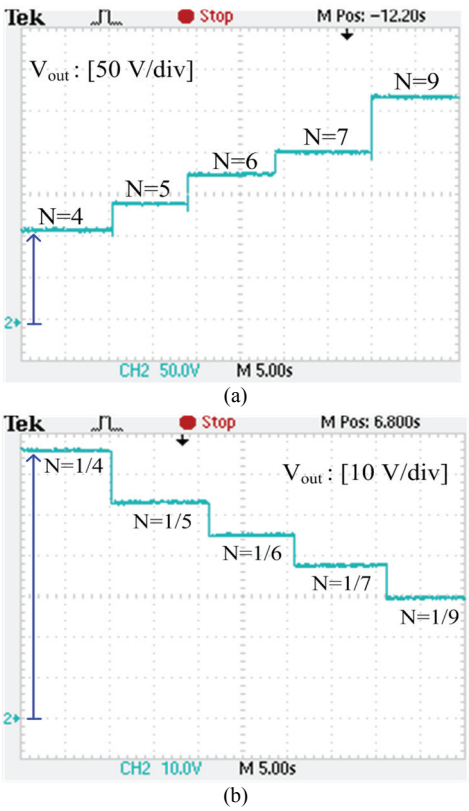

Fig. 17. Experimental waveforms showing transitions of the voltage levels in different voltage gain (N) modes. (a) For step-up operation ($V_{in} = 30V$). (b) For step-down operation ($V_{in} = 270V$).

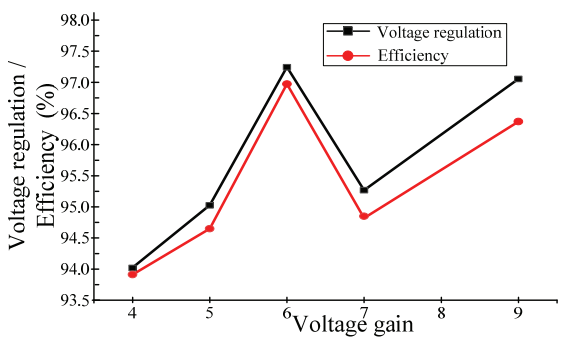

Fig. 18. Measured voltage regulation and efficiency curves of the prototype.

efficiency, including driver loss, is more than 97 %.

The percentage drop in voltage, from no load to full load, is as low as 3 %. Therefore, the converter is able to operate in the variable voltage gain mode without compromising the efficiency or the voltage regulation.

VII. Conclusions

A user-friendly, inductor-less bidirectional SC converter, having a variable voltage gain, has been proposed. The distinct feature of the proposed converter, when compared to other popular SC converters, is its ability to work with multiple voltage conversion ratio modes. A logic circuit has been developed to obtain multiple voltage conversion ratios in accordance with user inputs. The proposed converter has many advantages including compact size, lightweight, and high efficiency. In addition, the magnetic-less design makes it a suitable candidate for high temperature applications. Simulation and experimental results are presented to validate the performance of the converter. The voltage regulation of the converter prototype, obtained from experimentation, is less than 3%. The response time of the converter is as low as 5 ms. The proposed converter has a lower output impedance in both the SSL and the FSL when compared with existing SC topologies.

Acknowledgment

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