

Investigations of Multi-Carrier Pulse Width Modulation Schemes for Diode Free Neutral Point Clamped Multilevel Inverters

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Abstract

Multilevel Inverters (MLIs) are widely used in medium voltage applications due to their various advantages. In addition, there are numerous types of MLIs for such applications. However, the diode-less 3-level (3L) T-type Neutral Point Clamped (NPC) MLI is the most advantageous due to its low conduction losses and high potential efficiency. The power circuit of a 3L T-type NPC is derived by the conventional two level inverter by a slight modification. In order to explore the MLI performance for various Pulse Width Modulation (PWM) schemes, this paper examines the operation of a 3L (five level line to line) T-type NPC MLI for various types of Multi-Carriers Pulse Width Modulation (MCPWM) schemes. These PWM schemes are compared in terms of their voltage profile, total harmonic distortion (THD) and conduction losses. In addition, a 3L T-type NPC MLI is also compared with the conventional NPC in terms of number of switches, clamping diodes, main diodes and capacitors. Moreover, the capacitor-balancing problem is also investigated using the Neutral Point Fluctuation (NPF) method with all of the MCPWM schemes. A 1kW 3L T-type NPC MLI is simulated in MATLAB/Simulink and implemented experimentally and its performance is tested with a 1HP induction motor. The results indicate that the 3L T-type NPC MLI has better performance than conventional NPC MLIs.

Key words: 3-level inverter, FPGA, Multi-carrier pulse width modulation, Multilevel inverter, Pulse width modulation, Total harmonic distortion, Xilinx system generator

I. INTRODUCTION

Concerns about climate change are increasing the level of

interest in renewable energy systems such as wind and solar technologies [1]-[3]. These days, photovoltaic (PV) systems should be three-phase grid tied. To attain advantages such as lower weight, size and cost as well as higher efficiency, PV systems generally do not have transformers. However, this method creates the problem of inverter common-mode voltage (CMV), which generates leakage current flowing through the PV panel to the ground. To avoid this problem, a split DC link method is more efficient since it naturally avoids common-mode (CM) component circulation. MLIs are highly suitable for such PV systems. MLIs have attracted a great deal of

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interest over the last two decades due in part to their wide ranges of voltage and current ratings [4]-[10]. MLIs can be categorized into three basic types. These three types are NPC MLIs [5], Flying Capacitor MLIs [6] and Cascaded H-bridge MLIs [7]. All of these topologies have some disadvantages. For instance, the NPC-MLI requires more clamping diodes, the Flying Capacitor MLI requires more maintenance for the capacitors, and the Cascaded H-bridge MLI required a number of isolated DC sources. To overcome the drawbacks a 3-Level (3L) T-type NPC MLI was proposed in [11]-[19]. This inverter is referred to as T-type because the switches in each of the legs are arranged in the shape of the letter ‘T’ as shown in Fig. 1. The switches in a 3L T-type MLI are of two different ratings. The ratings of the switches S_{a1} and S_{a4} are four times the ratings of the switches S_{a2} and S_{a3} . In any operating mode, the switches S_{a2} and S_{a3} with anti-parallel diodes form a series combination reducing the required rating by four times ($V_{DC}/4$). Only one switch is activated from one leg to generate the positive and negative cycles. This decreases the conduction losses and increases the efficiency [19]. The operation of the 3L T-type MLI is described in section II.

Generally, three pulse width modulation (PWM) strategies are available for MLIs.

- Multi-carrier PWM
- Space Vector (SV) PWM
- Selective Harmonic Elimination (SHE) PWM

The Carrier Based PWM (CB-PWM) was first proposed in 1992 [20]. This method helps to attain a better voltage profile and a lower THD. However, it leads to power quality issues. To overcome this drawback the SHEPWM was introduced for MLIs, which is able to operate at higher levels (>3) and with modulation indexes [21]. However, this technique requires a lower switching frequency to reduce the switching losses. Thus, to overcome these drawbacks, the SVPWM was introduced, which is able to provide a lower harmonic and the best voltage profile among the PWM strategies [22]. The most common problems associated with MLIs include capacitor balancing problems, unbalancing of the split capacitors, which leads to increased voltage stresses, non-uniform switching, increased THD and development of circulating currents [23], [24], [29]-[31]. In this paper, Multi-Carrier PWM schemes are designed to avoid all of the above drawbacks by providing the maximum possible capacitor balancing. The capacitor balancing is calculated using the neutral point fluctuation (NPF) method. A comparative analysis of capacitor balancing is carried out for a T-type NPC MLI with various types of multi-carrier PWM schemes at the maximum modulation index (M_a). The main objective of this paper is to investigate the different available Multi-Carrier PWM schemes and their performance when compared with the T-type MLI for harmonic compensation and fundamental improvement [25], [26].

3-Level (3L) T-type MLIs are established technologies

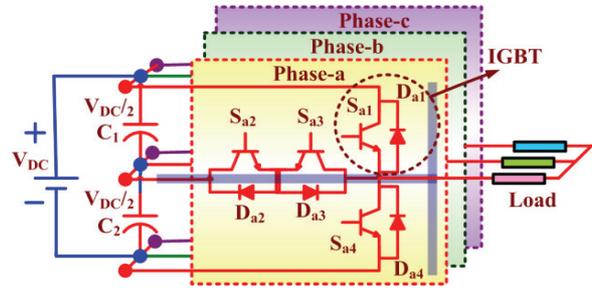


Fig. 1. Three-phase 3L T-type MLI.

TABLE I
SWITCHING STATES OF A 3 PHASE T-TYPE MLI (ONE LEG)

V_{OUT}	State	S_{a1}	S_{a2}	S_{a3}	S_{a4}
$+V_{DC}/2$	+1	ON	OFF	OFF	OFF
0	0	OFF	ON	OFF	OFF
0	0	OFF	OFF	ON	OFF
$-V_{DC}/2$	-1	OFF	OFF	OFF	ON

for AC voltage generation and they are well matched for medium/high power AC applications. The advantages of MLIs include minimizing the total harmonic distortion (THD) and a low dv/dt [12]-[17]. Nevertheless, possible irregularities are addressed, 35% of failures take place because of IGBT mechanisms (power parts) and because of capacitors and gate control techniques [12]. Still, conventional 2-level inverters are a viable solution since they are reliable, cost-effective and easy to reconstruct as T-type multilevel generators with slight rearrangements. In addition, 3L T-type inverters generate 3 level in phase voltage and 5 levels in line to line voltage.

II. OPERATION OF ONE LEG OF A 3L T-TYPE MLI

The three-phase 3L T-type MLI is operated in three modes of switching as shown in Table I. The operation of mode ‘+1’ can be achieved by conduction of the switch S_{a1} only. However, the switches S_{a1} and S_{a3} are conducted to provide a commutation path for the current. Similarly, mode ‘-1’ can be operated with the conduction of the switch S_{a4} only. However, the switches S_{a4} and S_{a2} are conducted to provide a commutation path.

A. State ‘+1’

In state ‘+1’, the switch S_{a1} is conducted and the output voltage is $+V_{DC}/2$. The equivalent circuit for this state is shown in Fig. 2(a). The current path is C_1 – S_{a1} –Load, the positive output voltage of $+V_{DC}/2$ at the load. In this mode, the switch S_{a2} , S_{a3} and S_{a4} are turned off and the diode D_{a2} , D_{a3} and D_{a4} are reversed biased.

When S_{a1} is conducting, the voltage across S_{a2} and S_{a3} is $V_{DC}/4$, and the voltage across S_{a4} is V_{DC} . The current commutation path when the switch S_{a1} is turned off is S_{a1} – C_1 – S_{a3} – D_{a2} . The blue line in Fig. 2(b) represents the commutation of S_{a1} and the current path.

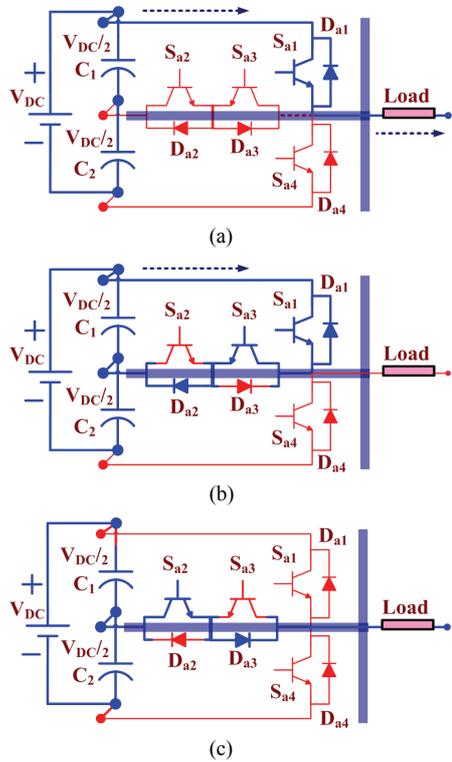


Fig. 2. Modes of operation of one leg of a three phase 3L T-type MLI for positive voltage level generation. (a) State '+1'. (b) Commutation of the switch S_{a1} . (c) State '0'.

B. State '0'

In state '0', either the switch S_{a2} or the switch S_{a3} is conducting. Thus, the neutral point 'N' is connected to the load, resulting in zero output voltage across the load. The equivalent circuit of the T-type MLI when the switch S_{a2} is conducting is shown in Fig. 2(c). The equivalent circuit of the T-type MLI when the switch S_{a3} is conducting is shown in Fig. 3(a). State '0' occurs between modes +1 and -1. In this state, the switches S_{a1} and S_{a4} are turned off, the diodes D_{a1} and D_{a4} are reversed biased, and the voltage across S_{a1} and S_{a4} is $V_{DC}/2$.

C. State '-1'

In state '-1', the switch S_{a4} is conducted and the output voltage is $-V_{DC}/2$. The equivalent circuit for this state is shown in Fig. 3(b). The current path to generate $-V_{DC}/2$ is C_2 –Load– S_{a4} , the negative output voltage $-V_{DC}/2$ at the load and in this mode. In addition, the switches S_{a1} , S_{a2} and S_{a3} are turned off and the diode D_{a1} , D_{a2} and D_{a3} are reversed biased. When S_{a4} is conducting, the voltage across S_{a2} and S_{a3} is $V_{DC}/4$ and the voltage across S_{a1} is V_{DC} . The current commutation path when the switch S_{a4} is turned off is S_{a4} – C_2 – S_{a2} – D_{a3} . The dark line in Fig. 3(c) represents the commutation of S_{a4} and the current path. The capacitor balancing is measured by the NPF method. In this method, the percentage of Neutral Point Fluctuation (%NPF) is calculated as follows:

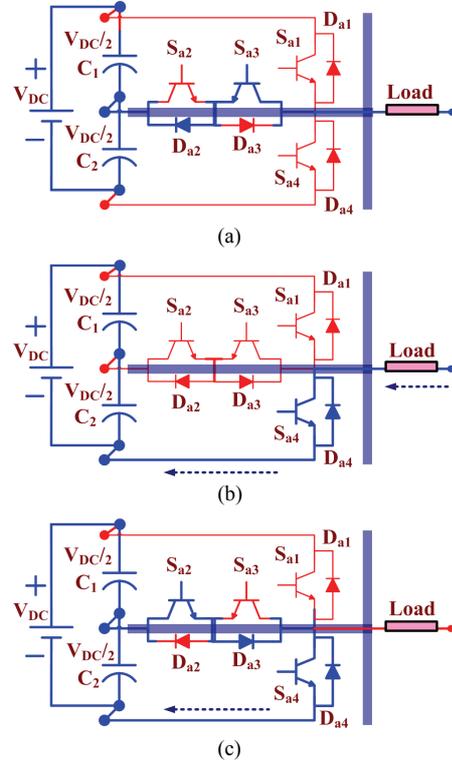


Fig. 3. Modes of operation of one leg of a three phase 3L T-type MLI for negative voltage level generation. (a) State '0'. (b) State '-1'. (c) Commutation of the switch S_{a4} .

$$\% NPF = \left\{ \frac{[(V_{DC}/n-1) - V_{C2}]}{V_{C2}} * 100 \right\} \quad (1)$$

The lower the %NPF value, the better balanced the split capacitors become.

D. Losses Calculation

In an inverter, the turn on and turn off of a switch leads to a rise in the junction temperature. Hence, the switching and conduction losses are considered during the loss calculation.

E. Conduction Losses

The voltage drop across the collector and the emitter multiplied by the current gives the conduction losses during the turning on of a switch. When turning off, the leakage current is low. Therefore, the conduction losses during turn off are neglected.

The conduction loss can be calculated as follows:

$$P_T = V_{CE} I_U \quad (2)$$

Where, V_{CE} is to the emitter voltage of a switch.

$$\left. \begin{aligned} P_D &= V_D I_U, V_{UO} = \frac{M_U^* V_{DC}}{V_P} \\ M_U^* &= M_U + M_{CM} \end{aligned} \right\} \quad (3)$$

Where, M_U^* is the actual modulating signal, V_P is the peak

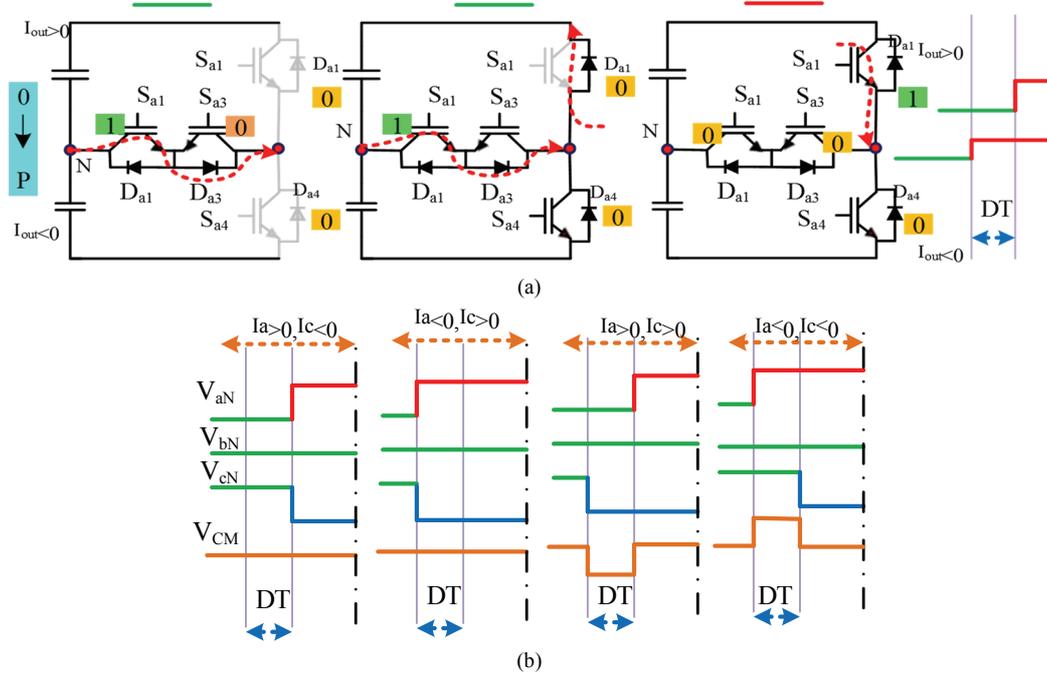


Fig. 4. Influence of DT on the CMV generation for a three-phase 3L T-type MLI. (a) Operating modes. (b) Waveforms.

voltage modulating signal, M_U is the ideal modulating signal, and M_{CM} is the CM modulating signal.

The duty ratio of the phase is given as follows:

$$\left. \begin{aligned} d_U &= (0.5T_Z + T_1 + T_2)/T_s \\ d_V &= (0.5T_Z + T_2)/T_s \\ d_W &= (0.5T_Z)/T_s \end{aligned} \right\} \quad (4)$$

Thus, the conduction losses can be expressed as:

$$P_{Cond,U} = \frac{1}{\pi} \int_f^{\pi+f} \left(d_U V_{CE} i_U + (1-d_U) V_D I_U \right) d(\omega t) \quad (5)$$

F. Switching Losses

When the switch is turned on, the current starts rising before the voltage comes down. Similarly, when the switch is turned off, the voltage starts rising before the current reaches the forward leakage current. During this period, the power losses are high. These losses can be reduced or minimized by selecting a PWM with fewer switching states. The switching losses can be expressed as follows:

$$E_{Switching\ loss} = \frac{E_{SWon} + E_{SWoff}}{2} \quad (6)$$

G. Dead Time Effect on the CMV

In this section, the influence of dead time (DT) on the CMV is analyzed. The CMV is the average sum of the inverter simultaneous three-phase output.

$$V_{CM} = \frac{V_{an} + V_{bn} + V_{cn}}{3} \quad (7)$$

For a 3L T type inverter, the dead time is applied between the top and bottom switches as shown in Fig. 4. During the voltage transition, two inverter phase legs switches are turned 'ON' in opposite direction to maintain zero CMV [32]. For e.g. when the phase inverter leg-a and leg-c switches are turned 'ON' at the same time with opposite polarity. In this case, due to the DT effect, a small notch appears in the output pulse magnitude. The CMV is zero when no DT is applied. When DT is applied to the opposite polarity switches during the switching period, a notch appears and its magnitude depends on the direction of the two-phase current. Hence, when DT is applied, the switching harmonics are preset in the CM current spectrum. This harmonics magnitude depends on the inverter-switching period and DT.

III. PULSE WIDTH MODULATION STRATEGIES

Various PWM strategies are available for multilevel converter applications [29], [30]. The carrier-based PWM (CB-PWM) schemes are considered here. CB-PWM is generally classified into the Phase Disposition (PD), Phase Opposition Disposition (POD) and Alternate Phase Opposite Disposition (APOD) categories. Generally, in CB-PWM, $n-1$ carrier signals are required, where n is the line-to-line number of levels. This paper also considers other PWM schemes such as the Phase Shifting Carrier (PSC), Interleaved Carrier (IC) and third harmonic elimination methods.

A. Phase Disposition (PD) PWM

The reference and carrier signal arrangements in PDPWM for a seven level MLI is shown in Fig. 5(a). In this technique,

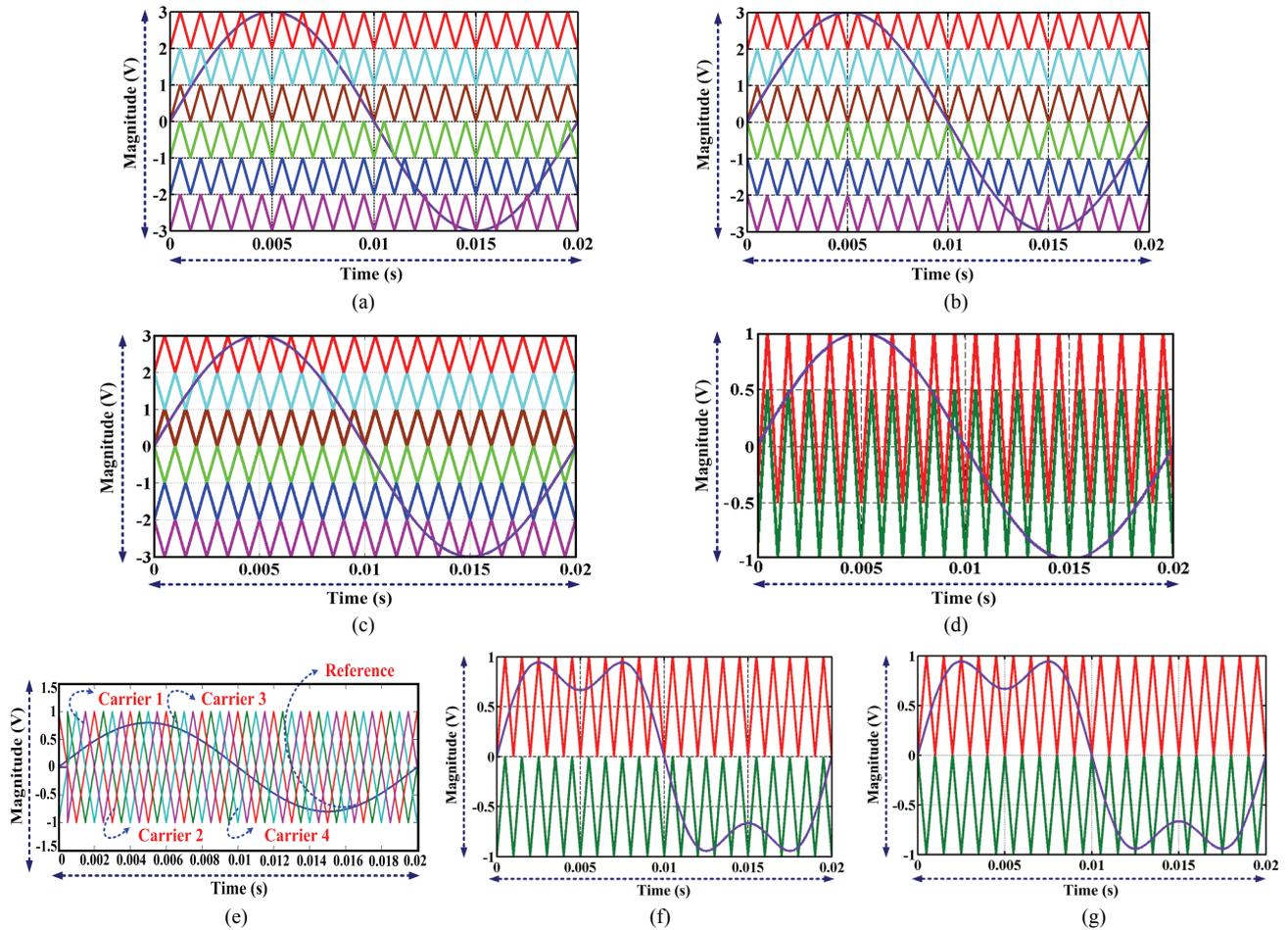


Fig. 5. Pulse Width Modulation (PWM) schemes. (a) PDPWM. (b) PODPWM. (c) APODPWM. (d) ICPWM. (e) PSCPWM. (f) 3rd PDPWM. (g) 3rd PODPWM.

all the carrier signals have the same amplitude and frequency, and all of the carriers are in phase with each other. High-frequency carrier signals are used without phase shifting and they are compared with a sinusoidal waveform to obtain pulses for switches. Six carriers are arranged for PDPWM to generate seven levels as shown in Fig. 5(a). The upper three carriers are used to generate three positive levels, the lower three carriers are used to generate three negative levels, and the zero level is generated without using a carrier.

The modulation index (M_a) and frequency ratio (M_f) are expressible as follows:

$$M_a = A_m / ((m-1) \cdot A_C), M_f = f_C / f_M \quad (8)$$

B. Phase Opposition Disposition (POD) PWM

This strategy is a combination of the phase opposition and disposition methods. Here, all the carrier signals have the same amplitude and frequency. However, carrier signals above the zero reference are phase shifted by 180 degrees with respect to carrier signals below the zero reference, as shown in Fig. 5(b). Six carriers are arranged for the POD PWM (the upper carrier and lower carrier have a 180-degree

phase shift) to generate seven levels. The upper three carriers are used to generate three positive levels, the lower three carriers are used to generate three negative levels, and the zero level is generated without using a carrier.

C. Alternative Phase Opposition Disposition (APOD) PWM

This is a constant switching frequency technique. However, the carrier signal is phase shifted by 180 degrees with respect to the signal below and below it. Therefore, every alternate carrier signal has the same phase, as shown in Fig. 5(c). Six carriers are arranged for the APODPWM to generate seven levels. The upper three carriers are used to generate three positive levels, the lower three carriers are used to generate three negative levels, and the zero level is generated without using the carrier. This method reduces the THD and voltage stress to some extent.

D. Interleaved Carrier (IC) PWM

This strategy greatly reduces the THD and improves the output voltage. The two-carrier arrangement for the ICPWM is shown in Fig. 5(d). In the ICPWM, both carriers have the same amplitude and frequency. However, both carriers overlap

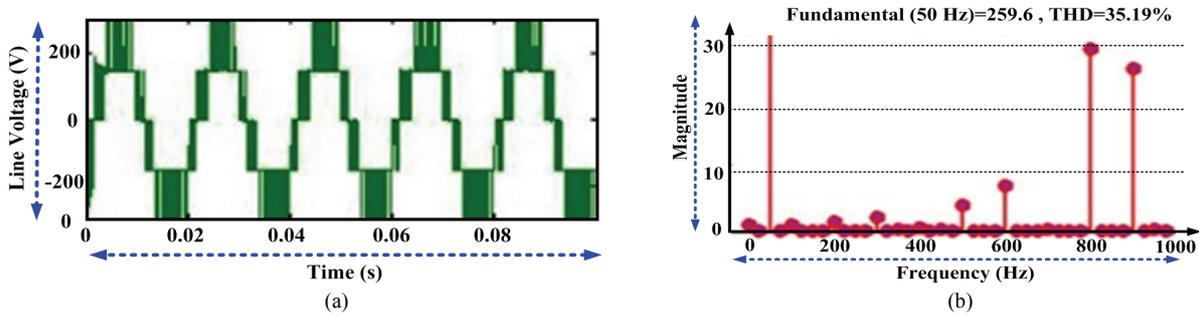


Fig. 6. Simulation results and investigation. (a) Output line voltage using PDPWM. (b) THD using PDPWM.

and the upper carrier is used to generate a positive level, the lower carrier is used to generate negative levels and the zero level is generated without using a carrier.

E. Phase Shifting Carrier (PSC) PWM

In the PSCPWM, instead of level shifting, a phase shift is introduced between every carrier signal, which results in a stepped output waveform with a low harmonic content. The four-carrier arrangement for the PSCPWM is shown in Fig. 5(e). Here, four carrier signals have the same amplitude and frequency. However, the carrier signals are phase shifted by a certain number of degrees (that depends on the number of carriers) with respect to each other.

F. Third Harmonic Elimination PWM

In third harmonic elimination PWM, all of the carrier signals with different frequencies are compared with a third harmonic injected sine wave as a reference signal. These reference signals have a flat-topped shape, which enables an improvement in the output voltage without entering the over modulation region. The carrier arrangements for third harmonic elimination with PD and POD are shown in Fig. 5(f) and 5(g), respectively.

In third harmonic elimination with the PD technique, all of the carrier signals have the same amplitude and frequency, and are in phase with each other. High-frequency carrier signals are used without phase shifting and compared with a third harmonic sinusoidal waveform to obtain pulses for switches. In third harmonic elimination with the POD technique, all of the carrier signals have the same amplitude and frequency. However, the carrier signals above the zero reference are phase shifted by 180 degrees with respect to the carrier signals below the zero reference. The high-frequency carrier signals are compared with a third harmonic sinusoidal waveform to obtain pulses for switches. The upper carriers are used to generate positive levels, the lower carriers are used to generate negative levels and the zero level is generating without using a carrier.

The third harmonic injected sine wave can be expressed as:

$$V_{ref} = V \sin \theta + \frac{V}{6} \sin 3\theta \quad (9)$$

Using the concept of third harmonic elimination PWM to eliminate a defined harmonic was proposed in [24], [28]. By using this PWM, the highest theoretical output power quality can be achieved.

IV. SIMULATION RESULTS

The performance of a 3L T-type NPC MLI with various multi-carrier PWM schemes is investigated using MATLAB/Simulink 9.1 (R2016b) with a 300V DC supply, 100 μ F split capacitors, and a 3kHz switching frequency fed to a 1.5HP induction motor. The output line voltage and THD spectra for the basic carrier-based PWM schemes (PDPWM, PODPWM and APODPWM) with the maximum modulation index ($M_a=1$), are shown in Fig. 6(a)-6(b), Fig. 7(a)-7(b) and Fig. 7(c)-7(d), respectively. Fig. 7(e)-7(f) and Fig. 7(g)-7(h) show the output line voltage and THD spectra for ICPWM and PSCPWM, respectively. Fig. 8(a)-8(b) and Fig. 8(c)-8(d) depicts the output line voltage and THD spectra for the 3rd PDPWM and 3rd PODPWM, respectively. The output line voltage and THD spectra for various carrier-based PWM schemes to T-type NPC MLIs are listed in Table II. Here, a better output line voltage (278.6V) is achieved by ICPWM at the maximum modulation index (M_a). Nevertheless, the THD is high (42.95%) when compared with the other schemes. PDPWM gives the lowest THD among the basic CB-PWM schemes.

In order to eliminate the 3rd harmonic quantity, the 3rd PDPWM provide a better voltage profile and THD when compared to all of the considered PWM schemes. The % Neutral Point Fluctuation (NPF) values for a T-type NPC MLI with various multi-carrier PWM schemes are presented in Table III.

Therefore, based on observations, it can be seen that PD and POD yield better DC-link voltages than the other PWM methods. Conduction losses are calculated for the T-type NPC MLI for the various PWM schemes. Then they are compared with the conduction losses for a conventional NPC MLI in Fig. 9. In Fig. 10, T-MLI NPC is compared with a conventional NPC for five line-to-line levels in terms of number of switches, clamping diodes, diodes and capacitors.

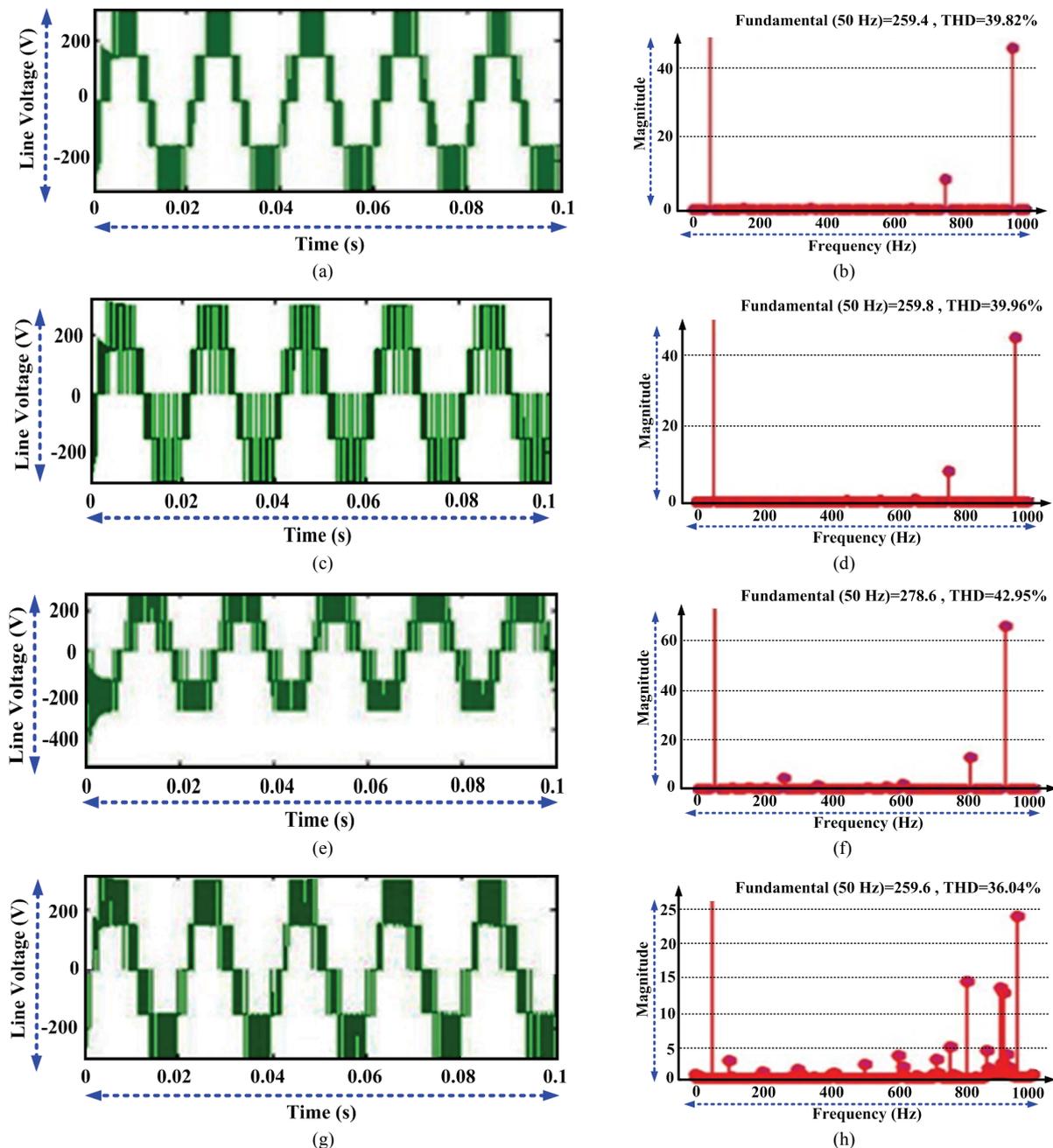


Fig. 7. Simulation results and investigation. (a) Output line voltage using PODPWM. (b) THD using PODPWM. (c) Output line voltage using APODPWM. (d) THD using APODPWM. (e) Output line voltage using ICPWM. (f) THD using ICPWM. (g) Output line voltage using PSCPWM. (h) THD using PSCPWM.

TABLE II
LINE VOLTAGE AND THD OF A T-TYPE NPC MLI WITH THE PDPWM, PODPWM, APODPWM, ICPWM AND PSC PWM TECHNIQUES

M_a	PD		POD		APOD		IC		PSC	
	V	THD%	V	THD%	V	THD%	V	THD%	V	THD%
1	259.6	35.1	259.4	39.8	259.8	39.96	278.6	42.95	259.6	36.04
0.9	233.6	33.8	233.4	37.6	233.8	37.8	250.7	41.1	233.6	35.6
0.8	207.6	31.7	207.5	36.5	207.8	36.8	222.8	39.5	207.6	32.9
0.7	181.7	34.6	181.5	38.3	181.8	35.8	195.1	40.5	181.7	35.8
0.6	155.7	39.5	155.6	42.1	155.8	40.3	167.1	41.2	155.7	37.2

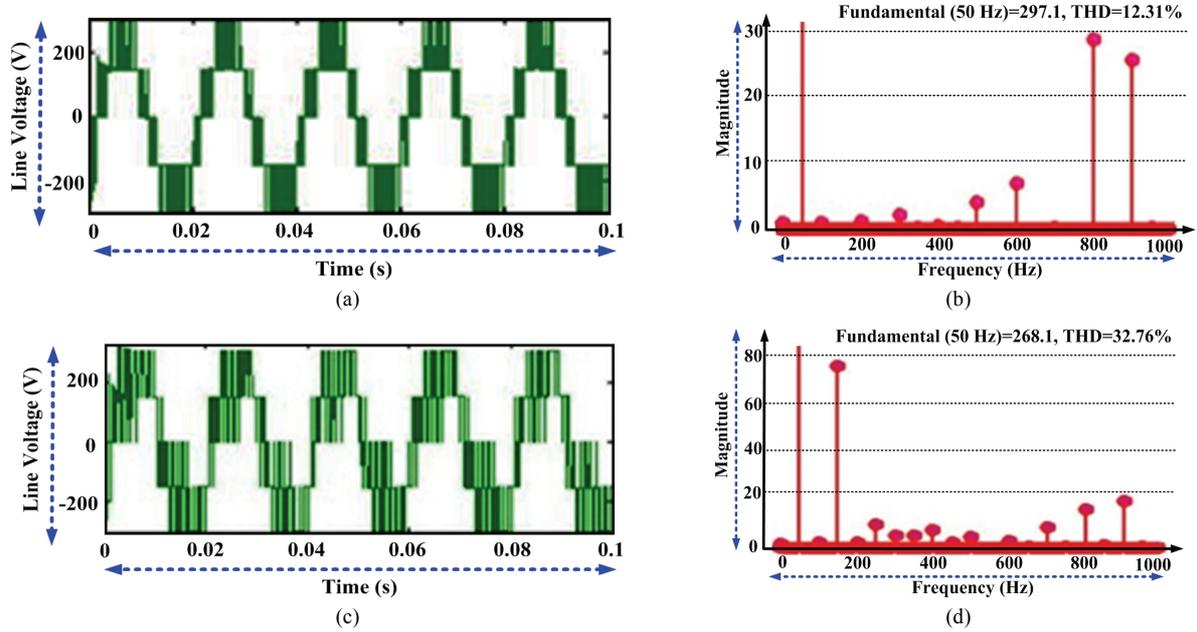


Fig. 8. Simulation result and investigations: (a) Output line voltage using 3rd PDPWM. (b) THD using 3rd PDPWM. (c) Output line voltage using 3rd PODPWM. (d) THD using 3rd PODPWM.

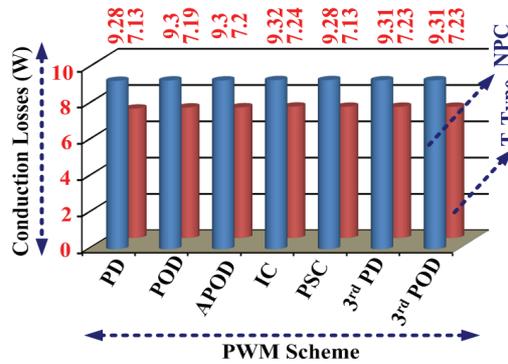


Fig. 9. Conduction losses for the conventional NPC MLI and a T-type NPC MLI with various PWM schemes.

TABLE III

PERCENTAGE OF NPF OF A T-TYPE NPC MLI WITH VARIOUS MULTI-CARRIER PWM SCHEMES

Scheme	PD	POD	APOD	IC	PSC	3 rd PD	3 rd POD
% NPF	0.6	0.6	1.2	0.8	0.6	3.2	3.2

It is observed that the required number of switches, main diodes and capacitors for the T-type MLI and the conventional NPC is the same. It is also observed that clamping diodes are not required for the design of the T-type MLI. However, they are required for the design of the conventional NPC.

When compared with the different PWM schemes used in previous publications [22], [29]-[31], the diode free NPC (T-MLI) is superior to the NPC topology in terms of fundamental line voltage, NPF and line voltage THD. These improvements are associated with neutral point clamping diode absentia. In addition, referencing the conduction losses

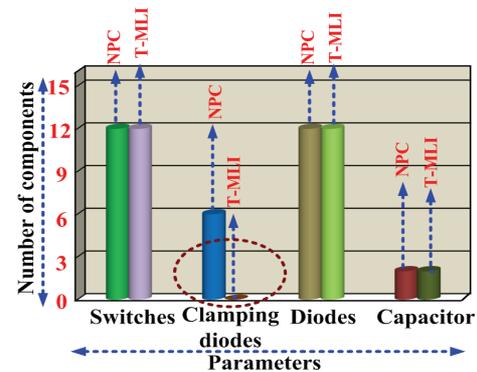


Fig. 10. Comparison of a T-type MLI and the conventional NPC in terms of the number of switches, clamping diodes, diodes and capacitors.

of the T-MLI with NPC topology is reduced to nearly 2 to 2.5W. Hence, the efficiency of the T-MLI is increased for all of the multicarrier and space vector PWM schemes.

V. EXPERIMENTAL RESULTS

A prototype of a 1 kW T-MLI (for five line-to-line level) has been developed in the laboratory using MOSFETs as shown in Fig. 11(a). The hardware consists of twelve IRF840 MOSFETs, where each leg carries four MOSFETs. The experimental setup has been integrated with the protection circuits. An HCPL4506 is used as an Opto-isolator, which provides isolation between the FPGA processor and the SK 100 MLI 066 T. An MC14584B is used for enhanced noise immunity to square up slowly changing waveforms. The MOSFETs are operated through drivers, which are connected

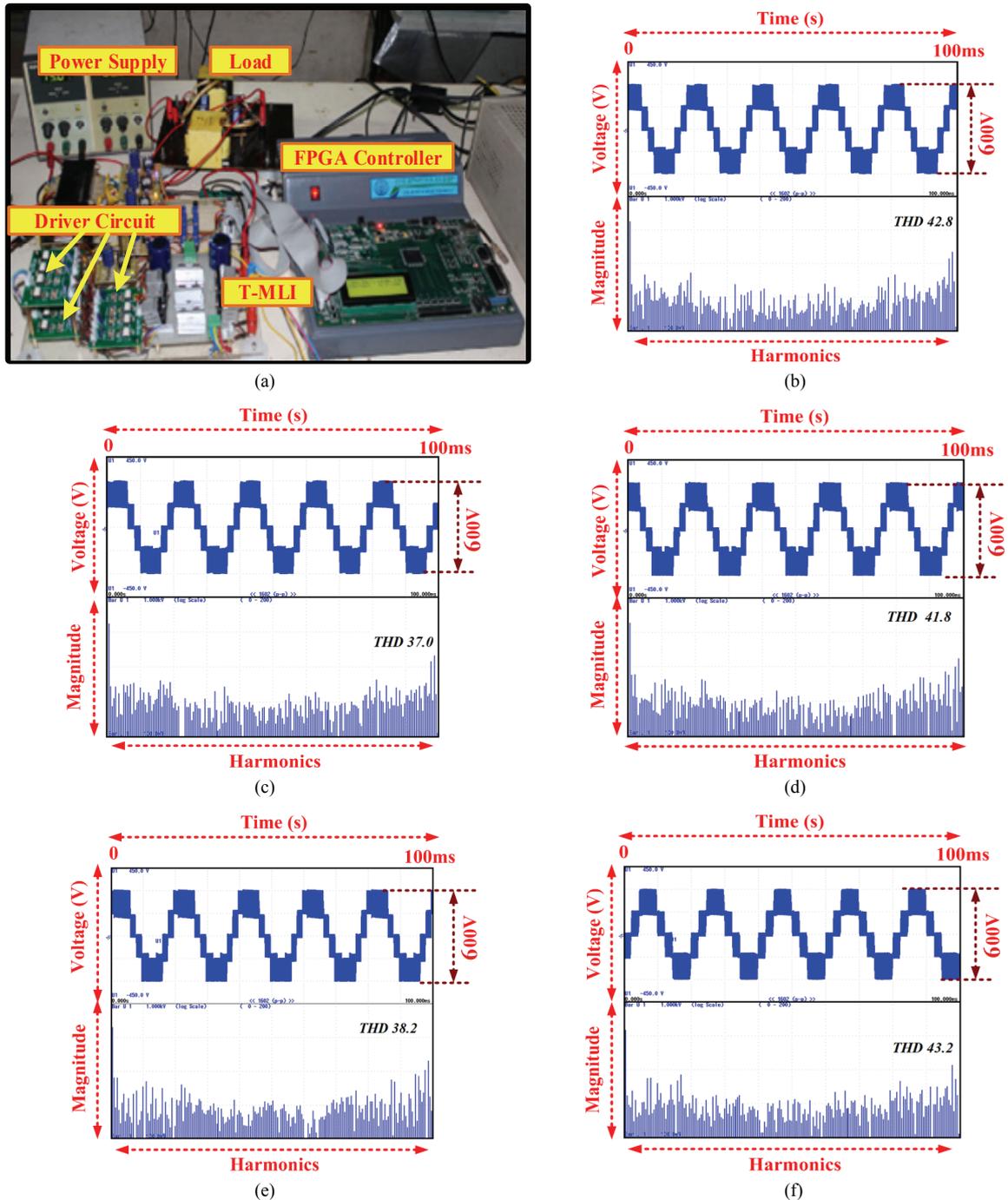


Fig. 11. Experimental results and investigations. (a) Experimental setup of a 1kW three phase T-type (for five line to line level) MLI. (b) Line voltage and THD spectra for APODPWM with $M_a = 0.9$. (c) Line voltage and THD spectra for PDPWM with $M = 0.9$. (d) Line voltage and THD spectra for PODPWM with $M_a = 0.9$. (e) Line voltage and THD spectra for PSCPWM with $M_a = 0.9$. (f) Line voltage and THD spectra for ICPWM with $M_a = 0.9$.

to a Xilinx Spartan XC3SD1800A-FG676-4 Spartan 3A FPGA board. All of the multi-carrier PWM schemes are developed in MATLAB/Simulink and connected to the FPGA board via MATLAB -Xilinx System Generator (XSG). The inverter front end is connected to a 3-phase rectifier with a 300V DC-link and two 100 μ F front-end DC-link capacitors, which produce the level of the inverter. To verify the validity

of the above-discussed PWM schemes, experimental tests are carried out with a 1.0HP induction motor at various M_a values. The fundamental frequency and switching frequency of the inverter are 50Hz and 3 kHz, respectively. The corroborating experimental results are captured using a six-channel YOKOGAWA spectrum analyzer.

One of the main contributions of this paper, when compared

with previously reported work on multi-carrier PWM schemes, is that all of the investigated PWM schemes for a T MLI are realized through FPGA implementation using MATLAB- Xilinx System Generator (XSG). The system generator has its own Simulink models that are in the three tabs called the Xilinx block-set. System Generator is a FPGA design tool from Xilinx that enables the use of the Matlab Simulink model-based design environment for FPGA design. While installing MATLAB/Simulink, XSG is installed on a PC/Laptop and then Xilinx block sets are included in the Simulink library. A functional simulation is possible even before compilation of the designed model. The compilation generates the files of the structural description of the system in a standard Hardware Description Language (VHDL/ Verilog) for the Integrated System Environment (ISE), which is suitable for Xilinx FPGAs. Initially, the hardware is tested with an APODPWM scheme for various modulation indices.

For conciseness, only the line voltage and its harmonics spectra for $0.9M_a$ are shown in Fig. 11(b). Here, it can be seen that the line voltage is a maximum of 232.9V with a 42.8% harmonics spectrum. When PDPWM and PODPWM are applied to the experimental verification at 0.9 modulation index, the line voltages and corresponding THDs are measured at 232.7V and 233.1V, and 37.0% and 41.8%, respectively (see Fig. 11(c) and Fig. 11(d)). Both methods work well to maintain the THD values, and these results show a close agreement with the simulation results. Next, a coloration experiment is performed for the PSC, line voltage and harmonic spectrum as shown in Fig. 11(e). It is observed that the line voltage magnitude remains the same (233.1V). However, the percentage of the THD decreases to 38.2%. These results demonstrate that the PSC provides better performance in terms of the THD profile for the entire modulation range. Fig. 11(f) shows waveforms for the line voltage and its harmonics spectra with the ICPWM scheme for $M_a=0.9$.

As in the simulations, it can be seen that the ICPWM is has a better DC link utilization when compared to the other PWM schemes. However, the THD is observed to be higher (43.2%) than the other methods.

VI. CONCLUSION

The output line voltage, THD and conduction losses of a 3L T-type NPC MLI are investigated for various multi-carrier PWM schemes, such as Phase Disposition (PD), Phase Opposition Disposition (POD), Alternate Phase Opposite Disposition (APOD), Phase Shifting Carrier (PSC), Interleaved Carrier (IC) and third harmonic elimination. For all of the PWM schemes. The capacitor-balancing problem is also investigated by using NPF. Based on investigations of a 3L T-type MLI, the PDPWM and PSCPWM provide a better performance in terms of THD profile for the entire modulation range. The PDPWM, PODPWM and ICPWM

have a better DC link utilization when compared to the other PWM schemes. The 3rd PDPWM provides a better voltage profile when compared to all of the PWM schemes. The 3L T-type MLI required a lower number of diodes when compared to the conventional NPC. The conduction losses of 3L T-type NPC MLIs are lower than those of the NPC MLIs, which indicates that the T-type NPC MLI is more efficient. Simulation and experimental results are provided and they show a good agreement with each other.

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