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Pulse-Width Modulation Strategy for Common Mode Voltage Elimination with Reduced Common Mode Voltage Spikes in Multilevel Inverters with Extension to Over-Modulation Mode

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Abstract

This paper presents a pulse-width modulation strategy to eliminate the common mode voltage (CMV) with reduced CMV spikes in multilevel inverters since a high CMV magnitude and its fast variations dv/dt result in bearing failure of motors, overvoltage at motor terminals, and electromagnetic interference (EMI). The proposed method only utilizes the zero CMV states in a space vector diagram and it is implemented by a carrier-based pulse-width modulation (CBPWM) method. This method is generalized for odd number levels of inverters including neutral-point-clamped (NPC) and cascaded H-bridge inverters. Then it is extended to the over-modulation mode. The over-modulation mode is implemented by using the two-limit trajectory principle to maintain linear control and to avoid look-up tables. Even though the CMV is eliminated, CMV spikes that can cause EMI and bearing current problems still exist due to the deadtime effect. As a result, the deadtime effect is analyzed. By taking the deadtime effect into consideration, the proposed method is capable of reducing CMV spikes. Simulation and experimental results verify the effectiveness of the proposed strategy.

Key words: Cascaded inverter, Common mode voltage (CMV), Multilevel inverter, Neutral point clamped (NPC), Pulse-width modulation (PWM), Spikes

I. INTRODUCTION

Multilevel inverters are becoming increasingly popular in motor-drive applications. The two well-known multilevel inverter topologies are neutral-point-clamped inverters and cascaded H-bridge inverters. When compared to conventional two-level inverters, multilevel inverters have several advantages including a better harmonic output profile, high voltage blocking capability, and redundant states in the space vector diagram. Therefore, multilevel inverters are more suitable in medium voltage drive applications than conventional two-level inverters. However, CMV still exists in multilevel inverters. High magnitude CMV and its fast variations dv/dt lead to shaft voltage and bearing current, which are responsible for bearing failures and reduce the life expectancy of motors. More than 30% of motor failures are due to bearing current damage [1]. Several mitigation techniques have been reported in the literature, including a shaft grounding system [2], insulated bearings and journals, ceramic bearings, conducting grease, a Faraday shield [3], and dual bridge inverters [4] to eliminate CMV. In practice, inverters and motors are connected by long cables, which contributes to a damped high-frequency ringing at the motor [5]. This results in an excessive overvoltage at the motor terminals. Due to this, motor insulation can be damaged. Several solutions have been proposed to alleviate this problem including motor terminal filters, inverter output filters, series reactors, and a new magnet wire [5]-[12]. Fast variations of CMV dv/dt also result in high-frequency common mode current or ground leakage current, which flow

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through the stray capacitors inside a motor. This high-frequency current is responsible for EMI, which can lead to improper operation of nearby working devices. Several techniques have been suggested to reduce this problem, such as common mode chokes [13], [14], transformers [15], grounding capacitors [15], active filters [16], snubber circuits and resonant converters [17], and insulated shielded cables with symmetrically oriented bundled conductors between the inverter and motor [18].

These techniques can be termed 'hardware solutions' since they involve modifying the motor configurations or adding new components to the system. Therefore, they can be bulky and expensive. Another way to mitigate CMV is to use 'software solutions', i.e. modifying the PWM techniques that control multilevel inverters. Some well-known PWM methods reported in the literature for controlling multilevel inverters are space vector modulation (SVPWM), carrier-based pulse-width modulation (CBPWM), and selective harmonic elimination (SHE). It is widely known that multilevel inverters are capable of reducing or eliminating CMV thanks to their large number of switching states as opposed to conventional two-level inverters. The authors of [19]-[21] and [22] attempted to reduce CMV by avoiding some of the switching voltage states responsible for generating a high CMV magnitude. Meanwhile, the authors of [23]-[27] and [28] proposed PWM strategies for complete CMV elimination by neglecting all of the switching states resulting in CMV. The authors of [29] proposed a complete CMV elimination with deadtime compensation in order to reduce CVM spikes. However, it is implemented by space vector modulation for only three-level NPC inverters and cannot be extended to n-level inverters, including NPC and cascaded H-bridge inverters. The authors of [30] presented a complete CMV elimination with reduced current ripple for multilevel inverters. The current ripple minimization is achieved by using a Harmonic Distortion Factor (HDF) [31] to obtain the optimum mapping function. The authors of [32] proposed a complete CMV elimination for multilevel inverters with reduced switching loss. The switching loss reduction is obtained by mapping the sequence that has double switching to a phase with the minimum absolute magnitude of phase current [32]. However, the spikes in the CMV waveform, which can still cause EMI and the bearing current problem [33]-[36], exist due to the deadtime effect. Therefore, the paper introduces a carrier-based pulse- width modulation strategy to completely eliminate CMV with a spike reduction for odd n-level inverters, including the cascaded and NPC inverters. The impact of deadtime is analyzed in detail. The modulation strategy is first proposed for the under- modulation mode and then extended to the over-modulation mode. The two-limit trajectory principle, which was presented in [37] for two-level inverters, is utilized to maintain linear modulation control over the whole modulation index range. Simulation and experimental results confirm the effectiveness of the proposed method.

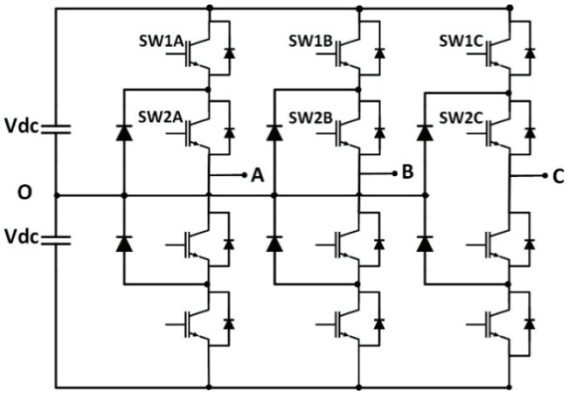


Fig. 1. Three-level neutral point clamped inverter.

II. Pulse-Width Modulation Strategy to Completely Eliminate the CMV in Multilevel Inverters

Despite the differences in the structure of cascaded and neutral point clamped inverters, a pulse-width modulation method for complete CMV elimination is derived for both topologies. Under the condition of balanced DC-link voltages, the pole voltage V_{AO} in Fig. 1 can be expressed as:

$$V_{AO} = (S_{1A}+S_{2A}).V_{DC} - V_{DC} \quad (1)$$

where S_{1A} and S_{2A} are the switching states of the switches SW1A and SW2A, respectively. For example, if S_{1A} is 1, then SW1A is ON. If S_{1A} is 0, then SW1A is OFF.

In three-level neutral point clamped inverters, the switching states are restricted as:

$$S_{1A} \leq S_{2A} \quad (2)$$

The pole voltage V_{XO} ($X \in \{A, B, C\}$) can then be generalized for odd n-level inverters as:

$$V_{XO} = (S_{1X} + S_{2X} + \ldots + S_{n\text{-}2X} + S_{n\text{-}1X}).V_{DC} - \frac{n-1}{2}.V_{DC} = (\sum_{j=1}^{n-1} S_{jX}).V_{DC} - \frac{n-1}{2}.V_{DC} \quad (3)$$

where $S_{1X} \leq S_{2X} \leq \ldots \leq S_{1\text{-}nX}$ for the NPC inverter topology, and n is the number of levels in the inverters.

The components $(\sum_{j=1}^{n-1} S_{jX}).V_{DC}$, $X \in \{A, B, C\}$ in (3) are called switching voltages.

The normalized switching voltages V_{Xn}, $X \in \{A, B, C\}$ can be expressed as:

$$V_{Xn} = \sum_{j=1}^{n-1} S_{jX} \quad (4)$$

The normalized switching voltages V_{Xn}, $X \in \{A,B,C\}$ can also be expressed based on the relationship between V_{XO} and V_{Xn}:

$$V_{Xn} = \frac{V_{XO}}{V_{DC}} + \frac{n-1}{2} \quad (5)$$

The normalized switching voltages V_{Xn} can be decomposed into two components L_X and s_X.

$$V_{Xn} = L_X + s_X;\ X\in \{A,B,C\} \quad (6)$$

where L_X is the base component of V_{Xn}, and s_X is the active component of V_{Xn}.

In one sampling period, L_X is a constant integer, while s_X has a value of 0 or 1.

The average value of the normalized switching voltage v_{xref}, $X\in\{A,B,C\}$ in one sampling period can be defined as:

$$v_{xref} = L_X + \varepsilon_X;\ X\in \{A,B,C\},\ (0\leq \varepsilon_X \leq 1) \quad (7)$$

where ε_X is the average active component of s_X.

In terms of the reference load voltages, the average value of the normalized switching voltage v_{xref} can also be expressed as:

$$v_{xref} = \frac{v^*_{XL}}{V_{DC}} + v^*_{off} \quad (8)$$

The offset voltage v^*_{off} can have any value between the two limits defined as:

$$-\frac{Min}{V_{DC}} \leq v^*_{off} \leq (n-1) - \frac{Max}{V_{DC}} \quad (9)$$

where Max = Maximum $\{v^*_{Al}, v^*_{Bl}, v^*_{Cl}\}$, Min = Minimum $\{v^*_{Al}, v^*_{Bl}, v^*_{Cl}\}$ and n is the number of levels in the inverter.

The instantaneous CMV V_{CM} for an n-level inverter can be expressed as:

$$V_{CM} = \frac{V_{AO}+V_{BO}+V_{CO}}{3} \quad (10)$$

The instantaneous CMV V_{CM} for an n-level inverter can also be written as:

$$V_{CM} = \frac{[V_{An}+V_{Bn}+V_{Cn}-\frac{3(n-1)}{2})]V_{DC}}{3} \quad (11)$$

In order for the CMV V_{CM} for an n-level inverter to be zero, the sum of V_{An}, V_{Bn} and V_{Cn} has to be equal to 3(n-1)/2. In this case, n is the number of levels in the inverter.

In terms of the average value of the normalized switching voltage v_{xref}, the CMV V_{CM} is zero when $v_{aref} + v_{bref} + v_{cref} = \frac{3(n-1)}{2}$. Since $v^*_{Al} + v^*_{Bl} + v^*_{Cl} = 0$, the condition of the zero CMV leads to $v^*_{off} = (n-1)/2$.

F, F_l and F_e are defined as the total switching voltage, total base voltage, and total active average switching voltage, respectively.

$$F = v_{aref} + v_{bref} + v_{cref} \quad (12)$$

$$F_L = L_A + L_B + L_C \quad (13)$$

$$F_e = \varepsilon_A + \varepsilon_B + \varepsilon_C \quad (14)$$

$$(0\leq F_e \leq 3,\ 0\leq \varepsilon_X \leq 1)$$

$$L_X = \begin{cases} Int(v_{xref})\ if\ v_{xref} < n-1 \\ n-2\ if\ v_{xref} = n-1 \end{cases} \quad (15)$$

$$0\leq L_X \leq n-2,\ X\in\{A,B,C\}$$

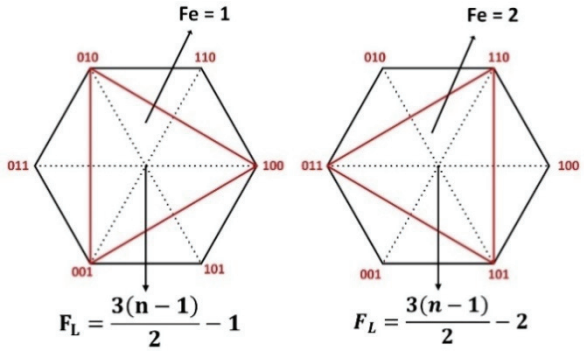


Fig. 2. Active voltage hexagonal diagrams of ($F_L = \frac{3(n-1)}{2} - 1$ & $F_e = 1$) and ($F_L = \frac{3(n-1)}{2} - 2$ & $F_e = 2$) [32].

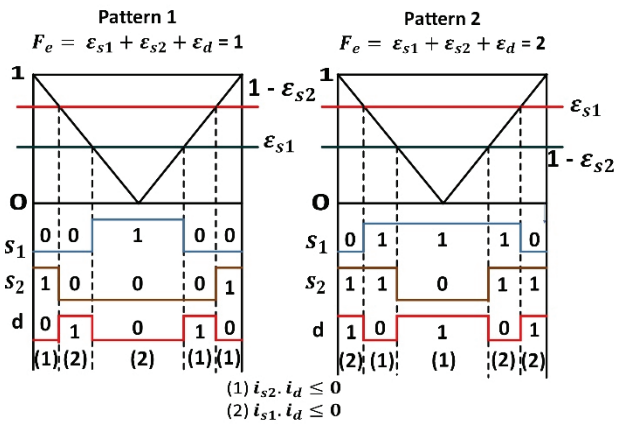


Fig. 3. Two virtual standardized PWM patterns [32].

$$\varepsilon_X = v_{xref} - L_X \quad (16)$$

where Int(v_{xref}) returns the smallest integer value of v_{xref}.

For an n-level inverter, the zero CMV condition leads to the two cases of F_L and F_e, i.e.:

$$F_L = 3(n-1)/2-2,\ F_e = 2 \quad (17)$$

$$F_L = 3(n-1)/2-1,\ F_e = 1 \quad (18)$$

Two-active voltage hexagonal diagrams corresponding to the two cases of F_e and F_L in (17) and (18) are shown in Fig. 2.

With the aid of base voltages, the reference voltage in a three-level NPC inverter can be synthesized by a virtual carrier-based PWM pattern similar to that of a two-level PWM. The two virtual standardized PWM patterns corresponding to $F_L = \frac{3(n-1)}{2} - 1$ & $F_e = 1$) and ($F_L = \frac{3(n-1)}{2} - 2$ & $F_e = 2$) are shown as follows:

For each virtual standardized pattern, there are six possible mapping functions that are shown in Table I. Which mapping function is selected depends upon the control purpose.

A block diagram of the complete CMV elimination PWM method for the under-modulation mode is shown in Fig. 4.

TABLE I [32]
POSSIBLE MAPPING FUNCTION AND MODULATING SIGNALS DETERMINATION

A → d B → s_1 C → s_2	A → d B → s_2 C → s_1	A → s_1 B → d C → s_2	A → s_2 B → d C → s_1	A → s_1 B → s_2 C → d	A → s_2 B → s_1 C → d
$\varepsilon_1=\varepsilon_B$ $\varepsilon_2=\varepsilon_C$	$\varepsilon_1=\varepsilon_C$ $\varepsilon_2=\varepsilon_B$	$\varepsilon_1=\varepsilon_A$ $\varepsilon_2=\varepsilon_C$	$\varepsilon_1=\varepsilon_C$ $\varepsilon_2=\varepsilon_A$	$\varepsilon_1=\varepsilon_A$ $\varepsilon_2=\varepsilon_B$	$\varepsilon_1=\varepsilon_B$ $\varepsilon_2=\varepsilon_A$

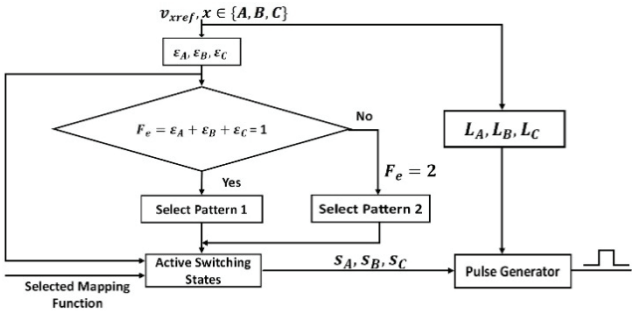


Fig. 4. Block diagram of the complete CMV elimination PWM method in odd n-level inverters [32].

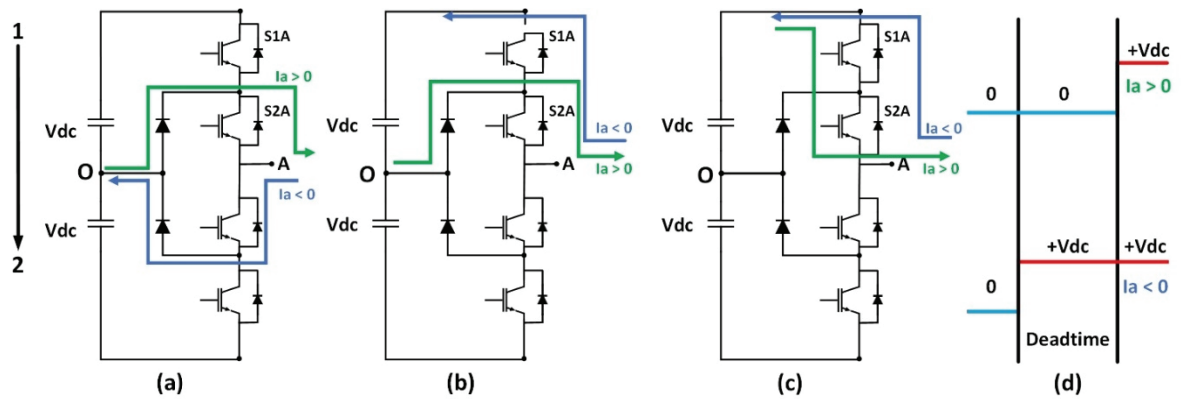


Fig. 5. Phase leg during a 1 → 2 transition. (a) Steady state V_{AO} = 0. (b) During dead time. (c) Steady state V_{AO} = $+V_{DC}$. (d) Pole voltage waveform with different current directions (I_{out} > 0: green, I_{out} < 0: blue) [29].

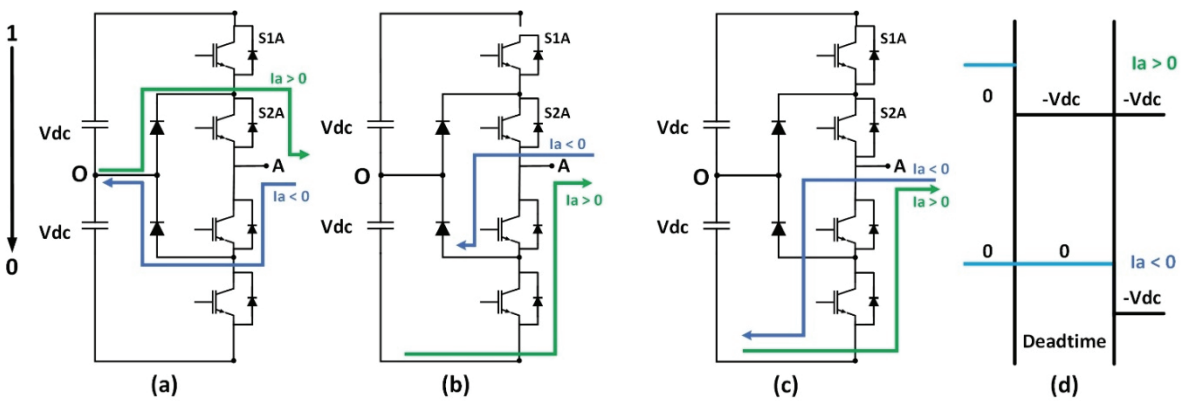


Fig. 6. Phase leg during a 1 → 0 transition. (a) Steady state V_{AO} = 0. (b) During dead time. (c) Steady state V_{AO} = $-V_{DC}$. (d) Pole voltage waveform with different current directions (I_{out} > 0: green, I_{out} < 0: blue) [29].

III. PROPOSED PULSE-WIDTH MODULATION METHOD FOR COMPLETE CMV ELIMINATION WITH SPIKE REDUCTION

A. Impact of Deadtime on the CMV Waveform

As a demonstration, the influence of deadtime is explained in the three-level NPC inverter topology. For n-level inverters, its impact remains the same. The spikes in a CMV waveform can be reduced by taking the deadtime effect into account. The deadtime, which is required to avoid shoot-through, is one of the reasons spikes occur in the CMV.

The effect of deadtime on CMV waveforms can be best illustrated by the example shown in Fig. 5, 6 and 7.

Fig. 5 represents phase leg A during a transition from the 1 to 2 state for two different phase current directions, i.e. $i_a > 0$ and $i_a < 0$. In this paper, positive current $i > 0$ is defined as one flowing towards the load while negative current $i < 0$ is one flowing away from the load or towards the inverter. During the deadtime shown in Fig. 5(b), the pole voltage depends upon the current direction. If the current i_A is positive,

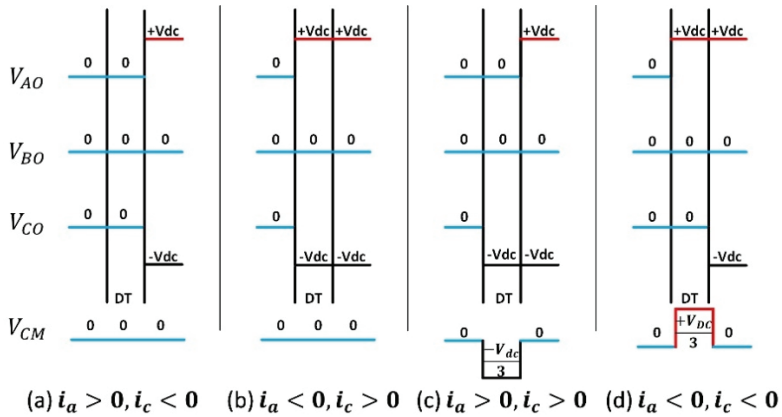


Fig. 7. Impact of dead time on CMV generation [29].

the pole voltage V_{AO} is equal to 0. If the current is negative, the pole voltage V_{AO} is equal to $+V_{DC}$. The same principle also applies to phase legs B and C.

Fig. 6 demonstrates phase leg A during a commutation from the 1 to 0 state for two different phase current directions, i.e. $i_a > 0$ and $i_a < 0$. During the deadtime period ($SW_{1A} = 0$, $SW_{2A} = 0$, $SW_{3A} = 1$, $SW_{4A} = 0$) as shown in Fig. 6(b), the pole voltage V_{AO} depends upon the phase current direction. If the current i_A is positive, the pole voltage V_{AO} is clamped to $-V_{DC}$ as shown in Fig. 6(d). On the other hands, if the current i_A is negative, the pole voltage V_{AO} is 0 as shown in Fig. 6(d). The same principle also applies to phase legs B and C.

Fig. 7 demonstrates CMV generation during the deadtime interval for a transition from the 111 to 210 state of three phase legs for 4 different phase current directions, i.e. $i_A > 0$ $i_C < 0$, $i_A < 0$ $i_C > 0$, $i_A > 0$ $i_C > 0$, $i_A < 0$, $i_C < 0$. In Fig. 7, the CMV remains zero during the deadtime if there are simultaneous commutations of the two-phase legs, where the current directions are opposite. If during the deadtime there are simultaneous commutations of the two-phase legs whose current directions are the same, there will be a CMV pulse during the deadtime. Based on this analysis, the complete CMV elimination pulse-width modulation strategy with spike reduction is proposed.

B. Proposed PWM Method for Complete CMV Elimination with Spike Reduction for the Under- Modulation Mode

The proposed PWM strategy for complete CMV elimination with spike reduction is based on the impact of deadtime on a CMV waveform as explained in section A.

There are six possible mapping functions available as shown in Table I. The control purpose, which is to reduce the CMV spikes, determines which phase maps into which sequence. In order to reduce the spikes in a CMV waveform, the simultaneous commutations of any two-phase legs whose current directions are opposite must be guaranteed. Therefore, the control purpose in this paper is to map any two-phase legs having opposite current directions to any two sequences having simultaneous commutations.

Switching patterns 1 and 2 are illustrated in Fig. 3, where the two particular phase currents shown at the bottom of Fig. 3 theoretically eliminate the CMV spikes during the deadtime interval. For the sake of brevity, only the first half of the switching period in pattern 1 is explained since the switching sequence is repeated in reverse in the second half of the switching period. In addition, pattern 2 is exactly the same as pattern 1. As far as pattern 1 is concerned, the two-level switching sequence of [s_1, s_2, d] in the first half of the switching period is 010→001→100. From 010 to 001, there are simultaneous commutations in the s_2 and d sequences. Therefore, the current condition of these two sequences must be $i_{s2}.i_d \leq 0$ in order for the CMV to be zero during the deadtime interval. From 001 to 100, there are simultaneous transitions of the s_1 and d sequences. Hence, the current condition of these two sequences must be $i_{s1}.i_d \leq 0$. Over one switching period of both patterns 1 and 2, as shown in Fig. 3, the sign of the d-sequence current is always opposite that of either the s_1-sequence or the s_2-sequence current. Moreover, since the frequency of the carrier is much larger than that of the three-phase currents ($f_{carrier}$ = 5 KHz, f_0 = 50 Hz), the signs of the three-phase currents can be assumed to be constant during a sampling period. As shown in Fig. 8, there are six regions where the sign of a particular phase current is opposite that of the other two-phase currents. In other words, the multiplication of one particular phase current with the other two-phase currents will be negative. For example, in Fig. 8, the phase-B current direction is opposite those of the phase-A and phase-C currents from the 0 to $\frac{\pi}{3}$ interval. Hence, phase B is mapped to the d-sequence while phase A and C are arbitrarily mapped to the s_1 and s_2 sequences for the $[0, \frac{\pi}{3}]$ interval. In other words, the task of reducing spikes in a CMV waveform is to map one particular phase whose current has the opposite sign with respect to that of the other 2 phases to the d-sequence. The other two phases will be mapped arbitrarily to either s_1 or s_2 because they does not have any impact on the CMV pulse during the deadtime.

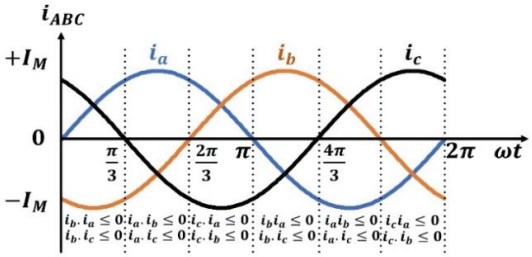


Fig. 8. Signs of three-phase current in a fundamental period.

The selected mapping function can be expressed in pseudo-code as follows:

If ($i_b.i_a \le 0$ && $i_b.i_c \le 0$)

Phase b → d sequence

Phase a → s_1 sequence

Phase c → s_2 sequence

Else if ($i_a.i_b \le 0$ && $i_a.i_c \le 0$)

Phase a → d sequence

Phase b → s_1 sequence

Phase c → s_2 sequence

Else if ($i_c.i_a \le 0$ && $i_c.i_b \le 0$)

Phase c → d sequence

Phase a → s_1 sequence

Phase b → s_2 sequence

C. *Proposed Method with Extension to the Overmodulation Mode*

Despite the difference in the linearity control, both the under-modulation and over-modulation modes are unified in this paper by utilizing the two-limit trajectory principle [37] [38]. The goal of using this principle is to maintain linear control in the over-modulation mode [37]. This principle can be implemented by either a carrier-based PWM or a space vector modulation method. In this paper, a carrier-based PWM method is used due to its simplicity when compared to space vector modulation. Before diving into the mathematical expression for the over-modulation mode, it is necessary to define the modulation index, i.e.:

$$m = \frac{V_{1m}}{\frac{V_{DCN}}{\sqrt{3}}} \quad (19)$$

where V_{1m} is the fundamental magnitude of the phase voltage. The component $^1/_{\sqrt{3}}V_{DCN}$ is the maximum fundamental magnitude of the conventional space vector modulation, and it is selected as the base value in this formula. However, any base values can be chosen. V_{DCN} is the total input DC-link voltage of the inverter.

In order to use the two-limit trajectory principle, the two limits corresponding to each of the modulation index ranges must be defined. There are three ranges in the PWM method for complete CMV elimination, i.e. $0 \le m \le \frac{\sqrt{3}}{2} (\approx 0.866)$, $\frac{\sqrt{3}}{2} \le m \le \frac{3\sqrt{3}\ln(3)}{2\pi} (\approx 0.9085)$ and $\frac{3\sqrt{3}\ln(3)}{2\pi} \le m \le \frac{3}{\pi} (\approx 0.9549)$.

The first modulation range $0 \le m \le \frac{\sqrt{3}}{2}$ is called the under-modulation range while $\frac{\sqrt{3}}{2} \le m \le \frac{3\sqrt{3}\ln(3)}{2\pi}$ and $\frac{3\sqrt{3}\ln(3)}{2\pi} \le m \le \frac{3}{\pi}$ are called over-modulation modes I and II, respectively.

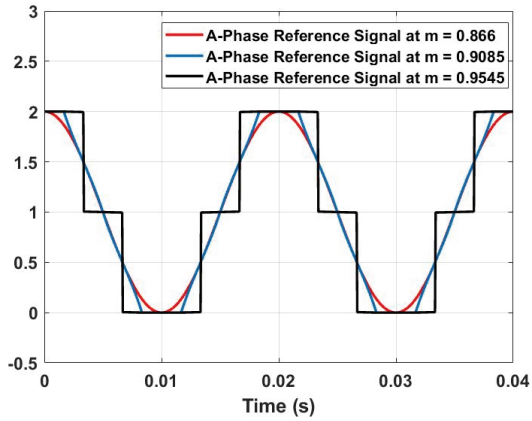


Fig. 9. A-phase reference modulating signal at m = 0.866 (under-modulation mode), m = 0.9085 (over-modulation mode I) and m = 0.9545 (over-modulation mode II).

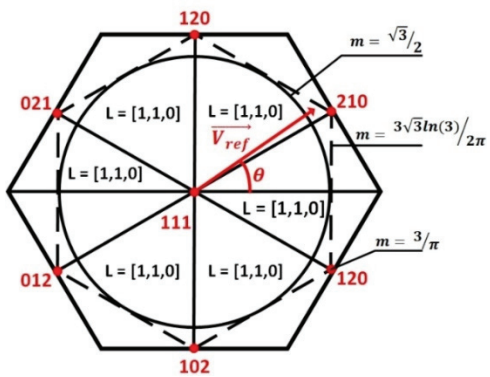


Fig. 10. Overmodulation mode for the zero CMV PWM method with modulation index limits corresponding to the three modulation index ranges, i.e. under-modulation, over-modulation mode I and over-modulation mode II.

Fig. 9 represents the A-phase reference modulating signals associated with three modulation indices, i.e. m = 0.866, 0.9085 and 0.9545. Meanwhile Fig. 10 illustrates the modulation index limits, i.e. m = 0, $\frac{\sqrt{3}}{2}$, $\frac{3\sqrt{3}\ln(3)}{2\pi}$, $\frac{3}{\pi}$ of the three modulation index ranges in the space vector diagram.

In the under-modulation range, the first limit $m_L = 0$ corresponds to the center point of the hexagonal diagram and the second limit $m_H = \frac{\sqrt{3}}{2}$ is the inscribed circle of the small dashed-line hexagon as shown in Fig. 10. The radius of the

inscribed circle is $\frac{1}{2}V_{DC}$.

In over-modulation mode I, the first limit $m_L = \frac{\sqrt{3}}{2}$ is the inscribed circle whose radius is $\frac{1}{2}V_{DC}$, while the second limit $m_H = \frac{3\sqrt{3}\ln(3)}{2\pi}$ is the dashed-line hexagon illustrated in Fig. 10.

In over-modulation mode II, the first limit $m_L = \frac{3\sqrt{3}\ln(3)}{2\pi}$ is the dashed-line hexagon, while the second limit $m_H = \frac{3}{\pi}$ is the six vertices of the dashed-line hexagon, which is represented by the red dots in Fig. 10.

The modulation index limits $\frac{\sqrt{3}}{2}$, $\frac{3\sqrt{3}\ln(3)}{2\pi}$ and $\frac{3}{\pi}$ can be derived by calculating V_{1m} from formula (20) and then substituting it into (19). The fundamental magnitude V_{1m} corresponding to a certain reference voltage vector can be calculated as:

$$V_{1m} = \frac{1}{2\pi}\int_0^{2\pi} \overrightarrow{V_{ref}}\, e^{-j\theta} d\theta \tag{20}$$

where V_{1m} is the fundamental magnitude of the phase voltage corresponding to a particular reference voltage vector. The reference voltage vector $\overrightarrow{V_{ref}}$ is defined as follows.

$$\overrightarrow{V_{ref}} = \begin{cases} 0 \; if \; m = 0 \\ 0.5V_{DC}e^{j\theta}(0 \le \theta \le 2\pi) \; if \; m = \frac{\sqrt{3}}{2} \\ \frac{V_{DC}e^{j\theta}}{2cos\theta}\left(\begin{smallmatrix} 0\le\theta\le\pi/6 \\ 11\pi/6\le\theta\le 2\pi \end{smallmatrix}\right) \; if \; m = \frac{3\sqrt{3}\ln(3)}{2\pi} \\ \frac{1}{\sqrt{3}}V_{DC}e^{j\pi/6}\left(\theta = \pi/6\right) if \; m = \frac{3}{\pi} \end{cases} \tag{21}$$

The reference voltage vector $\overrightarrow{V_{ref}}$ for the other values of the angle θ can be similarly derived.

In order to implement the carrier-based PWM method for both the under-modulation mode and over-modulation modes I and II, three reference signals must be defined, i.e.:

$$v_{xref,m} = (1 - \eta)v_{xref,mL} + \eta v_{xref,mH} \tag{22}$$

where $v_{xref,m}$ is the reference signal of phase X (X$\in \{A, B, C\}$) corresponding to a certain modulation index m ($0 \le m \le \frac{3}{\pi}$). $v_{xref,mL}$ and $v_{xref,mH}$ are the reference signals of phase X corresponding to the first and second limits of a particular modulation index range, respectively. η is a parameter that varies from 0 to 1. η is expressed as:

$$\eta = \frac{m - m_L}{m_H - m_L} \tag{23}$$

$$m_L = \frac{V_{1m,mL}}{\frac{1}{\sqrt{3}}V_{DC}} \tag{24}$$

$$m_H = \frac{V_{1m,mH}}{\frac{1}{\sqrt{3}}V_{DC}} \tag{25}$$

where m_L and m_H are the modulation index of the first and second limits corresponding to a particular modulation index range, respectively. m is the modulation index of the three reference signals. $v_{1m,mL}$ and $v_{1m,mH}$ are the fundamental magnitudes of the first and second limits, respectively.

$v_{1m,mL}$ and $v_{1m,mH}$ must be defined for a particular index range. For example, if $0 \le m \le \frac{\sqrt{3}}{2}(\approx 0.866)$, $v_{1m,mL}$ and $v_{1m,mH}$ are $v_{1m,m=0}$ and $v_{1m,m=0.866}$, respectively. The other modulation index ranges are similar.

$$v_{aref,m=0} = v_{bref,m=0} = v_{cref,m=0} = \frac{n-1}{2} \tag{26}$$

$$v_{aref,m=0.866} = \frac{n-1}{2}\cos(\omega t) + \frac{n-1}{2} \tag{27}$$

$$v_{bref,m=0.866} = \frac{n-1}{2}\cos(\omega t - \frac{2\pi}{3}) + \frac{n-1}{2} \tag{28}$$

$$v_{cref,m=0.866} = \frac{n-1}{2}\cos(\omega t - \frac{4\pi}{3}) + \frac{n-1}{2} \tag{29}$$

$$v_{aref,m=0.9085} = \begin{cases} (n-1) \; if \; \left(\begin{smallmatrix} 0\le\theta\le\frac{\pi}{6} \\ \frac{11\pi}{6}\le\theta\le 2\pi \end{smallmatrix}\right) \\ \frac{(n-1)}{2}\left[\frac{\cos(\theta)}{\cos(\theta-\frac{\pi}{3})} + 1\right] \; if \; \frac{\pi}{6} \le \theta \le \frac{\pi}{2} \\ \frac{(n-1)}{2}\left[\frac{\cos(\theta)}{\cos\left(\theta-\frac{2\pi}{3}\right)} + 1\right] \; if \; \frac{\pi}{2} \le \theta \le \frac{5\pi}{6} \\ \frac{(n-1)}{2}\left[\frac{\cos(\theta)}{\cos(\theta-\pi)} + 1\right] \; if \; \frac{5\pi}{6} \le \theta \le \frac{7\pi}{2} \\ \frac{(n-1)}{2}\left[\frac{\cos(\theta)}{\cos\left(\theta-\frac{4\pi}{3}\right)} + 1\right] \; if \; \frac{7\pi}{6} \le \theta \le \frac{3\pi}{2} \\ \frac{(n-1)}{2}\left[\frac{\cos(\theta)}{\cos(\theta-\frac{5\pi}{3})} + 1\right] \; if \; \frac{3\pi}{2} \le \theta \le \frac{11\pi}{6} \end{cases} \tag{30}$$

$v_{bref,m=0.9085}$ =

$$\begin{cases} \frac{(n-1)}{2}\left[-\frac{1}{2} + \frac{\sqrt{3}}{2}\frac{\sin(\theta)}{\cos(\theta)} + 1\right] \; if \; \left(\begin{smallmatrix} 0\le\theta\le\frac{\pi}{6} \\ \frac{11\pi}{6}\le\theta\le 2\pi \end{smallmatrix}\right) \\ \frac{(n-1)}{2}\left[-\frac{1}{2}\frac{\cos(\theta)}{\cos\left(\theta-\frac{\pi}{3}\right)} + \frac{\sqrt{3}}{2}\frac{\sin(\theta)}{\cos\left(\theta-\frac{\pi}{3}\right)} + 1\right] \; if \; \frac{\pi}{6} \le \theta \le \frac{\pi}{2} \\ \frac{(n-1)}{2}\left[-\frac{1}{2}\frac{\cos(\theta)}{\cos\left(\theta-\frac{2\pi}{3}\right)} + \frac{\sqrt{3}}{2}\frac{\sin(\theta)}{\cos\left(\theta-\frac{2\pi}{3}\right)} + 1\right] \; if \; \frac{\pi}{2} \le \theta \le \frac{5\pi}{6} \\ \frac{(n-1)}{2}\left[-\frac{1}{2}\frac{\cos(\theta)}{\cos(\theta-\pi)} + \frac{\sqrt{3}}{2}\frac{\sin(\theta)}{\cos(\theta-\pi)} + 1\right] \; if \; \frac{5\pi}{6} \le \theta \le \frac{7\pi}{6} \\ \frac{(n-1)}{2}\left[-\frac{1}{2}\frac{\cos(\theta)}{\cos\left(\theta-\frac{4\pi}{3}\right)} + \frac{\sqrt{3}}{2}\frac{\sin(\theta)}{\cos\left(\theta-\frac{4\pi}{3}\right)} + 1\right] \; if \; \frac{7\pi}{6} \le \theta \le \frac{3\pi}{2} \\ \frac{(n-1)}{2}\left[-\frac{1}{2}\frac{\cos(\theta)}{\cos\left(\theta-\frac{5\pi}{3}\right)} + \frac{\sqrt{3}}{2}\frac{\sin(\theta)}{\cos\left(\theta-\frac{5\pi}{3}\right)} + 1\right] \; if \; \frac{3\pi}{2} \le \theta \le \frac{11\pi}{6} \end{cases} \tag{31}$$

$v_{cref,m=0.9085}$=

$$\begin{cases} \frac{(n-1)}{2}\left[-\frac{1}{2} - \frac{\sqrt{3}}{2}\frac{\sin(\theta)}{\cos(\theta)} + 1\right] \; if \; \left(\begin{smallmatrix} 0\le\theta\le\frac{\pi}{6} \\ \frac{11\pi}{6}\le\theta\le 2\pi \end{smallmatrix}\right) \\ \frac{(n-1)}{2}\left[-\frac{1}{2}\frac{\cos(\theta)}{\cos\left(\theta-\frac{\pi}{3}\right)} - \frac{\sqrt{3}}{2}\frac{\sin(\theta)}{\cos\left(\theta-\frac{\pi}{3}\right)} + 1\right] \; if \; \frac{\pi}{6} \le \theta \le \frac{\pi}{2} \\ \frac{(n-1)}{2}\left[-\frac{1}{2}\frac{\cos(\theta)}{\cos\left(\theta-\frac{2\pi}{3}\right)} - \frac{\sqrt{3}}{2}\frac{\sin(\theta)}{\cos\left(\theta-\frac{2\pi}{3}\right)} + 1\right] \; if \; \frac{\pi}{2} \le \theta \le \frac{5\pi}{6} \\ \frac{(n-1)}{2}\left[-\frac{1}{2}\frac{\cos(\theta)}{\cos(\theta-\pi)} - \frac{\sqrt{3}}{2}\frac{\sin(\theta)}{\cos(\theta-\pi)} + 1\right] \; if \; \frac{5\pi}{6} \le \theta \le \frac{7\pi}{6} \\ \frac{(n-1)}{2}\left[-\frac{1}{2}\frac{\cos(\theta)}{\cos\left(\theta-\frac{4\pi}{3}\right)} - \frac{\sqrt{3}}{2}\frac{\sin(\theta)}{\cos\left(\theta-\frac{4\pi}{3}\right)} + 1\right] \; if \; \frac{7\pi}{6} \le \theta \le \frac{3\pi}{2} \\ \frac{(n-1)}{2}\left[-\frac{1}{2}\frac{\cos(\theta)}{\cos\left(\theta-\frac{5\pi}{3}\right)} - \frac{\sqrt{3}}{2}\frac{\sin(\theta)}{\cos\left(\theta-\frac{5\pi}{3}\right)} + 1\right] \; if \; \frac{3\pi}{2} \le \theta \le \frac{11\pi}{6} \end{cases} \tag{32}$$

$$V_{aref,m=0.9549} = \begin{cases} (n-1)\ if\ \left(\begin{smallmatrix} 0 \le \theta \le \frac{\pi}{3} \\ \frac{5\pi}{3} < \theta \le 2\pi \end{smallmatrix}\right) \\ \frac{(n-1)}{2}\ if\ \left(\begin{smallmatrix} \frac{\pi}{3} < \theta \le \frac{2\pi}{3} \\ \frac{4\pi}{3} < \theta \le \frac{5\pi}{3} \end{smallmatrix}\right) \\ 0\ if\ \frac{2\pi}{3} < \theta \le \frac{4\pi}{3} \end{cases} \quad (33)$$

$$V_{bref,m=0.9549} = \begin{cases} (n-1)\ if\ \frac{\pi}{3} < \theta \le \pi \\ \frac{(n-1)}{2}\ if\ \left(\begin{smallmatrix} 0 < \theta \le \frac{\pi}{3} \\ \pi < \theta \le \frac{3\pi}{2} \end{smallmatrix}\right) \\ 0\ if\ \frac{3\pi}{2} < \theta \le 2\pi \end{cases} \quad (34)$$

$$V_{cref,m=0.9549} = \begin{cases} (n-1)\ if\ \pi < \theta \le \frac{5\pi}{3} \\ \frac{(n-1)}{2}\ if\ \left(\begin{smallmatrix} \frac{5\pi}{3} < \theta \le 2\pi \\ \frac{2\pi}{3} < \theta \le \pi \end{smallmatrix}\right) \\ 0\ if\ 0 < \theta \le \frac{2\pi}{3} \end{cases} \quad (35)$$

where: n is the number of levels of the inverter. For example, n = 3 is used for a three-level NPC inverter.

The block diagram shown in Fig. 12 is drawn for complete CMV elimination with reduced CMV spikes for both the under-modulation and over-modulation modes I and II for an odd n-level inverter.

IV. Simulation and Experimental Results

A. Simulation Results

The proposed zero CMV PWM method with reduced CMV spikes is implemented for a three-level NPC inverter in the MATLAB Simulink environment under the condition of V_{DC} = 100V, f_0 = 50 Hz, $f_{carrier}$ = 5 KHz, $C_1 = C_2$ = 4700 μF, $R_a = R_b = R_c$ = 33.3 Ω and $L_a = L_b = L_c$ = 2.7 mH. A high DC-link capacitance value of 4700 μF is selected to smooth out the DC-link voltage. Hence, it has negligible effects on the output quality.

The performance criteria used to evaluate the harmonic distortion of the phase currents and line voltage output are Total Harmonic Distortion (THD) and Weighted Total Harmonic Distortion (WTHD), which are defined as [39]:

$$THD_I = \frac{1}{I_{1m}}\sqrt{\sum_{n=2}^{\infty} I_n^2} \quad (36)$$

$$THD_V = \frac{1}{V_{1mL}}\sqrt{\sum_{n=2}^{\infty} V_{nL}^2} \quad (37)$$

$$WTHD_V = \frac{1}{V_{1mL}}\sqrt{\sum_{n=2}^{\infty} \left(\frac{V_{nL}}{n}\right)^2} \quad (38)$$

where I_{1m} and I_n are the fundamental magnitudes of the phase current and the magnitude of phase current corresponding to the harmonic n, respectively. V_{1mL} and V_{nL} are the fundamental magnitudes of the line voltage output and the magnitude of the line voltage output corresponding to the harmonic n, respectively.

Line-line voltage waveforms of the proposed method for three different modulation indices, i.e. m = 0.8, 0.91 and 0.9374 along with the THD values as shown in Fig. 13. Three different modulation indices which are 0.8, 0.91 and 0.9374 correspond to the under-modulation, overmodulation mode I and overmodulation mode II, respectively. The general trend is that the THD of the line-line voltage of the proposed method decreases as the modulation index increases regardless of the modulation modes as shown Fig.16(b). This is due to the fact that the fundamental magnitude of the line-line voltage output V_{1mL} defined in (37) is proportional to the modulation index m and the magnitudes of harmonic components do not change significantly with a change of the modulation index. Therefore, according to (37), the THD of the line-line voltage output decreases as the modulation index increases. The THD of the line-line voltage of the proposed method is also compared with that of the other two methods, i.e. the Zero CMV PWM method with reduced current ripple [30] and the conventional sinusoidal PWM strategy as illustrated in Fig. 16(b). As expected, the THD of the line-line voltage in the conventional sinusoidal PWM method is much lower than that of the two Zero CMV PWM methods. This is due to the fact that the conventional sinusoidal PWM strategy utilizes the three-nearest vector principle, while the other two strategies use the three farthest vectors. Therefore, the conventional sinusoidal PWM method achieves the optimal harmonics performance as opposed to the two Zero CMV PWM strategies. In terms of the two Zero CMV PWM methods as shown in Fig. 16(b), the proposed Zero CMV PWM with reduced spikes has lower THD values of the line-line voltage than the Zero CMV PWM with reduced current ripple [30] for $m \le 0.75$ and $m \ge 0.85$. For $0.75 < m < 0.85$, the THD values of the line-line voltage in the proposed method are slightly higher than those of the Zero CMV PWM with reduced current ripple [30]. For example, at m = 0.8, the THD values of the line-line voltage for the proposed method, the Zero CMV PWM with reduced current ripple [30], and the conventional Sinusoidal PWM method are 43.93%, 43.55% and 24.79%, respectively. At m = 0.91, the THD values of the line-line voltage for the proposed method, the Zero CMV PWM with reduced current ripple [30], and the conventional Sinusoidal PWM method are 34.2%, 37.64% and 24.42%, respectively. However, in order to evaluate the true harmonic performance of the PWM methods, the WTHD defined in (38) is needed. This is because the low-order harmonic and high-order harmonic components are equally weighted in the THD formula. Fortunately, this is not the case in WTHD since the low-order harmonic components are weighted more heavily than the high-order harmonic components. The lower the WTHD, the better the PWM strategy is at suppressing low-order harmonic components. As shown in Fig. 16(a), the WTHD of the conventional sinusoidal PWM method is the most optimal for a reason similar to the one explained earlier. For the two Zero

CMV PWM methods, the one with reduced current ripple [30] has a significant improvement in terms of harmonic performance in the under-modulation mode and a slight improvement in the over-modulation modes when compared to the proposed one. The aim of the reduced current ripple method [30] is to select the optimal mapping function to reduce ripple. The three-phase current outputs of the proposed method along with their THD values are shown in Fig. 14 for three different modulation indices, i.e. m = 0.8, 0.91 and 0.9374. The THD of the phase current outputs of the proposed method decreases with an increase of the modulation index in the under-modulation mode and then gradually increases in over-modulation modes I and II as illustrated in Fig. 16(c). This is because in over-modulation modes I and II the low-order harmonic components become dominant. For the sake of comparison, the THD of the phase current output of the proposed method is compared with those of the other two methods, i.e. the ZMCV PWM with reduced current ripple [30] and the conventional sinusoidal PWM method. As expected, the THD of the phase current output in the conventional sinusoidal PWM method yields the lowest values for a reason similar to the one explained earlier. As for the two ZCMV PWM strategies, the proposed method produces lower THD values of the phase current output than those of the reduced current ripple method [30] for m ≤ 0.55. For 0.55 ≤ m ≤ 0.866, the reduced current ripple method [30] gives lower THD values than those of the proposed method. In over-modulation modes I and II, the current performance of the proposed method is comparable to that of the reduced current ripple method [30]. The total harmonics distortion (THD) and the weighted total harmonic distortion (WTHD) in the simulation are calculated up to 200th harmonic of the fundamental frequency (f_0 = 50 Hz). Simulated CMV waveforms are shown in Fig. 15 for m = 0.8, 0.91 and 0.9374. As can be seen in this figure, the simulated CMV is completely zero since in the ideal simulation environment the CMV magnitude only depends on the switching voltage states.

In terms of switching loss, the average value of the local (per carrier cycle) switching loss over the fundamental (for instance: for phase A) can be calculated as [31]:

$$P_{loss} = \frac{1}{2\pi}\frac{V_{DC}(t_{on}+t_{off})}{2T_s}\int_0^{2\pi} f_{iA}(\theta)d\theta \quad (39)$$

where t_{on} and t_{off} are the turn-on and turn-off times of the switching devices, respectively. In addition, $f_{iA}(\theta)$ is the switching current function, the instantaneous value of which is defined as a product of the number of commutations on the A phase in the switching period and the absolute value of its corresponding current $|i_A(\theta)|$.

$$f_{iA}(\theta) = k.|i_A(\theta)|; k = \begin{cases} 2 \; if \; A \rightarrow d \\ 1 \quad else \end{cases} \quad (40)$$

The switching loss function (SLF) is defined as:

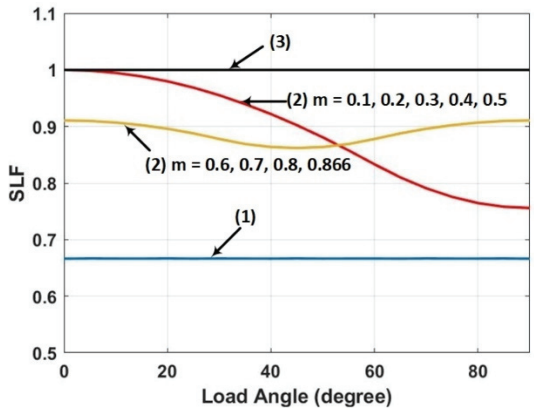


Fig. 11. Switching loss function (SLF) of the proposed method (3) versus the ZCMV PWM method with reduced current ripple (2) and the conventional sinusoidal PWM method (1).

$$SLF = \frac{P_{loss}}{P_0} \quad (41)$$

where P_0 is the maximum value of the switching loss attainable for the defined load current.

Fig. 11 illustrates the switching loss function (SLF) of the proposed method, the ZCMV PWM method with reduced current ripple [30], and the conventional sinusoidal PWM. The SLF of the ZCMV PWM method with reduced current ripple [30] depends on both the modulation index and the load angle. For 0.1 ≤ m ≤ 0.5, the SLF of the reduced current ripple method [30] ranges from 0.76 to 1. Meanwhile, it varies from 0.86 to 0.91 for 0.6 ≤ m ≤ 0.866. The typical power factor of an induction motor varies from around 0.85 to 0.9 at full load to as low as 0.2 at no load [40]. Therefore, at a power factor of 0.85 to 0.9, the switching loss of the reduced current ripple method [30] can be reduced from 9% to 12% for 0.6 ≤ m ≤ 0.866. Meanwhile, it can be reduced from 0% to 4% for 0.1 ≤ m ≤ 0.5 when compared to the proposed method. At a low power factor of 0.2, the switching loss reduction of the reduced current ripple strategy [30] is about 22% for 0.1 ≤ m ≤ 0.5. Meanwhile, it is around 10% for 0.6 ≤ m ≤ 0.866 as opposed to the proposed method. The conventional sinusoidal PWM strategy produces the lowest SLF at about 0.67. Meanwhile, the proposed method gives the highest SLF at 1.

B. Experimental Results

An experiment is conducted on a three-level neutral point clamped inverter with V_{DC} = 60V, $C_1 = C_2$ = 4700 μF, f_0 = 50 Hz, $f_{carrier}$ = 5 KHz, $R_a = R_b = R_c$ = 33.3 Ω, $L_a = L_b = L_c$ = 2.7 mH and deadtime = 2 μs. The experimental line-line voltage and phase current for the three different PWM methods, i.e. the conventional Sinusoidal PWM, the ZCMV PWM with reduced current ripple [30], and the proposed ZCMV PWM with reduced CMV spikes at a modulation index of m = 0.3 are shown in Fig. 17(a), (b) and (c), respectively. Similarly, the line-line voltage and phase current for the three PWM

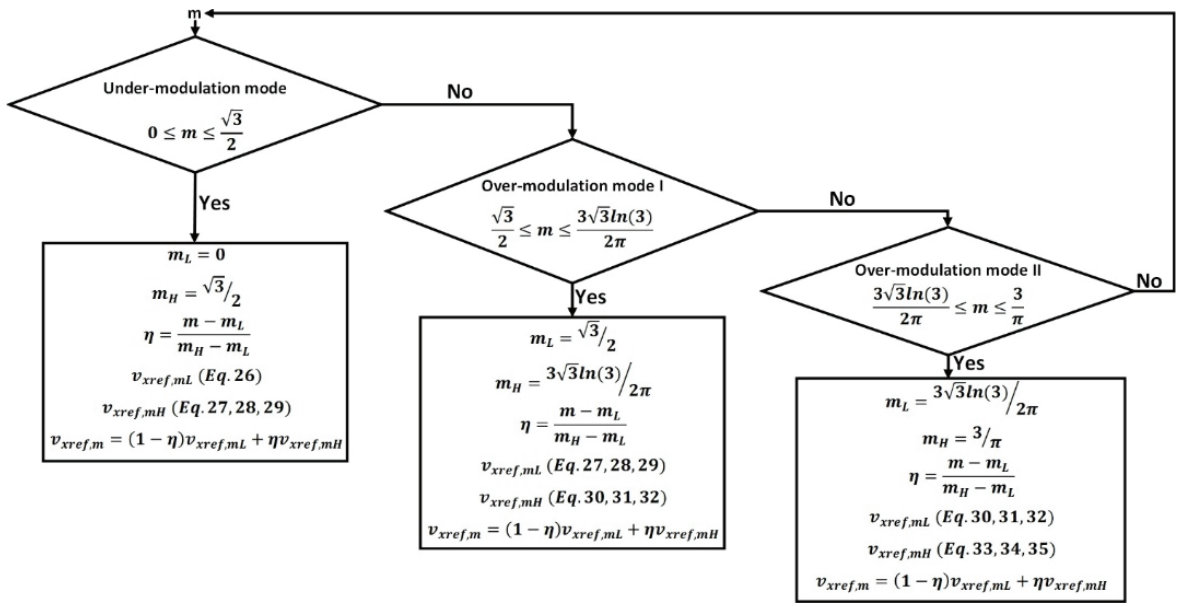
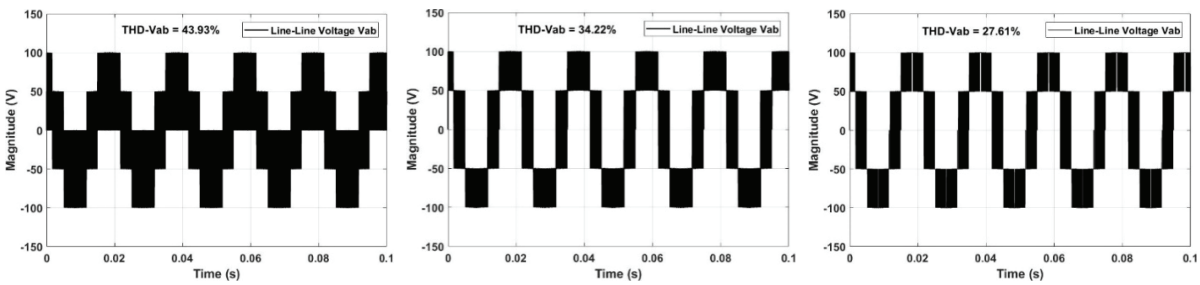
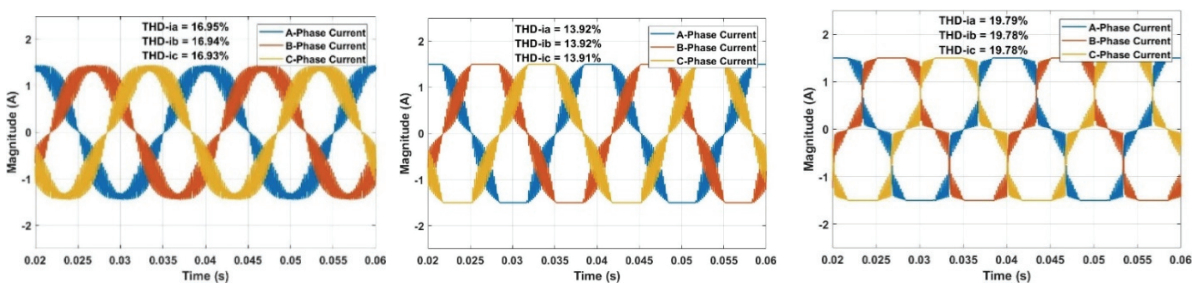


Fig. 12. Under-modulation and over-modulation modes for the complete CMV elimination PWM method by utilizing the two-limit trajectory principle.



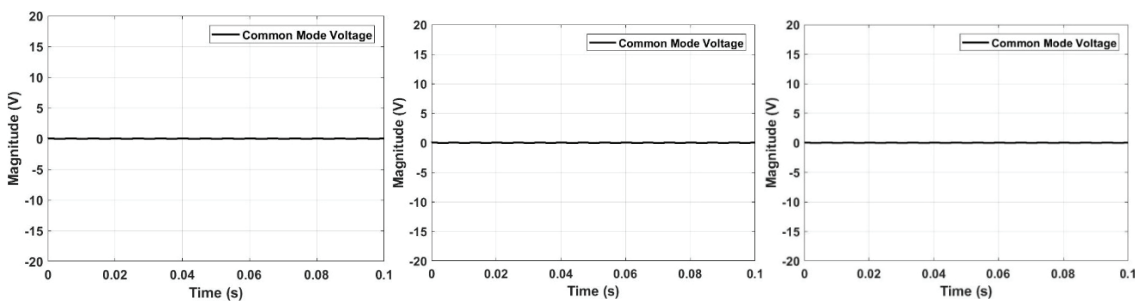
(a) (b) (c)

Fig. 13. Simulated line-line voltages for the proposed method. (a) m = 0.8. (b) m = 0.91. (c) m = 0.9374.



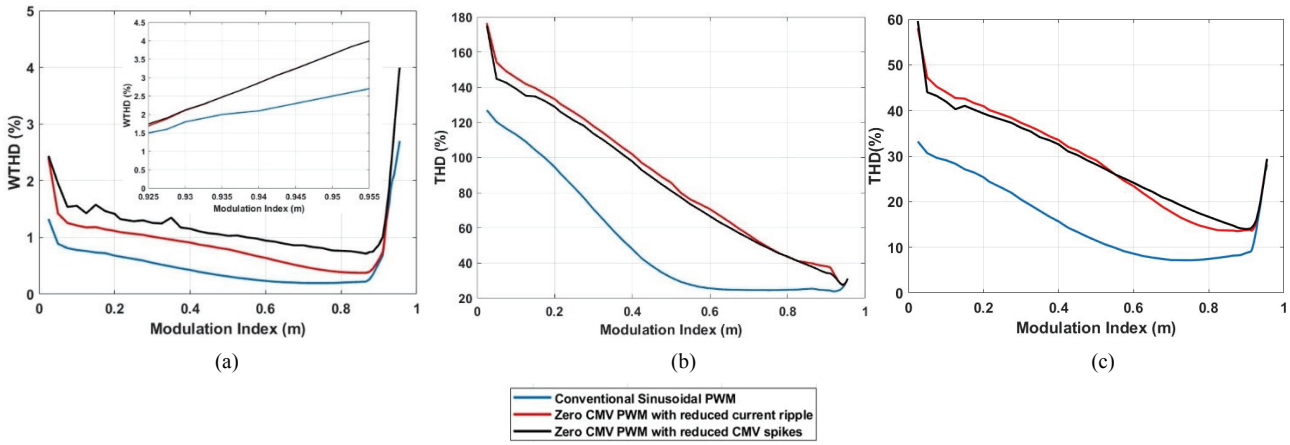
(a) (b) (c)

Fig. 14. Simulated three-phase currents i_a, i_b and i_c for the proposed method. (a) m = 0.8. (b) m = 0.91. (c) m = 0.9374.



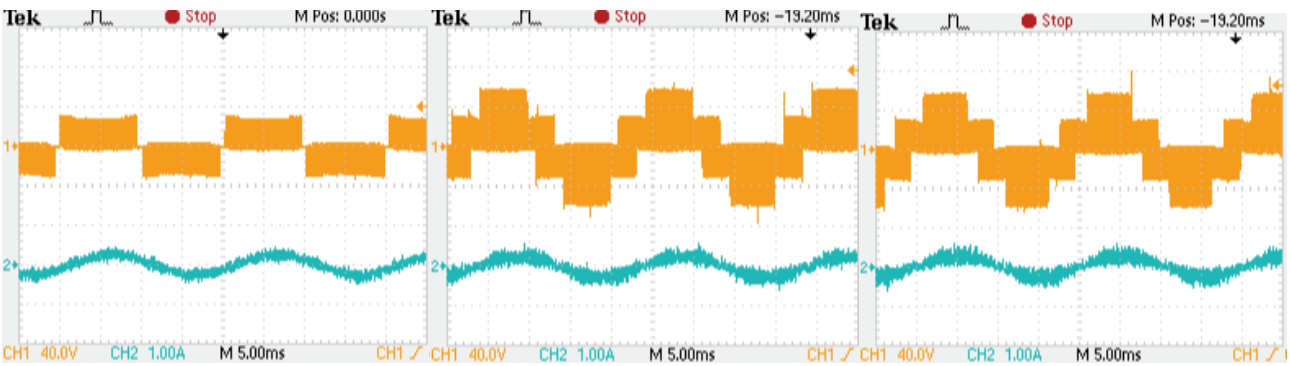
(a) (b) (c)

Fig. 15. Simulated common mode voltage waveforms for the proposed method. (a) m = 0.8. (b) m = 0.91. (c) m = 0.9374.



(a) (b) (c)

Fig. 16. Graphs showing. (a) WTHD of the simulated line-line voltage. (b) THD of the simulated line-line voltage. (c) THD of the simulated phase current with respect to the modulation index m for three different methods, i.e. the conventional sinusoidal PWM method, the Zero CMV PWM method with reduced current ripple [30], and the proposed Zero CMV PWM method with reduced CMV.

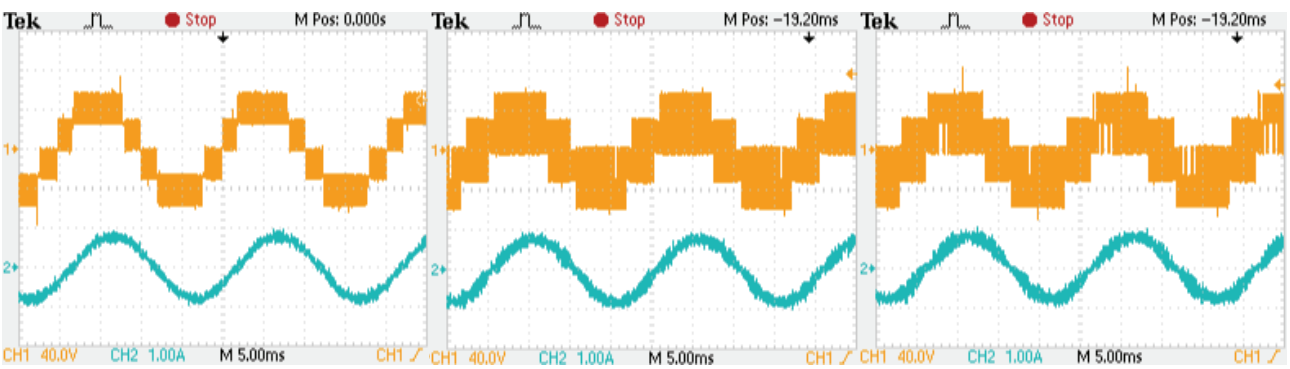


Top trace: 40V/div, 5ms/div
Bottom trace: 1A/div, 5ms/div
(a)

Top trace: 40v/div, 5ms/div
Bottom trace: 1A/div, 5ms/div
(b)

Top trace: 40V/div, 5ms/div
Bottom trace: 1A/div, 5ms/div
(c)

Fig. 17. Experimental line-line voltage output (top trace) and phase current output (bottom trace) at a modulation index of m = 0.3 (under-modulation mode). (a) For conventional sinusoidal PWM (THD_V = 88.2%, THD_I = 23.1%). (b) For zero CMV PWM with reduced current ripple (THD_V = 172.9%, THD_I = 42.39%) [30]. (c) For proposed Zero CMV PWM with reduced CMV spikes (THD_V = 158.16%, THD_I = 40.56%).

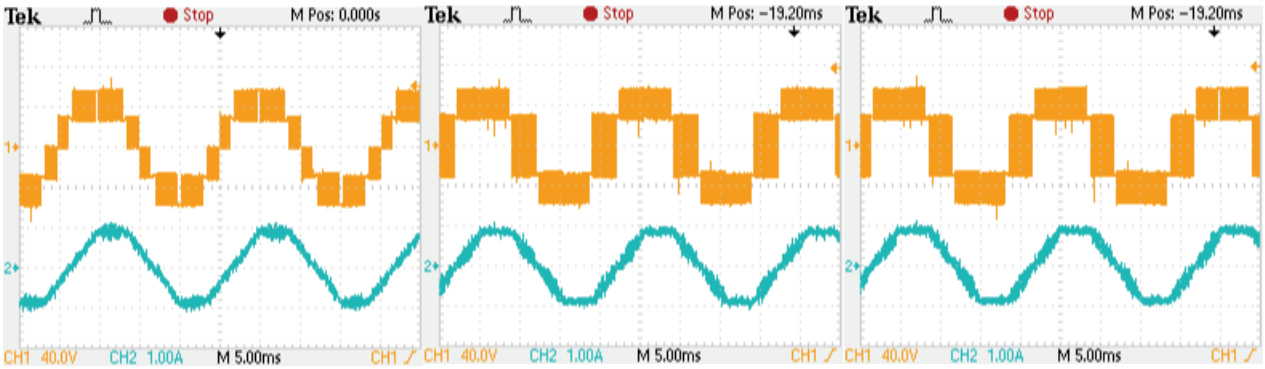


Top trace: 40V/div, 5ms/div
Bottom trace: 1A/div, 5ms/div
(a)

Top trace: 40v/div, 5ms/div
Bottom trace: 1A/div, 5ms/div
(b)

Top trace: 40V/div, 5ms/div
Bottom trace: 1A/div, 5ms/div
(c)

Fig. 18. Experimental line-line voltage output (top trace) and phase current output (bottom trace) at a modulation index of m = 0.8 (under-modulation mode). (a) For conventional sinusoidal PWM (THD_V = 29.35%, THD_I = 8.16%). (b) For zero CMV PWM with reduced current ripple (THD_V = 52.32%, THD_I = 14.23%) [30]. (c) For proposed Zero CMV PWM with reduced CMV spikes (THD_V = 53.32%, THD_I = 16.68%).

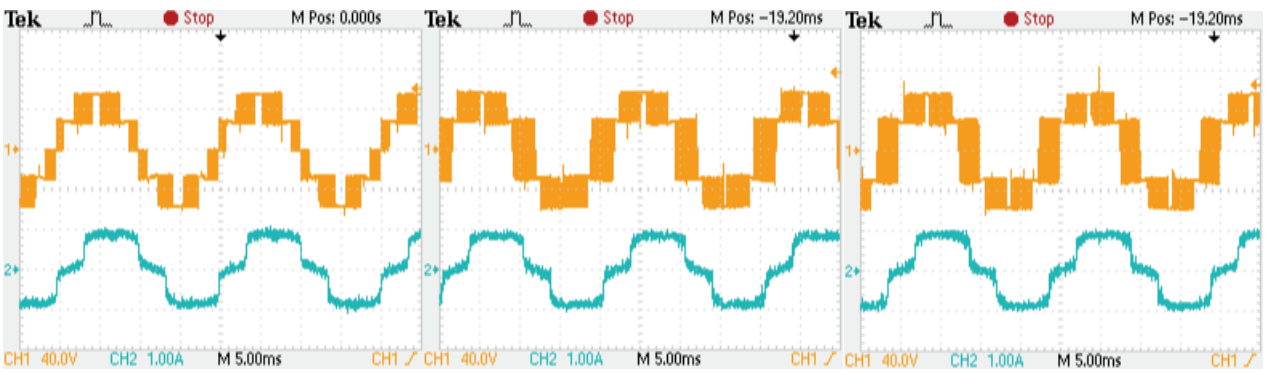


Top trace: 40V/div, 5ms/div
Bottom trace: 1A/div, 5ms/div
(a)

Top trace: 40V/div, 5ms/div
Bottom trace: 1A/div, 5ms/div
(b)

Top trace: 40V/div, 5ms/div
Bottom trace: 1A/div, 5ms/div
(c)

Fig. 19. Experimental line-line voltage output (top trace) and phase current output (bottom trace) at a modulation index of m = 0.91 (over-modulation mode I). (a) For conventional sinusoidal PWM (THD_V = 29.18%, THD_I = 8.81%). (b) For zero CMV PWM with reduced current ripple (THD_V = 43.48%, THD_I = 14.17%) [30]. (c) For proposed Zero CMV PWM with reduced CMV spikes (THD_V = 43.41%, THD_I = 14.21%).

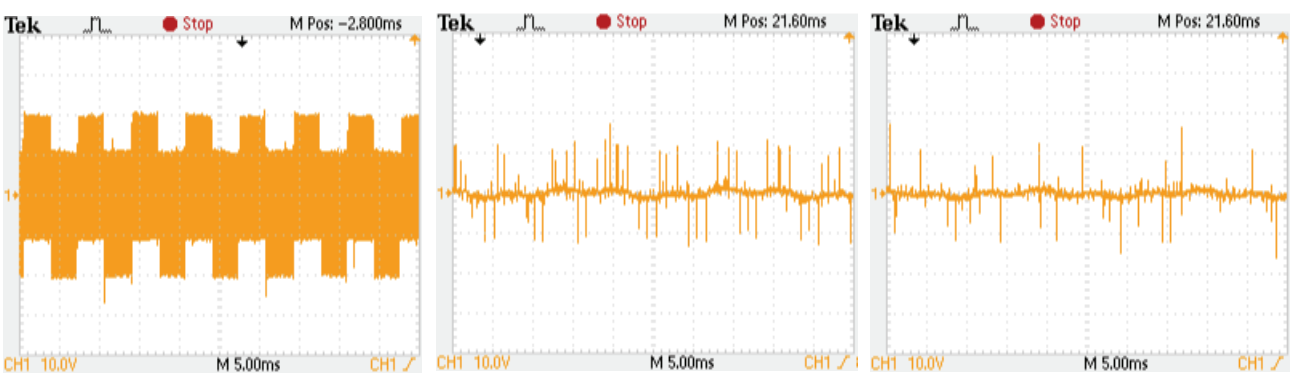


Top trace: 40V/div, 5ms/div
Bottom trace: 1A/div, 5ms/div
(a)

Top trace: 40V/div, 5ms/div
Bottom trace: 1A/div, 5ms/div
(b)

Top trace: 40V/div, 5ms/div
Bottom trace: 1A/div, 5ms/div
(c)

Fig. 20. Experimental line-line voltage output (top trace) and phase current output (bottom trace) at a modulation index of m = 0.9374 (over-modulation mode II). (a) For conventional sinusoidal PWM (THD_V = 29.45%, THD_I = 20.31%). (b) For zero CMV PWM with reduced current ripple (THD_V = 32.66%, THD_I = 22%) [30]. (c) For proposed Zero CMV PWM with reduced CMV spikes (THD_V = 32.39%, THD = 21.89%).

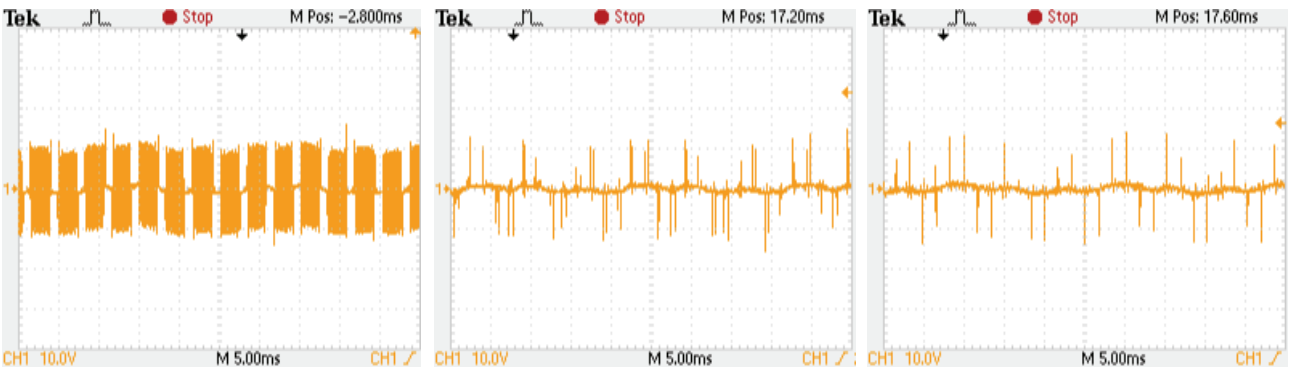


(a) (b) (c)

Fig. 21. Experimental CMV waveforms at a modulation index of m = 0.8 (under-modulation mode). (a) For conventional sinusoidal PWM. (b) For zero CMV PWM with reduced current ripple [30]. (c) For proposed Zero CMV PWM with reduced CMV spikes, Y-axis: 10V/div, X-axis: 5ms/div.

(a) (b) (c)

Fig. 22. Experimental CMV waveforms at a modulation index of m = 0.91 (over-modulation mode I). (a) For conventional sinusoidal PWM. (b) For zero CMV PWM with reduced current ripple [30]. (c) For proposed Zero CMV PWM with reduced CMV spikes, Y-axis: 10V/div, X-axis: 5ms/div.



(a) (b) (c)

Fig. 23. Experimental CMV waveforms at a modulation index of m = 0.9374 (over-modulation mode II). (a) For conventional sinusoidal PWM. (b) For zero CMV PWM with reduced current ripple [30]. (c) For proposed Zero CMV PWM with reduced CMV spikes, Y-axis: 10V/div, X-axis: 5ms/div.

strategies at m = 0.8, 0.91 and 0.9374 are shown in Fig. 18, 19 and 20, respectively. The experimental line-line voltage and phase current for the proposed method at different modulation indices bear a close resemblance to the ones shown in the simulation section. With regard to the THD values of the experimental line-line voltage, the general trend is that the THD values decrease as the modulation index increases. This is consistent with the results shown in Fig. 16(b). For example, at m = 0.8, the THD values of the experimental line-line voltage for the proposed method, the Zero CMV PWM with reduced current ripple [30], and the conventional Sinusoidal PWM method are 53.32%, 52.32% and 29.35%, respectively. At m = 0.91, the THD values of the experimental line-line voltage for the proposed method, the Zero CMV PWM with reduced current ripple [30], and the conventional Sinusoidal PWM method are 43.41%, 43.48% and 29.18%, respectively. The THD values of the line-line voltage for the conventional Sinusoidal PWM strategy is the lowest among the three methods. As far as the THD of the experimental phase current is concerned, it is consistent with the simulation results. The THD of the experimental phase current of the proposed method produces a lower value than that of the reduced ripple method [30] at m = 0.3. For example, it is 40.56% in the proposed method as opposed to 42.39% in the reduced ripple method [30]. At m = 0.8, the proposed strategy yields a higher THD value for the experimental phase current than that of the reduced ripple method [30]. In particular, it is 16.68% in the proposed method compared to 14.23% in the reduced ripple method [30]. At m = 0.91 and 0.9374, the current performance of the proposed method is comparable to that of the reduced ripple method [30]. In terms of CMV waveforms, the CMV of the conventional sinusoidal PWM method has a peak of 20V or one-third of the DC-link voltage (V_{DC} = 60V) at m = 0.8 as illustrated in Fig. 23(a). Meanwhile, it has a peak of 10V or one-sixth of the DC-link voltage at m = 0.91 and m = 0.9374 as demonstrated in Fig. 24(a) and Fig. 25 (a), respectively. The two zero CMV PWM methods virtually eliminate CMV despite some spikes still existing in the waveforms when compared to the other methods as shown in Fig. 23(b) and (c), Fig. 24(b) and (c), and Fig. 25(b) and (c). The proposed strategy obtains better CMV waveforms at the three modulation indices.

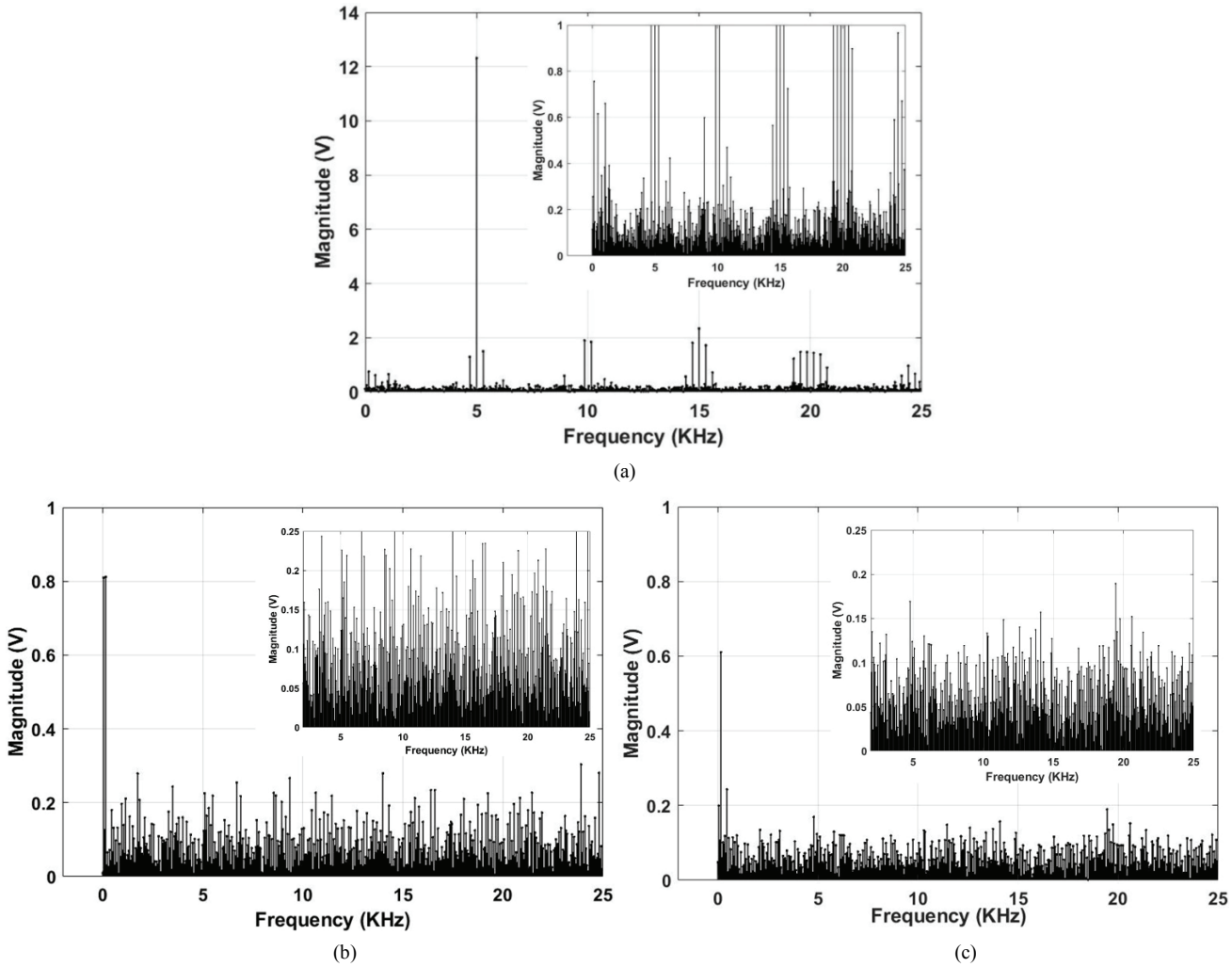


Fig. 24. Experimental frequency spectra of CMV waveforms at a modulation index of m = 0.8 (under-modulation mode). (a) For conventional sinusoidal PWM. (b) For zero CMV PWM with reduced current ripple [30]. (c) For proposed Zero CMV PWM with reduced CMV spikes.

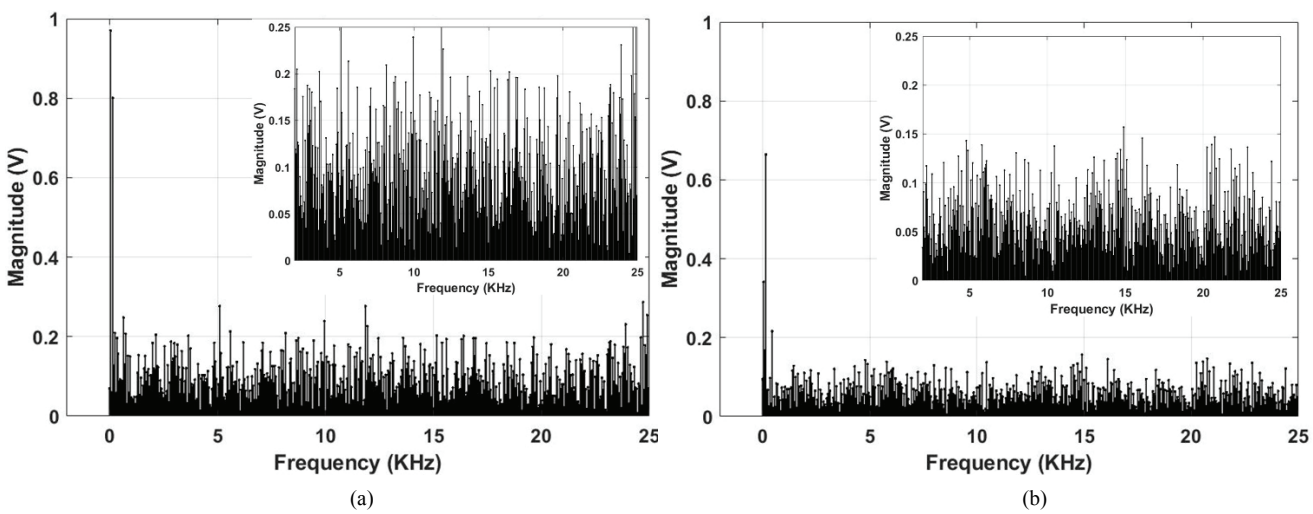
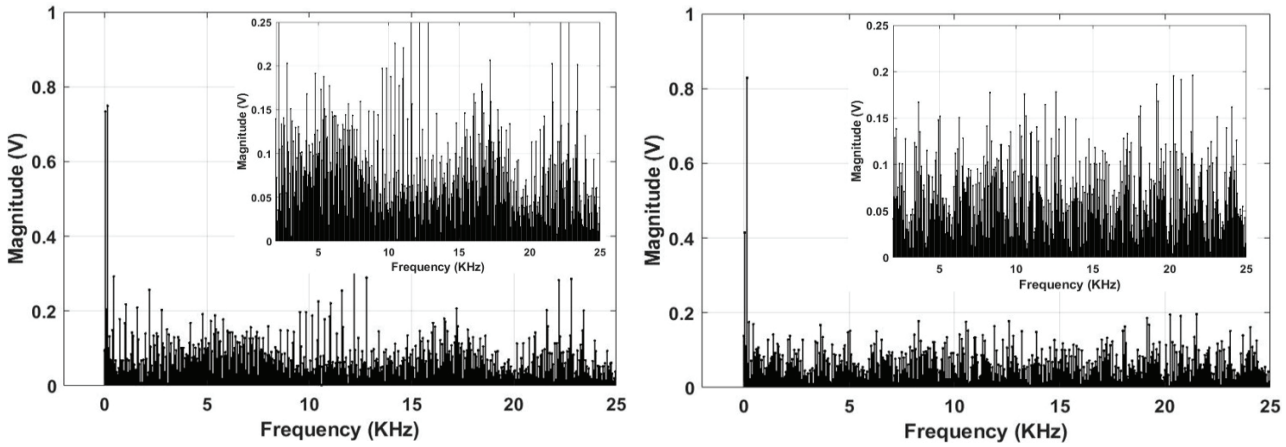


Fig. 25. Experimental frequency spectra of CMV waveforms at a modulation index of m = 0.91 (over-modulation mode I). (a) For zero CMV PWM with reduced current ripple [30]. (b) For proposed Zero CMV PWM with reduced CMV spikes.



(a) (b)

Fig. 26. Experimental frequency spectra of CMV waveforms at a modulation index of m = 0.9374 (over-modulation mode II). (a) For zero CMV PWM with reduced current ripple [30]. (b) For proposed Zero CMV PWM with reduced CMV spikes.

This is confirmed by the frequency spectra shown in Fig. 26, 27 and 28 for the three different modulation indices. At high frequencies ($f \geq 5$ KHz), as shown in the magnified frequency spectra, the magnitudes of the high-frequency components of the CMV in the proposed method are well below 0.2V. Meanwhile, it is above 0.2V in the Zero CMV PWM method with reduced current ripple [30] for the three modulation indices, i.e. m = 0.8, m = 0.91 and m = 0.9374. This validates the effectiveness of the proposed method for both the under-modulation and over-modulation modes.

V. Conclusions

This paper proposes a PWM strategy to eliminate the CMV of multilevel inverters with an extension to the over-modulation mode. This method utilizes the three zero CMV vectors. The modulation process of a multilevel inverter is simplified to that of a two-level inverter. Two standardized virtual PWM patterns are then proposed to cover the whole space vector diagram. There are six possible mapping functions corresponding to each PWM pattern and the mapping function selection depends upon the control purpose. The deadtime effect is thoroughly investigated and a zero CMV PWM method with reduced spikes is proposed. The proposed strategy is then extended to the over-modulation mode, where the analytical functions of the three reference modulating signals are explicitly derived. Experimental results confirm the effectiveness the proposed method in eliminating CMV and in reducing its spikes for both the under-modulation and over-modulation modes.

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