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High Quality DC-DC Boosting Converter Based on Cuk Converter and Advantages of Using It in Multilevel Structures

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Abstract

In this paper, a DC-DC converter is proposed based on the Cuk converter. The proposed converter has high efficiency and it can be used in multilevel DC-DC converters. A reduction of the inductors size in comparison to Cuk converter and a reduction in the inductors resistance negative effects on efficiency are the important points of the proposed converter. Its voltage ripple is reduced when compared to other converters. Its output voltage has a high quality and does not contain spikes. A theoretical analysis demonstrates the positive points of the proposed converter. The design and analysis of the converter are done in continues conduction mode (CCM). Experiments confirm the obtained theoretical equations. The proposed converter voltage gain is similar to that of a conventional Boost converter. As a result, they are compared. The comparison illustrates the advantages of the proposed converter and its higher quality. Furthermore, a prototype of the proposed converter and its combination with a 2x multiplier are built in the lab. Experimental results validate the analysis. In addition, they are in good agreements with each other.

Key words: Boost converter, DC-DC converter, Fuel cell applications, Multilevel converter, Photovoltaic applications, Spikes

I. INTRODUCTION

There are several problems when it comes to achieve a high voltage gain with conventional DC-DC converters [1]. The efficiency and operation quality of these converters are influenced by switching in high duty cycles. According to the voltage conversion ratio equations of conventional converters, they should convert input to a high voltage. However, problems like the inductor resistance effect, power loss and voltage drop on non-ideal components limit their operation in high duty cycles [2].

Solving these problems requires new topologies based on conventional converters such as boost, buck-boost [3], SEPIC, Cuk and Zeta converters. To increase the boosting gain, new topologies have been presented [4]. In some of them, the switching method between the inductors and capacitors have been changed. The others contain new methods such as the voltage-lift technique, which use multipliers and cascading as the second step of boosting the voltage. These topologies poses drawbacks that provide the motivations for proposing new structures [5], [6]. The main cause of these drawbacks is the base converter of multilevel systems. For example, using boost or SEPIC converters in a multilevel converter imposes voltage ripple on the output voltage [7]-[9].

Boost and buck-boost converters are conventional converters that have been frequently used in fuel cell systems and photovoltaic energy applications [8], [10]-[14]. In [10] and [11], a hybrid boost and a double switch buck-boost converter are used for PV systems to increase the voltage gain and to extract the maximum power by the MPPT method. The authors of [12] proposed a quadratic buck-boost converter with positive output voltage and a continuous input current. In addition, [13] considers a soft switching method to decrease the switching losses in a boost converter. Some of these papers discus new techniques such as using interleaved converters to make the input current continuous [14], [15].

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Using the interleaved method simultaneously reduces the output voltage ripple and the input current ripple [16]. Furthermore, it improves voltage gain and efficiency. The negative point of using conventional boost and buck-boost converters in interleaved and multilevel structures is the fact that they produce spikes in the inductors current and output voltage, which can be seen in the experimental results [14], [15].

The Cuk converter is another conventional converter that can be studied for boosting applications. The Cuk converter is used in various kinds of applications such as MPPT systems and multi-output converters [17], [18]. Thus, it can be a candidate for connecting renewable source to loads. The Cuk conversion voltage ratio makes it an unsuitable choice for use as a boosting mode converter. Its voltage gain has a lower value in comparison to a boost converter per the whole duty cycles. Both boost and Cuk converters have voltage gain equations equal to $\frac{1}{1-D}$ and $M=-\frac{D}{1-D}$, respectively. If the Cuk conversion ratio increases by some changes in its structure, it may convert voltage with higher qualities in comparison to conventional converters. Thus, the possibility of changing a Cuk converter to obtain a new high-quality structure for the boosting mode is investigated in this paper.

In this paper, a new boosting converter is proposed. Its structure is based on a Cuk converter with a new formation. The proposed converter does not contain additional parasitic components (inductor or capacitor) in comparison to Cuk converter. It is designed in a way that improves its efficiency and reduces its voltage ripple in comparison to conventional boost and Cuk converters. In addition, its voltage gain is similar to boost converter and it has higher values in comparison to Cuk converter. Furthermore, the negative impact of the inductor resistances in the proposed converter is less than those of Cuk and boost converters. The other positive point of the proposed converter is its high-quality current and voltage waveforms, which do not contain spikes. The proposed converter has an efficiency of more than 96% in $D\leq 0.65$ and more than 90% in $0.65 \leq D \leq 0.75$. This makes it a good choice to be used in the multilevel converters for photovoltaic and fuel cell applications. The extension of the converter to multilevel is possible by combining it with capacitors and diodes. The multilevel converter operates with a high efficiency, high voltage gain and good quality due to the high-quality factors of the proposed converter.

The paper is organized as follows. In section 1, a theoretical analysis of the proposed converter is done for the CCM condition. According to the analysis results, the voltage gain of the proposed converter and the boost converter are too similar. Thus, in section 2, prototypes of the proposed converter, its combination with a 2x multiplier, a boost converter and its combination with a 2x multiplier are built. Experimental results are used to validate analysis results in the previous sections. In addition, the efficiency curves, voltage ripple and voltage conversion ratio curves of both the prepared prototypes and the boost converter are extracted for comparing their operations under real conditions.

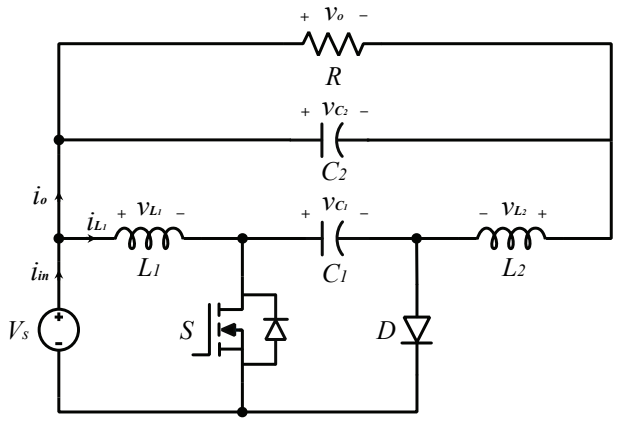


Fig. 1. Proposed converter topology.

II. Operation of the Proposed Converter

The proposed topology is a DC-DC boosting converter, where the quality of the operation and the outputs can be improved. The Cuk converter topology is changed for improving quality of the output voltage and for increasing its gain. Fig. 1 depicts the changed Cuk converter topology, where a new layout of the elements is visible. The location of charging capacitor is varied, which reforms the converter equations.

As shown in Fig. 1, the new topology involves the input source V_s, two inductors L_1 and L_2, two capacitors C_1 and C_2, a diode and a power switch. According to the topology, the circuit has two operations stages. In the first step, an analysis is done based on ideal elements and the CCM operation condition. Fig. 2(a) shows the switch on state and the circuit operation under this situation. Fig. 2(b) illustrates the switch off state as the second stage.

During the duty cycle, the power switch is turned on by a PWM signal and current flows in the charging elements (L_1, L_2 and C_1). In addition, i_{L1}, i_{L2} and V_{c1} denote current of the inductors and the capacitor voltage (key waveforms of the converter are illustrated in Fig. 2(c) to help understand the converter operation in the on and off states). Due to the reversal voltage, the diode is blocked. In this step, there are two loops for energizing the elements. The voltage of L_1 is equal to V_s, which increases the inductor current flow. The second loop consists of V_s, L_2, C_1 and a load, where the energy is delivered to L_2 by the source and C_1. The noticeable point is the simultaneous charging of the elements. Due to the paralleling of the diode and C_1, the diode voltage stress is similar to V_{c1}. According to the descriptions and Fig. 2(a), the circuit equations can be written as follows.

$$\begin{cases} L_1 \dfrac{di_{L1}}{dt} = V_s \\ L_2 \dfrac{di_{L2}}{dt} = V_s + v_{c1} - V_o \\ C_1 \dfrac{dv_{c1}}{dt} = i_{L2} \\ C_2 \dfrac{dv_{c2}}{dt} = \dfrac{V_o}{R} - i_{L2} \end{cases} \quad (1)$$

In the second stage, the power switch is turned off and the diode conducts. Similar to the previous step, there are two current loops. Through the diode, the inductor L_1 energizes the capacitor C_1. The other inductor L_2 discharges and supplies the output branch (C_2 and load). The inductor L_1 and V_s produce voltage stress on the power switch equal to V_s-V_{L1}. According to Fig. 2(b), the circuit equations can be obtained as follows.

$$\begin{cases} L_1 \dfrac{di_{L1}}{dt} = V_s - v_{c1} \\ L_2 \dfrac{di_{L2}}{dt} = V_s - V_o \\ C_1 \dfrac{dv_{c1}}{dt} = i_{L1} \\ C_2 \dfrac{dv_{c2}}{dt} = i_{L2} - \dfrac{V_o}{R} \end{cases} \quad (2)$$

The voltage conversion ratio is the most important parameter in a DC-DC converter. It is obtainable by the equations of the two stages. The inductors L_1 and L_2 make the voltage balanced through their charge and discharge. The inductors average voltage during a period is equal to zero due to their operations in transferring energy. The average voltage equation of the inductors can be written with equations (1) and (2). The DC values of i_{L1}, i_{L2}, v_{c1} and v_{c2} are assumed as I_{L1}, I_{L2}, V_{c1} and V_{c2} in the average voltage equation (equation (3)).

$$\begin{cases} DV_s + (1-D)(V_s - v_{c1}) = 0 \\ D(V_s + v_{c1} - v_o) + (1-D)(V_s - v_o) = 0 \end{cases} \quad (3)$$

From the equations, V_{c1} and V_o/V_s are obtained as follows.

$$V_{c1} = \frac{1}{(1-D)} V_s \quad (4)$$

$$\frac{V_o}{V_s} = \frac{1}{(1-D)} \quad (5)$$

The voltage conversion ratio of the proposed converter is similar to that of a boost converter. Thus, it has to be compared with conventional Cuk and boost converters.

A comparison between the proposed circuit and the others is possible by an analysis of the voltage and current stresses on the power switch, boundaries of the CCM and the DCM, variation ratio of current, variation ratio of voltage and minimum inductance of the inductors. The mentioned parameters are calculated for the proposed converter. Some of the important parameters are compared with DC-DC converters in Table I.

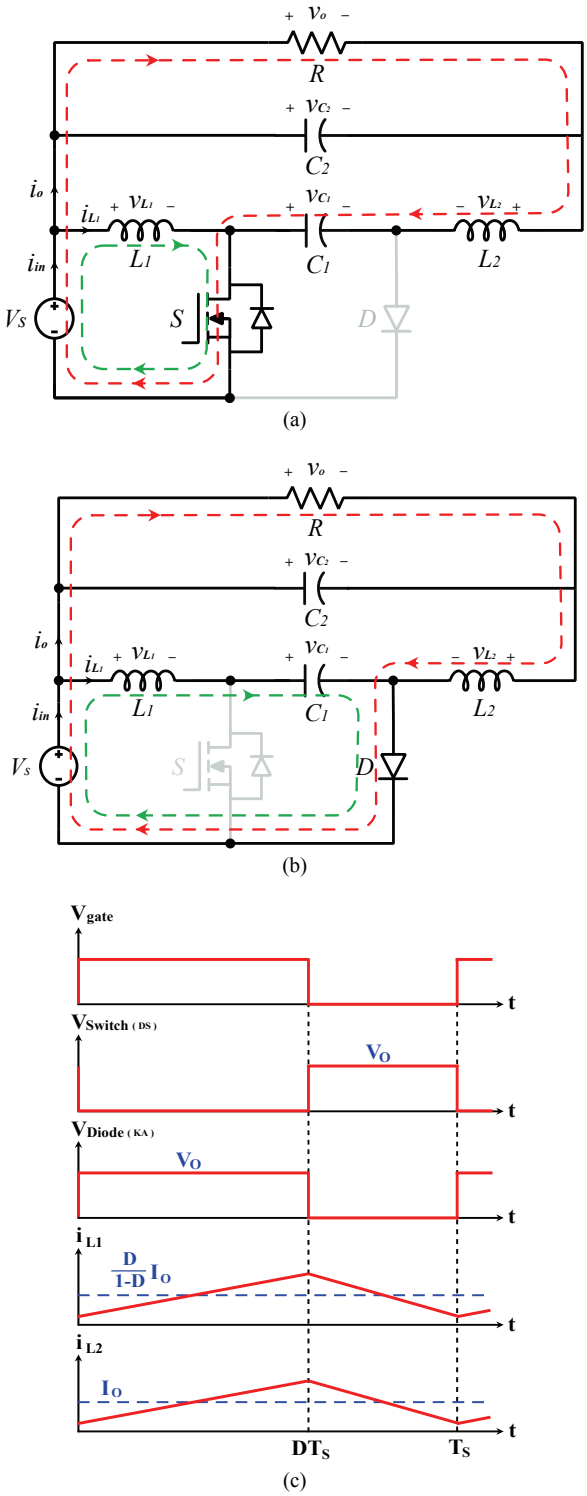


Fig. 2. Switch on and switch off states for the proposed converter. (a) First Stage, switch is on. (b) Second stage, switch is off. (c) Key waveforms of the converter.

The voltage stresses of the diode and the power switch are obtainable according to the stages. During the first stage, the diode is off and its reverse voltage is equal to:

TABLE I
COMPARISON OF THE PROPOSED CONVERTER WITH SIMILAR CONVERTERS

	Proposed converter	Cuk converter	SEPIC converter	Boost converter	Buck-Boost converter
M	$\frac{1}{1-D}$	$\frac{-D}{1-D}$	$\frac{D}{1-D}$	$\frac{1}{1-D}$	$\frac{-D}{1-D}$
L_{1min}	$\frac{(1-D)^2 R}{2f}$	$\frac{(1-D)^2 R}{2fD}$	$\frac{(1-D)^2 R}{2fD}$	$\frac{D(1-D)^2 R}{2f}$	$\frac{(1-D)^2 R}{2f}$
L_{2min}	$\frac{D(1-D)R}{2f}$	$\frac{(1-D)R}{2f}$	$\frac{(1-D)R}{2f}$	–	–
$\frac{\Delta Vo}{Vo}$	$\frac{D(1-D)}{8L_2C_2f^2}$	$\frac{(1-D)}{8L_2C_2f^2}$	$\frac{D}{RC_2f}$	$\frac{D}{RCf}$	$\frac{D}{RCf}$

$$V_{diode} = -V_{c1}$$
$$V_{diode} = -\frac{1}{1-D}V_s \quad (6)$$

In the second stage, the diode conducts and the power switch does not get a PWM signal. Therefore, its voltage stress is:

$$V_s - V_{L1} = V_{switch}$$
$$V_s - (V_s - V_{c1}) = V_{switch}$$
$$V_{switch} = V_{c1} = \frac{1}{1-D}V_s \quad (7)$$

The inductors make power balance between the input and the output. Based on the balance equation, I_{L1} and I_{L2} are found, which helps to derive the following current stress equations.

Power balance equation:

$$V_o i_o = V_s (i_{L1} + i_{L2}) \quad (8)$$

From equation (8):

$$i_{L1} = \frac{D}{1-D} i_o \quad (9)$$

$$i_{L2} = i_o = \frac{V_o}{R} \quad (10)$$

Current stress of the power switch:

$$I_{switch} = \frac{D}{1-D} I_o \quad (11)$$

Current stress of the diode:

$$i_{diode} = I_o \quad (12)$$

The variation ratio of the current defines the minimum inductance of the inductors for the continuous current mode (CCM). In DC-DC converters, the inductors and their characteristics are important and there are noticeable differences between them. Variation of the current for the inductors and their inductance can be obtained during the stages. The inductor current varies with the same values in switch on and switch off states. Thus, the inductors peak-to-peak current ripple can be calculated in one switch state as follows.

$$\Delta I_{L1} = \frac{DT_s}{L_1} V_s \quad (13)$$

$$\Delta I_{L2} = \frac{DT_s}{L_2} V_s \quad (14)$$

The current ripple for both of the inductors is similar. Thus, their current variation is:

$$\frac{\Delta I_L}{2} = \frac{DT_s}{2L} V_s \quad (15)$$

There is a boundary between the CCM and the DCM, which describes the inductance of the inductors. Based on the fact that I_{Lmin} has zero value in the boundary, the minimum inductance of the inductors can be calculated.

$$I_{L\min} = I_L - \frac{\Delta I_L}{2} \quad (16)$$

$$L_{1\min} = \frac{(1-D)^2 R}{2f} \quad (17)$$

$$L_{2\min} = \frac{D(1-D)R}{2f} \quad (18)$$

The last parameter is the peak-to-peak voltage ripple, which validates the quality of the output voltage. It can be derived by differential equations of the circuit. For the two capacitors in the proposed circuit, the voltage ripple is equal to:

$$\frac{\Delta V_{c1}}{V_{c1}} = \frac{RC_1}{D} f \quad (19)$$

$$\Delta V_{c2} = \Delta V_o$$
$$\frac{\Delta V_o}{V_o} = \frac{D(1-D)}{8L_2C_2f^2} \quad (20)$$

III. COMPARISON OF THE PROPOSED CONVERTER WITH CONVENTIONAL CONVERTERS

The proposed converter is comparable to conventional converters according to the obtained equations. The main comparison is done with boost and Cuk converters, which have structures and applications that are the same as the proposed converter. The compared equations in Table I consist of the voltage conversion ratio, minimum inductance

for the CCM condition and output voltage ripple.

The voltage conversion ratio of the proposed converter is similar to the boost. Changing the Cuk topology has made its application the same as the boost. In comparison to boost converter, the converter has less voltage ripple during operation and a higher efficiency (this is proved by experimental results).

Furthermore, the proposed converter's inductors seem to be smaller than the Cuk inductors. Based on the equations in Table I, the ratio of L_{min} for the proposed converter and the Cuk converter is D (in most of applications D is $0 \le D \le 0.8$). Smaller inductance result in a smaller voltage drop and less power loss in the proposed converter, which are important parameters in high duty cycle operations. In fact, the changed Cuk converter has a larger voltage conversion ratio in comparison to the Cuk (in the boosting mode) and it needs smaller inductors, which means less impact of the ESR on the output and a higher efficiency. The ratio between voltage ripple equations in Table I indicates that the proposed converter has less voltage ripple with the coefficient D.

A comparison with a Cuk converter shows that the proposed converter has a higher quality and a higher voltage conversion ratio in the boosting mode. Thus, the converter is compared to a boost converter in the experimental parts.

A. Comparison of Power Loss and Efficiency

The main part of converters losses can be classified into conduction loss and switching loss. The switching loss has to be analyzed in the diode and the power switch. However, flowing current in the components causes noticeable conduction loss in most of them. Thus, the conduction losses in the power switch, diode, inductors and capacitors have been investigated for the converters.

1) Power Switch Losses: the conduction loss of a switch has a general equation similar to (22). At the first step, I_{rms} for the switch should be obtained as follows.

$$I_{Srms} = \sqrt{\frac{\int_0^{DT} \left(i_{L1} + i_{L2}\right)^2 dt}{T}} = \sqrt{D}\left(i_{L1} + i_{L2}\right) \tag{21}$$

where I_{Srms} is the switch current of the proposed converter. The conduction loss of the power switch is equal to:

$$P_{SC} = I_{Srms}^2 . r_{DS} \tag{22}$$

By the use of equations (21) and (22), the final equation for the switch conduction loss of the proposed converter can be written as follows.

$$P_{SC} = \frac{r_{DS} . D}{\left(1 - D\right)^2 R_o} P_o \tag{23}$$

where r_{DS} is the resistance of the switch, which is equal to 0.04Ω. Furthermore, P_o is the output power of the converter. In addition, the boost and Cuk converters are analyzed and they have similar switch conduction loss equations.

The turn on and turn off losses of the switches of the proposed converter and the boost converter are equal to:

$$P_{SS} = \frac{Df}{2\left(1 - D\right)}\left(t_r + t_f\right) P_o \tag{24}$$

where P_{SS}, t_r and t_f are the switching loss, turn-on delay time and turn-off delay time of the power switch, respectively. The loss equation in the Cuk converter is as follows.

$$P_{SSC} = \frac{f}{2\left(1 - D\right)}\left(t_r + t_f\right) P_o \tag{25}$$

2) Diode Power Losses: the diode power loss can be classified into conduction loss, forward voltage drop loss and switching loss. Equation (26) illustrates the forward voltage drop loss of the diode (P_{Df}) for the proposed converter and the boost converter.

$$P_{Df} = \frac{V_f}{V_S}\sqrt{1 - D} . P_o \tag{26}$$

where V_F and V_S are the forward voltage drop of the diode and the input voltage, respectively. The loss in the Cuk converter is:

$$P_{DfC} = \frac{V_f}{DV_S}\sqrt{1 - D} . P_o \tag{27}$$

The second calculated loss of the diode is the conduction power loss (P_{DC}). The diode conduction loss for the converters is similar. It can be written as:

$$P_{DC} = \frac{r_D}{R_o\left(1 - D\right)} P_o \tag{28}$$

where r_D is the resistance of the diode. The last equation of the diode losses is the switching loss (P_{DS}), which can be derived as below for the proposed converter and the boost converter.

$$P_{DS} = \frac{t_{rr} f}{2} P_o \tag{29}$$

where t_{rr} is reverse recovery time of the diode. The switching loss of the diode in the Cuk converter is:

$$P_{DSC} = \frac{t_{rr} f}{2D} P_o \tag{30}$$

3) Inductors Conduction Loss: the conduction loss of the inductors (P_L) can be calculated by the following equations for the proposed converter and the Cuk converter.

$$P_L = I_{L1rms}^2 . r_{L1} + I_{L2rms}^2 . r_{L2} \tag{31}$$

$$P_L = \left(\frac{r_{L1} . D^2}{\left(1 - D\right)^2 R_o} + \frac{r_{L2}}{R_o}\right) P_o \tag{32}$$

where r_{L1} and r_{L2} are the inductors resistances. The loss equation for the boost converter is:

$$P_{LB} = \left(\frac{r_L}{(1-D)^2 R_o} \right) P_o \quad (33)$$

According to the design strategy (equal ripple for the inductors of both converters), the inductors sizes and their resistances have the same values ($r_{L1} = r_{L2} = r_L$). For an equal output power, a ratio between the converters (the proposed converter and the boost converter) conduction losses can be written as:

$$P_{LB} = \frac{1}{2D^2 - 2D + 1} P_L \quad (34)$$

Equation (34) demonstrates the higher conduction loss of the boost inductor in comparison to the sum of the inductor losses in the proposed converter. This is due to the distributed current in the two inductors of the proposed converter that makes the ratio in equation (34).

4) Capacitors Conduction Loss: the proposed converter has two capacitors similar to the Cuk converter. The capacitors resistances cause conduction losses which are analyzed, and their equations are:

$$P_{cc1} = r_{C1} \left(\frac{\sqrt{D}(1-D) + D\sqrt{1-D}}{1-D} \right)^2 \frac{P_o}{R_o} \quad (35)$$

where P_{CC1} and r_{C1} are the conduction loss of $C1$ and the capacitor resistance, respectively. The second capacitor loss is calculated as follows.

$$P_{cc2} = r_{C2} \left(\frac{\left(\sqrt{D}(1-D) + D\sqrt{1-D}\right)(1-D)}{2L_2 f} \right)^2 P_o R_o \quad (36)$$

The capacitors conduction loss of the Cuk converter are the same as those of the proposed converter. The boost converter has one capacitor, and its conduction loss is:

$$P_{ccb} = r_C \left(\frac{\sqrt{D}(1-D) + D\sqrt{1-D}}{1-D} \right)^2 \frac{P_o}{R_o} \quad (37)$$

5) Total Power Losses of the Converters: the losses can be compared one by one. However, it is preferable to compare the total loss of the converters. The inductors conduction losses of the converters have been compared (equations (32) and (33)) in Fig. 3 as an example. According to equation (34) and the equal voltage gain of the proposed converter when compared with the boost converter (equation (5)), the proposed converter has lower inductors conduction loss. The proposed converter and the Cuk converter have similar inductors conduction loss equations. The difference occurs due to their duty cycle at equal voltage gains. The Cuk converter has a higher duty cycle at the same voltage gain,

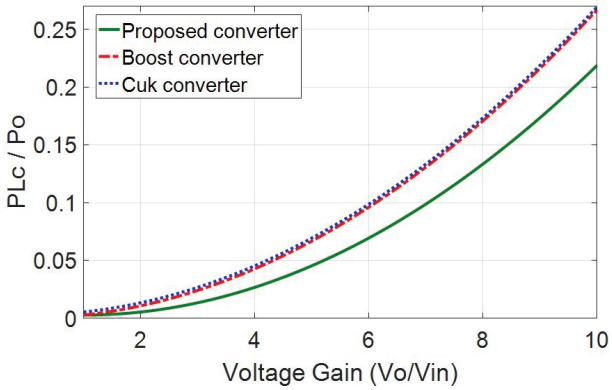


Fig. 3. Conduction loss of the inductors of the proposed converter, boost converter and Cuk converter.

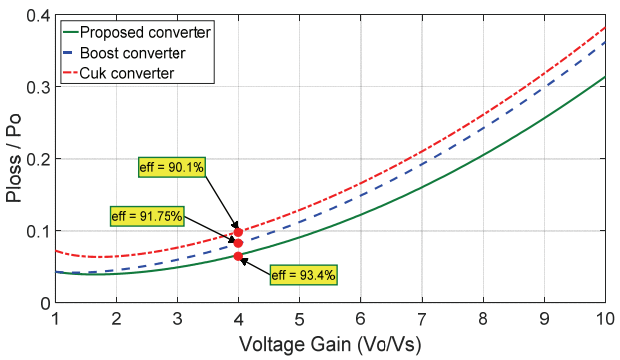


Fig. 4. Total power loss of the proposed converter, boost converter and Cuk converter per different voltage gains.

which is the reason for the higher loss in the Cuk converter (equation (32)).

Based on the power losses analysis of the converters (equations (21) to (37)), their total power losses are calculated. To compare them in a correct way, it is assumed that the properties of the converters components are the same. In the power losses calculations, r_{L1}, r_{L2}, r_D, r_{C1}, r_{C2}, r_{DS}, $t_r + t_f$ and t_{rr} are 0.2Ω, 0.2Ω, 0.04Ω, 0.01Ω, 0.01Ω, 0.04Ω, $108ns$ and $100ns$, respectively. Fig. 4 depicts the calculated total power loss for the converters. The values are in different voltage gains, which are united by dividing the total power loss into the output power.

The results demonstrate the lower power losses in the proposed converter in comparison to the boost and Cuk converters. In a voltage gain equal to 4, the value of the efficiency is shown on the curves. In the analysis, the core loss is not calculated, which needs to have core properties. The Cuk converter and the proposed converter contain two inductors, which means that their core losses are approximately the same. Thus, the analysis can be used to demonstrate the lower total power loss of the proposed converter in comparison with the Cuk converter. The boost converter has one inductor, which may cause a difference between the analysis and reality. Hence, an analytical part for

the core losses is prepared to complete the study.

6) Core Loss of Inductors: the ESR effect of the two inductors in the proposed converter is less than that of the one inductor in the boost converter. This is due to the distributed current in the inductors, which makes the ratio in equation (34). The relation between the inductors current of the proposed converter (i_{L1}, i_{L2}) and the boost converter i_L can be concluded from the experimental results (see Fig. 9 and Fig. 10),

where $i_{L1} + i_{L2} \simeq i_L$.

Furthermore, the distributed current has positive effects on the core losses of the inductors. The inductor core loss equation with a high frequency switching is as follows [19].

$$P_C = V_e \Delta P_C \tag{38}$$

$$\Delta P_C = a B_{pk}^{b} f^{c} \tag{39}$$

where P_C, V_e and ΔP_C are the core loss, core effective volume and core loss density, respectively. a, b and c (Steinmetz parameters [19]) depend on the core material properties. B_{pk}^{b} is defined as the flux density ripple (ΔB). The magnetic field intensities for a triangular current are:

$$H_{max} = \left[\frac{N}{L_e} \left(I_{dc} + \frac{\Delta I_L}{2} \right) \right]$$

$$H_{max} = \left[\frac{N}{L_e} \left(I_{dc} - \frac{\Delta I_L}{2} \right) \right] \tag{40}$$

where N and L_e are number of coil turns and the path length, respectively. The inductors of the proposed converter, the Cuk converter and the boost converter are designed for equal current ripples. Therefore:

$$\Delta H_B = \Delta H_P \tag{41}$$

where ΔH_B and ΔH_P are variations of the magnetic field intensities in the boost inductor and the proposed converter inductors. During normal operations, the flux ripple of both of the converters inductors can be assumed to be equal (Fig. 5). Fig. 5 shows a sample ferrite core curve, where the inductors operate in an area of the curve with similar slopes (so, $\Delta B_B = \Delta B_P$).

Equation (40) contains a dc bias value for the magnetic field (H_{dc}) that causes dc pre-magnetization [19]. The magnetic field dc bias has a relation with the Steinmetz parameters as shown in Fig. 6. The relation of the inductors current ($i_{L1} + i_{L2} \simeq i_L$) results in a higher H_{dc} in the boost inductor. This means $H_{dcB} > H_{dcP}$, which intensively increases Steinmetz parameters. It should be noticed that H_{dcB} and H_{dcP} are the dc bias magnetic field of the boost converter and the proposed converter, respectively. Using equation (40) and Fig. 6, it can be concluded that $a_B > a_P$ and $P_{cB} > P_{cP}$, where a_B, a_P, P_{cB} and P_{cP} are the Steinmetz parameter of the boost, Steinmetz parameter of the proposed converter, core loss of the boost converter's inductor and core loss of the proposed converter's inductors, respectively. However, the proposed converter has two inductors. The single inductor of the boost has more core loss due to its bigger Steinmetz parameters (in some operation points $a_B \geq 2a_P$, which means the core losses of the two inductors in the proposed converter are equal to or smaller than the core loss of the single inductor in the boost converter). As the main consequence of the experimental results and the theoretical descriptions, the distributed current in the proposed converter's inductors causes fewer losses in comparison with the single inductor of the boost converter. Thus, the below relation is acceptable.

$$P_{LB} + P_{cB} > P_{LP} + P_{cP} \tag{42}$$

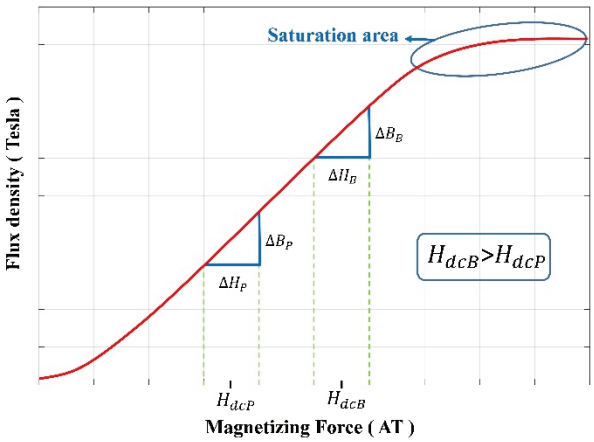


Fig. 5. Magnetizing curves of a sample ferrite core.

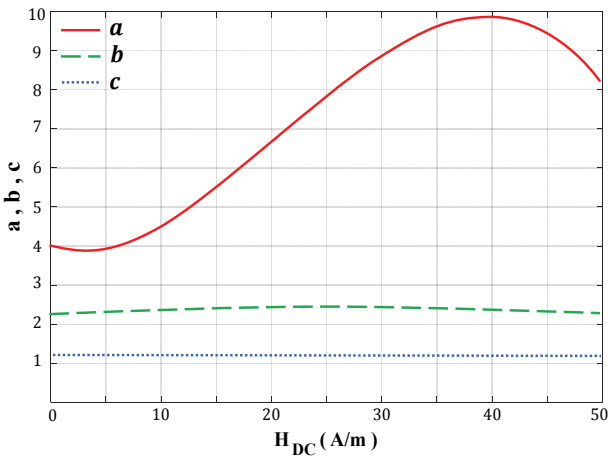


Fig. 6. Steinmetz parameters as a function of pre-magnetization H_{dc} for ferrite cores [19].

IV. Experimental Results

The results of experiments for the proposed converter and a boost converter complete the study. The important elements of the proposed converter are designed by its equations. The inductors are set for CCM conditions in the worst case based on (17) and (18). The variation of the inductors current is chosen as 0.2 per $D = 0.5$. The main parameters affecting the voltage drop in the converter are the inductors resistances, switch on resistance (R_{on}), and diodes forward voltage (V_{DF}). Details of the designed components for the prototype are listed in Table II.

To build a prototype of the proposed converter, suitable components should be chosen. The essential parameters of the components are similar to the values in Table II. For the inductors, ferrite cores of type ETD39 are used. The inductors are built with four strings of twisted wires that reduce the inductors resistance and skin effect. The capacitor (C_1) is $100\mu F$ electrolytic type. To decrease the ESR effect, each of the capacitors is paralleled with a $1\mu F$ capacitor of the polyester type. The converter needs an N-type MOSFET with a low resistance and it should not be damaged by a 200V reverse voltage. Thus, an IRFP260N with $r_{DS} = 0.04\Omega$ and $V_{DSS} = 200$V is a good choice. The diode has to be switched very quickly. Therefore, MBR20150CT (Schottky) is selected as the diode with a maximum $V_{DF} = 0.7$V. The isolating and gate driving are done by 6N137 and IR2104. Fig. 7 depicts the prepared prototype of the proposed converter, boost converter and multiplier module for both converters. The proposed converter is designed for an 80W output power. In addition, its transferring power increases to 150W with a multiplier. The proposed converter and its combination with a multiplier operate with an efficiency more than 90% to transfer the rated powers (80W and 150W) in the experiments. As mentioned in the previous section, because of the similarity between the voltage gains of the boost converter and the proposed converter, they have been compared during experiments. The employed components (MOSFET, diode, output capacitor, multiplier capacitors and inductor core) in the boost prototype are the same as those of the proposed converter. The inductor size in the Cuk based converter and the boost converter are assumed to be equal. According to the equations in Table 1, the boost converter needs a smaller inductor. In this study, the basis of the prototypes design is the current ripple and the inductors are chosen for low current ripples. The current ripples of the proposed converter's inductors have the same values (equations (13) and (14)). The current ripple in the boost converter is similar to that in the equations. Therefore, all of them have the same values. A low current ripple adds some advantages to the circuits. These advantages include operation in the current continuous mode under high load conditions, reduction of the core loss, and decreasing possibility of saturation and using smaller cores. If the inductors sizes are chosen by the minimum inductor equations, the converters current ripple increases, which may result in operation in the discontinuous current mode (the experiments consist of operations with various loads).

TABLE II
Specifications of the Prototype of the Proposed Converter

Parameter	Value
Input voltage	20 V
Inductors (L_1 and L_2)	1mH
Inductors resistances (r_1 and r_2)	0.2 Ω
Capacitor (C_1)	$100\mu F$
Output capacitor (C_2)	$10\mu F$
Switching frequency	50kHz
Switch on resistance (R_{on})	0.04 Ω
Diode forward voltage (V_{DF})	0.7 v
Resistive load (R)	75 Ω

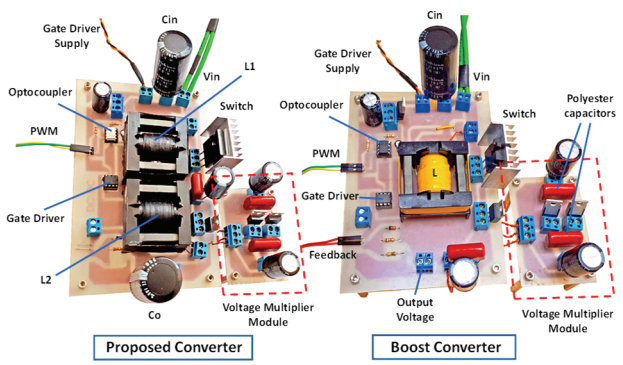


Fig. 7. Prototype of the proposed converter, boost converter and the voltage multiplier circuit.

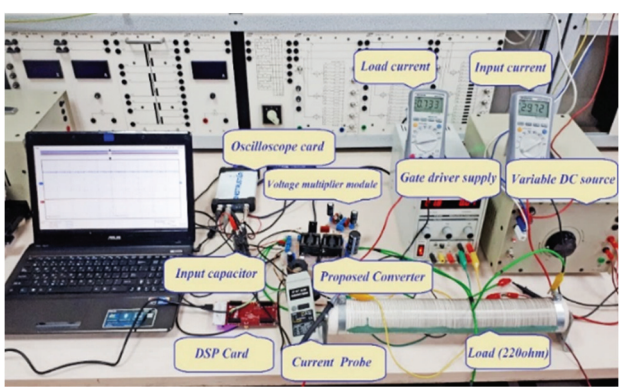


Fig. 8. Experimental setup composed of: a prototype of the proposed converter, load, current probe: OWON CP-05, DSP board: LAUNCHERXL-F28379D, and USB oscilloscope: INSTRUSTAR ISDS2062B pc based.

The experimental set up in Lab is shown in Fig. 8. The obtained experimental results are arranged according to important theoretical equations for the open loop and closed loop conditions.

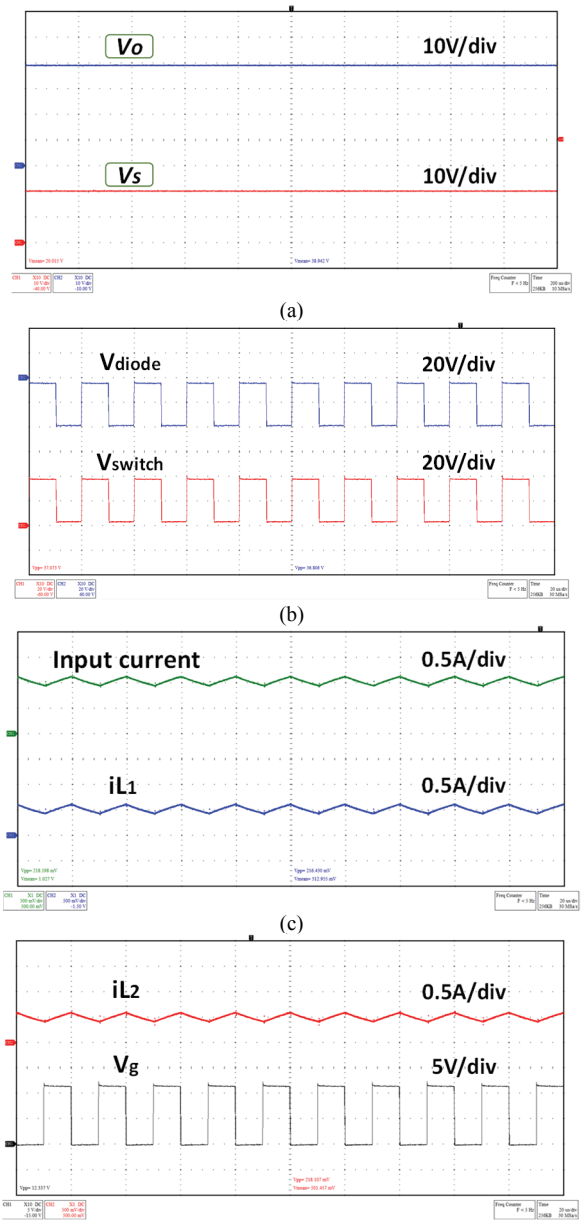


Fig. 9. Experimental results of the proposed converter for a duty cycle equal to 50%. V_s = 20V and V_o = 38.94V. (b) $V_{pp\text{-}Switch}$ = 37.073V and $V_{pp\text{-}diode}$ = 36.8V. (c) ΔI_{in} = 0.218 A, Δi_{L1} = 0.216 A, $I_{in(ave)}$ = 1.027 A and $i_{L1(ave)}$ = 0.513 A. (d) Δi_{L2} = 0.218 A and $i_{L2(ave)}$ = 0.501 A.

A. Open Loop Results

At a first step, experiments are conducted without a controller. The experimental results for the proposed converter are visible in Fig. 9, which contains results for switching with a 50% duty cycle.

Fig. 9(a) shows the input and output voltages. Based on the voltage conversion ratio equation, the output voltage per D = 0.5 for the converter has to be 40V. It is obtained as 38.94V by the experimental setup, which means there is a good agreement between the theoretical equation and the experimental

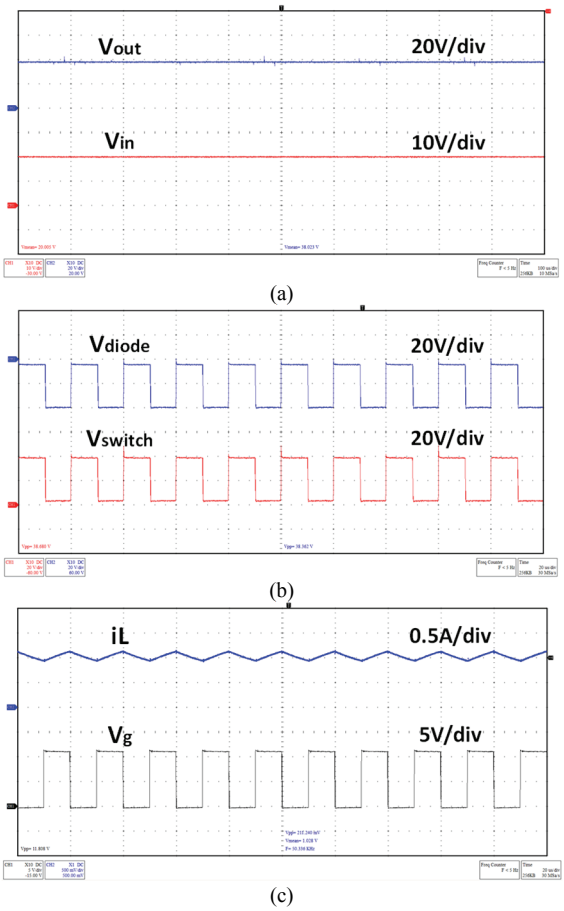


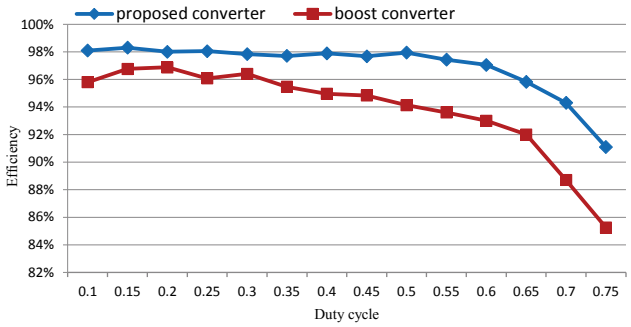
Fig. 10. Experimental results of a boost converter for a duty cycle equal to 50%. (a) *Vin* = 20V and *Vout* = 38V. (b) *Vpp-Switch* = 38.68V and *Vpp-diode* = 38.36V. (c) Δi_L = 0.211 A and $i_{L(ave)}$ = 1.028 A.

results. The difference can be neglected and it is due to the voltage drop on the components.

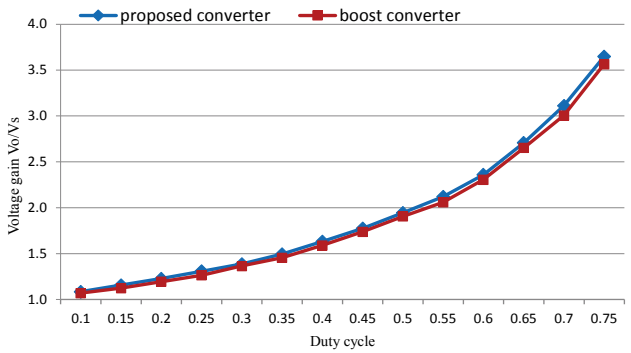
Based on equations (13) and (14), the variation of the current in the designed prototype is 0.2A, and in Fig. 9 the current ripples of I_{L1} and I_{L2} are equal to 0.216A and 0.218A for L_1 and L_2, respectively. This shows good agreement between the experimental setup and the analysis. According to the current variation equations, they increase in higher duty cycles.

Equations (6) and (7) introduce the maximum voltage stress on the diode and power switch as $\pm V_o$. Thus, when D is equal to 0.5, the voltage stress on the diode and MOSFET should be 40V as measured in Fig. 9(b).

It seems the converters operate in the same way. However, the proposed converter has more efficiency. According to equations (23) to (30), the power switch losses and diode losses are similar in the boost converter and the proposed converter. Thus, the difference occurs due to the conduction power loss and core loss of the inductors (the difference of the inductors conduction loss and their core loss have been fully discussed in the analytical part). In Fig. 11, the proposed converter and boost converter voltage gain and their efficiency



(a)



(b)

Fig. 11. Comparison of the boost and the proposed converter. (a) Efficiency of the converters per different duty cycles. (b) Voltage gain of the converters per different duty cycles.

TABLE III
EXPERIMENTAL RESULTS FOR CONTROLLED CONVERTERS
OUTPUT VOLTAGE = 60V, R_O = 75Ω

Parameter	Proposed converter	Boost converter
Maximum voltage stress on diode	55.366V	55.95V
Maximum voltage stress on switch	57.75V	58.39V
Inductors current ripple	Δi_{L1} = 0.269 A Δi_{L2} = 0.278 A	Δi_L = 0.279 A
Average current of inductors	i_{L1ave} = 1.750 A i_{L2ave} = 0.757 A	i_{Lave} = 2.624 A

per different duty cycles are compared (the efficiency difference is from 2% to 6%).

B. Closed Loop Results

A PI controller is used for the converters to regulate their output voltage during varying loads. The controllers set the outputs to 60V and loads are changed from 75Ω to 225Ω. The registered waveforms are similar to the previous ones, and they have been summarized in Table III.

According to the previous discussions, there are similarities between the converters. Thus, the efficiency curves for varying loads in Fig. 12 indicate the differences between the converters. The efficiency difference between the converters is from 2% to 6%. By increasing the load, the proposed converter operates with a higher efficiency and the difference goes up to 10%. It seems the inductors losses difference is

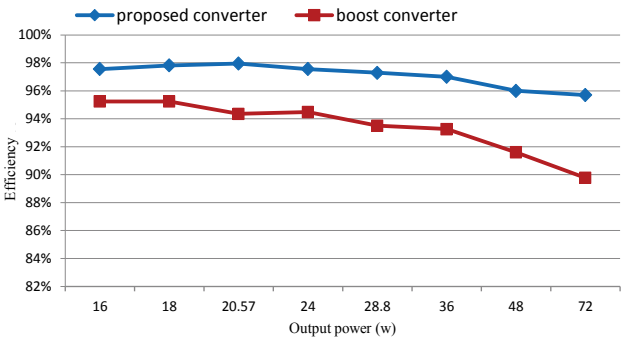


Fig. 12. Efficiency of the proposed converter and boost converter per different loads.

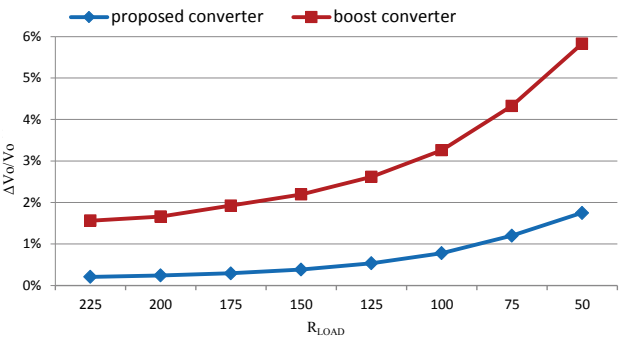


Fig. 13. Voltage ripple of the proposed converter and boost converter per different loads (extracted from the experimental results).

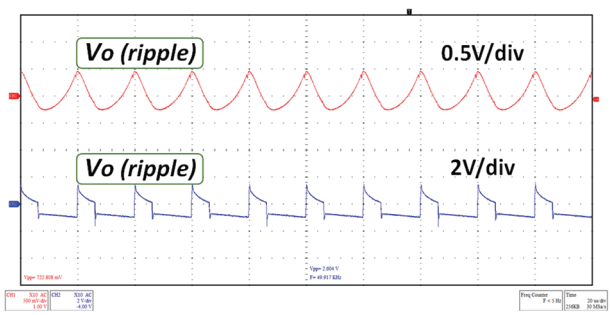


Fig. 14. Voltage ripple of the converters (red curve: the proposed converter; blue curve: the boost converter).

more visible at higher loads. The other criterion for comparison is the output voltage ripple, which is shown in Fig. 13, for the converters.

The equations in Table I show that the voltage ripple of the boost converter depends on the inverse of the load resistance and duty cycle (D). By increasing the load (reduction of the load resistance), the controller increases the duty cycle. Both of the changes have negative impacts on the voltage ripple. The proposed converter operates with different conditions. Its voltage gain does not depend on load variations (see Table I) and it has relationship with $D(1-D)$. In all of the conditions $D(1-D) < D$. Thus, the duty cycle increasing has less negative effects on the voltage ripple in the proposed converter. The described equations and their relations with

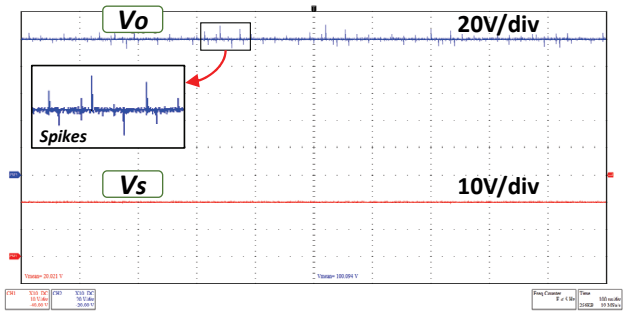


Fig. 15. Spikes in the output voltage of the boost-multiplier converter.

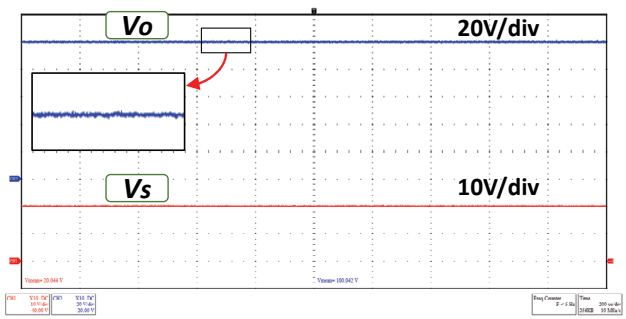


Fig. 16. High quality output voltage of the proposed-multiplier converter without spikes.

load variation are the main reasons for the difference between the converters voltage ripples (Fig. 13 clearly shows the difference and the load variation effect on the voltage ripple). As a result, the output voltage of the proposed converter has softer slope changes as shown in Fig. 14.

V. Combination of the Converters with a 2X Multiplier

In most applications, DC-DC converters should be combined with multipliers or they have to be used in multilevel converter structures. The basis of such a circuit is important and the lack of quality in the main converter influences the total output characteristics. Thus, the proposed converter is combined with a multiplier for studying its operation quality in this situation.

For the 2x multiplier, prototypes are prepared and connected to the proposed converter and boost converter (Fig. 7). However, most of the parameters, such as voltage gain, the current ripple, and voltage stress on the switch and diode, are similar in the converters. Therefore, the quality of their outputs is different. There are many spikes in the boost-multiplier converter as shown in Fig. 15.

The converters also have essential differences in their efficiency and output voltage ripple. The curves in Fig. 17 and Fig. 18 illustrate the efficiency of the combined converters in open loop and closed loop conditions.

The boost weakness in converting power with a lower efficiency is transferred to the boost-multiplier converter. By

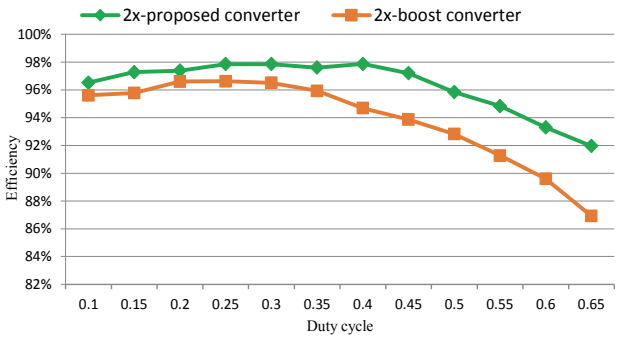


Fig. 17. Efficiency of the combined converters based on open loop experimental results (per different duty cycles and for R_o=150Ω).

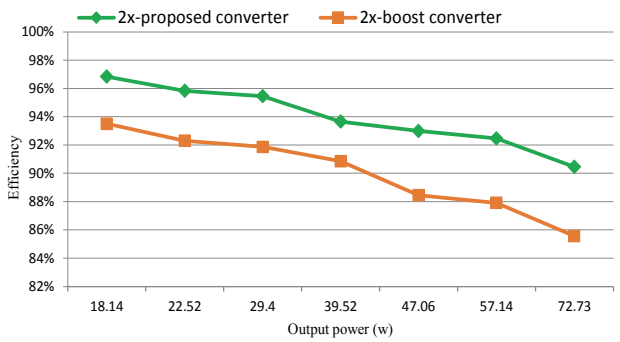


Fig. 18. Efficiency of the combined converters based on closed loop experimental results (output voltage = 100V; gain voltage = 5), 150Ω < R_o < 550Ω).

increasing the output power (Fig. 18) or duty cycle (Fig. 17), the difference becomes more obvious.

The rated power of the proposed converter depends on the input voltage. For example, it transfers 200W with an efficiency of more than 90% for an input voltage equal to 40V. The power losses in the converters reduce their efficiency. However, improving efficiency is important for most applications. Selection of the proposed converter components and its design achieve a high efficiency in duty cycles less than 0.8. According to the results, the efficiency of the proposed converter is more than 96% when D≤0.65 and it is more than 90% when 0.65≤D≤0.75. Furthermore, the converter with a 2x multiplier has an efficiency of more than 92% when D≤0.65. The consequence of adding the multiplier is a doubling of the voltage conversion ratio with little reduction in the efficiency. The combined converter increases the voltage conversion ratio until it reaches five times with high efficiency.

VI. Conclusion

A DC-DC converter is proposed where the boosting mode can be improved. The converter is analyzed, discussed and compared with other converters. Furthermore, a converter with a multiplier circuit is studied as a high voltage conversion

ratio converter. The theoretical analysis includes the main parameters such as the VCR, variation of the current, inductors design, voltage stress and efficiency. The design of the proposed converter is done based on theoretical equations. The obtained experimental results are in accordance with the analysis. The proposed converter operates with an efficiency of more than 96% and 90% when $D \leq 0.65$ and $0.65 \leq D \leq 0.75$, respectively. The high efficiency of the converter makes it as a good choice for use with a multiplier circuit. Experimental results verify the idea and the fact that the converter with a 2x multiplier operates with a high efficiency and doubles the voltage conversion ratio. Thus, it can be extended as a high efficiency and high-quality multilevel DC-DC converter.

In comparison to Cuk converter, the proposed converter has a lower voltage ripple, higher efficiency and higher voltage conversion ratio. In addition, it operates with better qualities in comparison to boost converter (lower voltage ripple, no spikes in the output voltage and higher efficiency).

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