JPE 19-4-20

https://doi.org/10.6113/JPE.2019.19.4.1054
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

Influence of Device Parameters Spread on Current Distribution of Paralleled Silicon Carbide MOSFETs

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Abstract

This paper systematically investigates the influence of device parameters spread on the current distribution of paralleled silicon carbide (SiC) MOSFETs. First, a variation coefficient is introduced and used as the evaluating norm for the parameters spread. Then a sample of 30 SiC MOSFET devices from the same batch of a well-known company is selected and tested under the same conditions as those on datasheet. It is found that there is big difference among parameters spread. Furthermore, comprehensive theoretical and simulation analyses are carried out to study the sensitivity of the current imbalance to variations of the device parameters. Based on the concept of the control variable method, the influence of each device parameter on the steady-state and transient current distributions of paralleled SiC MOSFETs are verified separately by experiments. Finally, some screening suggestions of devices or chips before parallel-connection are provided in terms of different applications and different driver configurations.

Key words: Current distribution, Devices parameters, Parallel-connected devices, Screening, Silicon carbide (SiC) MOSFET

I. INTRODUCTION

Silicon carbide (SiC) MOSFETs have excellent blocking voltage capability, high switching frequency, low losses, and high thermal conductivity [1], [2]. Currently, with limitations of the current rating of a single chip or device [3], power modules with paralleled multi-chips or the parallel connection of several discrete SiC MOSFET devices in a TO-package are commonly being developed to achieve high current capability [4]. However, there is a current imbalance among paralleled units (chips or devices) if their parameters or the parasitic parameters of their corresponding circuits are not perfectly matched. This may result in a difference in the power losses by the individual units in the form of conduction and switching losses, which can result in further thermal dissymmetry. In addition, a difference of the di/dt among all of the paralleled switches can lead to mismatches of the current overshoot during turn-on and voltage overshoot during turn-off. These overshoots may push devices out of their safe operating area (SOA), or even cause device destruction. Current de-rating, which is a common approach adopted to safeguard devices from destruction due to current imbalance, has the disadvantage of inhibiting the full utilization of the overall current capacity of paralleled chips or devices.

Recently, some researchers have studied current imbalance in terms of two main aspects, circuit parasitic parameters and devices parameters. With regards to circuit parasitic parameters mismatches, the effects of parasitic inductance mismatches on paralleled modules was studied in [5]. Meanwhile, the authors of [6] conducted similar studies on discrete devices and the authors of [7] extended this study to the multi-chips in power modules. An optimized driver circuit [5], auxiliary source connections [7] and a symmetrical power module structure [8] were proposed to improve transient current sharing in paralleled units. Even though it is possible to realize a sufficiently symmetrical circuit layout with almost perfectly matched parameters, a mismatch in the inherent device parameters can still lead to an uneven current distribution. Therefore, uniformity of the device parameters is a required precondition for adopting circuit layout symmetry as a means of realizing equal current sharing.

Manuscript received Jun. 18, 2018; accepted Apr. 17, 2019
Recommended for publication by Associate Editor Sang-Won Yoon.
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Although the fluctuations of device parameters are often limited by strict fabrication processes for commercial semiconductors, there is still a certain degree of inconsistency in device parameters. This is especially true for emerging SiC devices, where the spread of the device parameters is distinct. The main cause of this inconsistency may be the relatively immature manufacturing process control which has been reported in [9]-[11]. In addition, the higher the number of paralleled devices, with the aim of achieving a higher current capability, the higher the risks of SiC MOSFETs bearing static and dynamic over-currents. The large spread of the pinch-off voltage and reverse breakdown gate voltage of SiC JFET devices have been reported in [4], [12], [13]. In these studies, an individual gate driver circuit is used to solve this problem. Similar researches for SiC MOSFET devices have also been mentioned in a number of published studies [14]-[18]. The spread of on-resistance and threshold voltage, and their influences on the current distribution among paralleled SiC MOSFET devices, have been discussed. A de-rating calculation method was presented in [18] to avoid thermal overstress for paralleled SiC MOSFET devices. However, a systematic and comprehensive analysis of all the device parameters has not been reported yet. This is especially true for parasitic capacitance and trans-conductance. Moreover, the influence of the spread of device parameters on current distribution under different gate driver configurations and temperatures also needs to be discussed. These analyses are usually very important for gate driver design and form the basis for device screening methods.

This paper takes full consideration of device parameters spread and their influence on current distribution. In section II, 30 SiC MOSFET devices from the same batch are tested under the same condition used in the datasheet. The spread of the device parameters is presented using the coefficient of variation. The cause of the differences among the spreads of three parasitic capacitances are discussed. In section III, the influences of on-resistance, threshold voltage and trans-conductance on steady-state and transient current distributions are theoretically studied. The sensitivity of capacitance variations to current imbalance is quantitatively calculated by simulation software. In section IV, several pairs of different devices are selected from the samples for switching operation experiments in parallel connection. The obtained experimental results validate the theoretical and simulation analyses of the influence of all the parameters. The junction temperature variation at the maximum difference of the main device parameters is discussed in section V. Several valuable screening guidelines are provided in section VI. Some conclusions are given in section VII.

II. Device Parameters Spread

Generally, the current distribution of paralleled devices is a result of multiple factors including the device and circuit parameters. The device parameters include the on-resistance, threshold voltage, trans-conductance, internal gate resistance and parasitic capacitances. The spreads of the different device parameters are not the same. Thus, a norm needs to be defined to quantitatively assess the spread of the device parameters.

In experimental statistics, there are several norms, such as the range, variance, standard deviation and coefficient of variation, that describe the spread of data. Since the range only considers the two extrema, and cannot reflect the concentration and spread of a group of data, it is not widely used. The unit of variance is the square of the original data's unit, which often makes its real meaning difficult to understand [19]. Although the unit of the standard deviation is the same as that of the original data, it is not suitable for comparing the spread of different parameters in a sample. The coefficient of the variation δ_N is the ratio of the standard deviations σ_N to the mean μ_N. It is unit-less and usually expressed as a percentage [20]. It is a more suitable option for the description of the spread of parameters. Therefore, this paper uses δ_N to evaluate the spread of the device parameters.

$$\delta_N = \frac{\sigma_N}{\mu_N} \times 100\% \tag{1}$$

where N is the sample space, which is set to N=30 in this paper.

A. On-Resistance

In this paper, 30 SiC MOSFETs are tested at an ambient temperature of 25℃ and a gate voltage of +20V. The on-resistance spread of different devices with different drain currents is shown in Fig. 1. The devices with the largest and smallest on-resistances in the entire range of the drain current are No.6 and No.19, respectively. Moreover, in the 20A range of the drain currents, the δ_{30} of the on-resistance varies from 4% to 5.37% due to inconsistencies of the output characteristics of the different devices. The on-resistance of a power MOSFET is mainly composed of the channel resistance and the drift region resistance. These are affected by the device structure and fabrication technology such as the channel length, the cell width, the drift region thickness, etc. [21]. Therefore, it is difficult to keep them uniform even for the same batch of products from the same manufacturer.

B. Internal Gate Resistance

The internal gate resistance R_{G_int}, mainly depends on the film thickness and resistivity of the gate electrode material [22]. The spread of R_{G_int}, for the 30 SiC MOSFET devices selected in this paper is shown in Fig. 2. Although the datasheet gives a typical value of 4.6Ω for R_{G_int}, the actual value varies from device to device. Among these devices, the largest and smallest R_{G_int}, are 4.48Ω and 3.04Ω, which correspond to device No.21 and No.7, respectively. These are lower than the datasheet specifications. The mean of R_{G_int} is 3.79Ω, its standard deviation is 0.463Ω, and the coefficient of variation is 12.2%, which indicate that R_{G_int} has a large

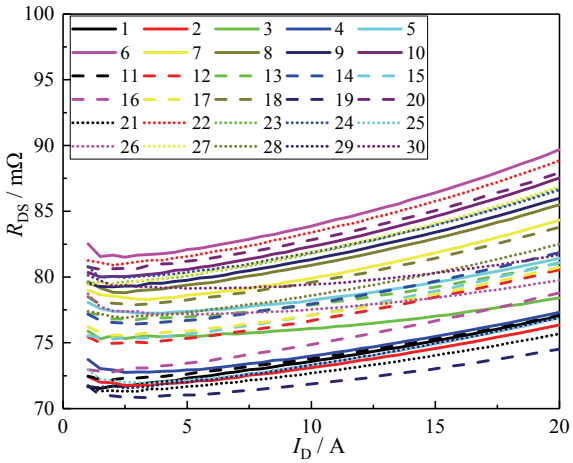


Fig. 1. R_{DS}-I_D curve of SiC MOSFET devices.

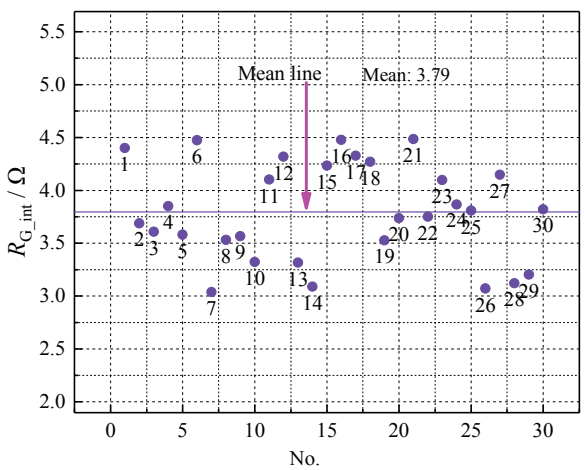
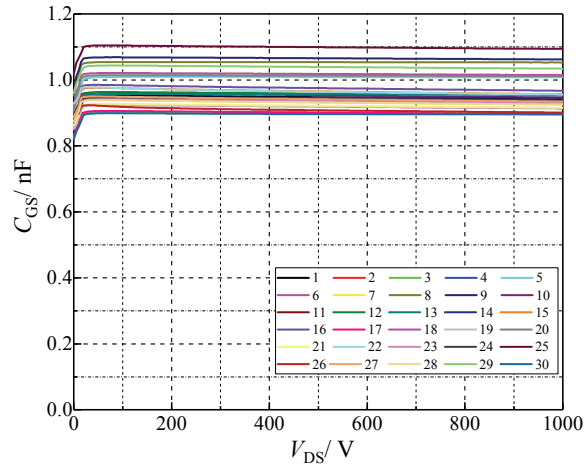


Fig. 2. Spread of internal gate resistance.

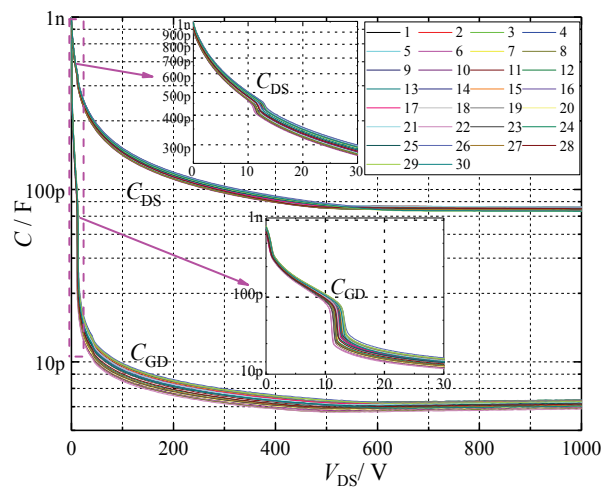
spread. This may be caused by the tolerance of the chip size and sheet thickness.

C. Parasitic Capacitances

MOSFET internal parasitic capacitances include gate-source capacitance C_{GS}, gate-drain capacitance (or reverse transfer capacitance) C_{GD} and drain-source capacitance C_{DS}. Generally, C_{GS} is assumed to be constant with the voltage [23]. As shown in Fig. 3(a), although C_{GS} has little variation with V_{DS} below the value of 20V, it is not more than 8% of the steady-state value. In addition, whether in turn-on or turn-off transient stage, the V_{DS} value is relatively high and much higher than the 20V during the current rising or falling stage. In addition, the variation of C_{GS} with V_{DS} does not exceed 1%. As shown in Fig. 4, the spread of C_{GS}, which may be caused by the tolerance control of the oxide thickness and cell width also remains constant under the varying of V_{DS}. However, C_{GD} and C_{DS} both dramatically decrease with an increase of V_{DS} as shown in Fig. 3(b), since both are constituted by the depletion layer capacitance, which depends on the width of the depletion layer and the junction area of the drain region of the body [24]. In addition to the inverse



(a)



(b)

Fig. 3. C-V curves of a SiC MOSFET. (a) C_{GS} -V_{DS}; (b) C_{DS}-V_{DS} and C_{GD} -V_{DS}.

variation with V_{DS}, there is a large change of C_{GD} around the Miller platform voltage 12.5V. This is because the doping concentrations in the JFET region and the drift region are different, which results in the two depletion layers having different capacitances [23], [25]. Thus, it is significantly different from the rate of decrease at less and more than 12.5V. This abrupt change of C_{GD} around 12.5V results in large spread as shown in Fig. 4.

D. Transfer Characteristics

The transfer characteristics of a MOSFET are crucial for the transient current distribution in parallel-connection applications [26]. In this paper, the transfer curves of 30 SiC MOSFET devices are measured under the same conditions of V_{DS} = 20V and T_C = 25℃. It can be seen from Fig. 5 [27] that there is still a large spread of the transfer curves even though the devices are drawn from the same batch.

During the current rising or falling stage, the MOSFETs are operating in the saturation region and the drain current is expressed by (2) [28]. The transfer characteristics can also be

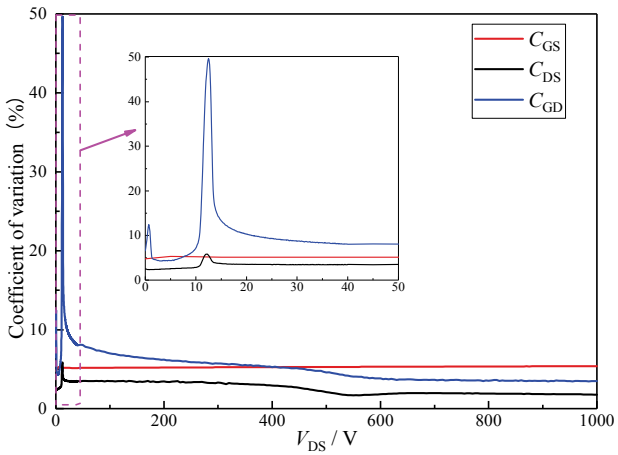


Fig. 4. Coefficient of the variation of parasitic capacitances.

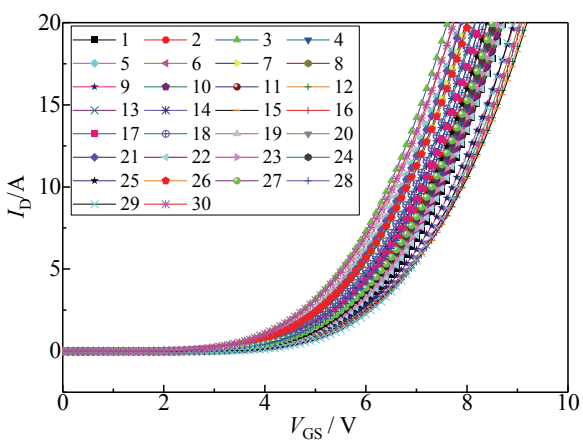


Fig. 5. Transfer curves of SiC MOSFET devices [27].

regarded as a function of the threshold voltage V_{th} and the trans-conductance g_{fs}.

$$i_D = g_{fs}\left(V_{GS} - V_{th}\right) \tag{2}$$

$$V_{th} = \frac{\sqrt{4\varepsilon_s kTN_A \ln\left(N_A/n_i\right)}}{C_{OX}} + \frac{2kT}{q}\ln\left(\frac{N_A}{n_i}\right) - \frac{Q_{OX}}{C_{OX}} \tag{3}$$

$$g_{fs} = \frac{\mu_{ni}C_{OX}Z}{L_{CH}}\left(V_{GS} - V_{th}\right) \tag{4}$$

where ε_s, k, q, T, N_A, n_i, μ_{ni}, C_{OX}, Z and L_{CH} are the material dielectric constant, Boltzmann constant, electronic charge amount, Kelvin temperature, acceptor impurity concentration, intrinsic carrier concentration, channel electron mobility, gate oxide capacitor, cell length perpendicular to the cross section and channel length, respectively. Q_{OX} is the total effective oxide charge, including the moving ionic charge, oxide trap charge, fixed oxide charge and interfacial charge.

Even though current SiC material technology has been greatly improved, it is still not as mature as silicon technology, especially in terms of controlling defects. Slight inconsistencies in these defects may bring about differences in the interface and oxide layer quality resulting in differences in Q_{OX} in the oxide layer. According to (3), the Q_{OX} differences can lead to

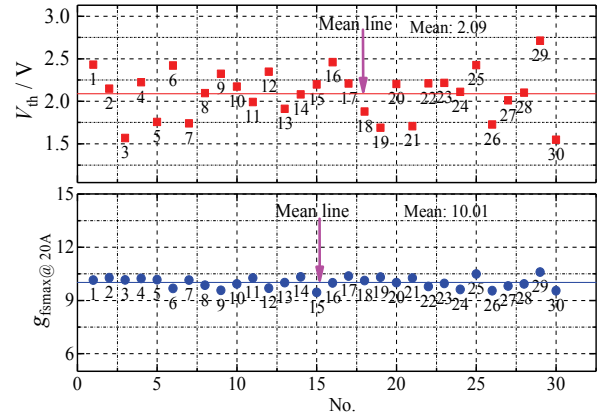


Fig. 6. Spread of threshold voltage and trans-conductance.

a large spread of V_{th}. In addition, the C_{OX} difference, caused by production processes such as inconsistent doping concentrations and thickness of the gate oxide layer, can also lead to inconsistencies in V_{th} [29]. On the other hand, as shown in (4), g_{fs} is also affected by the differences in C_{ox}, V_{GS}, V_{th} and other fabrication parameters [25]. The dispersion of V_{th} also affects that of g_{fs}. In addition, g_{fs} is variable with the current. Therefore, g_{fsmax} is taken as an example to present the spread of g_{fs}. As shown in Fig. 6, the spread of V_{th} is larger than that of g_{fsmax}. The variation coefficients δ_{30} of V_{th} and g_{fsmax} for the 30 devices selected in this paper are 13.8% and 3.73%, respectively.

In summary, for the 30 SiC MOSFETs selected in this paper, the δ_{30} of the threshold voltage and the gate resistance are larger with both exceeding 10%. In contrast, the δ_{30} of the on-resistance and trans-conductance are relatively small. Although the δ_{30} of C_{GD} changes sharply around 12.5V, it decreases with an increasing V_{DS}. For a V_{DS} above 400V, among the three capacitances, the δ_{30} of C_{GS} is the largest followed by that of C_{GD}, while C_{DS} has the smallest δ_{30}. In this case, the value of δ_{30} is less than 6% for all of them.

III. Influence of Device Parameters on Current Distribution

The above analysis shows that the device parameters still have a large spread, even though the tested products were drawn from the same batch and produced by the same manufacturer. Thus, this section focuses on the impact of device parameters mismatch on steady-state and transient current distributions.

A. On-Resistance

If it is assumed that the same gate driver circuit is used to supply the gate pulse for both of the paralleled devices, there is no disparity in the gate bias voltages. When all of the paralleled devices are fully on, a steady-state equivalent circuit of paralleled devices is shown in Fig. 7. Assume that the circuit layout is symmetrical, all of the stray resistances are considered to be equal and can be uniformly expressed as R_{stray}. The jth branch current I_{Dj} can be expressed by (5).

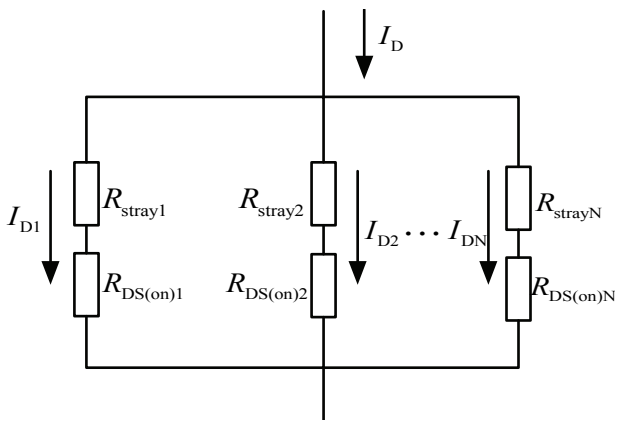


Fig. 7. Steady-state equivalent circuit of paralleling devices.

$$I_{Dj} = \frac{I_D}{\left(R_{DS(on)j} + R_{stray}\right)\sum_{i=1}^{N}\frac{1}{R_{DS(on)i} + R_{stray}}} \quad i, j=1,2,\cdots, N \quad (5)$$

where $R_{DS\,(on)i}$ and $R_{DS\,(on)j}$ are devices' on-resistances for the ith and j^{th} branches, respectively. I_D is the total current. N is the number of paralleled devices.

The steady-state current imbalance m can be defined as:

$$m=\frac{\left|I_{Dmax} - I_{Dmin}\right|}{I_D/N} \quad (6)$$

where I_{Dmax} and I_{Dmin} are the maximum and minimum of the steady state current of paralleled devices.

Substituting (5) into (6) yields the steady-state current imbalance of N devices in parallel as:

$$m=\frac{\left|R_{DS(on)max} - R_{DS(on)min}\right|}{\frac{1}{N}\sum_{j=1}^{N}\frac{\left(R_{DS(on)max}+R_{stray}\right)\left(R_{DS(on)min}+R_{stray}\right)}{R_{DS(on)j} + R_{strayj}}} \quad (7)$$

According to (7), it can be observed that the steady-state current distribution depends on the differences among the on-resistances provided that the layout is symmetrical. Although increasing the stray resistance of the paralleled branches can reduce the imbalance of the steady-state current, this is undesirable since it introduces extra power loss.

B. Internal Gate Resistance and Parasitic Capacitances

The rising or falling speed of the gate voltage mainly depends on the rate of charging or discharging of the device input capacitance. The turn-on and turn-off delay time is a function of the input parasitic capacitance and the gate resistance, which can be expressed as:

$$t_{don} = \left(R_{G\_int} + R_{G\_ext}\right)\left[C_{GS} + C_{GD}(V_{DS\_off})\right]\ln\frac{V_{GH}}{V_{GH} - V_{EE} - V_{th}} \quad (8)$$

$$t_{doff} = \left(R_{G\_int} + R_{G\_ext}\right)\left[C_{GS} + C_{GD}(V_{DS\_on})\right]\ln\frac{V_{GH} + V_{EE}}{V_{GP} + V_{EE}} \quad (9)$$

where R_{G_int} and R_{G_ext} are internal and external gate resistances, and V_{GH} and $-V_{EE}$ are the positive and negative bias gate voltages. V_{GP} is the gate Miller platform voltage.

During turn-on or turn-off transients, the current distribution depends on the difference among switching delay times and on the difference among current changing rates. Furthermore, the current rate is influenced by many factors including the common-source parasitic inductance, threshold voltage, trans-conductance, etc. It is difficult to deduce the exact analytical formula that relates the switching delay time to the current sharing. Therefore, in this paper, a simulation model consisting of a parallel combination of two devices is built in LTSPICE and used to study the current distribution by deliberately changing the C_{GS} and R_{G_ext} values.

In order to quantitatively describe the transient current distribution of paralleled devices, an evaluation indicator should be defined. Usually, the transient current imbalance is defined based on the difference in the peak values of the transient currents [30]-[32]. However, there is no peak value for the turn-off transient current if the difference in the turn-off delay time is not too large. Therefore, in this paper, the ratio α of the maximum absolute value of transient current difference to the base value is used to define transient current imbalance.

$$\alpha = \frac{\left|\Delta i_D\right|_{max}}{I_B} \times 100\% \quad (10)$$

In (10), $|\Delta i_D|_{max}$ represents the maximum absolute value of the transient current difference. This is the largest instantaneous current unbalance over the entire transient period. I_B is the base value and it represents the current value at the first turn-off.

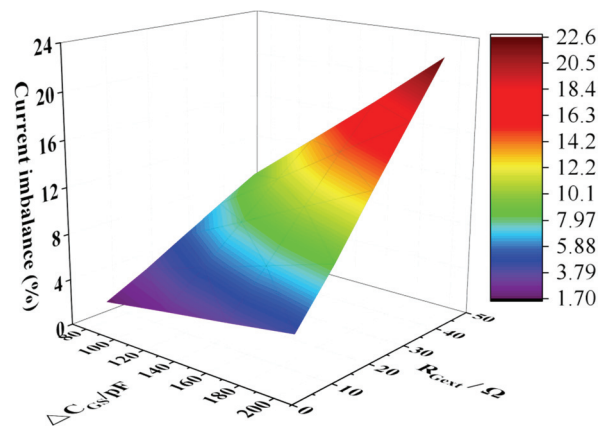
In Fig. 8, both the turn-on and turn-off current imbalance increase with an increasing difference of C_{GS} under the same gate resistance. The slope of the current imbalance also increases with the gate resistance. This means that the sensitivity of the influence of the C_{GS} mismatch on the current imbalance increases with the gate resistance. In addition, if the difference of C_{GS} is held constant, the current imbalance also increases with an increasing gate resistance due to the consequent increase in the difference of the switching delay time.

C. Threshold Voltage and Trans-Conductance

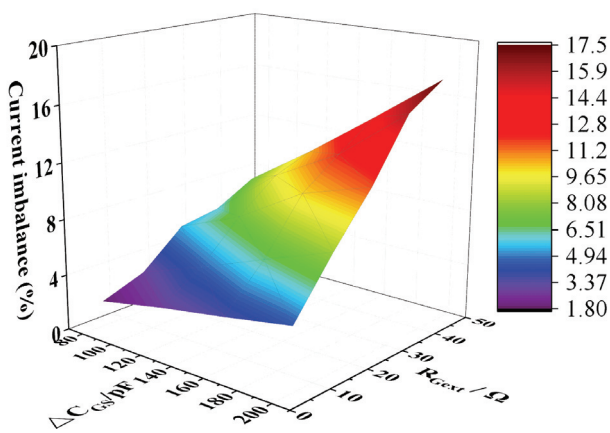
During the transient process, when the gate bias voltage exceeds V_{th}, the current starts to increase. According to (2), the drain current of the saturated region mainly depends on the gate bias voltage, V_{th} and g_{fs}. Assuming that a single driver is adopted for the paralleled SiC MOSFETs so that their gate bias voltages are the same, the maximum current difference can be derived from (2) and expressed as (11).

$$\Delta i_{Dmax} = \frac{\Delta g_{fs} i_D + \Delta g_{fs}\sum_{j=1}^{N} g_{fsj} V_{thj}}{\sum_{j=1}^{N} g_{fsj}} + g_{fsmin} V_{thmax} - g_{fsmax} V_{thmin} \quad (11)$$

where Δi_{Dmax} is the maximum transient current difference. g_{fsmax} and g_{fsmin} are the maximum and minimum trans-conductance,



(a)



(b)

Fig. 8. Current imbalance under different C_{GS} and R_{G_ext}. (a) Turn-on current imbalance. (b) Turn-off current imbalance.

respectively. V_{thmax} and V_{thmin} are the maximum and minimum threshold voltages, while Δg_{fs} is the difference of the trans-conductance. i_D is the total transient current.

Similarly, taking two devices as an example, N is equal to two. Assuming that the difference between the trans-conductance values is small enough that it can be approximated that $g_{fs1}= g_{fs2}= g_{fs}$, (11) can be simplified to:

$$\frac{i_{D1}-i_{D2}}{V_{th1}-V_{th2}}=\frac{\Delta i_D}{\Delta V_{th}}=-\frac{g_{fs}}{2}<0 \tag{12}$$

When the V_{th} variation is very small, it can be further approximated that $V_{th1}=V_{th2}$. In addition, (11) can be simplified to:

$$\frac{i_{D1}-i_{D2}}{g_{fs1}-g_{fs2}}=\frac{\Delta i_D}{\Delta g_{fs}}=\frac{i_{DT}}{g_{fs1}+g_{fs2}}>0 \tag{13}$$

For paralleled devices, the greater the difference of either the V_{th} or g_{fs} values, the more severe the current imbalance becomes. Moreover, current imbalance increases with the current levels. According to (12), the derivative of the current imbalance with respect to the difference of V_{th} is negative. This indicates that the device with the largest V_{th} carries the least drain current during switching transients. Conversely, as presented in (13), the derivative of the current imbalance with respect to the difference of g_{fs} is positive. Hence, the device with the largest g_{fs} conducts most drain current during switching transients. Therefore, the two parameters have offsetting or supporting impacts on current sharing, which depend on the relative values of V_{th} and g_{fs} of the two devices.

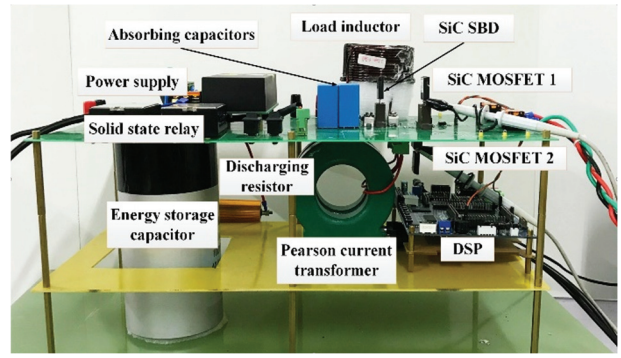


Fig. 9. Double pulse test platform for two-paralleled devices.

IV. Experimental Analysis

A. Experiment Platform

As shown in Fig. 9, a double pulse test platform with two-devices connected in parallel is set up. The test platform includes a digital signal processor, DC bus-bar, driver circuit, charging and discharging loop and auxiliary power supply. In order to avoid the influence of circuit parasitic parameters' mismatch, the circuit layout is designed to be as symmetrical as possible.

Typically, the rising and falling times of the current and voltage for SiC MOSFETs are in the range of 20ns-100ns. To ensure the reliability of measurement results in the actual test, a bandwidth margin of 3-5 times is generally needed, which is at least 52.5MHz-87.5MHz as calculated by (14) [33].

$$\mathrm{BW}=0.35/\min[t_r,t_f] \tag{14}$$

The selected measuring probe fully meets the bandwidth requirements of the signal under test. In addition, the external gate resistances are separately connected to each of the two devices and a resistance value of 37.5Ω is used in all of the experiments in this paper unless otherwise specified.

B. On-resistance R_{DS}

In this paper, two devices, identified as No. 4 and No. 23, with a large difference in the on-resistance values and small differences of other parameters' values, are selected. The on-resistances of devices No. 4 and No. 23 at 20A are 77.32 mΩ and 86.77 mΩ, respectively. Fig. 10 shows that No. 23 conducts less of the steady-state current due to its higher on-resistance. Although the steady-state current imbalance m between No. 4 and No. 23 is 11.1% and remains constant, the

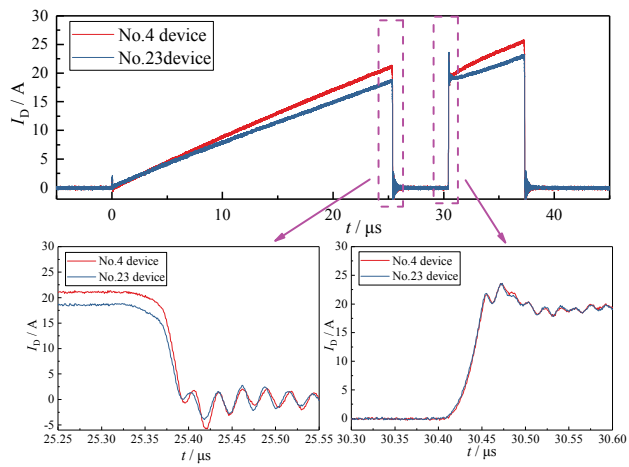


Fig. 10. Current distribution of paralleled devices No.4 and No.23.

difference in the actual steady-state current increases with the load current as a result of the gradual increase in the average current, as depicted by (6). The turn-on transient current imbalance is only 3.8% despite the large difference in on-resistance between the two devices. However, the turn-off transient current imbalance reaches 16.8%. This demonstrates that the switching transient current distribution is not sensitive to the spread of the on-resistance. However, the on-resistance indirectly affects the turn-off current distribution by influencing the initial current difference just before turn-off.

C. Gate-source Capacitance C_{GS}

There are many factors that affect the transient current distribution among paralleled units. It is hard to select proper experimental sample from the 30 devices since the spread of V_{th} is relatively large. Thus, it is difficult to control each of the variables separately. In this paper, devices No.24 and No.27, with almost equal parameter values, are used to study the influence of differences in the parasitic capacitances or internal gate resistance between devices by the insertion of a capacitor or a resistor. The most important parameters of devices No.24 and No.27 are shown in Table I. Fig. 11 shows that both the steady-state and transient current imbalances are very small, where a value of 0.5% is calculated for the steady-state current and values of 4.3% and 3.4% are calculated for the turn-on and turn-off transient currents, respectively. This indicates that this set of devices can be selected as a reference.

Among all of the devices, the difference of C_{GS} between devices No. 25 and No. 30 is the largest and reaches 200pF under a bias voltage of 500V. To avoid the superposition effect of the other parameters, devices No.24 and No.27 are selected. Then, 110pF and 220pF ceramic capacitors are connected in parallel across the gate-source terminal of device No.24. As shown in Fig. 12, the turn-on and turn-off transients of device No.24 is slower than that of device No.27. Therefore, device No.27 carries more current during turn-on

TABLE I
PARAMETERS OF DEVICES NO.24 AND NO.27

Parameters	No.24	No.27	Differences
C_{GS}@500V/pF	942.49	941.29	1.20
C_{DS}@500V/pF	78.17	77.97	0.20
C_{GD}@500V/pF	5.46	5.38	0.08
R_{DS}@20A/mΩ	86.61	86.68	-0.07
V_{th}/V	2.11	2.01	0.10
g_{fsmax} /A/V	9.62	9.81	-0.19
R_{G_int}/Ω	3.86	4.15	-0.29

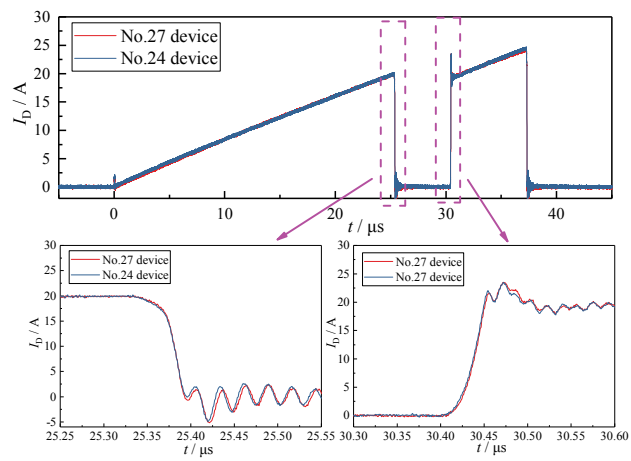


Fig. 11. Current distribution of paralleled devices No.24 and No.27.

transients, and less current during turn-off transients. When ΔC_{GS} is 110pF, the turn-on and turn-off transient current imbalances are 10.4% and 10.3% as shown in Fig. 12 (a). When ΔC_{GS} is 220pF, the turn-on and turn-off transient current imbalances are 14.3% and 15.9% as shown in Fig. 12 (b). This means that the spread of C_{GS} and its effect on the transient current distribution under a 37.5Ω external gate resistance cannot be ignored. In addition, similar to the above simulation results, the effect of a C_{GS} mismatch on the transient current under the parallel configuration of SiC MOSFETs is also related to the gate resistance. As shown in Fig. 12 (c), the turn-on and turn-off transient current-imbalances are 8.3% and 10.1% when the external gate resistance is 10Ω. This shows that the effect of a C_{GS} mismatch on the transient current of paralleled MOSFETs can be ignored under a small external gate resistance. As for the steady-state current distribution, there is a negligible effect of C_{GS}.

Generally, there are two concepts for the gate driver circuit, the fully decoupling driver configurations (FDDC) and the partly decoupling driver configurations (PDDC) as shown in Fig. 13. All of the experiments described above are conducted under the FDDC. Thus, the external gate resistances are separately connected. According to the above analysis, the sensitivity of the transient current imbalance to ΔC_{GS} also depends on the decoupling gate resistance due to the switching delay difference. To fairly compare two configurations, $R_{G\_ext1}=R_{G\_ext2}=2R_{G\_ext}$ is used to achieve a comparable switching

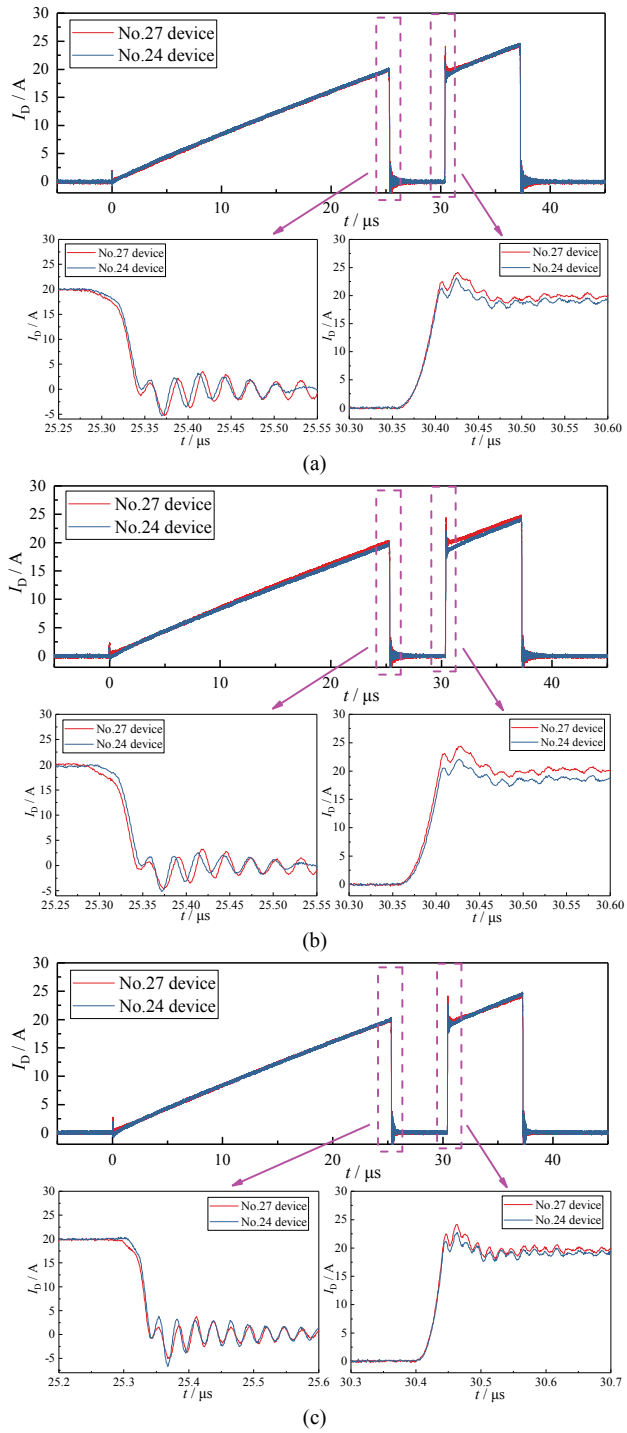


Fig. 12. Current distribution under different C_{GS} and R_{G_ext}. (a) C_{GS}=110pF, R_{G_ext}=37.5Ω. (b) C_{GS}=220pF, R_{G_ext} =37.5Ω. (c) C_{GS}=220pF, R_{G_ext} =10Ω.

speed. As can be seen in Fig. 14, the transient current imbalance for the turn-on and turn-off are 7.38% and 8.65% at rising time and falling time of 28.8ns and 26.1ns. This is similar to the FDDC with 29.6ns and 31.2ns in Fig. 12(b). In contrast, the PDDC, with a smaller decoupling gate resistance, can mitigate the transient current imbalance caused by the spread of C_{GS}.

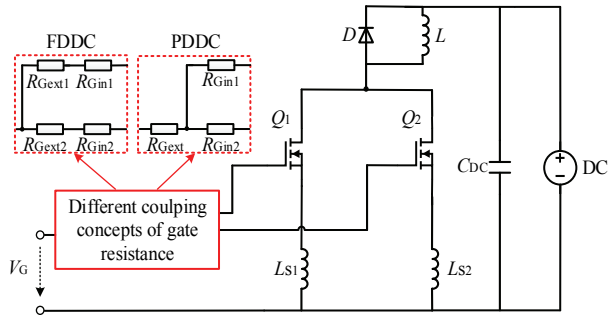


Fig. 13. Two gate driver concepts.

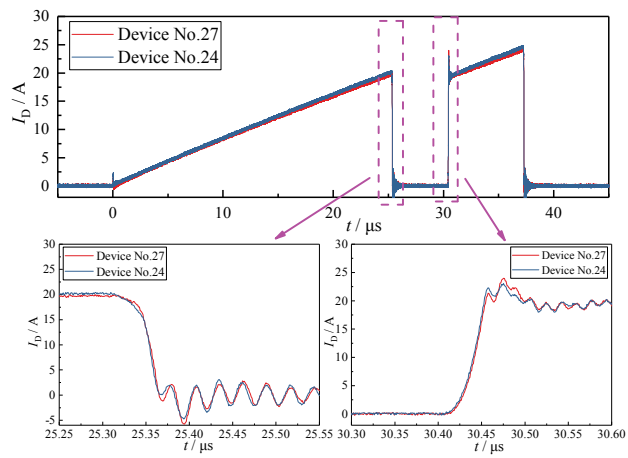


Fig. 14. Current distribution with ΔC_{GS}=220pF under the PDDC.

D. Drain-source Capacitance C_{DS}

Under a clamped inductive load, the drain current rises first and then V_{DS} falls during the turn-on process. Then a reverse sequence of these events happens. Thus, V_{DS} is relatively high during the entire current rising and falling stage. This means that the spreads of C_{DS} and C_{GD} are relatively small due to the high drain-source voltage bias for the analysis of the transient current distribution. The maximum value of ΔC_{DS} for the 30 devices is 11 pF at 200V and 6 pF at 500V. Similarly, a ceramic capacitor is connected in parallel with device No.24 to mimic this difference. As shown in Fig. 15, the transient currents of devices No.24 and No.27 are almost the same under a ΔC_{DS} of 10pF. This means that the influence of the C_{DS} spread on the transient current distribution can be ignored. Furthermore, the C_{DS} mismatch has negligible effect on the steady-state current distribution. Thus, the C_{DS} screening may be neglected before paralleled application.

E. Gate-drain Capacitance C_{GD}

Similar to C_{DS}, the spread of C_{GD} is also small during the current rising and falling stages. The range for the 30 devices at 500V is less than 1pF. Limited by the capacitance range of the high-voltage ceramic capacitors, a ceramic capacitor of 3pF is connected in parallel with device No.24. As shown in Fig. 16, C_{GD} has little effect on the current rising and falling in comparison to C_{GS} due to its comparatively much smaller

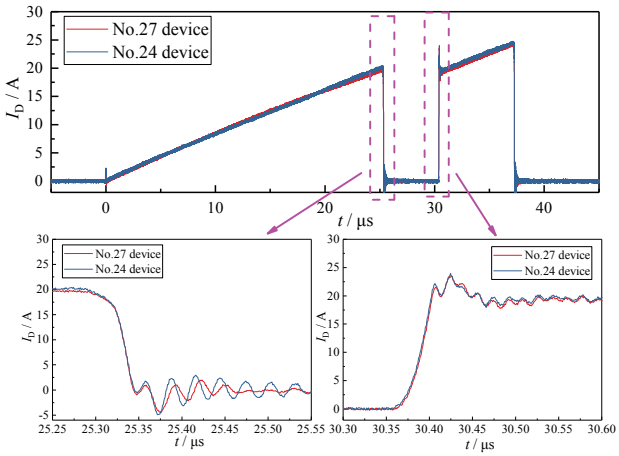


Fig. 15. Current distribution of paralleled devices No.24 and No.27 under ΔC_{DS}=10pF.

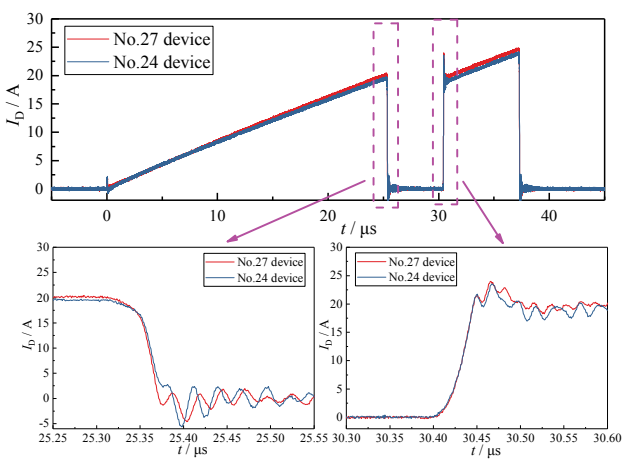


Fig. 16. Current distribution of paralleled devices No. 24 and No. 27 under ΔC_{GD}=3pF.

value. However, the displacement current caused by the fast rate of the change of V_{DS} flows through C_{GD}. Thus, there is obviously a current difference during the rising or falling stage of V_{DS}. The turn-on and turn-off current imbalances are 10% and 13.3%, respectively. Generally, both C_{GD} and ΔC_{GD} are small at a high bias voltage. In addition, the maximum difference of C_{GD} for the 30 samples measured in this paper is not more than 1pF. Thus, it can be regarded that the corresponding current imbalance does not exceed 10%. Moreover, similar to C_{GS} and C_{DS}, C_{GD} has little effect on the steady-state current distribution.

F. Internal gate resistance R_{G_int}

The static test results presented in the previous section show that the range of R_{G_int} for the 30 devices selected in this paper is 1.4Ω. In order to avoid too large a gate resistance, which can amplify the influence of the parasitic capacitance, the 1.4Ω difference of the resistance, under a 10Ω external gate resistance, is inserted to study the influence of R_{G_int} on current distribution in this paper. As shown in Fig. 17, the

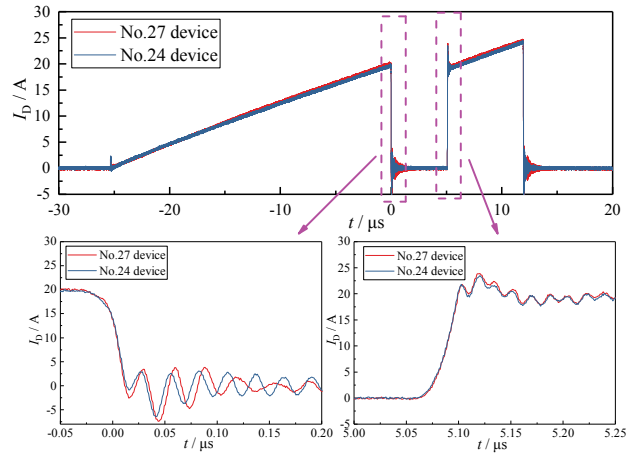


Fig. 17. Effect of R_{G_int} on the current distribution of paralleled devices.

TABLE II
PARAMETERS COMPARISON OF DEVICES NO.12, NO.19, NO.4 AND NO.30

Parameters	No.12	No.19	No.4	No.30
C_{GS}@500V /pF	958.81	920.12	938.79	896.35
C_{DS}@500V/ pF	81.25	82.13	81.36	81.67
C_{GD}@500V/ pF	5.86	5.89	5.86	5.62
V_{th} /V	2.36	1.69	2.20	1.55
g_{fsmax}/ A/V	9.58	10.02	10.19	9.30
R_{G_int}/Ω	4.32	3.52	3.85	3.82

turn-on and turn-off transient current imbalances are 4.8% and 6.6%, respectively. In addition, the difference of R_{G_int} has almost no effect on the steady-state current distribution. Therefore, the spread in the R_{G_int} values may not be considered before the parallel connection of SiC MOSFET devices.

G. Threshold Voltage V_{th} and Trans-conductance g_{fs}

For an experimental investigation of the influence of V_{th} and g_{fs} on transient current distribution, two pairs of devices from the 30 devices sample are selected in this paper. Devices No. 4 and No. 30 are uses as the first pair and No. 12 and No.19 are used as the second pair. There are several reasons behind this choice. First, it is not necessary to ensure the consistency of on-resistance due to its insignificant influence on transient current distribution. Second, the influence of the differences in the values of R_{G_int}, C_{DS} and C_{GD} is relatively small. Third, the spread of the parasitic capacitance C_{GS} is small, implying that its distribution is centralized. Thus, devices with satisfactory parameters can be directly selected from the sample. The parameters of the selected devices are shown in Table II. For the first pair, device No.12 has larger V_{th} and smaller g_{fs} values when compared to device No.19. For the second pair, device No.4 has larger values for both V_{th} and g_{fs} when compare to those of device No.30. As shown in Fig. 18, device No.19 turns on earlier and its drain current rises faster. This indicates that the effects of the threshold voltage

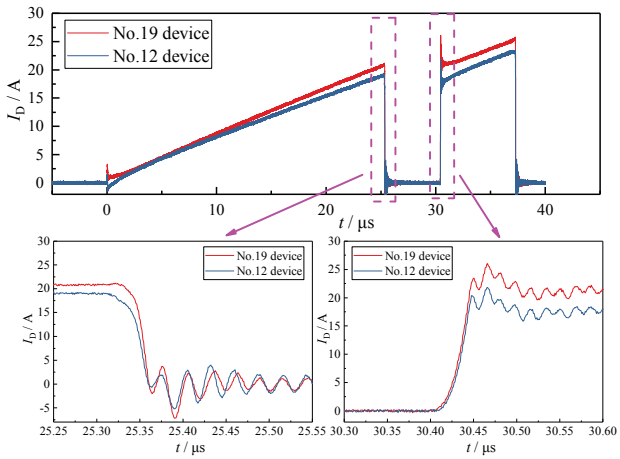


Fig. 18. Current distribution of paralleled devices No. 12 and No. 19.

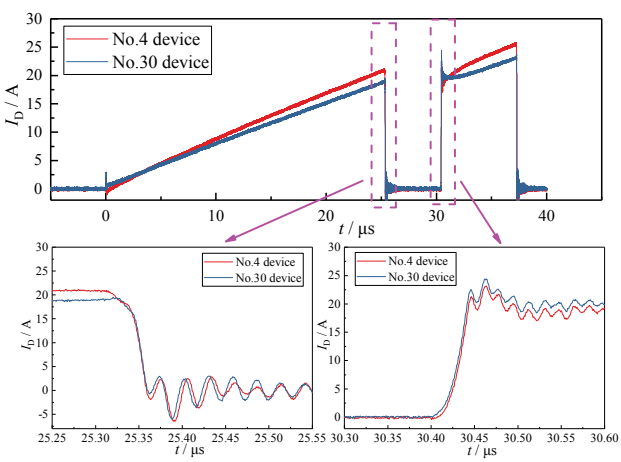


Fig. 19. Current distribution of paralleled devices No. 4 and No. 30.

mismatch and trans-conductance mismatch have a positive compensation effect, resulting in an increased current imbalance. The turn-on and turn-off transient current imbalances are 23.7% and 23.2%, respectively. However, for the second pair, Fig. 19 shows that the turn-on and turn-off transient current imbalances are 10.3% and 4.6%, respectively. This is because the offsetting impacts between V_{th} and g_{fs} make the turn-on and turn-off current distribution significantly better than those of the first pair. Thus, the overall effects of V_{th} and g_{fs} should be considered. Actually, the trans-conductance is a variable with drain current, which is difficult to screen with a single measured value. Transfer curves screening combined the threshold voltage and trans-conductance may be a better way to address this issue, which will be further developed in future research work.

H. Influence of Junction Temperature on Current Distribution

The temperature dependency of the characteristic parameters of SiC MOSFET devices has been widely reported [34], [35]. The important parameters that are sensitive to temperature are the threshold voltage, on-resistance and trans-conductance.

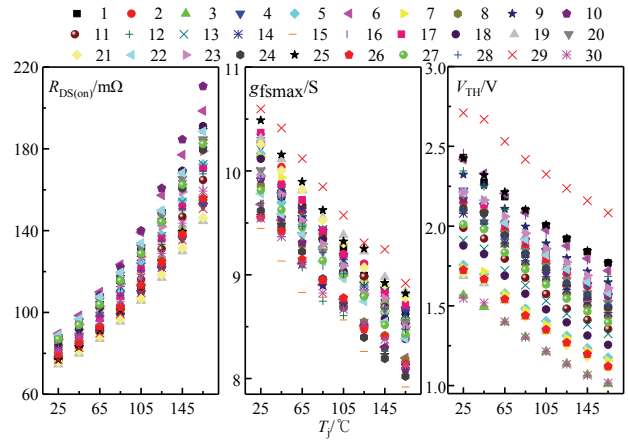


Fig. 20. Device parameters spread under various temperatures [36].

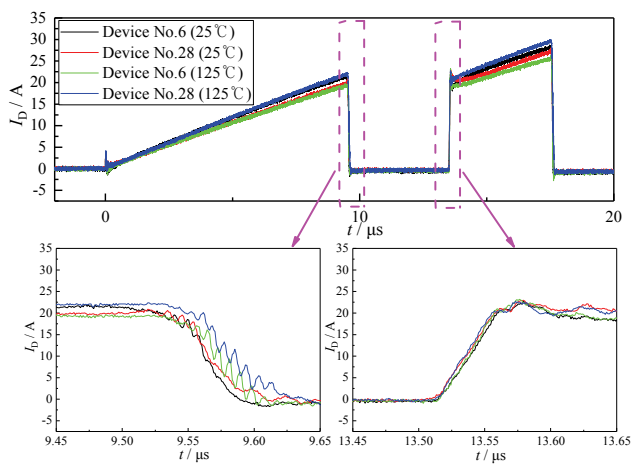


Fig. 21. Current distribution at different temperatures.

However, the spread of these parameters at different temperatures should be further discussed. The same samples mentioned above are tested in the range of 25℃-165℃. As shown in Fig. 20 [36], the overall variation of the on-resistance increases with an increasing junction temperature, while the spread of the threshold voltage and trans-conductance display a low sensitivity to junction temperature.

A set of devices, No. 6 and No. 28, is taken as an example to illustrate the influence of junction temperature on the current distribution of paralleled devices. As shown in Fig. 21, the steady-state current difference at 125℃ is larger than that at 25℃. This is because the on-resistances of devices No. 6 and No. 28 are 90mΩ and 83 mΩ at 25℃, whereas they are 157 mΩ and 135 mΩ at 125℃. As for the transient current distribution, the drain current of the same device increases with the junction temperature due to the negative temperature coefficient of the transfer characteristic. On the other hand, the transient current difference between devices No. 6 and No. 28 is almost unchanged at different junction temperatures. Therefore, a devices screening strategy based on the characteristic parameters measured at separate temperature conditions is better for actual parallel applications. That is, the on-resistance

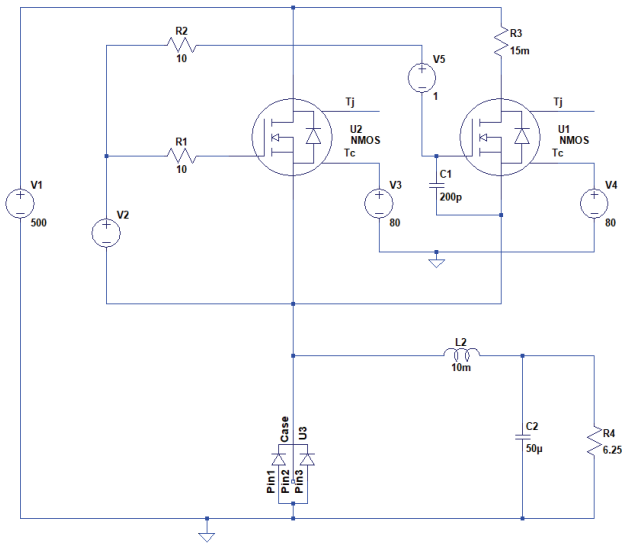


Fig. 22. DC-DC buck converter model with two paralleled devices.

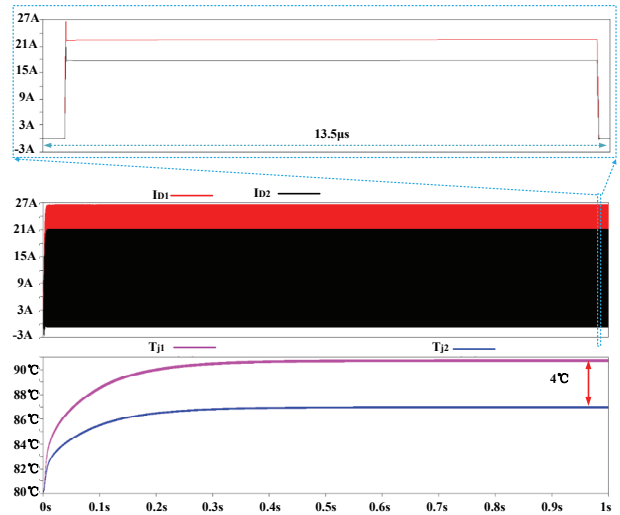


Fig. 23. Junction temperature variation of two paralleled devices.

can be measured at the operating temperature and the transient parameters such as the threshold voltage and trans-conductance can be measured at room temperature.

V. Junction Temperature Variation

Usually, thermal dissymmetry is a main cause of devices damage in parallel-connection applications. The junction temperature variation of paralleled devices due to current imbalance caused by device parameters spread should be further discussed. Generally, the device switches only twice for each test, and the increase of the device junction temperature due to the power loss is negligibly small. Thus, an actual converter needs to be built. However, the junction temperature is very difficult to measure. In this paper, a simple buck DC-DC converter model is built in LTSPICE as shown in Fig. 22. The device model is available from the manufacturer. A voltage source of 1V, an external capacitor of 180pF and a parasitic resistor of 15mΩ are added into the loop of one device to evaluate the influence of the main device parameters spread on the junction temperature variation.

Generally, the case temperature is controlled within the range of 50℃-80℃, which depends on different cooling conditions [37]. In this paper, the initial case temperature of both devices is set as 80℃. The total steady-state current of the two paralleled devices is 40A. As shown in Fig. 23, the steady state current unbalance of the two paralleled devices is about 24%, and the transient current unbalance is about 28%. Moreover, the temperature variation of the two paralleled devices is about 4℃, and the corresponding difference of the temperature rising approaches 54%. If the circuit parameters and thermal path dissymmetry are also considered, this temperature variation gets larger. Therefore, more attention should be paid to the device parameter spread and screening in parallel-connection applications.

VI. Screening Guideline for Paralleling

With the measurement results from the same production batch of SiC MOSFET devices, it can be seen that the spread of the threshold voltage is the largest, followed by those of the internal gate resistance, on-resistance and trans-conductance, in that order. Despite the fact that the spread of the gate-drain parasitic capacitance changes rapidly near the 12.5V region, the spreads of the other two parasitic capacitances almost remain constant with an increasing drain-source voltage. In addition, from comprehensive theoretical and experimental analyses of the effect of device parameters mismatches on the current distribution of paralleled SiC MOSFET devices, the most influential parameters are determined to be the on-resistance, threshold voltage, trans-conductance and gate-source parasitic capacitance.

For the steady-state current distribution, the device's on-resistance has a significant effect and needs to be screened, while the other device parameters do not have a significant effect. The other device parameters have more influence on the transient current distribution than the steady-state current distribution. However, the effects of R_{G_int}, C_{DS} and C_{GD} on the transient current distribution are relatively small and can be ignored due to the small actual variations of their values. Therefore, the main factors affecting the transient current distribution are V_{th}, g_{fs} and C_{GS}. For the transient current distribution among paralleled SiC MOSFET devices, there is an overall effect, which may be an offsetting or a supporting function of the threshold voltage and trans-conductance. The overall effects of V_{th} and g_{fs} on the transient current distribution are complicated and depends on the relationship between their actual values. The influence of the difference of C_{GS} on the current distribution depends on the gate resistance. Whether the effects of ΔC_{GS} should be considered or not depends on the actual value of the selected gate resistance. In high frequency applications, the gate resistance is generally

small and its effect can be ignored. In low switching speed applications, the effect of the difference of the gate-source capacitance can also be mitigated by adopting a partly decoupling driver configuration. Moreover, it is better to use main parameters measured at the operating temperature for device screening before parallel connection.

VII. Conclusions

This paper systematically discusses the spread of device parameters and their influence on the current distribution of paralleled SiC MOSFET devices. Test results shows that there is large parameter spread among SiC MOSFET devices from the same batch. Based on the control variable method, comprehensive theoretical and experimental analyses of the effect of device parameters mismatches on the current distribution among paralleled SiC MOSFET devices are conducted. Experimental results show that the main parameters that need to be screened are the threshold voltage, transconductance, on-resistance and gate-source capacitance. The temperature dependency of the spread of these main device parameters and their influence on current distribution are discussed. The transient current distribution is not sensitive to temperature. Meanwhile, the steady-state current distribution is affected by temperature. The device screening should consider the actual operating temperature of paralleled devices. In actual applications, if different main parameters need to be screened, which also depends on different driver configurations and switching speeds, a gate driver configuration is recommended to eliminate the influence of the spread of the gate-source capacitance. All of these suggestions are useful for the screening of devices or chips before device paralleling in power circuits or multi-chips paralleling in power modules.

Acknowledgment

The authors of this paper wish to express their sincere gratitude to the National Key R&D Program of China and the Fundamental Research Funds for the Central Universities under Grant which supported this research via sponsorship number of 2018YFB0905703 and 2018QN015 respectively.

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