

# Active CDS-Clamped L-Type Current-Fed Isolated DC-DC Converter

Minh-Khai Nguyen\*, Truong-Duy Duong\*\*, Young-Cheol Lim†, and Joon-Ho Choi\*\*

\*Department of Electrical Engineering, Chosun University, Gwangju, Korea

†, \*\*Department of Electrical Engineering, Chonnam National University, Gwangju, Korea

## Abstract

In this paper, an active capacitor-diode-switch (CDS) snubber is proposed for L-type current-fed isolated DC-DC converters. The proposed CDS-clamped converter has a number of advantages. It can achieve wide range zero-voltage switching (ZVS) on two switches, a continuous input current with a low ripple, a reduction of one active switch and high efficiency. The operating principles, analysis and parameter design guideline are presented. A 300 W prototype is built to test the proposed converter. Simulation and experimental results are shown at 30 V input voltage and 400 V output voltage.

**Key words:** Active snubber, Current-fed half-bridge (CFHB) converter, DC-DC conversion, Galvanic isolation, L-type, Zero-voltage switching (ZVS)

## I. INTRODUCTION

Two-stage grid-connected inverters are usually utilized to connect renewable energy sources to the AC utility voltage. In the first stage, a high voltage gain DC-DC converter is generally used to convert a low-voltage source into a constant DC bus voltage. Many high boost DC-DC converters have been investigated to obtain a high DC bus voltage from a low input voltage. Topologies with and without a coupled inductor are usually used in non-isolated DC-DC converters to achieve a high output voltage gain [1], [2]. In isolated DC-DC converter topologies, a high-frequency step-up transformer is used to isolate the input and output. Because current-fed isolated converters [2]-[23] have a boost function and a low input current ripple, they are suitable for high boost voltage gain applications such as fuel cell power systems.

Recently, many current-fed isolated converters have been developed in half-bridge and full-bridge topologies. A current-fed half-bridge (CFHB) converter was proposed in [3] with reduced power devices. Since the half-bridge topology cannot generate a zero voltage at the primary side of the

transformer, the utilization of the high-frequency transformer is decreased. Thus, CFHB converters are only suitable for low power applications. For a high boost voltage gain and high power applications, current-fed full-bridge (CFFB) converters are addressed in [7]-[12]. In CFFB converters, a single inductor is connected to the full-bridge circuit in series at the low-voltage side. Due to the resonance between the output capacitance of the primary switches and the leakage inductor of the transformer, voltage spikes appear on the switches in CFFB converters. Various solutions such as using soft-switching techniques [3]-[9], and adding passive [10] and active [11], [12] snubbers have been carried out to eliminate these voltage spikes. To reduce the input current ripple, the current stress of the devices and the size of the magnetic components, an interleaved CFFB converter was proposed in [13]. This converter uses a larger number of switches and transformers.

The original L-type CFHB converter in [14] uses two inductors and two switches in interleaved operation. When compared to other current-fed isolated converters, the L-type CFHB converter has the lowest input current. In addition, the utilization of a high-frequency transformer in the L-type CFHB converter is best because the voltage at the primary side of the transformer has three levels: positive, zero and negative. However, the conventional L-type CFHB converter has a voltage spike problem at turn-off due to the leakage inductor of the transformer. In order to solve the voltage

Manuscript received Nov. 3, 2017; accepted Feb. 6, 2018

Recommended for publication by Associate Editor Yan Xing.

†Corresponding Author: yclim@chonnam.ac.kr

Tel: +82-62-530-1743, Chonnam National University

\*Dept. of Electrical Eng., Chosun University, Korea

\*\*Dept. of Electrical Eng., Chonnam National University, Korea

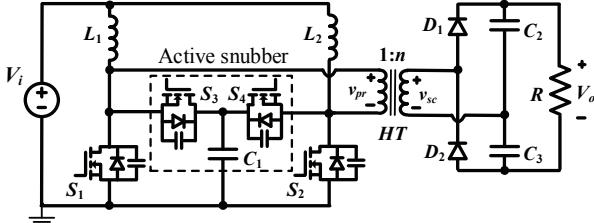


Fig. 1. Conventional L-type current-fed half-bridge (CFHB) DC-DC converter with an active-clamped snubber.

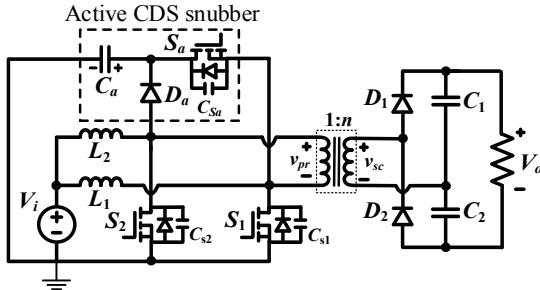


Fig. 2. Proposed active CDS-clamped L-type CFHB DC-DC converter.

spike problem in the conventional L-type CFHB converter, various topologies have been proposed [15]-[22]. Active-clamped L-type CFHB converters were introduced in [15]-[20]. Fig. 1 shows the conventional L-type CFHB converter [17], [18] with an active-clamped snubber. It consists of two boost inductors ( $L_1$ ,  $L_2$ ), two main switches ( $S_1$ ,  $S_2$ ), an active-clamped snubber that uses two auxiliary switches ( $S_3$ ,  $S_4$ ) and one clamping capacitor ( $C_1$ ), a high-frequency boost transformer (HT), a voltage doubler rectifier ( $D_1$ - $D_2$ - $C_2$ - $C_3$ ) and a load ( $R$ ). The major advantages of the L-type CFHB converter with an active-clamped snubber are as follows: 1) the switches operate under the zero-voltage switching (ZVS), 2) the clamping capacitor voltage is constant across all of the switches, 3) the gate drive implementation is simple and 4) the input current ripple is very low. In [19], a series-resonant circuit is attached to the secondary side of an L-type CFHB converter as a voltage-doubler rectifier to clamp the surge voltage of the switches. Two active-clamped L-type CFHB converters with interleaved operation in the parallel input and series output configuration were proposed in [21]. Instead of using a single large transformer, two small transformers are used in [22] to reduce the voltage ratings of the primary switches and secondary diodes in an L-type CFHB converter. However, the active-clamped snubber in [15]-[21] use one clamping capacitor and two auxiliary switches (CDS). The proposed CDS-snubber CFHB DC-DC converter has all of the inherent advantages of conventional L-type CFHB converters but uses one less active

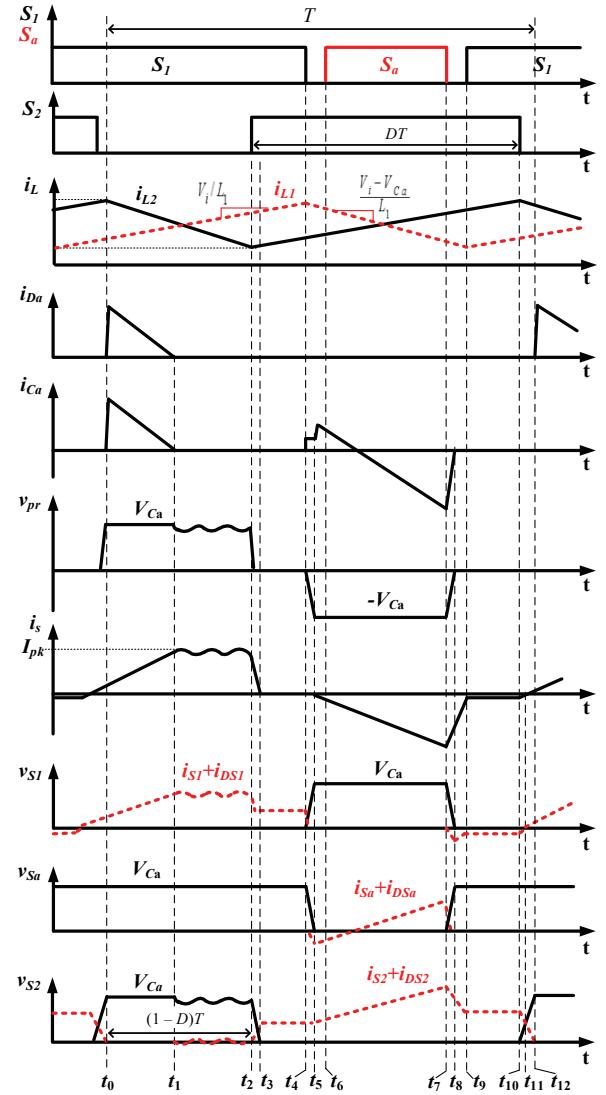


Fig. 3. Operating waveforms of the proposed CDS-clamped converter.

switch in the snubber circuit. Moreover, the proposed converter achieve wide range ZVS on two switches and hard switching on one switch. The operating modes, analysis, and design considerations for the proposed converter as well as the simulation and experimental results are shown.

## II. PROPOSED CDS SNUBBER FOR CFHB DC-DC CONVERTER

The proposed CDS-clamped L-type CFHB DC-DC converter is shown in Fig. 2. Two boost inductors ( $L_1$  and  $L_2$ ), two switches ( $S_1$  and  $S_2$ ), and an active CDS snubber circuit with one switch ( $S_a$ ), one diode ( $D_a$ ) and one capacitor ( $C_a$ ) are connected to the primary winding of the high-frequency transformer (HT). The secondary winding of the transformer (HF), two diodes ( $D_1$  and  $D_2$ ) and two capacitors ( $C_1$  and  $C_2$ ) are connected to a resistive load ( $R$ ) at the high-voltage side. When compared to the conventional

This paper proposes a novel active-clamped snubber for L-type CFHB DC-DC converters. The proposed active-clamped snubber uses one clamping capacitor, one diode and one auxiliary switch (CDS). The proposed CDS-snubber CFHB DC-DC converter has all of the inherent advantages of conventional L-type CFHB converters but uses one less active

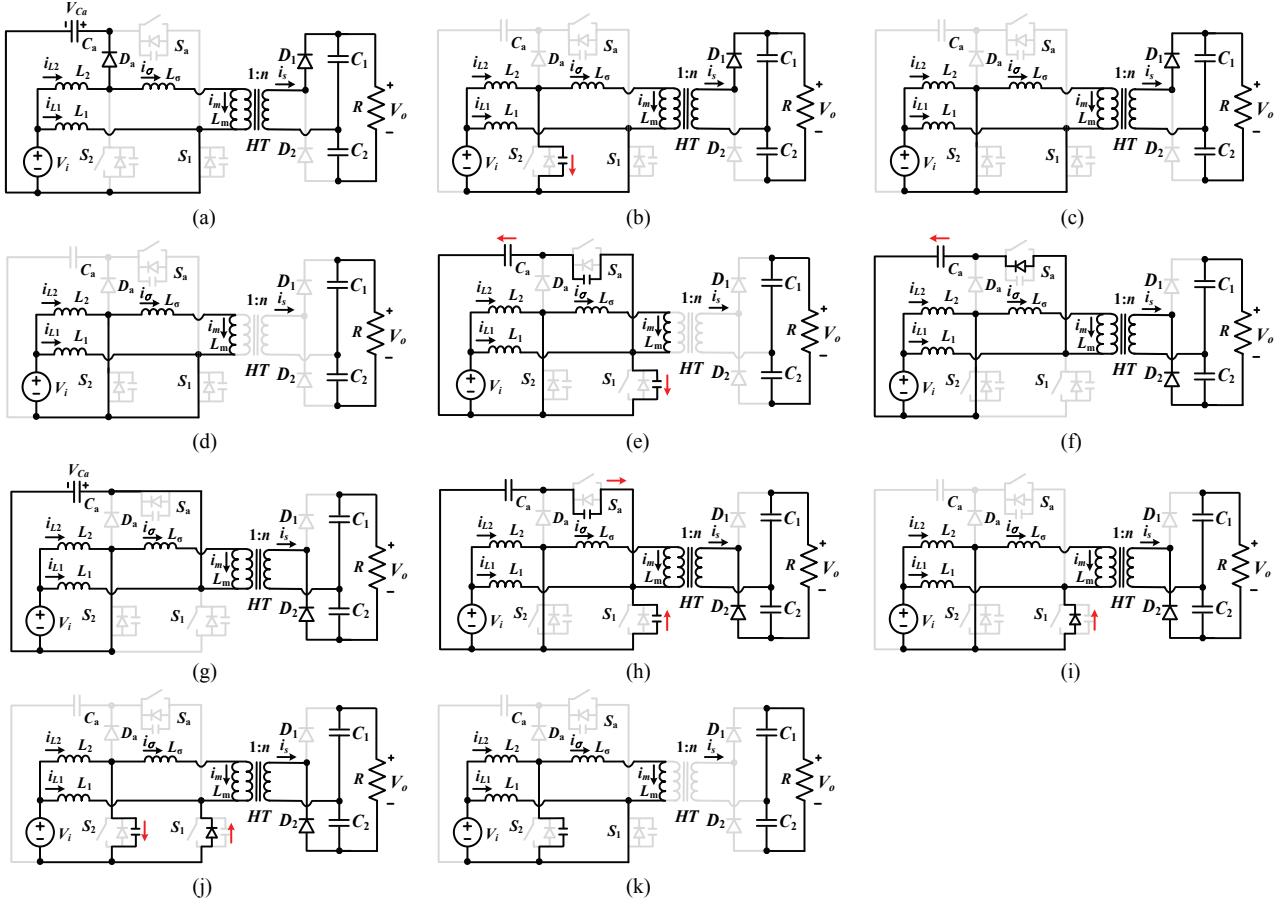


Fig. 4. Equivalent circuits of the proposed converter for different intervals.

active-clamped L-type CFHB converter in Fig. 1, the proposed CDS-clamped converter has one less active switch associated with its insulated gate drive circuit. As a result, the cost of the proposed converter is reduced.

Fig. 3 shows operating waveforms of the proposed CDS-clamped converter. The gating control signals of the switches  $S_1$  and  $S_2$  are operated with a  $180^\circ$  phase shift. The gating control signal of the switch  $S_a$  is complementary to that of the switch  $S_1$ . A dead-time between  $S_1$  and  $S_a$  is used to turn on  $S_1$  and  $S_a$  with ZVS.

#### A. Operating Modes

The following conditions are assumed for the operation and analysis of the proposed converter: 1) the inductance of the  $L_1$  and  $L_2$  inductors is large enough to maintain a constant current; 2) the capacitance of the  $C_a$ ,  $C_1$  and  $C_2$  capacitors is large enough to maintain a constant capacitor voltage; 3) all of the diodes and switches are ideal; 4) the high-frequency transformer is modeled by means of a leakage inductor ( $L_\sigma$ ) connected to an ideal transformer ( $T$ ) and a magnetizing inductance ( $L_m$ ); 5) the current flow to the windings of the transformer and inductors increases or decreases linearly; and 6) small capacitors  $C_{S1}$ ,  $C_{S2}$  and  $C_{Sa}$  are connected to the power switches  $S_1$ ,  $S_2$  and  $S_a$  in parallel. Fig. 4 shows equivalent

circuits of the proposed converter for different intervals.

**Interval 1**– $[t_0 - t_1]$ , Fig. 4(a):  $S_1$  is turned on, while  $S_a$  and  $S_2$  are turned off. The inductor  $L_1$ , the capacitor  $C_a$  and the primary winding of the transformer are charged, while the inductor  $L_2$  is discharged. The  $D_a$  and  $D_1$  diodes are forward-biased, while the  $D_2$  diode is reverse-biased. The primary voltage of the transformer is  $V_{Ca}$ . The secondary side of the transformer generates a positive voltage. The following is obtained:

$$\begin{cases} L_2 \frac{di_{L2}}{dt} = V_i - V_{Ca} \\ L_1 \frac{di_{L1}}{dt} = V_i \end{cases} \text{ and } \begin{cases} L_\sigma \frac{di_\sigma}{dt} = V_{Ca} - \frac{V_o}{2n} \\ L_m \frac{di_{Lm}}{dt} = \frac{V_o}{2n} \end{cases} \quad (1)$$

The secondary current of the transformer increases linearly from zero to the peak value and is calculated by:

$$i_s = \frac{1}{2n^2} \left( \frac{2nV_{Ca} - V_o}{L_\sigma} - \frac{V_o}{L_m} \right) t. \quad (2)$$

**Interval 2**– $[t_1 - t_2]$ , Fig. 4(b): When the inductor  $L_2$  is discharged, the primary winding current is charged, and the  $D_a$  diode is reverse-biased. The leakage inductor  $L_\sigma$  resonates with the snubber capacitor  $C_{S2}$ . The following equations are as follows:

$$\begin{cases} L_2 \frac{di_{L2}}{dt} = V_i - v_{CS2} \\ L_1 \frac{di_{L1}}{dt} = V_i \end{cases} \text{ and } \begin{cases} L_\sigma \frac{di_\sigma}{dt} = v_{CS2} - \frac{V_o}{2n} \\ i_{CS2} = C_{S2} \frac{dv_{CS2}}{dt} = i_{L2} - i_\sigma. \end{cases} \quad (3)$$

$$\begin{cases} v_{CS2} = \frac{V_o}{2n} + \left( V_{Ca} - \frac{V_o}{2n} \right) \cos \omega_0(t - t_1) \\ i_{CS2} = -\sqrt{\frac{C_{S2}}{L_\sigma}} \left( V_{Ca} - \frac{V_o}{2n} \right) \sin \omega_0(t - t_1), \end{cases} \quad (4)$$

where  $\omega_0 = 1/\sqrt{L_\sigma C_{S2}}$  is the angular resonant frequency.

The secondary side of the transformer generates a positive voltage. The secondary current of the transformer is expressed as:

$$i_s = I_{pk} + \frac{1}{n} \left[ \frac{V_i - V_{Ca}}{L_1} (t - t_1) + \sqrt{\frac{C_{S2}}{L_\sigma}} \left( V_{Ca} - \frac{V_o}{2n} \right) \sin \omega_0(t - t_1) \right], \quad (5)$$

where  $I_{pk}$  is the peak value of the secondary current of the transformer.

**Interval 3**—[ $t_2 - t_3$ , Fig. 4(c)]: At  $t_2$ ,  $S_2$  is turned on, while  $S_1$  remains on and  $S_a$  remains off. The  $D_1$  diode remains forward-biased.

**Interval 4**—[ $t_3 - t_4$ , Fig. 4(d)]: At  $t_3$ ,  $S_1$  and  $S_2$  remain on, while  $S_a$  remains off. The  $D_1$  diode is turned off with ZCS. The  $L_1$  and  $L_2$  inductors are charged. The primary voltage of the transformer is short-circuited by  $S_1$  and  $S_2$ . All of the diodes are reverse-biased and the secondary voltage of the transformer is zero. It is possible to obtain:

$$\begin{cases} L_1 \frac{di_{L1}}{dt} = L_2 \frac{di_{L2}}{dt} = V \\ L_\sigma \frac{di_\sigma}{dt} = L_m \frac{di_{Lm}}{dt} = 0. \end{cases} \quad (6)$$

**Interval 5**—[ $t_4 - t_5$ , Fig. 4(e)]: At  $t_4$ ,  $S_1$  is turned off, while  $S_a$  remains off and  $S_2$  remains on. The  $C_{S1}$  capacitor is charged by the current of  $(i_{L1} + i_m)/2$ , while the  $C_{Sa}$  capacitor is discharged by the same current of  $(i_{L1} + i_m)/2$ .

**Interval 6**—[ $t_5 - t_6$ , Fig. 4(f)]: At  $t_5$ , the capacitor  $C_{S1}$  voltage reaches  $V_{Ca}$ , and the body diode of  $S_2$  is forward-biased. The  $C_a$  capacitor is charged by the current of  $(i_{L1} + i_m)$ .

**Interval 7**—[ $t_6 - t_7$ , Fig. 4(g)]: At  $t_6$ , the direction of the current of  $S_a$  reverses and  $S_a$  is turned on with ZVS. The inductor  $L_2$  is charged, while the inductor  $L_1$ , the capacitor  $C_a$  and the primary winding of the transformer are discharged. The primary voltage of the transformer is  $-V_{Ca}$ . After passing through the step-up transformer, the secondary voltage is negative. The  $D_a$  and  $D_1$  diodes are reverse-biased, while the  $D_2$  diode is forward-biased. The following is obtained:

$$\begin{cases} L_2 \frac{di_{L2}}{dt} = V_i \\ L_1 \frac{di_{L1}}{dt} = V_i - V_{Ca} \end{cases} \text{ and } \begin{cases} L_\sigma \frac{di_{L\sigma}}{dt} = -V_{Ca} + \frac{V_o}{2n} \\ L_m \frac{di_{Lm}}{dt} = -\frac{V_o}{2n}. \end{cases} \quad (7)$$

The secondary current of the transformer is calculated by:

$$i_s = \frac{-1}{2n^2} \left( \frac{2nV_{Ca} - V_o}{L_\sigma} - \frac{V_o}{L_m} \right) (t - t_5). \quad (8)$$

**Interval 8**—[ $t_7 - t_8$ , Fig. 4(h)]: At  $t_7$ ,  $S_a$  is turned off, while  $S_1$  remains turned off and  $S_2$  remains on. The  $C_{S1}$  capacitor is discharged, while the  $C_{Sa}$  capacitor is charged. The secondary current of the transformer decreases from its negative peak value.

**Interval 9**—[ $t_8 - t_9$ , Fig. 4(i)]: At  $t_8$ , the capacitor  $C_{Sa}$  voltage reaches  $V_{Ca}$ , and the body diode of  $S_1$  is forward-biased.

**Interval 10**—[ $t_9 - t_{10}$ , Fig. 4(i) or 4(d)]: At  $t_9$ , the direction of the current of  $S_1$  reverses and  $S_1$  is turned on with ZVS, while  $S_a$  remains turned off and  $S_2$  remains on. The secondary current of the transformer decreases to zero. If the current that flows to the body diode of  $S_1$  goes to zero, the body diode of  $S_1$  is reverse-biased. An equivalent circuit, in this case, is shown in Fig. 4(d). The  $D_2$  diode is turned off with ZCS.

**Interval 11**—[ $t_{10} - t_{11}$ , Fig. 4(j)]: At  $t_{10}$ ,  $S_2$  is turned off, while  $S_1$  remains on. The  $C_{S2}$  capacitor is charged.

**Interval 12**—[ $t_{11} - t_{12}$ , Fig. 4(k)]: At  $t_{11}$ ,  $S_2$  is turned off, while  $S_1$  remains turned on and  $S_a$  remains off. The  $C_{S2}$  capacitor is discharged. This interval ends when the capacitor  $C_{S2}$  voltage is equal to  $V_{Ca}$ .

### B. Output Voltage Gain

Ignoring the dead-time between  $S_1$  and  $S_a$  and applying the volt-second balance law to the inductor  $L_2$ , in a steady state, (1), (3), (6) and (7) yield:

$$V_{Ca} = \frac{V_i}{1 - D}. \quad (9)$$

where  $D$  is the duty cycle of the switch  $S_2$ .

From (2), the peak value of the secondary current of the transformer at  $t_1$  is:

$$I_{pk} = \frac{1}{2n^2} \left( \frac{2nV_{Ca} - V_o}{L_\sigma} - \frac{V_o}{L_m} \right) k \cdot t_2, \quad (10)$$

where  $k$  is a constant less than 1 and equal to  $t_1/t_2$ .

From (2), (5) and (8), the absolute value of the average secondary current is calculated as:

$$|\bar{i}_{sc}| = \frac{1}{2n^2 T} \left[ \begin{aligned} & \left( \frac{2nV_{Ca} - V_o}{L_\sigma} - \frac{V_o}{L_m} \right) \frac{t_1^2}{2} + 2n^2 I_{pk} (t_2 - t_1) \\ & + 2n \left( \frac{V_i - V_{Ca}}{L_1} \right) \frac{(t_2 - t_1)^2}{2} \\ & + \left( \frac{2nV_{Ca} - V_o}{L_\sigma} - \frac{V_o}{L_m} \right) \frac{(t_6 - t_5)^2}{2} \end{aligned} \right]. \quad (11)$$

Substituting  $t_1 = k \cdot t_2$ ,  $t_2 = (1 - D)T$ ,  $t_5 = T/2$ ,  $t_6 = (3 - D)T/2$ ,  $V_{Ca}$  in (9) and  $I_{pk}$  in (10) into (11). Then simplifying it yields:

$$\begin{aligned} |\bar{i}_{sc}| &= \frac{(1-D)TV_i}{2n} \left( \frac{1+k+k^2}{L_\sigma} - \frac{(1-k)^2 D}{L_1} \right) \\ &\quad - \frac{(1-D)^2 TV_o}{4n^2} \left( \frac{1+k+k^2}{L_\sigma} + \frac{(1+k)^2}{L_m} \right), \end{aligned} \quad (12)$$

Because the leakage inductor ( $L_\sigma$ ) is very small in comparison with the input inductor ( $L_1$ ) and the magnetizing inductance ( $L_m$ ), the average secondary current of the transformer in (12) is approximated as:

$$|\bar{i}_{sc}| \approx \frac{(1+k+k^2)(1-D)T}{2nL_\sigma} \left( V_i - \frac{1-D}{2n} V_o \right). \quad (13)$$

Solving (13) with  $|\bar{i}_{sc}| = 2I_o$  yields:

$$G = \frac{V_o}{V_g} \approx \frac{2n}{1-D} - \frac{8n^2 L_\sigma I_o}{(1+k+k^2)(1-D)^2 TV_i}, \quad (14)$$

where  $I_o$  is the output current.

### C. ZVS Condition

To achieve ZVS of the  $S_1$  and  $S_a$  switches, the energy stored in the leakage inductor  $L_\sigma$  in intervals 5 and 8 should be large enough to charge and discharge the  $C_{s1}$  and  $C_{sa}$  capacitors. This results in:

$$L_\sigma I_{\sigma\_peak}^2 \geq (C_{s1} + C_{sa}) \left( \frac{V_i}{1-D} \right)^2, \quad (15)$$

where  $I_{\sigma\_peak}$  is the peak value of the leakage current.

The dead-time between  $S_1$  and  $S_a$  is ensured to switch  $S_1$  on during interval 9. The dead-time value should be chosen in the range of the quarter of the resonant time created by the leakage inductance ( $L_\sigma$ ) and the parasitic capacitances ( $C_{s1}$ ,  $C_{sa}$ ). The dead-time can be calculated as:

$$T_{deadtime} = \frac{\pi}{2} \sqrt{L_\sigma (C_{s1} + C_{sa})}, \quad (16)$$

## III. INDUCTOR AND CAPACITOR SELECTIONS

### A. Inductance Selection

Two boost inductors are selected based on the peak-to-peak current ripple passing through to the inductors. Assuming that  $L_1 = L_2$ , the peak-to-peak inductor  $L_1$  and  $L_2$  currents are the same as:

$$\Delta I_{L1} = \Delta I_{L2} = \frac{V_{ca} - V_i}{L_1} (1-D)T = \frac{V_i}{L_1} DT \quad (17)$$

Assuming that  $I_{L1} = I_{L2} = I_i/2 = 0.5P_o/V_i$ , the required boost inductance should be:

$$L_1 = L_2 = \frac{2V_i^2 DT}{a\% P_o}, \quad (18)$$

where  $a\%$  is the inductor current ripple.

TABLE I  
SIMULATION AND EXPERIMENTS PARAMETERS

Converter Parameters	Values
Output power ( $P_o$ )	300 W
Input voltage range ( $V_i$ )	30 V ~ 50 V
Maximum source current ( $I_i$ )	10 A
Output voltage ( $V_o$ )	400 V
Inductors ( $L_1$ and $L_2$ )	370 $\mu$ H
Transformer	Turn ratio 1:2
Primary inductance	210 $\mu$ H
Leakage inductance	3 $\mu$ H
$C_a$	3.3 $\mu$ F/ 305 V
$C_1 = C_2$	82 $\mu$ F/ 400 V
$C_{s1}=C_{s2}=C_{sa}$	1 nF/ 300 V
Switching frequency	60 kHz

### B. Capacitance Selection

The  $C_a$  capacitor is designed so that one-half of the resonant time created by  $C_a$  and  $L_\sigma$  is over the turn-off time of the  $S_1$  switch. The value of  $C_a$  should be:

$$C_a > \frac{(1-D)^2 T^2}{\pi^2 L_\sigma}. \quad (19)$$

The  $C_{s2}$  capacitor is chosen so that the resonant time created by  $C_{s2}$  and  $L_\sigma$  in interval 2, as shown in Fig. 4(b), does not exceed the interval time of stage 2. The value of  $C_{s2}$  should be:

$$C_{s2} < \frac{(1-k)^2 (1-D)^2 T^2}{4\pi^2 L_\sigma}. \quad (20)$$

The output capacitors ( $C_1$  and  $C_2$ ) are selected as follows. The  $C_1$  and  $C_2$  capacitor currents are the same as and equal to the negative output current respectively when the secondary voltage of the transformer is zero, as shown in Fig. 4(d). To limit the peak-to-peak output voltage ripple by  $b\%$ , the capacitance should be:

$$C_1 = C_2 = \frac{(2D-1)T}{2b\% R}, \quad (21)$$

where  $R$  is the resistive load.

## IV. SIMULATION AND EXPERIMENTAL RESULTS

### A. Simulation Results

A PSIM simulation was used to simulate the operating principle of the proposed CDS-clamped L-type CFHB DC-DC converter. The parameters are as follow:  $L_1 = L_2 = 370 \mu$ H,  $C_a = 3.3 \mu$ F,  $C_1 = C_2 = 82 \mu$ F, and  $R = 700 \Omega$ . The drain-to-source on-resistance and body-diode threshold voltage of the MOSFETs were set to 8 m $\Omega$  and 1.3 V, respectively. The forward voltage of the diodes was set to 0.8 V. The turn ratio of the high-frequency transformer was 2. The leakage inductance and the magnetizing inductance at the primary side of the transformer were 3  $\mu$ H and 210  $\mu$ H,

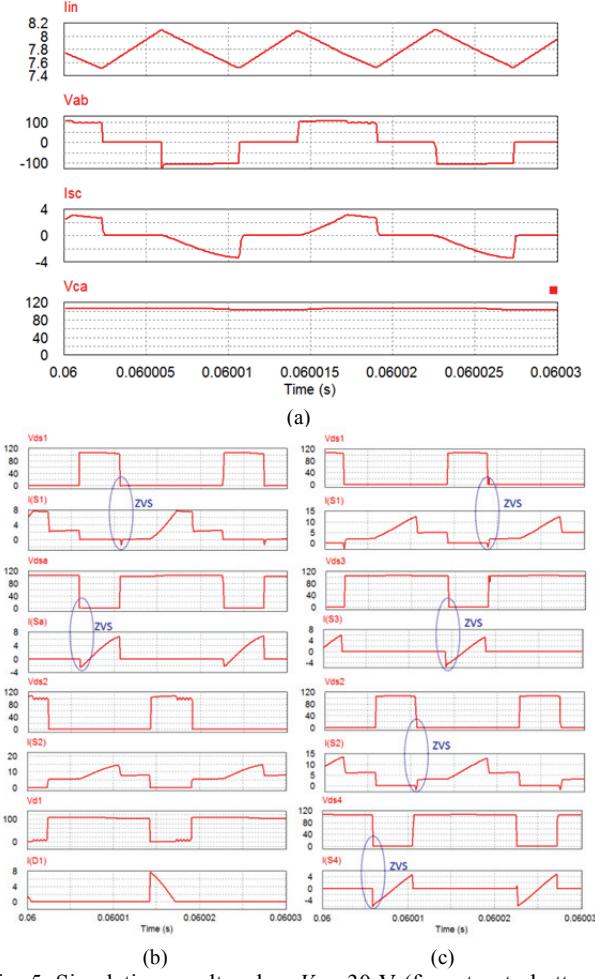


Fig. 5. Simulation results when  $V_i = 30$  V (from top to bottom): (a) Input current, primary voltage, secondary current and capacitor  $C_a$  voltage; (b) Drain-source voltage and current of  $S_1$ ,  $S_a$ ,  $S_2$  and voltage and current of diode  $D_1$  in the proposed converter; (c) Drain-source voltage and current of  $S_1$ - $S_4$  in the conventional CFHB converter.

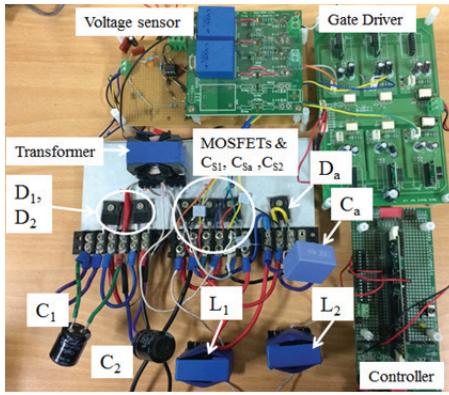


Fig. 6. Photograph of the experimental setup.

respectively. The dead-time between  $S_1$  and  $S_a$  to turn on the switches with ZVS was set to  $0.5 \mu\text{s}$ . The switching frequency was  $60 \text{ kHz}$ . The input voltage was in a range from  $30 \text{ V}$  to  $50 \text{ V}$ , and the output voltage was  $400 \text{ V}$ .

Fig. 5 shows simulation results for the proposed CDS-clamped L-type CFHB DC-DC converter when  $V_i = 30 \text{ V}$ . The input current is continuous. As shown in Fig. 5(b), the  $S_1$  and  $S_a$  switches are turned on under ZVS. The ZVS performance of the conventional CFHB is shown in Fig. 5(c) with all of the switches. These simulation results match to the theoretical analysis.

### B. Experimental Results

A  $300 \text{ W}$  laboratory prototype was constructed to verify the operating theory of the proposed CDS-clamped L-type CFHB DC-DC converter. A photograph of the prototype of the proposed converter is shown in Fig. 6. The same parameters as those used in the simulation were used in the experiment. One STPS60SM200C Schottky diode and three IRFP4668PbF MOSFETs were used on the primary side, while two DSEI30-06A diodes were used on the secondary side. The high-frequency transformer was built using a PQ40/40 core. The magnetic inductance measured from the primary side was  $210 \mu\text{H}$ . The leakage inductance measured at the primary winding by shorting the second winding was  $3 \mu\text{H}$ . The two boost  $L_1$  and  $L_2$  inductors were  $370 \mu\text{H}$ . The  $C_a$  capacitor was  $3.3 \mu\text{F}$  /  $305 \text{ V}$ . Two  $82 \mu\text{F}$  /  $400 \text{ V}$  capacitors were used for  $C_1$  and  $C_2$ . The three snubber  $C_{S1}$ ,  $C_{Sa}$  and  $C_{S2}$  capacitors were  $1 \text{nF}$  /  $300 \text{ V}$ . The dead-time between  $S_1$  and  $S_a$  was  $0.5 \mu\text{s}$ . Because the duty cycle of the current-fed half-bridge topology should be larger than  $0.5$  [15], the maximum input voltage should be  $50 \text{ V}$  when the turn ratio of the HF transformer is fixed to  $2$ . To guarantee the high efficiency of the proposed converter, the input voltage should not be less than  $30 \text{ V}$ . Hence, the input voltage range is from  $30 \text{ V}$  to  $50 \text{ V}$ .

Fig. 7 shows experimental results for the proposed converter at an output power of  $228 \text{ W}$  ( $76\%$  load) when  $V_i = 30 \text{ V}$ . The output voltage was boosted to  $400 \text{ V}$  from a  $30 \text{ V}$  input voltage. The input current is continuous with a low ripple. As shown in Figs. 7(c)-7(f), the  $S_1$  and  $S_a$  switches are turned on with ZVS, where the gating signals of the switches are applied after the voltage across them equal zero. At that time, the body-diodes of the switches are conducting before the switches begin conducting. Two rectifier  $D_1$  and  $D_2$  diodes are turned off with zero-current switching (ZCS) as shown in Fig. 7(b).

Fig. 8 shows experimental results for the proposed converter at an output power of  $30 \text{ W}$  ( $10\%$  load) when  $V_i = 30 \text{ V}$ . As shown in Fig. 8, the  $S_1$  and  $S_a$  switches are turned on with ZVS. In addition, the proposed converter was operating under the light load condition. Therefore, the current of  $S_2$  seems to equal zero when the  $S_2$  switch is turned on, and the two rectifier  $D_1$  and  $D_2$  diodes are turned off with ZCS at a  $10\%$  load.

Fig. 9 shows experimental waveforms at  $V_i = 30 \text{ V}$  when the load is suddenly changed from  $30 \text{ W}$  to  $228 \text{ W}$ . A simple

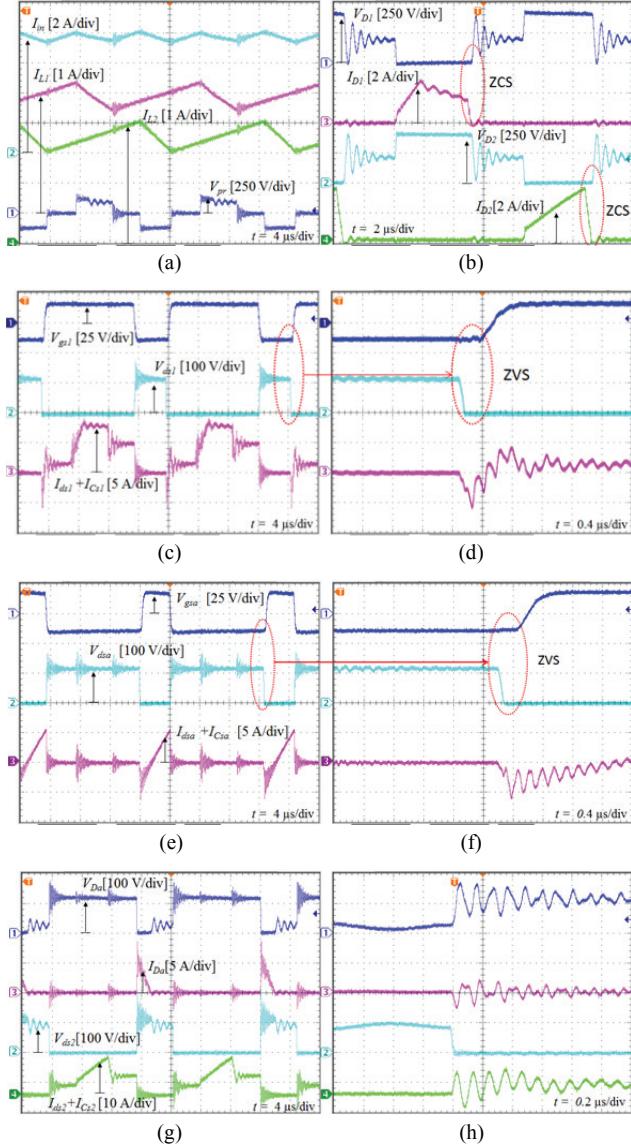


Fig. 7. Experimental waveforms for the proposed converter at an output power of 228 W when  $V_i = 30$  V (from top to bottom): (a) Input and inductor currents, and primary voltage; (b) Voltage and current of diodes  $D_1$  and  $D_2$ ; (c) Gate-source voltage, drain-source voltage and current of  $S_1$ ; (d) Enlarged waveforms of (c); (e) Gate-source voltage, drain-source voltage and current of  $S_a$ ; (f) Enlarged waveforms of (e); (g) Voltage and current of diode  $D_a$ , and drain-source voltage and current of  $S_2$ ; (h) Enlarged waveforms of (g).

TABLE II

INPUT CURRENT RIPPLE WHEN  $P_o = 228$  W

	Calculation	Simulation	Experiment
$V_i = 30$ V	7.7 %	7.8 %	8.9 %
$V_i = 40$ V	6.8 %	7.1 %	8.3 %
$V_i = 50$ V	0 %	0.1 %	2.5 %

PID controller was used in this experiment to maintain 400 V at the output. Table II shows the input current ripple of the proposed CDS-clamped converter when  $P_o = 228$  W. Since

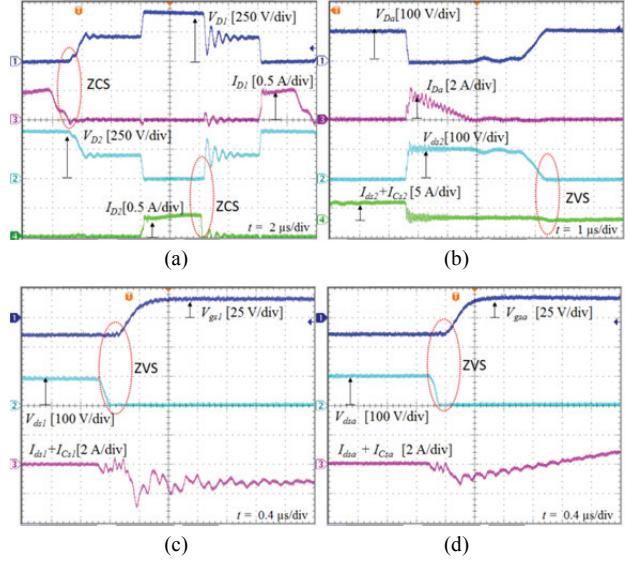


Fig. 8. Experimental waveforms for the proposed converter at an output power of 30 W when  $V_i = 30$  V (from top to bottom): (a) Voltage and current of diodes  $D_1$  and  $D_2$ ; (b) Voltage and current of diode  $D_a$ , and drain-source voltage and current of  $S_2$ ; (c) Gate-source voltage, drain-source voltage and current of  $S_1$ ; (d) Gate-source voltage, drain-source voltage and current of  $S_a$ .

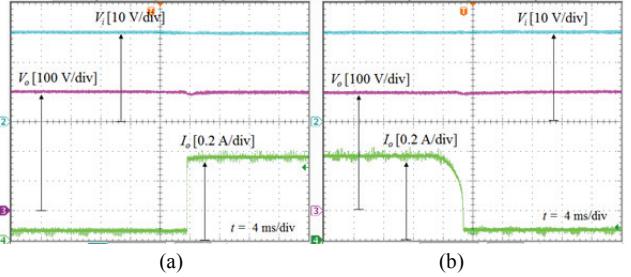


Fig. 9. Experimental waveforms with load changes: (a) From 30 W to 228 W; (b) From 228 W to 30 W (from top to bottom; input voltage, output voltage and load current).

the input current is the sum of the inductor  $L_1$  and  $L_2$  currents, the peak to peak input current ripple is calculated as [22]:

$$r_i \% = \frac{\Delta I_i}{I_i} = \frac{V_i (2D - 1)T}{L_1 I_i}. \quad (22)$$

From Table II, it can be seen that the experimental input current ripple is slightly higher than that from the calculation and simulation. This is because the values of the inductors  $L_1$  and  $L_2$  in the prototype are not exactly the same and equal to 370  $\mu$ H. Like the L-type CFHB DC-DC converter, the proposed CDS-clamped converter exhibits a low input current ripple.

Fig. 10 shows the measured efficiency of the proposed CDS-clamped converter. The power converter rating is 300 W at full load. The measured efficiency at  $V_i = 50$  V is higher than that at  $V_i = 30$  V. The maximum efficiency of the proposed CDS-clamped converter is 97.3% at 183 W (61% load) when  $V_i = 50$  V. The measured efficiency of the proposed converter

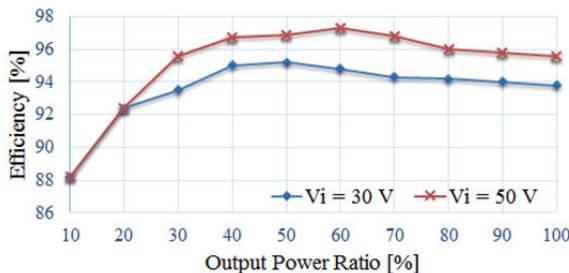


Fig. 10. Measured efficiency of the proposed CDS-clamped converter.

TABLE III  
PARAMETERS USED FOR POWER LOSS CALCULATION

MOSFETs	IRFP4668PbF (200 V, 130 A, 8 mΩ)
Diodes	$D_a$ : STPS60SM200C (200 V, 30 A) $D_1$ and $D_2$ : DSEI 30-06A (600 V, 37 A)
ESR of $C_a$ (3.3 μF/305VDC)	5.2 mΩ
ESR of $C_1, C_2$ (82 μF/450VDC)	585 mΩ
Inductor core	EER4042 (3600 nH/N <sup>2</sup> )
Transformer core	PQ40/40
Copper wire resistivity	$1.724 \cdot 10^{-6} \Omega \cdot \text{cm}$

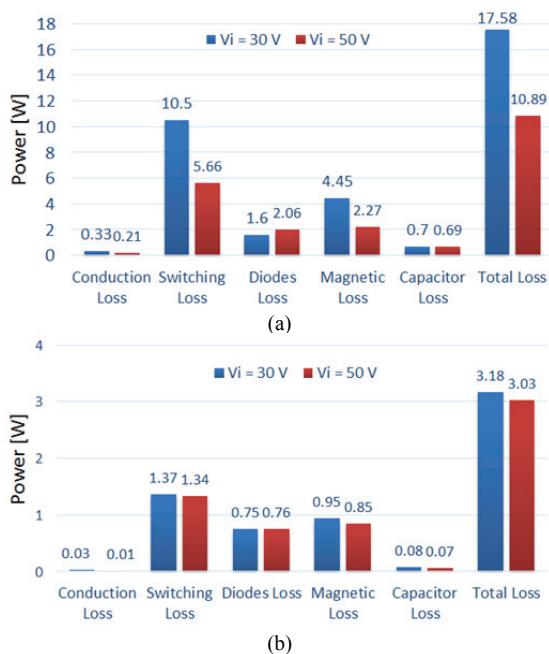


Fig. 11. Calculated power loss distribution of the proposed converter at: (a)  $P_o = 300\text{ W}$ ; (b)  $P_o = 30\text{ W}$ .

under a light load (10% load) is 88.2%. The converter efficiency can be improved by designing a printed circuit board (PCB) circuit to decrease the parasitic losses.

Figs. 11(a) and 11(b) show the power loss calculation of the proposed converter at full load (300 W) and light load (30 W), respectively. The parameters used for the power loss calculations of the two converters are listed in Table III. The

switching loss, diode loss and magnetic loss are the main contribution to the total loss of the proposed converter. Because the proposed converter operates with a high current at an output power of 300 W and an input voltage of 30 V, its power loss is significant. It is worth noting that the proposed converter can be operated at a higher power of 300 W. Because the current of the power supply in the laboratory is limited to 10 A, the experimental results at low power were shown to validate the operating principle of the proposed converter.

## V. CONCLUSION

An active CDS-clamped L-type current-fed isolated DC-DC converter was proposed in this paper. The major advantages of the proposed converter are as follows: 1) the two switches operate under ZVS with a wider power range; 2) the input current ripple is low; 3) one active switch and its insulated gate drive circuit are saved; and 4) the efficiency is high. The operating modes, analysis, and design considerations for the proposed converter as well as simulation results are presented. A 300 W laboratory prototype was built to verify the operating theory of the proposed converter. The proposed converter is suitable for fuel cell applications where a varying low dc input voltage is converted to a high stabilized DC output voltage with continuous source current and galvanic separation requirements.

## REFERENCES

- [1] W. Li and X. He, "Review of nonisolated high-step-up dc/dc converters in photovoltaic grid-connected applications," *IEEE Trans. Ind. Electron.*, Vol. 58, No. 4, pp. 1239-1250, Apr. 2011.
- [2] M. Muhammad, M. Armstrong, and M. A. Elgendi, "A nonisolated interleaved boost converter for high-voltage gain application," *IEEE J. Emerg. Sel. Topics Power Electron.*, Vol. 4, No. 2, pp. 352-362, Jun. 2016.
- [3] F. Z. Peng, H. Li, G.-J. Su, and J. S. Lawler, "A new ZVS bidirectional dc-dc converter for fuel cell and battery application," *IEEE Trans. Power Electron.*, Vol. 19, No. 1, pp. 54-65, Jan. 2004.
- [4] J. C. Hernandez, M. C. Mira, G. Sen, O. C. Thomsen, and M. A. E. Andersen, "Isolated boost converter with bidirectional operation for supercapacitor applications," *J. Power Electron.*, Vol. 13, No. 4, pp. 507-515, Jul. 2013.
- [5] H. Wu, K. Sun, L. Zhu, and Y. Xing, "An interleaved half-bridge three-port converter with enhanced power transfer capability using three-leg rectifier for renewable energy applications," *IEEE J. Emerg. Sel. Topics Power Electron.*, Vol. 4, No. 2, pp. 606-616, Jun. 2016.
- [6] H. Lee, H.-G. Kim, H. Cha, T.-W. Chun, and E.-C. Nho, "Coupled inductor-based parallel operation of a qZ-Source full-bridge DC-DC converter," *J. Power Electron.*, Vol. 15, No. 1, pp. 1-9, Jan. 2015.
- [7] S. Jalbrzykowski and T. Citko, "Current-fed resonant

- full-bridge boost dc/ac/dc converter,” *IEEE Trans. Ind. Electron.*, Vol. 55, No. 3, pp. 1198-1205, Mar. 2008.
- [8] I. O. Lee, “A hybrid PWM-resonant DC-DC converter for electric vehicle battery charger applications,” *J. Power Electron.*, Vol. 15, No. 5, pp. 1158-1167, Sep. 2015.
- [9] P. Xuewei and A. K. Rathore, “Novel bidirectional snubberless naturally commutated soft-switching current-fed full-bridge isolated dc/dc converter for fuel cell vehicles,” *IEEE Trans. Ind. Electron.*, Vol. 61, No. 5, pp. 2307-2315, May 2014.
- [10] M. Nymand and M. A. E. Andersen, “High-efficiency isolated boost dc–dc converter for high-power low-voltage fuel-cell applications,” *IEEE Trans. Ind. Electron.*, Vol. 57, No. 2, pp. 505-514, Feb. 2010.
- [11] A. Mousavi, P. Das, and G. Moschopoulos, “A comparative study of a new ZCS dc–dc full-bridge boost converter with a ZVS active-clamp converter,” *IEEE Trans. Power Electron.*, Vol. 27, No. 3, pp. 1347-1358, Mar. 2012.
- [12] U. R. Prasanna and A. K. Rathore, “Extended range ZVS active-clamped current-fed full-bridge isolated dc/dc converter for fuel cell applications: analysis, design, and experimental results,” *IEEE Trans. Ind. Electron.*, Vol. 60, No. 7, pp. 2661-2672, Jul. 2013.
- [13] Z. Ouyang, G. Sen, O. C. Thomsen, and M. A. E. Andersen, “Analysis and design of fully integrated planar magnetics for primary-parallel isolated boost converter,” *IEEE Trans. Ind. Electron.*, Vol. 60, No. 2, pp. 494-508, Feb. 2013.
- [14] P. J. Wolfs, “A current-sourced DC-DC converter derived via the duality principle from the half-bridge converter,” *IEEE Trans. Power Electron.*, Vol. 40, No. 1, pp. 139-144, Feb. 1993.
- [15] S. K. Han, H.-K. Yoon, G.-W. Moon, M.-J. Youn, Y.-H. Kim, and K.-H. Lee, “A new active clamping zero-voltage switching PWM current fed half-bridge converter,” *IEEE Trans. Power Electron.*, Vol. 20, No. 6, pp. 1271-1279, Nov. 2005.
- [16] A. K. Rathore, A. K. S. Bhat, and R. Oruganti, “Analysis, design and experimental results of wide range ZVS active-clamped L-L type current-fed dc/dc converter for fuel cells to utility interface,” *IEEE Trans. Ind. Electron.*, Vol. 59, No. 1, pp. 473-485, Jan. 2012.
- [17] S. J. Jang, C. Y. Won, B. K. Lee, and J. Hur, “Fuel cell generation system with a new active clamping current-fed half-bridge converter,” *IEEE Trans. Energy Convers.*, Vol. 22, No. 2, pp. 332-340, Jun. 2007.
- [18] H. Xiao and S. Xie, “A ZVS bidirectional dc–dc converter with phase-shift plus PWM control scheme,” *IEEE Trans. Power Electron.*, Vol. 23, No. 9, pp. 813-823, Mar. 2008.
- [19] J. M. Kwon and B. H. Kwon, “High step-up active-clamp converter with input-current doubler and output-voltage doubler for fuel cell power systems,” *IEEE Trans. Power Electron.*, Vol. 24, No. 1, pp. 108-115, Jan. 2009.
- [20] S. A. Teston, E. G. Carati, J. P. da Costa, R. Cardoso, and C. M. de Oliveira Stein, “Comparison of two connection possibilities of the clamp capacitor in the active-clamped ZVS current-fed half-bridge converter” in *Proc. IEEE COBEP/SPEC*, pp. 1-6, 2015.
- [21] U. R. Prasanna and A. K. Rathore, “Current-fed interleaved phase-modulated single-phase unfolding inverter: analysis, design, and experimental results,” *IEEE Trans. Ind. Electron.*, Vol. 61, No. 1, pp. 310-319, Jan. 2014.
- [22] C. Yoon, J. Kim, and S. Choi, “Multiphase dc–dc converters using a boost-half-bridge cell for high-voltage and high-power applications,” *IEEE Trans. Power Electron.*, Vol. 26, No. 2, pp. 381-388, Feb. 2011.
- [23] M. K. Nguyen, Y. C. Lim, J. H. Choi, and G. B. Cho, “Isolated high step-up dc–dc converter based on quasi-switched-boost network,” *IEEE Trans. Ind. Electron.*, Vol. 63, No. 12, pp. 7553-7562, Dec. 2016.



**Minh-Khai Nguyen** (S’09–M’12) received his B.S. degree in Electrical Engineering from the Ho Chi Minh City University of Technology, Ho Chi Minh City, Vietnam, in 2005; and his M.S. and Ph.D. degrees in Electrical Engineering from Chonnam National University, Gwangju, South Korea, in 2007 and 2010, respectively. He was a Lecturer at the Ho Chi Minh City University of Technology and Education, Ho Chi Minh City, Vietnam. He is presently working as an Assistant Professor at Chosun University, Gwangju, South Korea. His current research interests include impedance-source inverters and power converters for renewable energy systems.



**Truong-Duy Duong** received his B.S degree in Electronic Telecommunication Engineering from the Ho Chi Minh City University of Technology and Education, Ho Chi Minh City, Vietnam, in 2015 and his M.S. degree in Electrical Engineering from Chonnam National University, Gwangju, South Korea, in 2018. He is presently working towards his Ph.D. degree in the Department of Electrical Engineering, Chonnam National University, Gwangju, South Korea. His current research interests include the topologies and control of dc–dc converters and dc–ac inverters.



**Young-Cheol Lim** (M’85) was born in Jeollanam-do, South Korea, in 1953. He received his B.S. degree in Electrical Engineering from Chonnam National University, Gwangju, South Korea, in 1975; and his M.S. and Ph.D. degrees in Electrical Engineering from Korea University, Seoul, South Korea, in 1977 and 1990, respectively. In 1981, he became a Professor at Chonnam National University, where he was the Director of the Research Center for High-Quality Electric Components and Systems from 1998 to 2007. He is the coauthor of three books. He has authored or coauthored more than 200 published technical papers. His current research interests include power electronics, control instruments and neuro-fuzzy control. Dr. Lim was the President of Korea Institute of Power Electronics (KIPE), in 2009. He has been involved in various academic societies, such as the KIPE, the Korean Institute of Electrical Engineers (KIEE), and the Institute of Control, Automation and Systems Engineers, South Korea. He has received a number of awards, including a 2000 KIPE Best Paper Award and a 2001 KIPE Academic Award.



**Joon-Ho Choi** (S'98-M'02) received his B.S., M.S. and Ph.D. degrees in Electrical Engineering from Soongsil University, Seoul, South Korea, in 1996, 1998 and 2002, respectively. Since 2003, he has been a Professor at Chonnam National University, Gwangju, South Korea. His current research interests include the operation, integration and control strategies of distributed generation, distribution automation, and the modelling and operation algorithms for smartgrids. Dr. Choi is a Life Member of the KIEE and The Korean Institute of Illuminating and Electrical Installation Engineers, and a Committee Member of IBS Korea. Since 2004, he has been an Associate Editor of the Transactions of the KIEE.