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New Generalized SVPWM Algorithm for Multilevel Inverters

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Abstract

In this paper a new generalized space vector pulse width modulation scheme is proposed based on the principle of reverse mapping to drive the switches of multilevel inverters. This projected scheme is developed based on the middle vector of the subhexagon which holds the tip of the reference vector, which plays a major role in mapping the reference vector. A new approach is offered to produce middle vector of the subhexagon which holds tip of the reference vector in the multilevel space vector plane. By using middle vector of the subhexagon, reference vector is linked towards the inner two level sub-hexagon. Then switching vectors, switching sequence and dwell times corresponding to a particular sector of a two-level inverter are determined. After that, by using the two level stage findings, the switching vectors related to exact position of the reference vector are directly generated based on principle of the reverse mapping approach and do not need to be found at n level stage. In the reverse mapping principle, the middle vector of subhexagon is added to the formerly found two level switching vectors. The proposed generalized algorithm is efficient and it can be applied to an inverter of any level. In this paper, the proposed scheme is explained for a five-level inverter and the performance is analyzed for five level and three level inverters through MATLAB. The simulation results are validated by implementing the propose scheme on a V/f controlled three-level inverter fed induction motor using dSPACE control desk.

Key words: Diode clamped MLI, Generalized SVPWM algorithm, MLI, Modified SVPWM, SVPWM

I. INTRODUCTION

In recent years, multi-level inverters (MLIs) have become the most popular choice for use in moderate to high power applications [1]-[3], due to their significantly lower semiconductor voltage stress, superior harmonic performance and reduced switching losses. MLIs can be categorized into neutral point diode clamped (NPC), capacitor clamped and cascaded MLIs. The NPC inverters are ideal due to the advantages of the single bus utilization and ease of control [4]. Other researchers have focused their concentration on different pulse width-modulation (PWM) methods for MLIs since the output performance of MLIs depends on type of PWM technique used. The carrier based sine PWM (SPWM) and space vector PWM (SVPWM) are the most popular schemes [5]-[8]. The SVPWM became popular since it can produce an output with a low harmonic distortion, greater flexibility in terms of switching sequence selection and favorable digital implementation [6]-[8]. However, the SVPWM approach involves vast, tedious calculations such as sectors/subsector identification, switching time calculation and optimum switching vector sequence selection.

So far, various approaches [6]-[26] have been proposed to implement SVPWM for MLIs. Among these, [6]-[10] and [20] were developed based on two-level space vector concept. They tend to involve complicated computations as number of levels increases. The algorithms in [11]-[13], [16], [17], and [21] were developed based on the decomposition principle. A simple SVPWM approach was presented in [14], which involves huge calculations. The authors of [18]-[19] proposed introducing an offset vector. The identification of the position of the offset vector is required to identity subsectors. However,

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this is difficult, and increases as the number of levels increases. In [22], [23] carrier based SVPWM is proposed, which is not involved direct digital implementation. In [24], [25] a SVPWM is proposed by transferring the normal reference frame into a 60^0 alignment, which involves mathematical complexity in dwell time calculations. The algorithm proposed in [26] involves mathematical equations. In all these schemes, the complexity involved and memory requirements increase with an increase in the output voltage levels. This makes the implementation of the SVPWM scheme quite expensive. An author presented a simplified algorithm [15] based on integer/fractional part decomposition, which is quite simple. An extension of this algorithm to produce all possible switching states including redundant switching states is presented in [27]. However, this does involve intense mathematical computations. In addition, extending this to different bus clamping and advanced bus clamping PWM methods is quite challenging.

In this article, a new generalized SVPWM approach is proposed to drive the switches of multilevel inverters. Switching vector recognition, switching sequence generation with all of the necessary redundant switching states and dwell time computation are done only at a two level stage, and may or may not need information on the exact position of the reference vector in the multilevel space vector plane (SVP). In addition, this approach can be easily extended to different bus clamping and advanced bus clamping SVPWM methods to further enhance the performance of the inverter.

This method is quite simple and involves few mathematical reckonings for the mapping and reverse mapping of vectors and it does not require any lookup tables when compared to the existing SVPWM strategies. Further, this SVPWM algorithm can be applicable for inverters of any level. In this paper, the proposed scheme is explained for five-level inverter and performance is analyzed for five level and three level inverters through MATLAB. In addition, performance is validated by implementing it on a V/f controlled three-level inverter fed induction motor using dSPACE control desk.

This article is organized as follows. The proposed approach is explained in Section II. Simulation results are illustrated in Section III. Experimental results are illustrated in Section IV. Finally, some conclusions are given in Section V.

II. Proposed Approach

The SVP of a five-level inverter is shown in Fig 1. For the sake of simplicity, the redundant vectors are not revealed. This SVP can be viewed in form of small sub-hexagons. They are inner subhexagon and higher level subhexagon (HLS) which contains tip of the reference vector (V_{ref}). These two sub-hexagons can be treated as SVP of a two-level inverter. However, the voltage vectors of inner subhexagon are switch between the lowermost levels and voltage vectors of HLS are switch between higher level voltages.

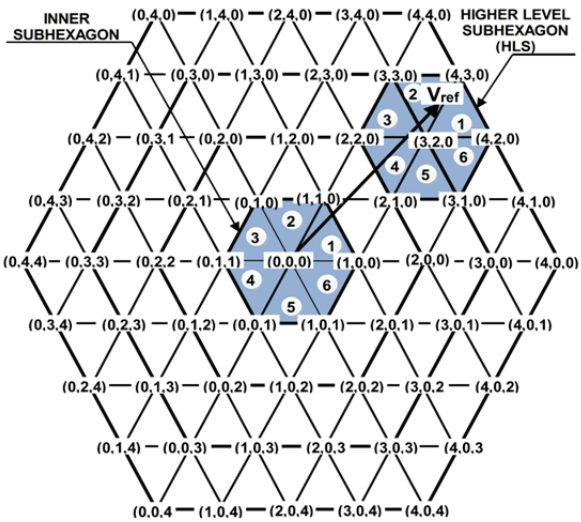


Fig. 1. Space vector plain of a five level inverter.

In this projected technique, the higher level voltage vector V_{ref} is simplified in to a two level hexagon by the principle of mapping. After mapping of V_{ref} to the inner subhexagon, the switching vectors recognition, switching sequence generation and dwell time computation corresponding to the sector of a two-level inverter is done using imaginary switching concept. Then these two level findings are translated into the switching states of the HLS by using reverse mapping approach. This complete approach is developed mainly based on the middle vector of the HLS and it plays a major role in mapping the subhexagon.

A simplified procedure is presented in this paper to recognize the middle vector of the subhexagon, which contains the tip of V_{ref}. Based on this, a new generalized SVPWM algorithm is to be developed in this article. The steps involved in implementing this algorithm can be explained with the help of Fig. 2.

A. 3-Φ to 2-Φ Voltage Conversion

The first instantaneous three phase input voltages are:

$$v_x = V_m \cos \omega t \tag{1}$$

$$v_y = V_m \cos\left(\omega t - \frac{2\pi}{3}\right) \tag{2}$$

$$v_z = V_m \cos\left(\omega t - \frac{4\pi}{3}\right) \tag{3}$$

These instantaneous 3-Φ input voltages are converted into instantaneous 2-Φ voltages by using transformation matrix (4).

$$\begin{pmatrix} V_{ref\_\alpha} \\ V_{ref\_\beta} \end{pmatrix} = \frac{2}{3}\begin{pmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{pmatrix}\begin{pmatrix} v_x \\ v_y \\ v_z \end{pmatrix} \tag{4}$$

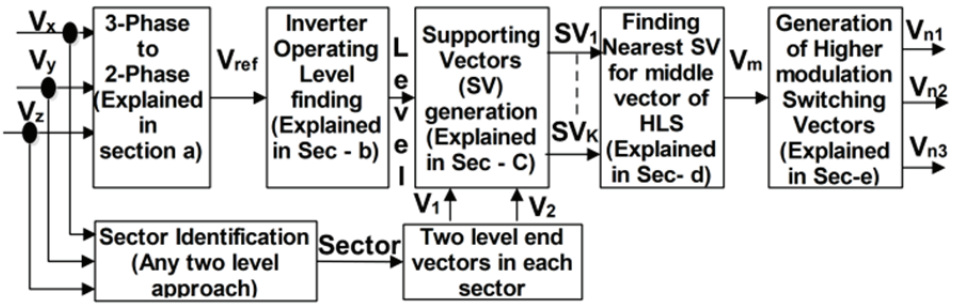


Fig. 2. Steps involved in the proposed SVPWM algorithm.

Using expression (4), the instantaneous magnitude of "V_{ref}" is synthesized by following expression (5).

$$V_{ref} = \sqrt{\left(V_{ref\_\alpha}\right)^2 + \left(V_{ref\_\beta}\right)^2} \tag{5}$$

B. Identifying the Operating Level of an Inverter

An n-level inverter can be driven to work in any level between two to "n" by controlling the modulation index (M). Hence, the SVP of a five level inverter can be viewed since it is operated in different levels. There are two level, three level, four level and five level, and these are represented by L=2, L=3, L=4 and L=5 as shown in Fig. 3. These operating levels can be easily identified based on the magnitude tip of the revolving vector V_{ref}. When the tip of V_{ref} is revolves in the region surrounded by a two level hexagon, the inverter is operated in two level (L=2). When the tip of V_{ref} is revolving in the region between a two level hexagon and a three level hexagon, the inverter can be operated in three level (L=3). Similarly, the remaining operating levels are identified based on the magnitude tip of the revolving vector V_{ref}.

The operating level of MLI can be easily obtained by using the following expression (6). Let the maximum length of n-level voltage vector along 0^0 axes is V_{dc} and modulation index of each level is M.

$$L = 2 + \text{integer}\left(\frac{V_{ref}}{M}\right) \tag{6}$$

The M of each level can be obtained easily by using expression (7).

$$M = \left(\frac{V_{dc}}{n-1}\right) \tag{7}$$

C. Supporting Vectors Generation

As stated previously, the SVP of five-level is in the form of an inner subhexagon with (0,0,0) as the middle vector and HLS which holds the tip of the vector V_{ref}. However, the position of this HLS is not fixed. It varies based on the magnitude and position of the revolving vector V_{ref}. The various locations of the HLS, when V_{ref} is revolving in sector

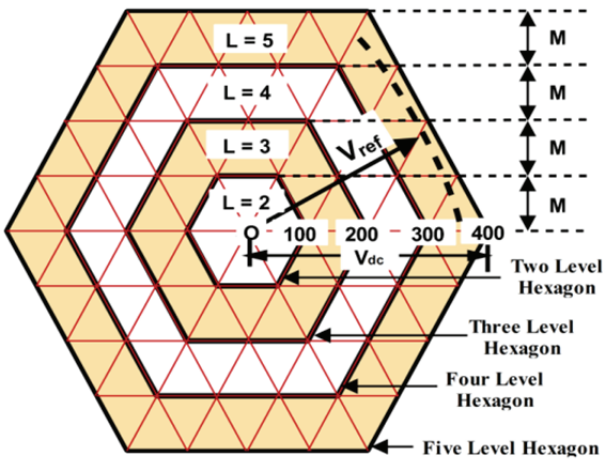


Fig. 3. Inverter operating levels.

1 of the five level operation are shown in Fig. 4, with shaded regions for ease of recognition. In these vectors (3,0,0), (3,1,0), (3,2,0) and (3,3,0) are lying just below the V_{ref} revolving in five level operation. Among them, one vector which is nearest to the tip of the V_{ref} is acts as the middle vectors of HLS. Since the reference vector is revolving, each vector acts as a middle vector of the HLS at any one instance based on the position of V_{ref}. Hence these vectors are most suitable as the middle vector of HLS in sector 1. Similarly, in all of the other sectors, the vectors lying just below the V_{ref} revolving in five level operation are most suitable for middle vector of HLS in the respective sector.

The vectors which are most suitable to act as middle vector of HLS in each sector are called supporting vectors. Therefore, the middle vector of the HLS positions shown in Fig. 4 are recognized as supporting vectors of the sector 1 of five level operation. Similarly for any n-level inverter, the vectors that are lying just below the vector V_{ref} revolving in the level "L" act as middle vectors in different positions of HLS, and these are called supporting vectors of particular sector. These supporting vectors in each sector are directly generated with the help of the operating level of the inverter and two level two input vectors, by using simple procedure, there is no need to store this in look up tables. The supporting vectors generation when V_{ref} is revolving in five-level

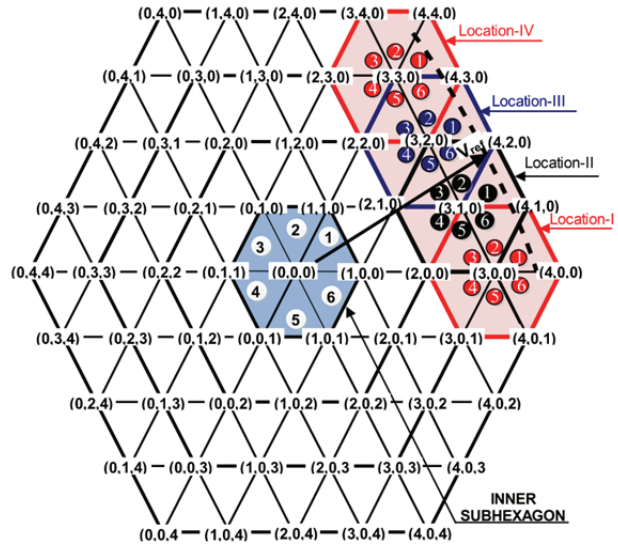


Fig. 4. Different locations of HLS.

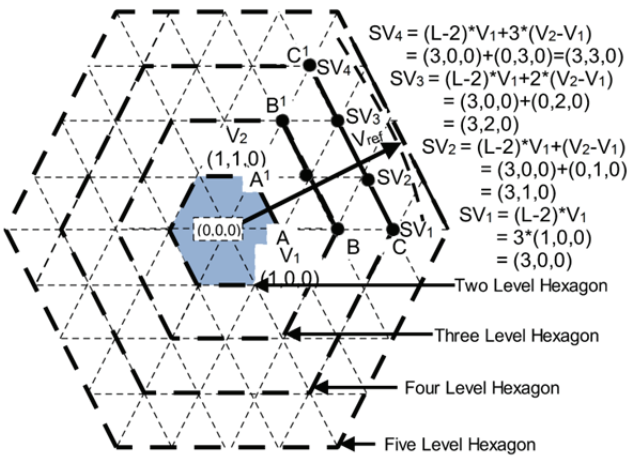


Fig. 5. Supporting vectors generation.

operation of sector 1 are shown in Fig. 5. In this case, the lines AA^1, BB^1 and CC^1 are parts of 2 level, 3 level and 4 level hexagons, respectively. It may also be noted that part AA^1, contains two, two level vectors V_1 and V_2. These vectors are specified as input vectors related to sector 1. Part CC^1 contains supporting vectors of five level operation.

The number of supporting vectors "K" in each sector are determined by using the following expression.

$$K = L - 1 \tag{8}$$

Among them, the first supporting vector for any level of operation is generated by multiplying the first two level input vector V_1 by L-2. After that, the remaining supporting vectors are generated by repetitively adding the two input vectors difference to the first supporting vector.

Therefore, the supporting vectors of each sector lying just below a particular level of operation are generated by using the following matrix equation (9).

$$\begin{pmatrix} SV_1 \\ SV_2 \\ \vdots \\ SV_{K-1} \\ SV_K \end{pmatrix} = \begin{pmatrix} (L-2)V_1 \\ (L-2)V_1 + (1)(V_2 - V_1) \\ \vdots \\ (L-2)V_1 + (K-2)(V_2 - V_1) \\ (L-2)V_1 + (K-1)(V_2 - V_1) \end{pmatrix} \tag{9}$$

Where SV_k indicates K^{th} supporting vector.

D. Identifying the Nearest Supporting Vector for the Middle Vector of the HLS

After generating of all the supporting vectors related to each sector, the nearest vector to the tip of the V_{ref} need to identify. This can be done by calculating the distance "d" of each supporting vector from V_{ref} by using the following matrix equation (10).

$$\begin{pmatrix} d_1 \\ \vdots \\ d_K \end{pmatrix} = \begin{pmatrix} \left|V_{ref\_\alpha} - SV_{1\_\alpha}\right| + \left|V_{ref\_\beta} - SV_{1\_\beta}\right| \\ \vdots \\ \left|V_{ref\_\alpha} - SV_{K\_\alpha}\right| + \left|V_{ref\_\beta} - SV_{K\_\beta}\right| \end{pmatrix} \tag{10}$$

Where (V_{ref_α}, V_{ref_β}) and (SV_{k_α}, SV_{k_β}) are the coordinates of V_{ref} and k^{th} supporting vector, respectively. Among them, the vector that has the smallest distance "d" is chosen as the middle vector of the HLS that contains the tip of V_{ref}.

E. Higher Modulation Switching Vector Generation

In the projected method, the HLS which holds the tip of V_{ref} is mapped to the inner subhexagon, which involves mapping of sector related to V_{ref} of HLS to the inner subhexagon. This is done by subtracting the middle vector (V_m) of HLS from the vector V_{ref}. The resultant vector V_z is mapped into inner subhexagon as mapped reference vector (V_{ref_m}) as shown in Fig. 6.

After mapping of V_{ref} to the inner subhexagon, the coordinates ($V_{ref\_m\alpha}$, $V_{ref\_m\beta}$) of this mapped vector V_{ref_m} are found by using by using the following expression (11).

$$\begin{aligned} V_{ref\_m\alpha} &= V_{ref\_\alpha} - V_{m\_\alpha} \\ V_{ref\_m\beta} &= V_{ref\_\beta} - V_{m\_\beta} \end{aligned} \tag{11}$$

Where (V_{ref_α}, V_{ref_β}) and (V_{m_α}, V_{m_β}) are the coordinates of V_{ref} and V_m, respectively.

Since the inner subhexagon is treated conceptually as two levels inverter, the nearest three adjacent vectors, switching sequence generation and dwell time computation corresponding to the vector V_{ref_m} of inner subhexagon are distinguished by using any two level CSVPWM.

Then these two level vector findings are translated to the vectors of a higher level subhexagon by using reverse mapping approach. This involves adding vector V_m of HLS to the previously generated two level vectors. If V_{21}, V_{22}, V_{23} and V_{24} are the nearest adjacent switching vectors related to the two level inner subhexagon, the n-level switching vectors

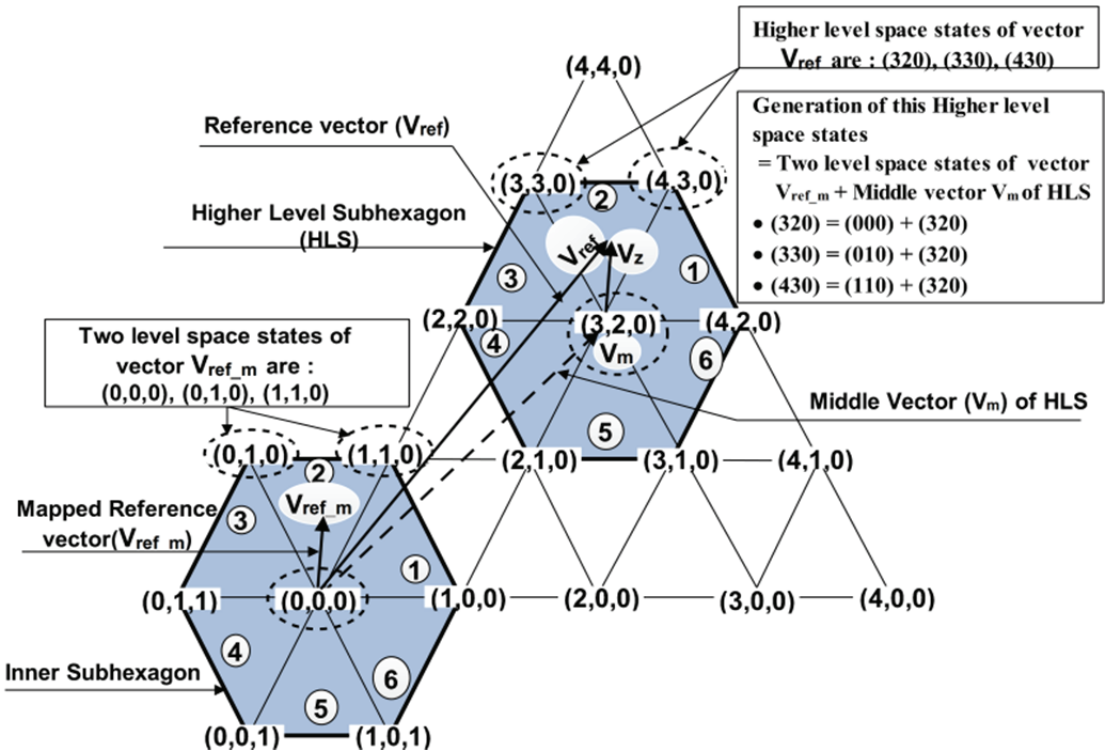


Fig. 6. Higher level voltage vector generation.

related to the exact position of V_{ref} are found by using the resultant matrix equation (12).

$$\begin{pmatrix} V_{n1} \\ V_{n2} \\ V_{n3} \end{pmatrix} = \begin{pmatrix} V_{21} \\ V_{22} \\ V_{23} \end{pmatrix} + \begin{pmatrix} V_m \\ V_m \\ V_m \end{pmatrix} \quad (12)$$

The generation of higher level voltage switching vectors based on reverse mapping principle, is depicted in Fig.5. Therefore, in the projected principle, lookup tables are not used to generate actual switching vectors and the exact position of reference vector need not to be identified. The actual switching vectors to be switched and the optimum sequence are automatically generated. For example, consider the five level inverter in sector 1 and redrawn as Fig. 6.

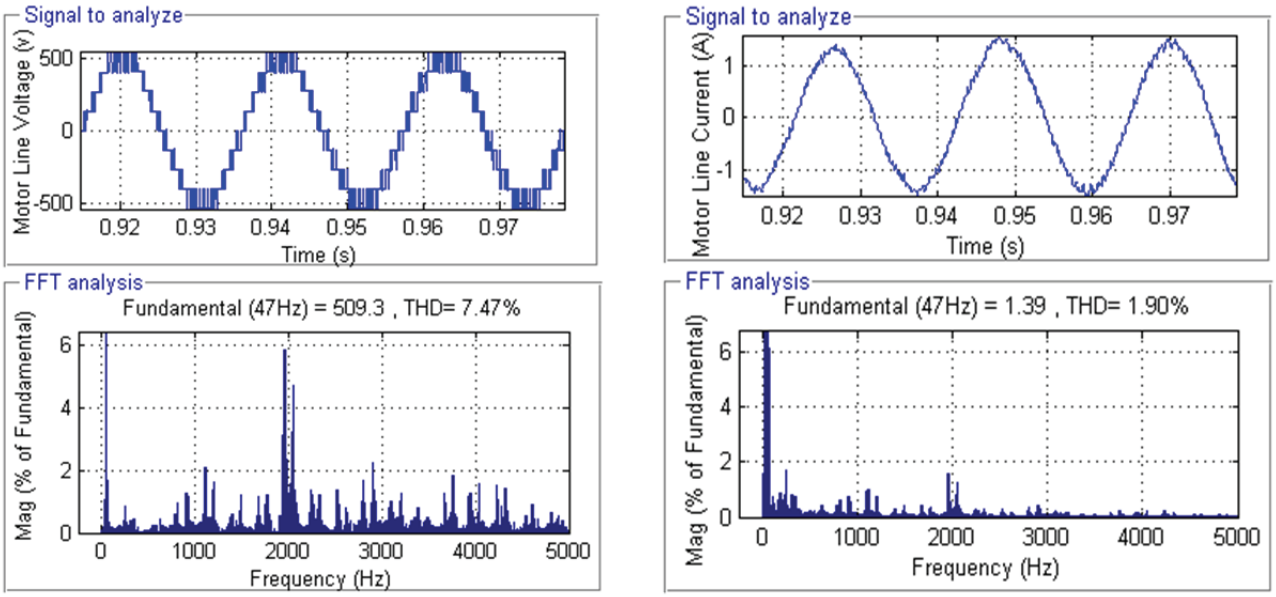
In this, the tip of the instantaneous V_{ref} lies in sector 2 of the HLS. The reference vector is mapped to sector 2 of the inner subhexagon as V_{ref_m} by subtracting the vector V_m from the vector V_{ref}. Then the nearest three adjacent vectors (0,0,0), (0,1,0) and (1,1,0) related to the sector of mapped vector V_{ref_m} are generated. After finding the two level voltage vectors, the higher level voltage vectors related to the exact position of V_{ref} are generated by using reverse mapping principle. This involves adding of the two level voltage vectors into the middle vector (3,2,0) of HLS. This gives vectors of (3,2,0=0,0,0+3,2,0), (3,3,0=0,1,0+3,2,0), and (4,3,0=1,1,0+3,2,0), which are the vectors associated with sector 2 of HLS which contains the tip of V_{ref}. Similarly, the vectors related to the exact position of V_{ref} at any instant of all the sectors are directly generated by using two level findings for any n level inverter.

III. Simulation Results

The performance of new generalized SVPWM algorithm with a switching sequence of 0127 is verified by using MATLAB/Simulink. The sampling frequency considered in this algorithm is 2000Hz. The simulation is conducted on volts/Hz controlled five level and three level inverter fed induction motor at no load without filters. Simulation waveforms of the motor line voltage and the motor no load line current along with their related THD's are presented at different fundamental frequencies of 47Hz (higher modulation level), 33Hz (medium modulation level) and 20Hz (lower modulation level).

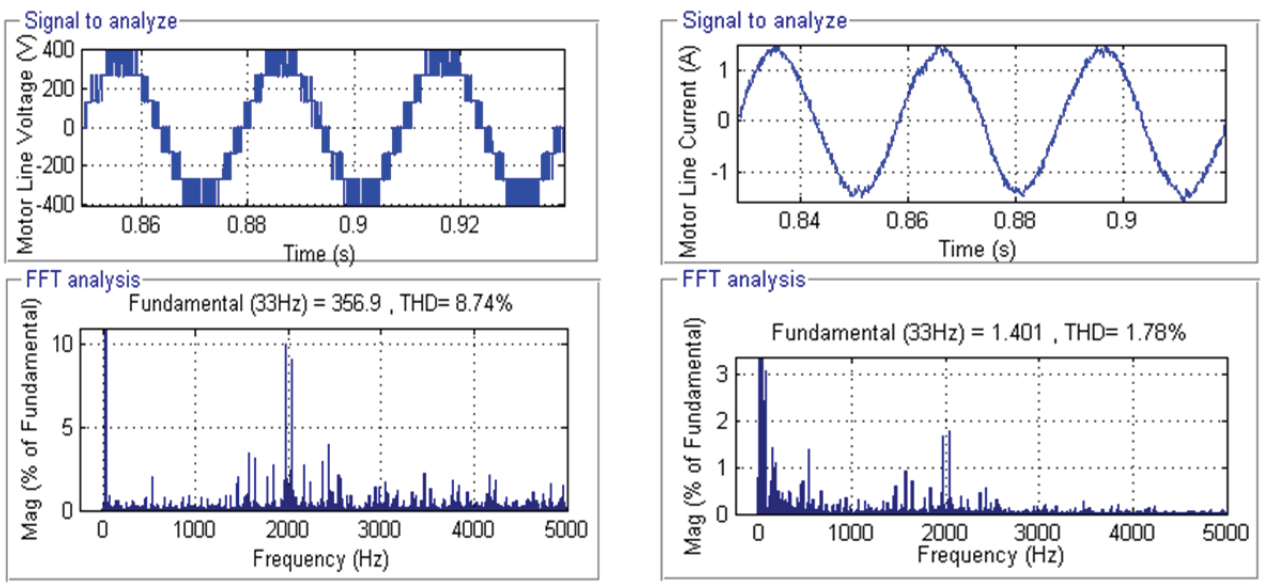
Fig. 7 and Fig. 8 shows simulation result of V/F controlled five level inverter fed induction motor at frequencies of 47Hz and 33Hz, respectively. Fig. 7(a)-(b) shows motor line voltage waveform and line current waveforms with their relative THDs at a frequency of 47Hz.

Fig. 8(a)-(b) show motor line voltage waveforms and line current waveforms with their relative THDs at a frequency of 33Hz. From Fig. 8(a) it can be observed that at a lower modulation frequencies of 33Hz, a five level inverter produces only four levels in the output line voltage with an increased THD.



(a) (b)

Fig. 7. Five level simulation waveforms at a frequency of 47Hz: (a) Motor line voltage waveform with THD; (b) Motor no-load line current waveform with the THD.

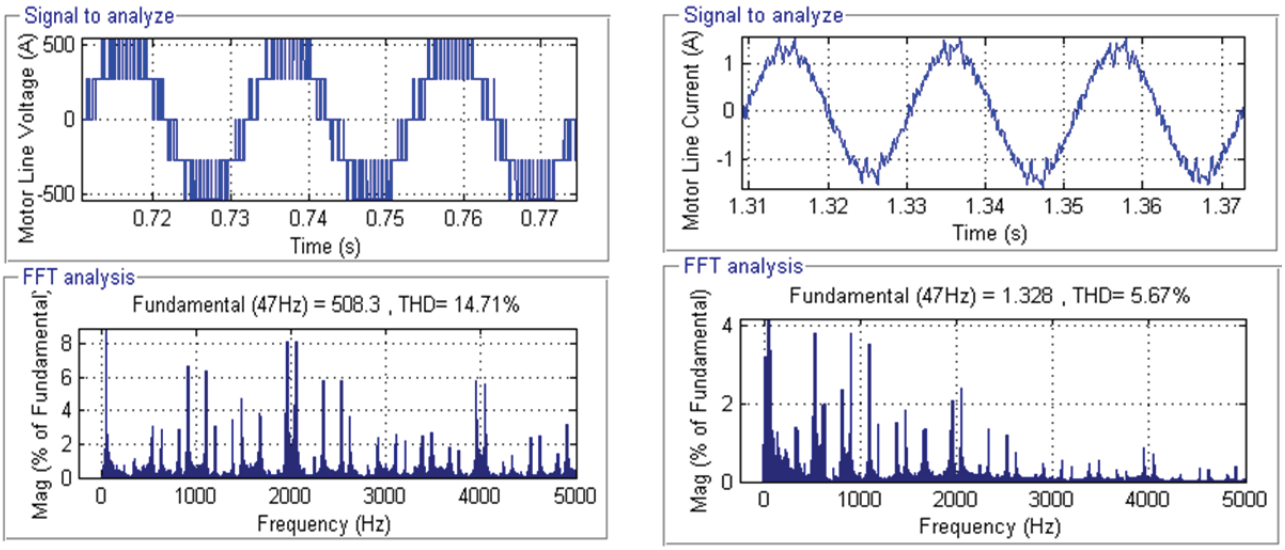


(a) (b)

Fig. 8. Five level simulation waveforms at a frequency of 33Hz: (a) Motor line voltage waveform with THD; (b) Motor no-load line current waveform with THD.

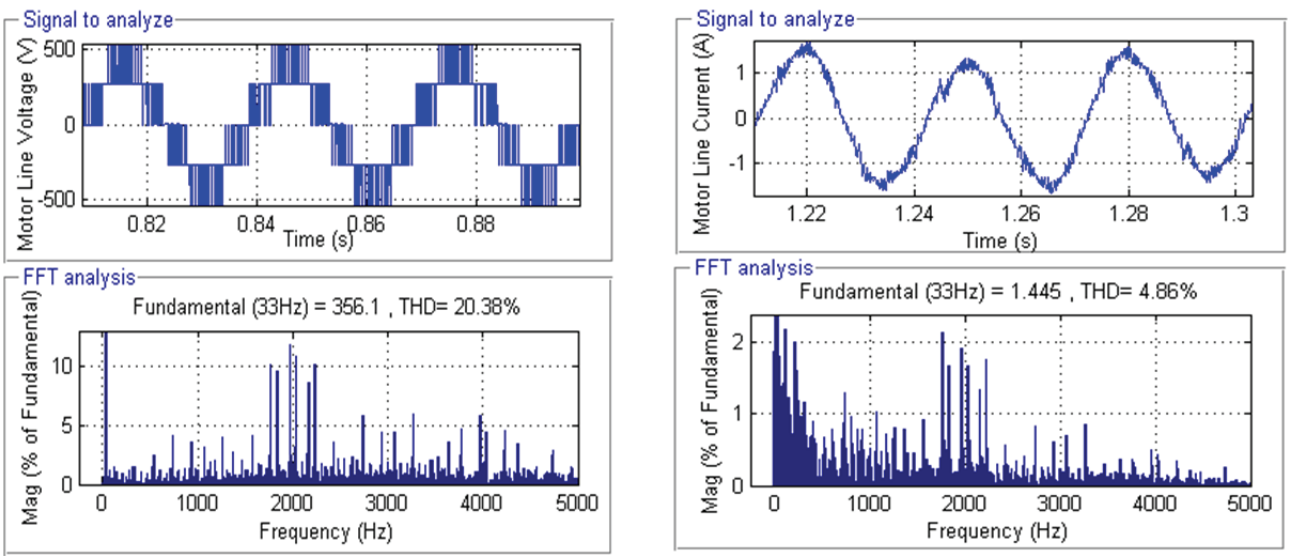
Fig. 9 and Fig. 10 shows simulation results of a V/F controlled three level inverter fed induction motor at frequencies of 47Hz and 33Hz, respectively. Fig. 9(a)-(b) shows motor line voltage waveforms and line current waveforms with their relative THDs at a frequency of 47Hz. Fig. 10(a)-(b) shows motor line voltage waveforms and line current waveforms with their relative THDs at a frequency of 33Hz. Fig.10 specifies the motor line voltage and line current THD at a frequency of 20Hz.

From Fig. 11(a) it can be observed that at lower modulation frequencies of < 25Hz, a three level inverter produces only two levels in the output line voltage with an increased THD. From the THD spectrum of the simulated waveforms, the harmonic dominance is observed at frequencies of 1000Hz and 2000Hz, which are integral multiples of the sampling frequency. The higher frequency harmonics are easily eliminated by using small filter components. Therefore, the performance of the inverter is improved by increasing the sampling frequency.



(a) (b)

Fig. 9. Three level simulation waveforms at a frequency of 47Hz: (a) Motor line voltage waveform with THD; (b) Motor no-load line current waveform with THD.



(a) (b)

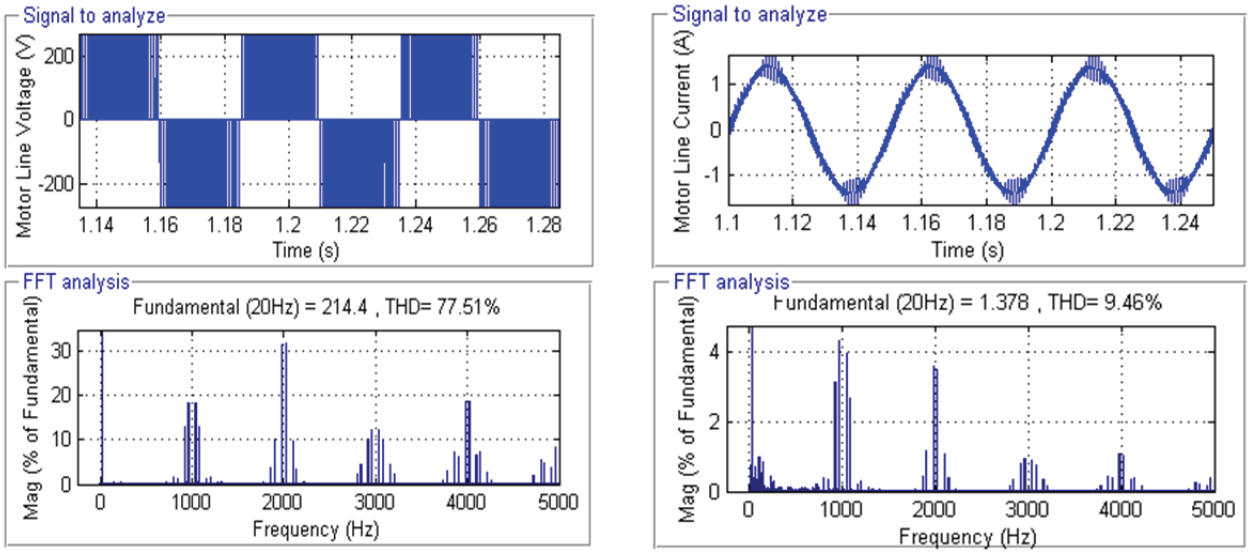
Fig. 10. Three level simulation waveforms at a frequency of 33Hz: (a) Motor line voltage waveform with THD; (b) Motor no-load line current waveform with THD.

IV. Experimental Results

The simulation results above have been validated by implementing the proposed SVPWM on an IGBT based volts/Hz controlled three level inverter fed induction motor with an input dc link voltage of 510V. The real time implementation of the proposed method is done using dSPACE advanced control desk 1104, consisting of a DS1104 PPC603e / 250 MHz controller board. A Textronix TDS 2014 C series digital storage oscilloscope with voltage and current sensors is used to capture the motor input voltage and current, respectively. The experimental setup shown in Fig. 12.

Fig. 13-Fig. 15 shows three level inverter line voltage and no load line current experimental waveforms along with numerical THD values at frequencies of 47Hz, 33Hz and 20Hz, respectively. A comparison graph of the motor line voltage THD and no-load line current THD for the simulation and experimental results are shown in Fig. 16 and Fig. 17 at different frequencies.

By observing the above two graphs, it is clear that the simulation and experimental results are almost similar throughout the frequency range of 40Hz to 49.95Hz.



(a) (b)

Fig. 11. Three level simulation waveforms at a frequency of 20Hz: (a) Motor line voltage waveform with THD; (b) Motor no-load line current waveform with THD.

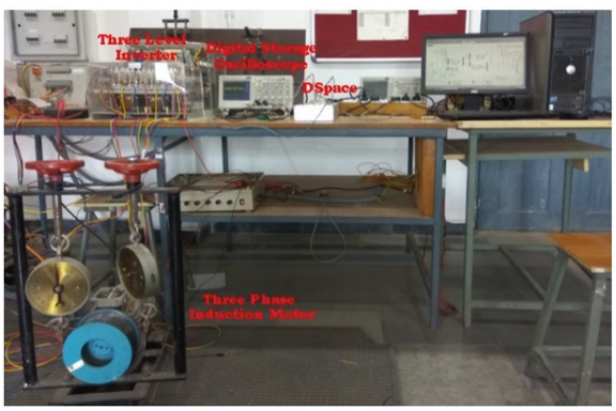


Fig. 12. Experimental setup.

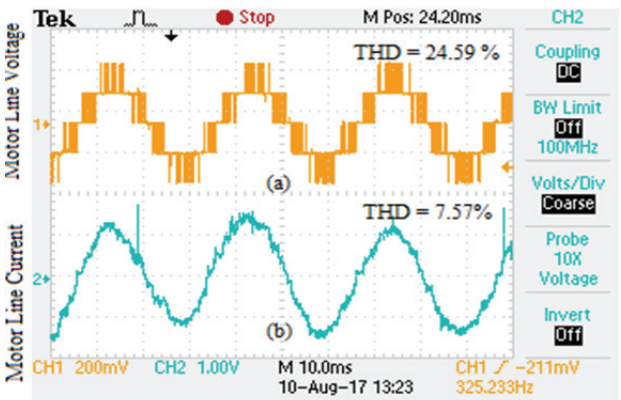


Fig. 14. Three level experimental waveforms with THD at a frequency of 33Hz; (a) Motor line voltage; (b) Motor no-load line current.

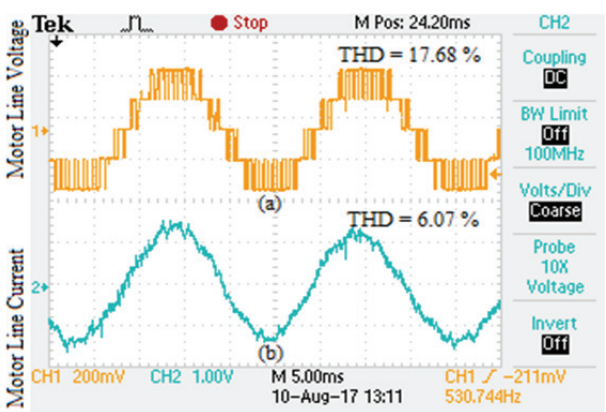


Fig. 13. Three level experimental waveforms with THD at a frequency of 47 Hz: (a) Motor line voltage; (b) Motor no-load line current.

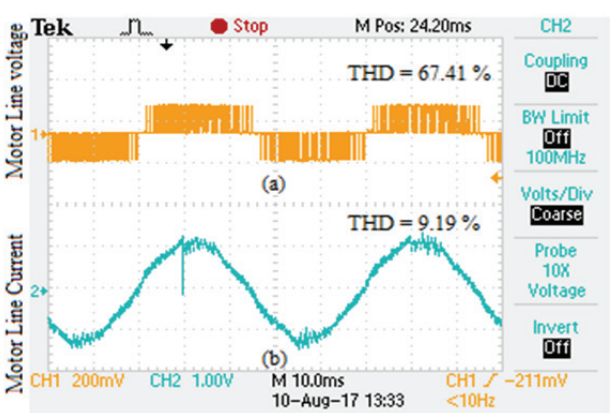


Fig. 15. Experimental waveforms with THD at a frequency of 20Hz: (a) Motor line voltage; (b) Motor no-load line current.

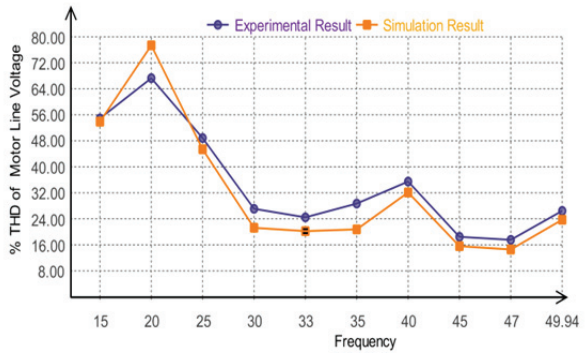


Fig. 16. Motor line voltage THD through simulation and experimental results.

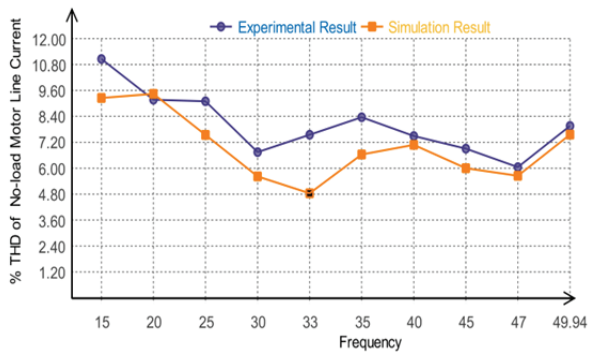


Fig. 17. Motor line current THD through simulation and experimental results.

V. Conclusions

A new generalized SVPWM algorithm for MLI has been presented in this article. It only involves a few mathematical calculations for the mapping and reverse mapping of vectors when compared to existing SVPWM strategies. In this method, the switching vectors, switching sequence and dwell times are determined at two level stage only. There is no need to find them at n level stage and also note that the exact positions of reference vectors is need not identified. This algorithm can be extended for any level with fixed number of steps without using any lookup tables. Therefore, this algorithm is very simple and efficient. Due to generalization, this algorithm is a suitable option for grid/standalone system based MLIs with different non-conventional energy sources.

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