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Design Methodology of Passive Damped *LCL* Filter Using Current Controller for Grid-Connected Three-Phase Voltage-Source Inverters

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Abstract

In grid-connected voltage-source inverters (VSIs), when compared with a simple inductive *L* filter, the *LCL* filter has a better performance in attenuating the high frequency harmonics caused by the pulse-width modulation of power switches. However, the resonance peaks generated by the filter inductors and capacitors can make a system unstable. In terms of simplicity and filter design cost, a passive damping method is generally preferred. However, its high power loss and degradation in high frequency harmonic attenuation are significant demerits. In this paper, a mathematical design solution for a passive *LCL* filter to derive filter parameters suppressing the high frequency current harmonics to 0.3% is proposed. The minimum filter inductance can be obtained to reduce the size of the filter. Furthermore, a minimum damping resistance design considering a current controller is analyzed for a stable closed-loop system. The proposed design method is verified by experimental results using a 5-kW three-phase prototype inverter.

Key words: Current control, *LCL* filters, Passive damping, Stability analysis, Voltage-source inverters

I. INTRODUCTION

In grid-connected voltage-source inverters (VSI), the excessive current harmonics caused by the pulse-width modulation (PWM) of power switches should be limited. The current harmonic limitations are specified in the IEEE-519 standard [1]. For safety issues, disturbances caused by current harmonics should be avoided so they do not affect other loads connected to the same grid. In order to attenuate current harmonics, input filters such as the simple inductive L and the LCL combination structure are widely used in grid-connected inverter applications [2]. In the conventional L filter, a high filter inductance should be used to satisfy current harmonic standards which may increase the size and cost of the filter.

To overcome this problem, the *LCL* filter has been proposed, as shown in Fig. 1, to achieve better attenuating performance against the current harmonics. It has a smaller filter inductance than the L filter. However, the *LCL* filter generates a resonance peak caused by the *L* and *C* resonant network. It can make the closed-loop system unstable, which results in a divergence of the output current. To suppress the resonance peak, various damping methods have been proposed such as active damping methods [3]-[11], passive damping methods [12]-[18], and hybrid damping methods [19], [20]. The active damping methods include single-loop methods and multi-loop methods, which use digital filters such as notch filters and additional feedback loops. However, both methods require complex control techniques, and multi-loop methods also require additional sensors. The passive damping methods use a passive damping resistor, which is a simple method that guarantees a high damping

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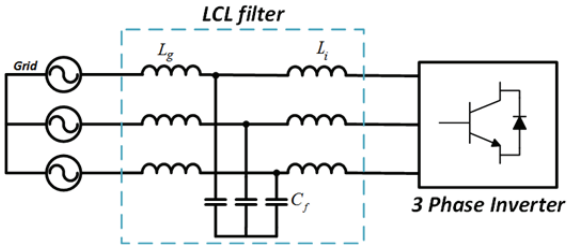


Fig. 1. Structure of an LCL filter for grid-connected three-phase inverters.

robustness. However, due to the damping resistor, there are additional power losses and performance degradation in high frequency harmonic attenuation. Alternately, the hybrid methods combine active and passive methods to reduce the power losses and improve the damping robustness. Consequently, in order to use passive damping methods that feature the simplest configuration, precise and detailed design guides are required to minimize side effects.

Previous studies of passive damping methods [12]-[18] presented various ways to design filter parameters such as inductors, capacitors and damping resistors. However, these methods do not present mathematical solutions to directly derive filter parameters that can suppress high frequency current harmonics to 0.3%, as specified by the IEEE-519. Therefore, it is hard to minimize the filter parameters. The authors of [6]-[8] show mathematical approaches to designing the high frequency current harmonics. However, damping resistors are not considered, which is a significant issue affecting the high frequency attenuation, the power loss and the stability issues.

This paper presents a mathematical design solution for passive *LCL* filters to directly derive optimal filter parameters that can suppress the high frequency current harmonics to 0.3%. In addition, by using this design solution, the minimum inductance can be derived to satisfy the IEEE-519 regulations, which can reduce the size of the filter. Furthermore, the power loss of the *LCL* filter is analyzed to show that it is reduced by the minimum filter inductance. In addition, a stable current controller is designed considering the damping resistor. The minimum damping resistance can be mathematically derived to obtain lower power loss, less performance degradation in the high frequency harmonic attenuation, and enough of a gain and phase margin of the current controller, which can guarantee the stable operation of the closed-loop system.

This paper is organized as follows. In Section II, a mathematical approach to derive the magnitudes of the current harmonics and the power loss is presented. In Section III, an IMC is used to design a current controller, and the minimum damping resistance is obtained. In Section IV, an analytical design methodology is presented, which is based on the mathematical analysis presented in Sections II and III. In Section V, experimental results using a 5-kW prototype three-phase inverter verify the validity and performance of the proposed design methodology.

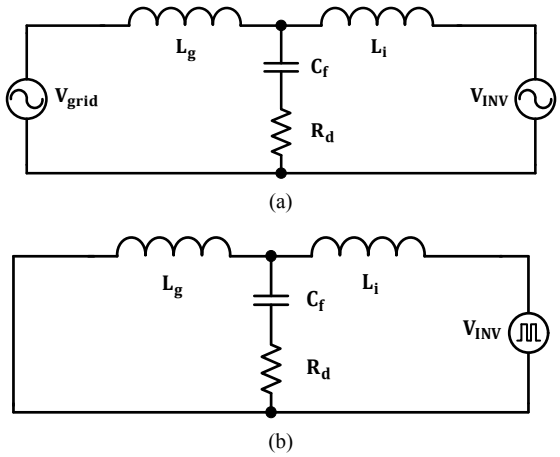


Fig. 2. Equivalent models of a passive LCL filter: (a) At line frequency; (b) At a high frequency.

II. Analysis of a Passive LCL Filter Model

In this Section, the passive *LCL* filter circuit is analyzed and the magnitude of the grid-side current harmonics is mathematically derived. A theoretical method to satisfy the IEEE-519 standard is presented. Finally, the power loss in an *LCL* filter is analyzed to be expressed in a mathematical formula. This formula is used in Section IV to show the power loss reduction using the minimum filter inductance.

A. Passive LCL Filter

Fig. 2(a) shows the structure of a passive *LCL* filter. It has an additional filter capacitor when compared with the conventional L filter. A schematic of an *LCL* filter at a high frequency is shown in Fig. 2(b). The *LCL* circuit is characterized so that the grid-side current harmonics are reduced by the filter capacitor C_f. However, the resonance caused by the L and C network occurs at the frequency described in (1), which induces the resonance peaks and unstable closed-loop system operation.

$$\omega_r = \sqrt{\frac{L_i + L_g}{L_i L_g C_f}} \tag{1}$$

The instability of a closed-loop system can be interpreted by the inverter voltage to the grid-side current transfer function of the *LCL* filter. In a transfer function without damping resistance, which is described in (2), a second order term in the denominator does not exist. Therefore, the transfer function makes the closed-loop system unstable and is analyzed by the Routh-Hurwitz's stability criterion [21]. However, in the case of the *LCL* filter with a damping resistance, which is described in (3), the second order term in the denominator appears and the stability of the closed-loop

system can be guaranteed by tuning the damping resistance R_d.

$$G(s)=\frac{i_g(s)}{V_{INV}(s)}=\frac{1}{L_iL_gC_fs^3+(L_i+L_g)s} \quad (2)$$

$$G(s)=\frac{i_g(s)}{V_{INV}(s)}=\frac{sC_fR_d+1}{L_iL_gC_fs^3+(L_i+L_g)R_dC_fs^2+(L_i+L_g)s} \quad (3)$$

However, due to the damping resistance, a zero in the numerator can induce performance degradation in high frequency harmonic attenuation. The effectiveness of high frequency harmonic attenuation decreases as the damping resistance increases. In addition, power loss increases as the damping resistance increases. Therefore, a minimum resistance design is required for the filter design. The design of a damping resistance considering both the minimum value and the stability of the closed-loop system is covered in Section III.

B. Current Harmonics at the Grid-side

In Fig. 2(b), the phase voltage harmonics at the inverter side generate current harmonics in the grid side. The voltage harmonics are inevitable factors due to the pulse-width modulation (PWM) by the switching mechanism of the inverter. As shown in Fig. 3(a), those voltage harmonics are generated at each switching frequency. In addition, they also produce grid-side current harmonics at each switching frequency.

IEEE-519 states that grid-side current harmonics over 35th order of the fundamental frequency at a rated power should be attenuated to under 0.3% of the rated current. The highest current harmonics appear at around the fundamental switching frequency. These values should be limited to satisfy the IEEE-519 standard. Conventional studies have presented rough design guides to suppress current harmonics [12]-[18]. These methods make it difficult to tightly match the magnitudes of the current harmonics exactly to 0.3%. Therefore, a mathematical approach is a better solution to systematically design the *LCL* filter. The magnitude of the current harmonics can be designed by following three steps.

First, the expression of the phase voltage harmonics should be obtained by a mathematical approach for a precise design. For the sinusoidal PWM method, the phase voltage harmonics can be mathematically expressed by using the double Fourier integral method based on a Bessel function as follows [15]:

$$V_{m,n}=\frac{4V_{dc}}{\pi}J_n\left(q\frac{\pi}{2}M\right)\sin\left(\left[m+n\right]\frac{\pi}{2}\right)\sin\left(n\frac{\pi}{3}\right) \quad (4)$$

where M is the modulation index at the rated load, V_{dc} is the dc link voltage, m is the order of the switching frequency, n is the order of the sideband of the fundamental frequency, ω_c is the carrier angular frequency, ω_o is the fundamental angular frequency, $q=m+n(\omega_o/\omega_c)$, and J_n is the Bessel function

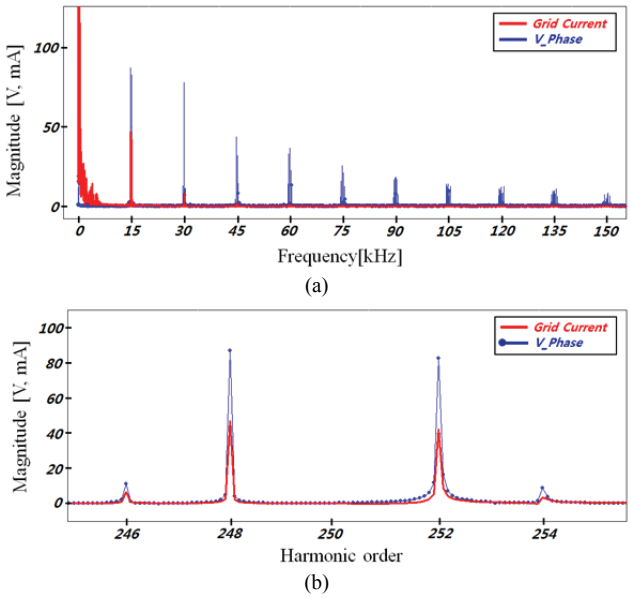


Fig. 3. FFT results of the inverter voltage and grid current (15 kHz): (a) Entire frequency; (b) Around the switching frequency.

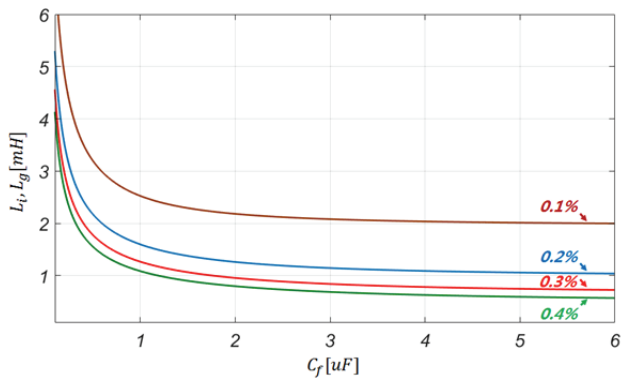


Fig. 4. Parameter values according to various current harmonics.

represented by the integral form. The phase voltage harmonics of other modulation methods, such as the space vector PWM and the discontinuous PWM, are shown in [15].

Second, the transfer function of the *LCL* filter, represented in (3), is designed by the terms of the filter parameters. This transfer function determines the amount of current injections from the inverter-side voltage to the grid-side current.

Finally, the magnitudes of the current harmonics can be calculated by the product of the transfer function in (3) and the voltage harmonics in (4). Fig. 3(b) shows that the highest current harmonics occur at the double side band of the fundamental switching frequency (m=1, n=-2 and m=1, n=2) and can be expressed as follows:

$$I_{1,-2}=\frac{V_{1,-2}\cdot\left|G\left(j\omega_{1,-2}\right)\right|}{\sqrt{3}} \quad (5)$$

$$I_{1,+2}=\frac{V_{1,+2}\cdot\left|G\left(j\omega_{1,+2}\right)\right|}{\sqrt{3}} \quad (6)$$

where $V_{1,-2}$ and $V_{1,+2}$ denotes the magnitudes of the phase

voltage harmonics at m=1, n=-2 and m=1, n=2, respectively.

As a result, the current harmonics expressed in (5) and (6) should be lower than 0.3% of the rated current. Since the value of (3) becomes smaller as the frequency rises, the current harmonic in (5) has to be a value higher than (6) to be considered.

Fig. 4 shows an example of the filter inductance and capacitance combination for various current harmonics using (5). The red line (0.3%) in Fig. 4 is the threshold for the IEEE-519 standards. The current harmonics can be designed to be 0.1% or 0.2%. However, this increases the size of the filter components. Therefore, the design should be targeted to 0.3% for the minimum size of the filter.

C. Power Loss in an LCL filter

The power losses in an *LCL* filter are the conduction loss through a winding resistor in the filter inductor and the damping resistor. The winding resistance is the value produced by the winding through the wire to make the inductor. The conduction loss in the winding resistor can be calculated as follows:

$$P_{winding} = {I_{ref}}^2 \left(R_i + R_g \right) \tag{7}$$

where R_g and R_i represent the winding resistor in the grid and in the inverter-side filter inductance, and I_{ref} is the current reference. The winding resistance changes according to the filter inductance. In a solenoid, the inductance is proportional to the square of the turn ratio of the wire as follows:

$$L = \frac{n^2}{\Re} \tag{8}$$

where $\Re$ is the reluctance of the magnetic core used in the filter inductor. Since the winding resistance is proportional to the turn ratio of the wire, the winding resistance increases proportionally to the square root of the filter inductance as follows:

$$R_{winding} = k\sqrt{L} \tag{9}$$

where k is the constant value that defines the other values of the winding resistor. As a result, a higher filter inductance can induce a higher winding resistance to have a higher conduction loss.

The conduction loss in the damping resistor can be calculated separately by the fundamental (60 Hz) and the harmonic current flowing through the damping resistor [15]. The conduction loss is calculated using the voltage and impedance formed in the *R-C* branch. Assuming the fundamental current in the grid-side is a purely sinusoidal waveform, the voltage at the R-C branch is calculated as follows:

$$V_{R-C} = \sqrt{{V_g}^2 + \left(\omega_f L_g I_{ref} \right)^2} \tag{10}$$

where $V_{R\text{-}C}$ is the voltage at the *R-C* branch, and V_g is the grid voltage. Since the impedance of the damping resistor is a lot smaller than the filter capacitor at the fundamental frequency, the power loss by the fundamental current can be simply shown as follows:

$$P_f = R_d \left(\omega_f C_f V_{R-C} \right)^2 . \tag{11}$$

Using the same method as above, the conduction caused by the current harmonic is calculated as shown in (12). For simple calculation, only the dominant current components ($m = 1,2\,, n = \pm 2$) that make up the current harmonic are included in (12).

$$P_h = R_d \sum_{m=1,2} \sum_{n=\pm 2} \left| \frac{j\omega_{m,n} L_g V_{m,n} G\left(j\omega_{m,n} \right)}{\sqrt{3}\left(R_d + 1 / j\omega_{m,n} C_f \right)} \right|^2 . \tag{12}$$

The total conduction loss in the damping resistor is the sum of (11) and (12). The conduction loss can be reduced by decreasing the damping resistance and the filter capacitance. A low filter capacitance results in a high impedance in the *R-C* branch, which induces a small current with a low conduction loss.

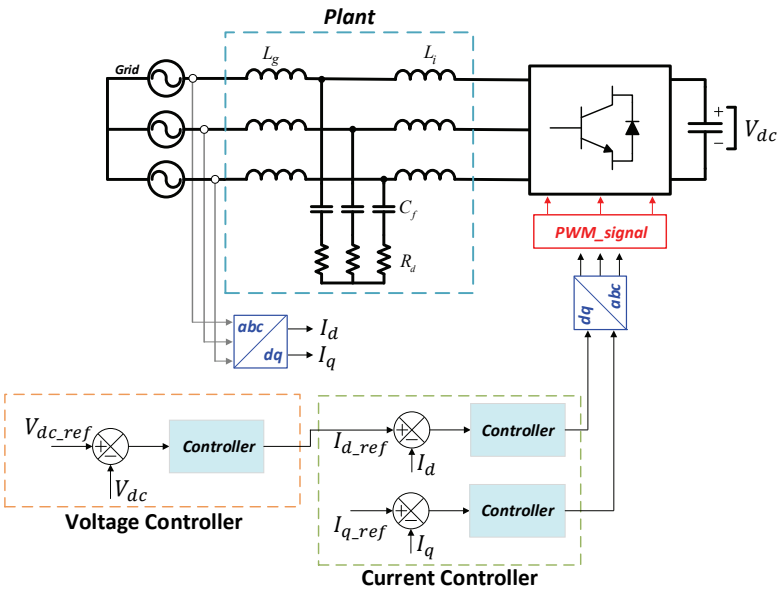
III. CURRENT CONTROLLER DESIGN

Fig. 5(a) shows the two control loops used in grid connected three-phase inverters. One of the control loops is an outer loop to regulate the output DC voltage, and the other is an inner loop to track the sinusoidal current reference. The inner loop can make the system unstable due to the resonance peaks generated from the *L* and *C* network.

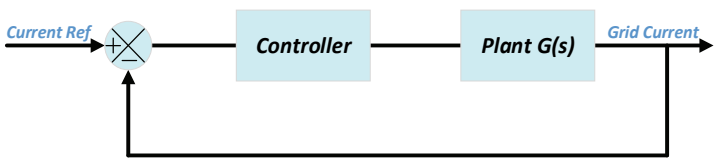
Fig. 5(b) shows the structure of the inner control loop. This inner loop contains a current controller and a plant function. The transfer function of the plant comes from the *LCL* filter expressed by (3). To make the closed-loop system stable, the open-loop transfer function in the inner loop should have a positive gain (GM) and phase margin (PM). Since a 180° phase lag occurs at the resonance frequency, the resonance peak should be lower than 0 dB for a positive GM, where the resonance peak can be suppressed by the damping resistor. In addition, the crossover frequency of the open-loop transfer function should be lower than the resonance frequency to avoid a negative PM.

The damping resistance is recommended to be one-third of the impedance of the filter capacitor at the resonant frequency [16]. Since the above method does not consider the current controller design, accurate values of the GM and PM cannot be derived. Therefore, for the current controller, a detail design methodology using specific values for the GM and PM is required.

PI controllers are mostly used for power control applications as current controllers [23]. There are several tuning methods such as Tyreus-Luyben and Ziegler-Nichols [24], as well as the IMC, which is applied in this paper. Using the IMC, accurate values of the GM and PM can be effectively

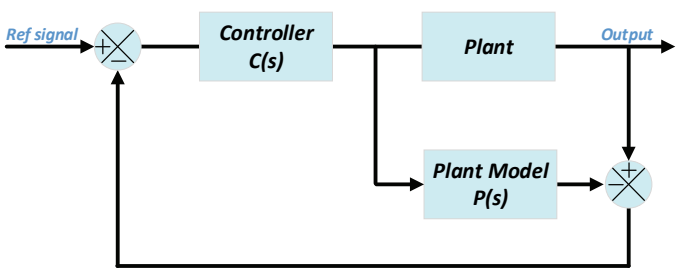


(a)

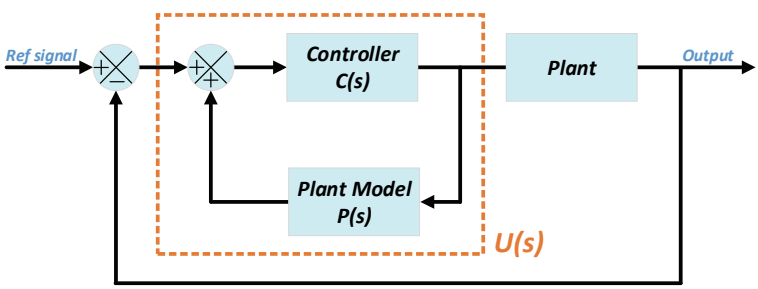


(b)

Fig. 5. Controller diagram of a 3 phase inverter: (a) Entire system, (b) Inner loop.



(a)



(b)

Fig. 6. Block diagram of an internal model controller: (a) IMC structure; (b) Classical control system structure.

obtained when compared with other tuning methods. The PI coefficients are directly matched to the plant model's parameters and the desired crossover frequency is easily obtained. As a result, the current controller can be easily derived for the desired GM and PM values.

Fig. 6(a) shows the control system structure of an IMC. It is a design method using the plant model. Due to its unique structure, the IMC can suppress all of the plant dynamics and

it can make the output value equal to the input value for all of the time variables. The controller $C(s)$ is expressed by the plant model parameters and the desired crossover frequency. To easily implement it in a PI controller, the IMC structure shown in Fig. 6(a) can be changed into the classical control structure shown in Fig. 6(b). In (13), $U(s)$ is defined as the classical controller. It can be expressed as a product of the first-order low pass filter and an inverse function of the plant model. There are more detail descriptions in [25].

In the frequency range below the resonant frequency, the *LCL* filter looks like a simple inductive *L* filter. Therefore, the IMC can be designed using an *L* filter for the following two reasons. First, the crossover frequency is designed to be lower than the resonant frequency. Second, the performance of the controller is mainly affected by the characteristics of the operating frequency lower than the crossover frequency. With the L model, the structure of $U(s)$ can be derived as follows:

$$U(s)=\frac{\alpha}{s}P^{-1}(s)=\alpha(L_i+L_g)+\frac{\alpha(R_g+R_i)}{s}=K_p+\frac{K_i}{s} \quad (13)$$

where α is the desired cross-over angular frequency.

The structure of $U(s)$ is identical to the structure of a PI controller. As a result, the PI coefficient and the desired crossover frequency are directly designed by the plant model and the variable α respectively.

For the inner loop system stability, a positive GM and PM should be guaranteed. The open-loop transfer function is defined by (14) and the delays of the sampling and PWM signals can be neglected for the sake of a simple calculation.

$$H(s)=U(s)\cdot G(s) \quad (14)$$

For a positive GM, the magnitude at the resonance frequency should be lower than 0 dB as follows:

$$\left|H(j\omega_r)\right|=\left(K_p+\frac{K_i}{\omega_r}\right)\cdot\frac{\sqrt{(L_iL_g)\cdot\left[L_iL_g-(L_i+L_g)\cdot R_d^2C_f\right]}}{R_d(L_i+L_g)^2} \quad (15)$$

Neglecting small terms such as K_i/ω_r, the minimum damping resistance with the desired GM can be obtained as follows:

$$R_d=\sqrt{\frac{(\alpha L_iL_g)^2}{(L_i+L_g)\cdot\left[x^2(L_i+L_g)+\alpha^2L_iL_gC_f\right]}} \quad (16)$$

where x represents the desired GM in the dB scale. As a result, the minimum damping resistance guarantees system stability. It also reduces the power loss and performance degradation in the high frequency harmonic attenuation.

For a sufficient PM, the crossover frequency should be considered in the controller design. If the crossover frequency is close to the resonant frequency, the PM can be insufficient due to a 180° phase lag at the resonance frequency. Considering the delays of the sampling and PWM signals, the crossover frequency should be 0.3 times lower than the resonant frequency as follows [26]:

$$f_c<0.3*f_r \quad (17)$$

where f_c is the crossover frequency, and f_r is the resonant frequency.

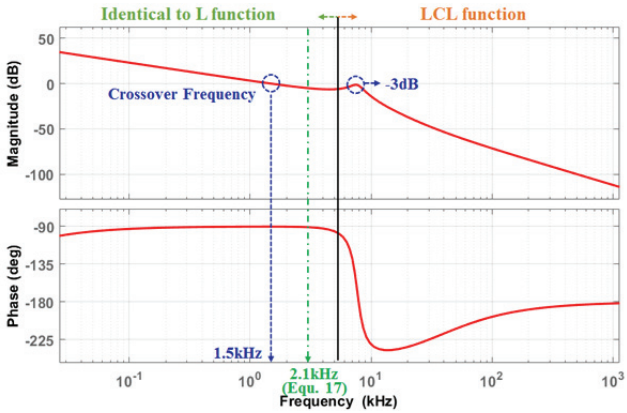


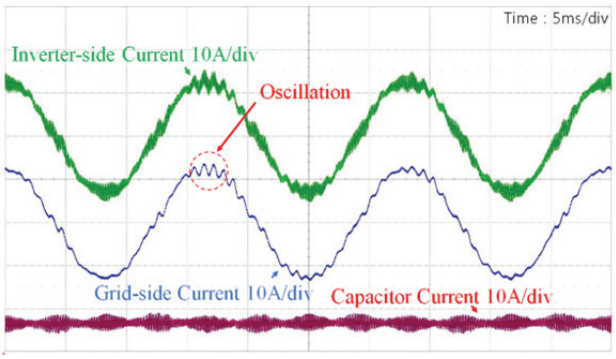
Fig. 7. Open-loop transfer function $H(s)$ using the IMC method.

TABLE I
PARAMETER OF $H(S)$

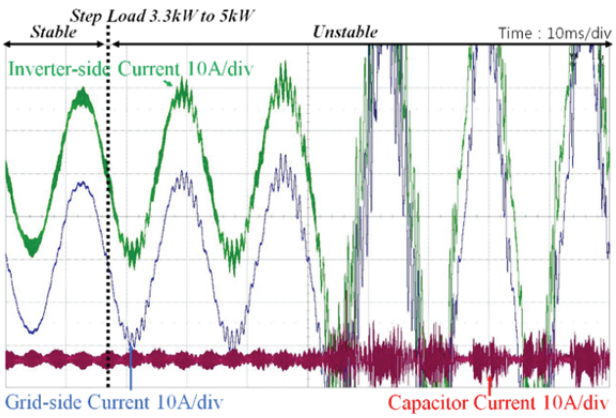
Parameter	Value
Switching frequency	15 kHz
Crossover frequency	1.5 kHz
Resonant frequency	7.1 kHz
L_i, L_g	2 mH
C_f	0.5 uF
R_d	9.42 Ω
R_i, R_g	10 mΩ
K_p	37
K_i	188

Fig. 7 shows an example of the open-loop transfer function $H(s)$ to which the IMC is applied. The parameters of the *LCL* filter and current controller are listed in Table I. Below the resonant frequency, the transfer function of the *LCL* filter operates like an *L* filter which guarantees (13). The resonant peak is suppressed to have -3 dB by (16). In addition, the desired crossover frequency is set to 0.1 times the switching frequency to satisfy (17). Therefore, a positive GM and PM are guaranteed using the proposed design to have a stable closed-loop system.

Fig. 8 shows experiment results with a high crossover frequency. Even if the GM is properly selected by the damping resistor, the system can be unstable when the PM is not guaranteed by the crossover frequency. In this case, the crossover frequency is selected to be higher than 0.3 times the resonant frequency, which can obtain an insufficient PM. For this reason, Fig. 8(a) shows oscillations in the steady state operation, and Fig. 8(b) shows unstable waveforms when a



(a)



(b)

Fig. 8. Unstable system with a high crossover frequency: (a) Steady state operation at 3.3kW; (b) Step load from 3.3kW to 5kW.

TABLE II
PARAMETER OF A THREE-PHASE INVERTER SYSTEM

Parameter	Value
Grid Voltage	220V
Grid Frequency	60Hz
DC-Link Voltage	380V
Switching Frequency	15kHz
Output Power	5kW

step load is applied. As a result, the current controller should be designed well even if damping resistance exists in the converter.

IV. FILTER DESIGN

A. Filter Design Requirements

When designing an *LCL* filter, there are several design requirements for the power constraints and system stability [16], [27]. These requirements have to be satisfied before other considerations such as efficiency and size. The filter design requirements are as follows:

1) The resonant frequency of the *LCL* filter should be limited for system stability. For the lower boundary, the resonant frequency should be higher than the crossover frequency. Because of the 180° phase lag at the resonance frequency as well as the delays of the sampling and pulse width modulation, the PM cannot be sufficient at the crossover frequency. To avoid this problem, the resonant frequency should be 0.3 times higher than the crossover frequency as shown in (17). For the upper boundary, the resonant frequency should be lower than the Nyquist frequency described as follows [16]:

$$f_r < 0.5 * f_s \tag{18}$$

where f_s is the switching frequency.

2) Using a phase diagram in the steady state, the minimum output DC voltage is related to the total filter inductance as follows [27]:

$$V_{dc.\min} > \sqrt{3} \cdot \sqrt{V_{LN}{}^2 + \left(\omega_{grid} L_{total} I_{ref}{}^2\right)} \tag{19}$$

where V_{LN} is the line to neutral grid voltage. With the desired output DC voltage and the rated current, the maximum filter inductance can be derived from (19) as follows:

$$L_{total} < \frac{\sqrt{\frac{V_{DC}{}^2}{3} - V_{LN}{}^2}}{\omega_g I_{ref}}. \tag{20}$$

3) The reactive power by the filter capacitor should be lower than 5% of the rated power as shown in (21) [16].

$$C_f < \frac{0.05 \cdot P_{rated}}{V_{LN}{}^2 \omega_g} \tag{21}$$

B. Proposed Mathematical Design Solution

When compared to existing design methods [12]-[18], the proposed mathematical design solution is presented to directly find the values of the filter parameters that suppress high frequency current harmonics to 0.3%. Furthermore, a minimum filter inductance can be obtained, which can reduce the size of the filter. Since the inductor is made up of magnetic cores, the filter inductor is more serious in terms of its cost and size than the filter capacitor. Reducing the inductance is the preferred method to decrease the total cost and filter size. The mathematical design solution is shown in the following steps based on the design methods from Section II and III. The following steps are carried out under the condition listed in Table II.

1) By applying the IMC in the current controller, the minimum damping resistance can be mathematically derived using (16) to ensure closed-loop system stability. The GM is set to 3 dB and the crossover frequency is set to 0.1 times the switching frequency

for smooth control [28]. The minimum damping resistance can be calculated as follows:

$$R_d = \sqrt{\frac{\left(\alpha L_i L_g\right)^2}{\left(L_i + L_g\right)\cdot\left[\left(-3dB\right)^2\cdot\left(L_i + L_g\right) + \alpha^2 L_i L_g C_f\right]}}. \quad (22)$$

2) Under the sinusoidal PWM method, the filter inductance and capacitance should satisfy the grid-side current harmonics with 0.3% as follows:

$$\frac{I_{1,-2}}{I_{ref}} = \frac{V_{1,-2}\cdot\left|G\left(j\omega_{1,-2}\right)\right|}{\sqrt{3}} = 0.3\%. \quad (23)$$

By substituting (22) into (23), the obtained filter inductance and capacitance makes the grid-side current harmonics as 0.3%. It also guarantees system stability with the minimum damping resistance. The filter inductance ratio between the grid side and the inverter side is one to one because of its simple calculation and stability reasons [17].

3) The selected filter inductance and capacitance from the above procedure can be drawn as the dotted red line in Fig. 9(a). In the upper region of the dotted red line, the grid-side current harmonics are lower than 0.3%, and vice versa.

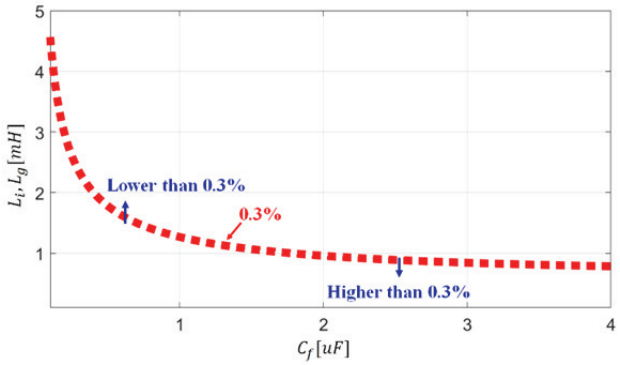
4) Finally, lines are drawn with circle markers that limit the filter inductance and capacitance. The lines are the previous design requirements from (17), (18), (20) and (21). The minimum filter inductance can be obtained under the above conditions.

Fig. 9(b) shows the filter inductance and capacitance from the mathematical design methodology. In this system, the design requirements from (20) and (21) limit the filter inductance and capacitance as 9 mH and 6.8 uF, respectively. The other design requirements from (17) and (18) are illustrated in Fig. 9(b), where the dotted red line represents the minimum and maximum filter inductances. By numerically solving the above analysis, the minimum and maximum filter inductances can be obtained as follows:

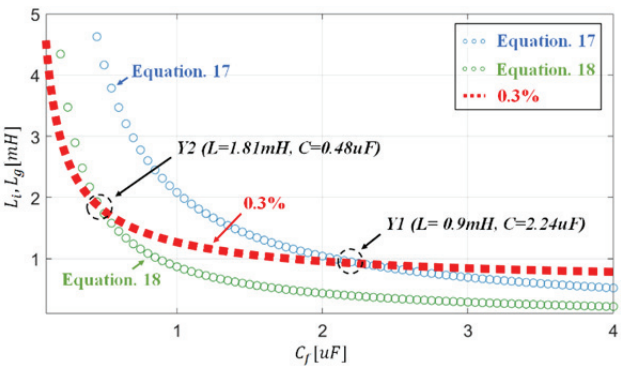
$$L_{Y1} = \frac{V_{1,-2}}{(0.3\%)\sqrt{3}\alpha^3}\sqrt{\frac{0.129\omega_s^2 + 4\alpha^4 x^2 + 0.72\alpha^2}{(16\omega_s^2\alpha^4 - 5.7\omega_s^4\alpha^2 + 0.5\omega_s^6)x^2 - 0.5\omega_s^4\alpha^2 + 2.8\omega_s^2\alpha^4 + 0.09\omega_s^6}} \quad (24)$$

$$L_{Y2} = \frac{V_{1,-2}}{(0.3\%)\sqrt{3}\alpha^3}\sqrt{\frac{4\omega_s^2 x^2 + 16\omega_s^2\alpha^2 + 64\alpha^2}{144\omega_s^4 x^2 + 832\alpha^2 x^2}} \quad (25)$$

The obtained minimum and maximum filter inductance are illustrated in Y1 (L=0.9 mH, C=2.24 uF) and Y2 (L=1.81 mH, C=0.48 uF) in Fig. 9(b). The minimum filter inductance is limited by (17), which guarantees a sufficient PM. The maximum filter inductance is limited by (18) to have a resonant frequency lower than the Nyquist frequency.



(a)



(b)

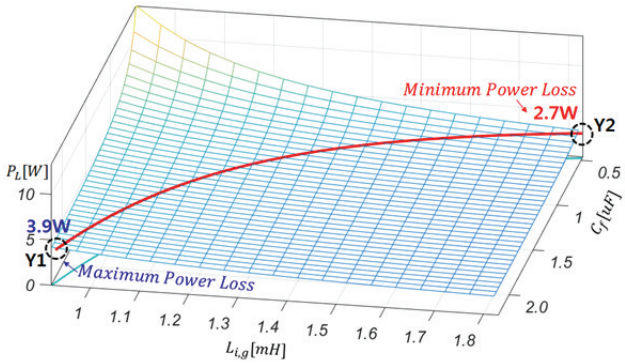
Fig. 9. Filter L and C of the proposed design methodology: (a) Satisfying the grid-side current harmonic as 0.3%; (b) Final design including the design requirements.

C. Power Loss Analysis in an LCL Filter

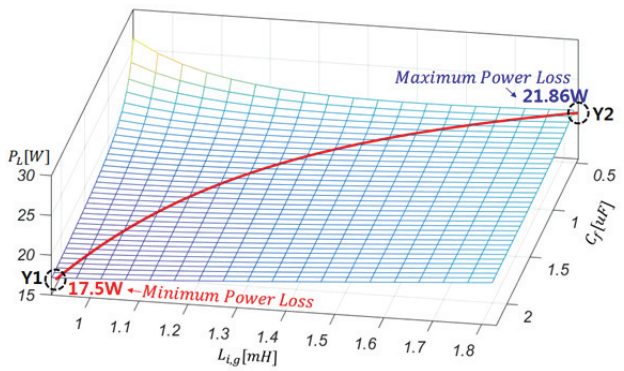
The power loss at the rated power is analyzed for the filter inductance and capacitance satisfying 0.3%, which is obtained in the above procedure. The power loss is shown in Fig. 10, where the red line shows the power loss at the 0.3% harmonic limitation.

The damping resistance is calculated as 5.7 Ω in the Y1 design and as 11.9 Ω in the Y2 design. Since the filter capacitance becomes smaller as the filter inductance increases, a high impedance is formed in the *R*-*C* branch. The power loss in the damping resistor decreases as the filter inductance increases. As a result, the minimum power loss is 2.7 W at the maximum filter inductance (Y2), and the maximum power loss is 3.9 W at the minimum filter inductance (Y1). They are both shown in Fig. 10(a).

However, because of the winding resistance of the filter inductor, the total power loss increases as the filter inductance increases. The winding resistance is calculated as 40 mΩ in the Y1 design and as 56.5 mΩ in the Y2 design. The other remaining winding resistances are calculated by (9). Since the power loss due to the winding resistance is relatively higher than the power loss due to the damping resistance, the total power loss reaches its maximum at the maximum filter inductance (Y2) of 21.86 W. In addition, the total power loss is minimized at the minimum filter inductance



(a)



(b)

Fig. 10. Power losses in an LCL filter: (a) Damping resistance loss; (b) Total power loss including the winding resistance loss.

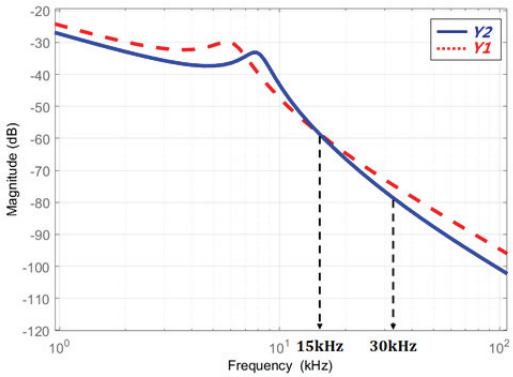


Fig. 11. Bode plot of G(s) with respect to filter inductance.

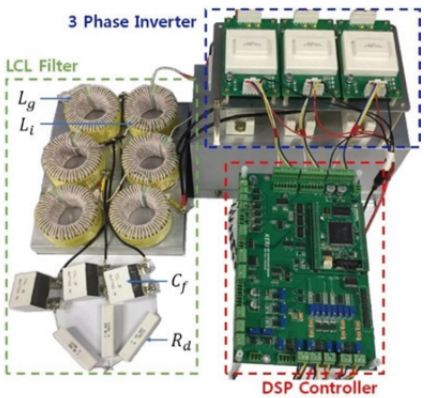


Fig. 12. 5-kW prototype three-phase inverter.

(Y1) of 17.5 W. These results are shown in Fig. 10(b).

As a result, the minimum power dissipation in the damping resistor appears at the maximum inductance with the minimum capacitance. However, due to the winding resistance, the minimum total power loss can be obtained at the minimum inductance with the minimum winding resistance.

D. Performance Analysis

In Fig. 11, a bode plot of $G(s)$ graphically shows how the high attenuation performances at the left double side band of the switching frequency (15 kHz) can be the same as each other even though they have different filter inductor values (Y1 and Y2). At first, the higher inductance has a better high frequency attenuation performance. However, the resonant frequency decreases as the filter capacitance increases and it shifts the slope of the transfer function $G(s)$ more quickly from -20 dB/decade to -40 dB/decade. Therefore, even though the filter inductances are different from each other, the mathematical analysis in (5) can be used to adjust the filter capacitance to obtain the same high frequency attenuation performance at the desired operating frequency. At the second harmonics of the switching frequency (30 kHz), the higher inductance in the Y2 design exhibits better attenuation performance. Since the current harmonics at the second harmonics of the switching frequency are much smaller than the values at the fundamental switching frequency, this attenuation performance is not considered for the IEEE-519 standards.

V. Experiment Results

The mathematical solution from Section IV is verified with a 5-kW prototype grid-connected three-phase inverter. The circuit configuration is shown in Fig. 12. A digital signal processor (TMS320f28335) is used to regulate the grid-side current and output DC voltage. The parameters of the Y1 and Y2 designs are chosen to show the validity of the proposed design. The design candidate of Y1 represents the targeted minimum filter inductance and the design of Y2 represents the conventional filter parameters with a large enough inductance. These two cases show that the Y2 filter inductance can be reduced to the Y1 filter inductance for obtaining the same current harmonic level limited to 0.3%. In addition, the power loss is reduced in the Y1 design. These results are summarized in Tables III and IV.

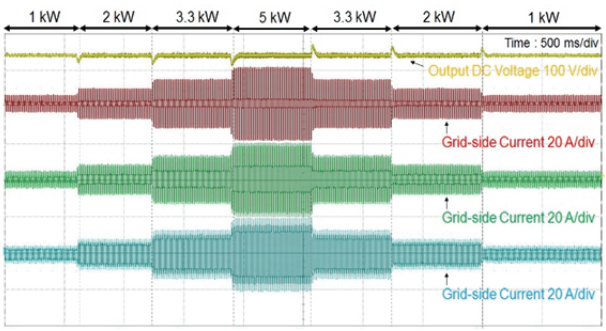
The current controllers of Y1 and Y2 are designed by considering the minimum damping resistor. Fig. 13 shows stable operation under step load changes, where the DC output voltage and the three-phase currents of Y1 and Y2 do not diverge. As shown in Fig. 14, which is a smaller time scale from Fig. 13, the three-phase currents are stabilized without oscillations when the load changes.

TABLE III
EXPERIMENT RESULTS OF Y1 AND Y2

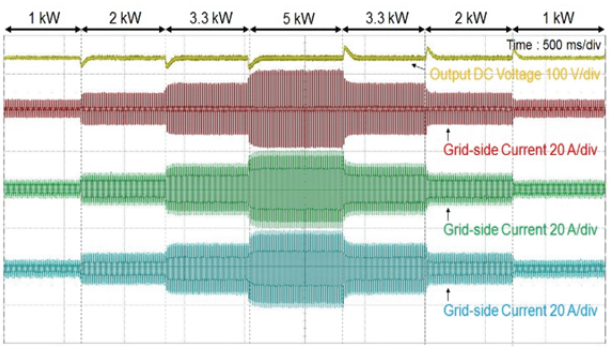
L_i, L_g	C_f	R_d	$I_{1,-2}/I_{ref}$
0.93mH	2.29uF	6Ω	0.289%
1.87mH	0.47uF	12Ω	0.286%

TABLE IV
POWER LOSSES OF Y1 AND Y2

	$R_{winding}$	P_{daming}	$P_{winding}$	P_{total}
Y1	40mΩ	4.5W	13.69W	18.19W
Y2	58mΩ	2.88W	19.85W	22.73W



(a)



(b)

Fig. 13. Experimental results of step-load changes: (a) Y1 (L=0.93 mH, C=2.29 uF); (b) Y2 (L=1.87 mH, C=0.47 uF).

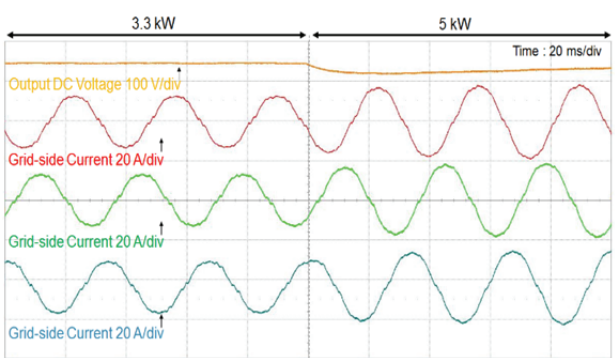
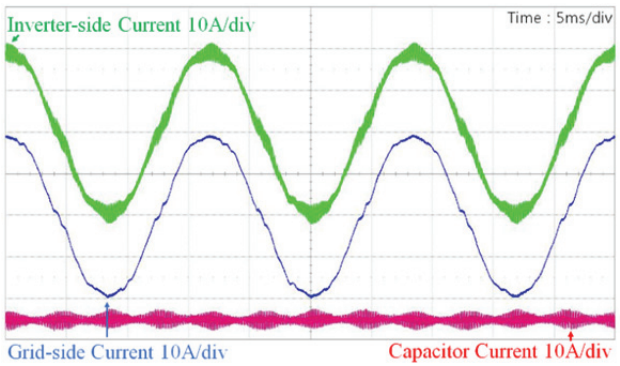
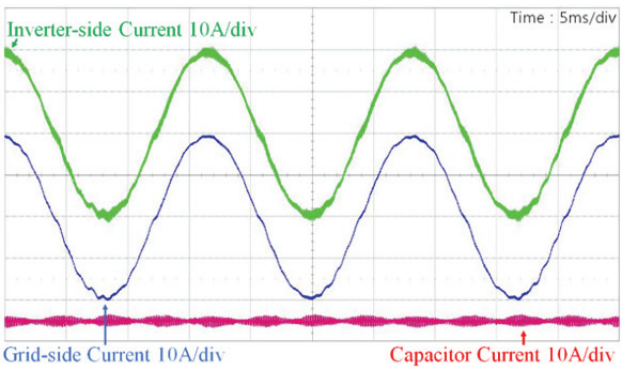


Fig. 14. Experimental results of step-load change with a smaller time scale (3.3 kW to 5 kW, Y1).

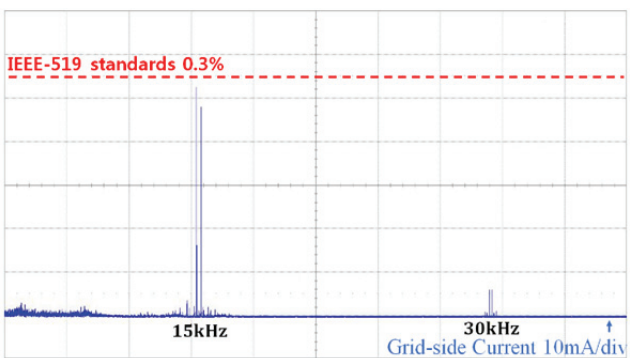


(a)

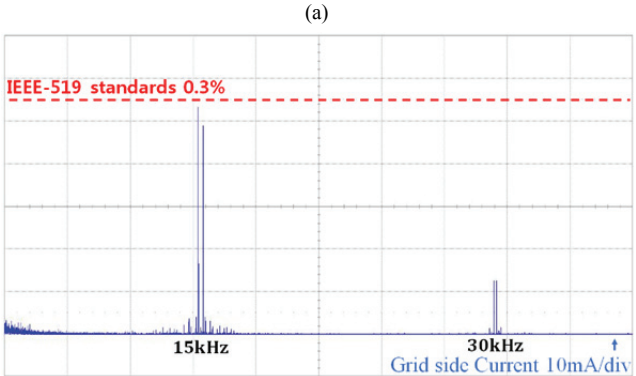


(b)

Fig. 15. Experimental results of steady-state waveforms under the rated 5 kW: (a) Y1 (L=0.93 mH, C=2.29 uF), (b) Y2 (L=1.87 mH, C=0.47 uF).



(a)



(b)

Fig. 16. Frequency spectrum results: (a) Y1 (L=0.93 mH, C=2.29 uF), (b) Y2 (L=1.87 mH, C=0.47 uF).

Fig. 15 shows the steady state of Y1 and Y2 under the rated 5 kW, and the design of Y2 has lower current ripples at the inverter-side due to the high filter inductance. However, due to the high filter capacitance in the Y1 design, both the Y1 and Y2 designs have nearly the same current ripples at the grid-side.

In Fig. 16, the frequency spectrum results of the Y1 and Y2 designs shows that the grid-side current ripples are nearly the same with the current harmonics of $I_{1,-2}$ /I_{ref} as 0.289% and 0.286%, respectively. These values tightly satisfy the IEEE-519 standards. The Y2 design has lower current harmonics at the second switching frequency due to the inductance difference, as shown in Fig. 6. As a result, the Y1 design has the minimum filter inductance, which is twice as small as the inductance of Y2, while satisfying the IEEE-519 standards.

Table IV shows the power loss at the rated power in the LCL filter according to the designs of Y1 and Y2. Similar to the simulation results shown in Fig. 9, the power loss in the damping resistance is higher in the Y1 design at 4.5 W than that in the Y2 design at 2.88 W. Since the winding resistance of the Y1 design is 40 mΩ, which is lower than that of the Y1 design at 58 mΩ, the total power loss decreases in the Y1 design to 18.19 W, which is lower than that of the Y2 design at 22.73 W.

VI. CONCLUSIONS

This paper proposed the mathematical design solution for the passive LCL filter to directly derive optimal filter parameters that can suppress high frequency current harmonics limited to 0.3%. Using this solution, the filter parameters can be minimized to satisfy the IEEE-519 regulation up to 0.3%. In addition, the minimum filter inductance is mathematically derived, which can reduce the size of the filter. The power loss in the *LCL* filter can be decreased by using the minimum inductance. Furthermore, a stable current controller can be designed using the minimum damping resistance that is mathematically derived to obtain a lower power loss, less performance degradation in terms of the high frequency harmonic attenuation, and enough gain and phase margins of the current controller, which can guarantee the stable operation of the closed-loop system. Finally, experimental results verify both the effectiveness of the proposed solution and the stable current controller design using the minimum damping resistance.

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