JPE 18-4-23

https://doi.org/10.6113/JPE.2018.18.4.1211
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

Power Distribution Control Scheme for a Three-phase Interleaved DC/DC Converter in the Charging and Discharging Processes of a Battery Energy Storage System

Bing Xie*, Jianze Wang*, Yu Jin*, Yanchao Ji†, and Chong Ma**

†,*School of Electrical Engineering and Automation, Harbin Institute of Technology, Harbin, China
**State Grid Fushun Electric Power Supply Company, Fushun, China

Abstract

This study presents a power distribution control scheme for a three-phase interleaved parallel DC/DC converter in a battery energy storage system. To extend battery life and increase the power equalization rate, a control method based on the nth order of the state of charge (SoC) is proposed for the charging and discharging processes. In the discharging process, the battery sets with high SoC deliver more power, whereas those with low SoC deliver less power. Therefore, the SoC between each battery set gradually decreases. However, in the two-stage charging process, the battery sets with high SoC absorb less power, and thus, a power correction algorithm is proposed to prevent the power of each particular battery set from exceeding its rated power. In the simulation performed with MATLAB/Simulink, results show that the proposed scheme can rapidly and effectively control the power distribution of the battery sets in the charging and discharging processes.

Key words: Interleaving bidirectional operation, Power distribution, Power correction algorithm, State of charge

I. INTRODUCTION

Battery energy storage technology has been vigorously developed because of the wide application of renewable energy to power systems [1], [2]. Energy storage technology can solve the intermittence and volatility of renewable energy power generation and optimize the structure, scheduling management, and operation mode of traditional power grids [3], [4]. At present, the research and application of battery energy storage technology has evolved from low voltage–small capacity to high voltage–large capacity [5]-[7]. A three-phase interleaved DC/DC converter outputs small ripple currents, helps extend battery life, and is suitable for high-power energy storage applications [8], [9].

Manuscript received Dec. 2, 2017; accepted Feb. 26, 2018
Recommended for publication by Associate Editor Jonghoon Kim.
†Corresponding Author: 13b906008@hit.edu.cn
Tel: +86-18686738589, Harbin Institute of Technology
*School of Electrical Engineering and Automation, Harbin Institute of Technology, China
**State Grid Fushun Electric Power Supply Company, China

An energy storage system typically consists of multiple modules arranged in parallel. Therefore, power distribution is an important research area [10], [11]. In this study, the power distribution scheme of an energy storage unit is investigated based on a three-phase interleaved parallel DC/DC converter. In [12], a power distribution control method for a battery energy storage system (BESS) without master–slave control was proposed to achieve independent control of each module with the same operation mode. The power distribution of cascaded H-bridge modules was realized by introducing the zero-sequence voltage and closed-loop control of each module [13]. A three-level battery charging–discharging balancing control was proposed for a cascaded converter [14]. Sub-module power distribution was achieved by adjusting the zero-sequence current, amplitude of modulation wave, and reference current. A cascaded bipolar BESS was proposed for high-voltage and large-capacity applications; this system separates the energy storage unit from the module multilevel converter (MMC) [15]. State-of-charge (SoC) balance control is realized by adjusting the input time of each battery unit in

the MMC bridge arm, which increases the control difficulty of the entire system. In [16], fuzzy control was applied to the power distribution control scheme of a BESS. To realize power distribution among different modules, reference [17] described a control method based on step-wave rotation modulation, but it was suitable for full-bridge converters. In [18] and [19], droop control without master–slave control was used in the power distribution of a DC microgrid. As load power increases, droop control decreases output voltage and adjustment precision. Therefore, determining the droop coefficient is difficult. Reference [20] proposed a dynamic distribution method for load power applied to DC-distributed energy storage systems. An adaptive droop control method based on SoC was introduced. This method solves the problem of voltage drop in the traditional droop control and limits the equalization rate under the premise of ensuring the stability and control accuracy of a control system. However, the droop coefficient is inversely proportional to the *n*th of SoC, which is unsuitable for the charging process of battery sets. A power distribution method for the charging process of DC microgrids was introduced in [21]. The droop coefficient is inversely proportional to the injected power. Hence, battery sets with low SoC absorb more power during the charging process than battery sets with high SoC. Power equalization can be gradually realized while disregarding battery charging mode and battery life. A power distribution control method based on SoC was proposed for a vanadium battery parallel system [22]. This method can accurately realize the reasonable distribution of power but with a slow distribution rate.

To extend the life of battery sets while increasing equalization rate, the current study presents a charge and discharge power distribution control strategy based on the *n*th order of the SoC for a three-phase interleaved parallel DC/DC power converter. In particular, this strategy accelerates power distribution by changing the current correction parameters. To solve the problem of DC bus voltage drop in the discharging process, this study introduces the DC bus voltage compensation coefficient to strengthen the control and maintain the stability of the DC bus voltage. In two-stage charging mode, a power correction algorithm is proposed to prevent the charging power of each module from exceeding its rated value while keeping the sum of the charging power constant. The theoretical analysis results verify the rationality of the power distribution scheme for the three-phase interleaved parallel converter based on the *n*th order of the SoC. A simulation model is established to verify the theoretical analysis results based on MATLAB/Simulink.

II. Operation Mode and Controller Design

A. Topology

Compared with the traditional buck–boost converter, the

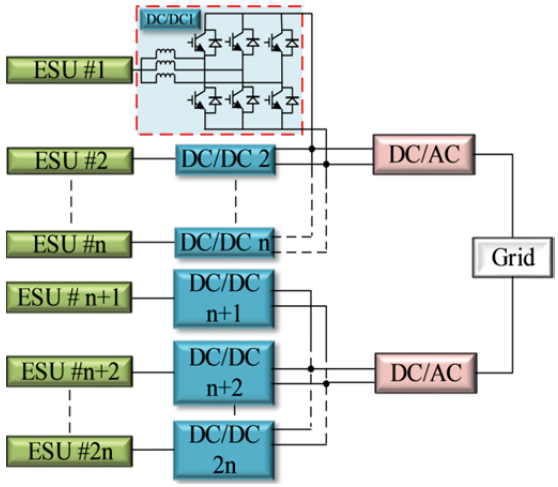


Fig. 1. Topology of the BESS based on the three-phase interleaved DC/DC converter.

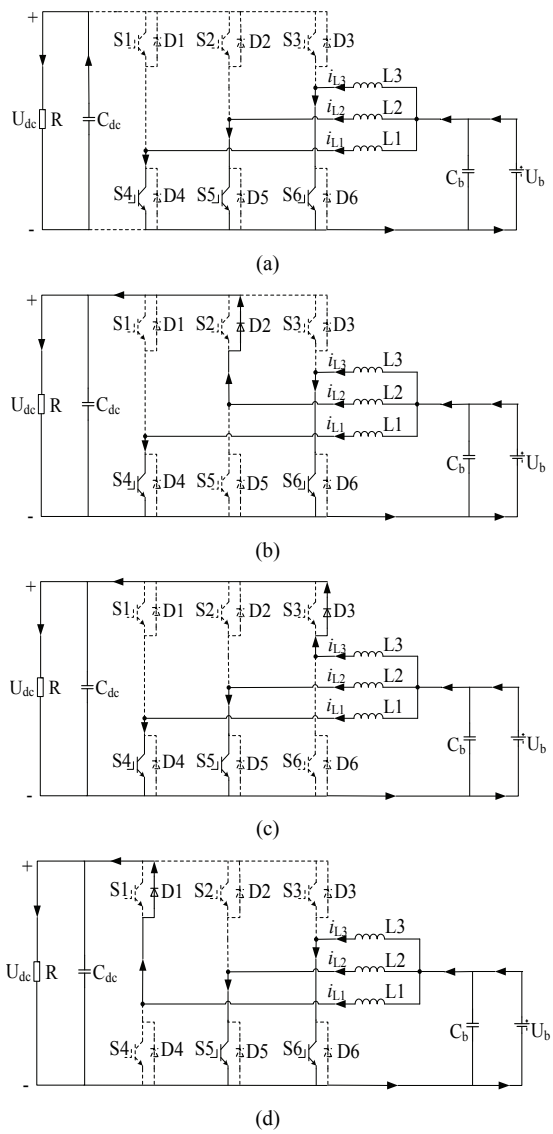


Fig. 2. Equivalent circuit of six work modes in boost mode: (a) Modes 1, 3, 5; (b) Mode 2; (c) Mode 4; (d) Mode 6.

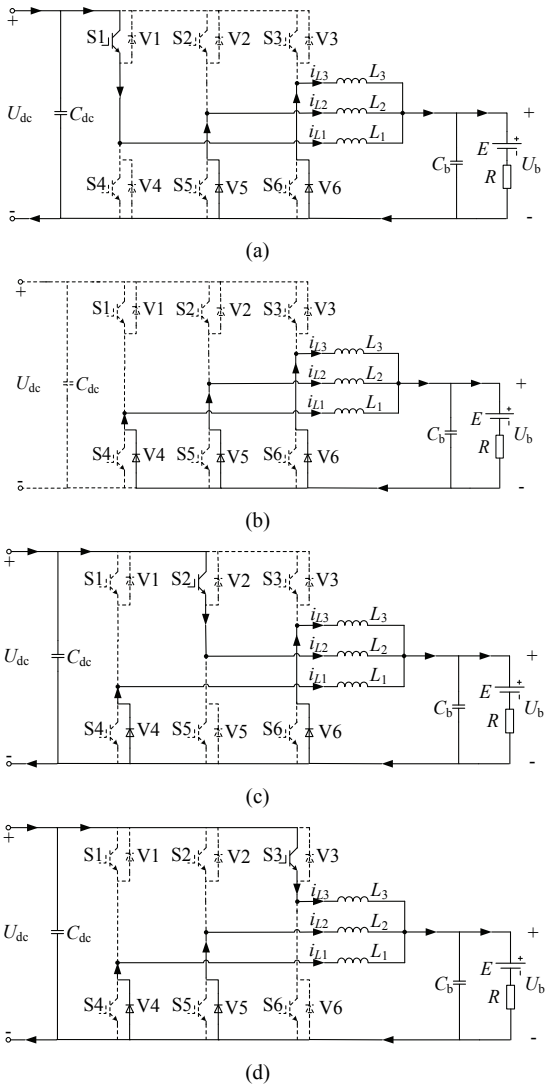


Fig. 3. Equivalent circuit of six work modes in buck mode: (a) Mode 1; (b) Modes 2, 4, 6; (c) Mode 3; (d) Mode 5.

three-phase interleaved DC/DC converter is suitable for large power applications and exhibits the advantages of effectively reducing the current ripple factor, which can extend battery life, and requiring less inductance [23]–[25]. Fig. 1 shows the topology of a BESS based on the three-phase interleaved DC/DC converter.

B. Operation Mode

A three-phase interleaved DC/DC converter can achieve bidirectional power flow between the high and low voltage sides. The converter has two operation modes: boost, in which the battery is in discharge state; and buck, in which the DC bus system charges the battery.

1) Boost Mode:

The duty factors of switch tubes S_4, S_5, S_6 are D_4, D_5, D_6, and the duty ratios D_4, D_5, D_6 are set as $D>2/3T_s$ (T_s is the switch period). Assume that the circuit is in continuous conduction mode (CCM). The circuit will have six work modes within a period. The equivalent circuits of the six work modes in boost mode are shown in Fig. 2.

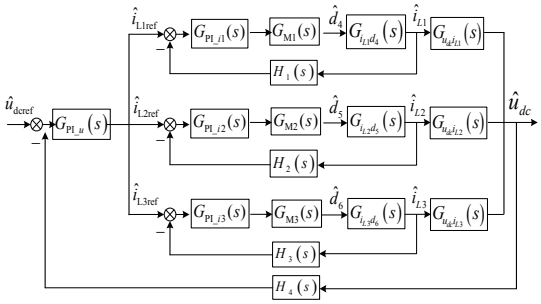


Fig. 4. Control diagram of the converter in boost mode.

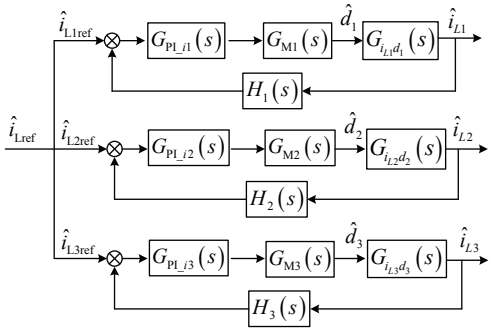


Fig. 5. Control diagram of the converter in constant current charging mode.

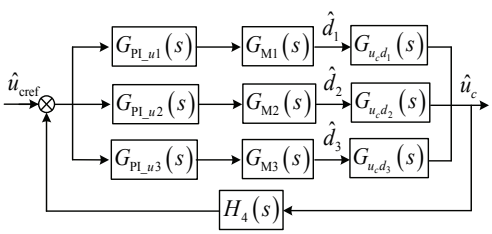


Fig. 6. Control diagram of converter in constant voltage charging mode.

2) Buck Mode:

The duty factors of switch tubes S_1, S_2, S_3 are D_1, D_2, D_3, and the duty ratios D_1, D_2, D_3 are set to $D'<1/3T_s$ (T_s is the switch period). Assume that the circuit is in CCM. The circuit will have six work modes within a period. The equivalent circuits of the six work modes in boost mode are shown in Fig. 3.

C. Controller Design

1) Controller Design in Boost Mode:

In this study, the proportional–integral (PI) control is used to achieve steady-state operation. The control structure is shown in Fig. 4. To realize three-phase current equalization, three-phase current is controlled independently. Phase-shifting technology can reduce the output current ripple. The reference values of the three-phase inductor current are $\hat{i}_{L1ref}$, $\hat{i}_{L2ref}$, and $\hat{i}_{L3ref}$. Functions $G_{u_{dc}i_{L1}}(s)$, $G_{u_{dc}i_{L2}}(s)$, and $G_{u_{dc}i_{L3}}(s)$

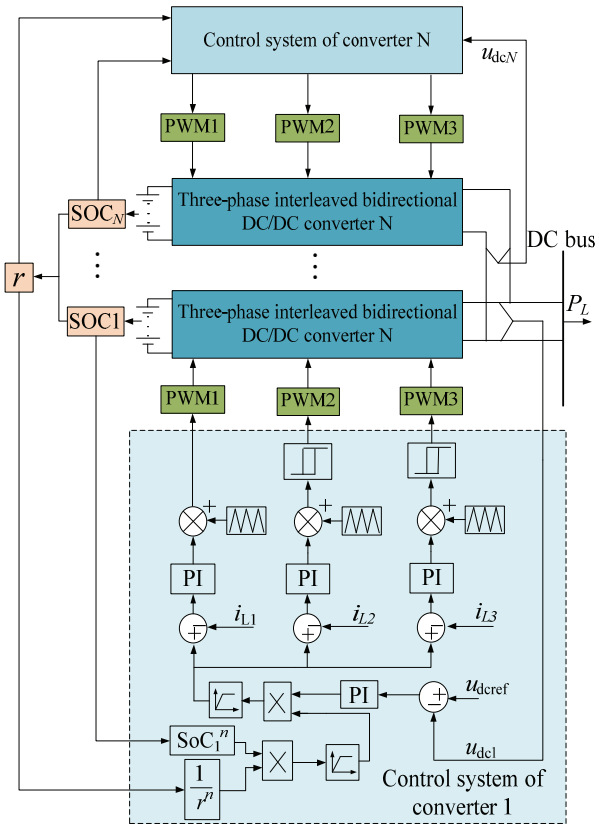


Fig. 7. Overall control diagram of discharge power distribution.

are the transfer functions from the DC bus voltage to the inductance current. $G_{M1}(s)$, $G_{M2}(s)$, and $G_{M3}(s)$ are the transfer functions of modulation. $H_1(s)$, $H_2(s)$, and $H_3(s)$ are the transfer functions of the sampling current. $G_{PI\_i1}(s)$, $G_{PI\_i2}(s)$, and $G_{PI\_i3}(s)$ are the transfer functions of the PI controllers. $G_{i_{L1}d_4}(s)$, $G_{i_{L2}d_5}(s)$, and $G_{i_{L3}d_6}(s)$ are the transfer functions from the inductor current to the duty cycle. $H_4(s)$ is the transfer function of the sampling voltage.

2) Controller Design in Buck Mode:

The battery is charged when the converter is in buck mode. A two-stage charging method is adopted in this study. Figs. 5 and 6 show the control structure of the converter during constant current charging and constant voltage charging, respectively. In Fig. 5, the inductance currents $\hat{i}_{L1ref}$, $\hat{i}_{L2ref}$, and $\hat{i}_{L3ref}$ are the reference values. $G_{i_{L1}d_1}(s)$, $G_{i_{L2}d_2}(s)$, and $G_{i_{L3}d_3}(s)$ are the transfer functions from the inductor current to the duty cycle. $G_{PI\_i1}(s)$, $G_{PI\_i2}(s)$, and $G_{PI\_i3}(s)$ are the transfer functions of the PI current controllers. In Fig. 6, $G_{u_cd_1}(s)$, $G_{u_cd_2}(s)$, and $G_{u_cd_3}(s)$ are the transfer functions from the capacitor voltage of the battery side to the duty cycle. $G_{PI\_u1}(s)$, $G_{PI\_u2}(s)$, and $G_{PI\_u3}(s)$ are the transfer functions of the PI voltage controllers.

III. Control Strategy Analysis

A. Control Scheme for Discharging Power Distribution

Fig. 7 shows the control structure for the discharging power distribution based on the nth order of SoC. Assume that two energy storage modules are connected in parallel to the DC side and disregard the influence of the power limit of the control system. The relationship between the output power of the two modules in the discharging state is deduced. The reference value of converter 1 for current control can be expressed as

$$i_{1ref} = (k_{up1} + \int k_{ui1}dt) \cdot \frac{SoC_1^{\,n}}{r^n} \cdot (u_{dcref} - u_{dc1}) . \quad (1)$$

The reference value of converter 2 for current control can be expressed as

$$i_{2ref} = (k_{up2} + \int k_{ui2}dt) \cdot \frac{SoC_2^{\,n}}{r^n} \cdot (u_{dcref} - u_{dc2}) , \quad (2)$$

where k_{up1}, k_{ui1} and k_{up2}, k_{ui2} are the PI controller parameters of the voltage loop in the control system of converters 1 and 2. $SoC_i^{\,n}/r^n$ is the correction parameter of the current reference value. r is the compensation coefficient of the DC bus voltage, and its value can reach $\min\{SoC_1, SoC_2, \cdots, SoC_N\}$. The role of r is to maintain DC bus voltage stability and prevent it from falling.

The parameters of the two PI controllers are equal, as shown in

$$k_{up1} = k_{up2} , \quad (3)$$

$$k_{ui1} = k_{ui2} . \quad (4)$$

Two energy storage modules are connected in parallel. Hence,

$$u_{dc1} = u_{dc2} . \quad (5)$$

In discharge mode, if the SoC of the battery is within the normal operating range, then the voltage of the battery is nearly the same and can be approximated as

$$u_{b1} = u_{b2} . \quad (6)$$

The output power of the battery in module1 can be expressed as

$$P_1 = 3i_{1ref} \times u_{b1} . \quad (7)$$

The output power of the battery in module2 can be expressed as

$$P_2 = 3i_{2ref} \times u_{b2} . \quad (8)$$

When (1) to (8) are combined, we can conclude that

$$\frac{P_1}{SoC_1^{\,n}} = \frac{P_2}{SoC_2^{\,n}} . \quad (9)$$

This conclusion is extended to the following:

$$\frac{P_1}{SoC_1^{\,n}} = \frac{P_2}{SoC_2^{\,n}} = \cdots = \frac{P_N}{SoC_N^{\,n}} . \quad (10)$$

Therefore, when the BESS operates in discharging mode, the discharging power of the battery is proportional to the *n*th order of the SoC. The battery with high SoC output more power. In practical applications, the rated discharge power of each energy storage module in the power distribution process should be considered. From the comparison of the load power P_L and rated power P_E of the BESS, the power distribution control in the discharging process can be divided into two modes.

1) $P_L \geq P_E$*:*

The BESS cannot fully meet the power demand of the load; hence, each module discharges with the rated power.

2) $P_L < P_E$*:*

The BESS can meet the power demand of the load, whereas the assigned power P_i for some modules exceeds the rated power. The assigned power can be derived as

$$P_i = P_L \cdot \frac{\mathrm{SoC}_i^{\,n}}{\sum_{i=1}^{N} \mathrm{SoC}_i^{\,n}} \quad i = 1, 2, \cdots N \,. \tag{11}$$

To make the BESS work in normal operation during the discharging process, the control parameters in the discharge state should be limited as follows.

1) Limitation of the Maximum Discharge Power of each Module

The discharge power of each module shall not exceed its rated power according to the two operation modes of the power distribution control.

$$P_{di} \leq P_{ed} \quad i = 1, 2, \ldots, N \,. \tag{12}$$

where P_{di} is the assigned discharge power of the *i*th module, and P_{ed} is the rated power of each module.

2) Limitation of SoC for the Battery in each Module:

The battery can work normally when the SoC is within a safe range. If the SoC exceeds the safe range, then the operating condition will shorten battery life and even result in an unstable operation. The module with an SoC that is outside the safe range should be removed from the BESS, whereas the other modules should continue to operate in power distribution mode.

When the BESS works during the discharging process, the safety range of the SoC is

$$\mathrm{SoC}_i \geq 0.2 \quad i = 1, 2, 3 \cdots N \,. \tag{13}$$

3) Limitation of the Equalization Rate:

The upper limit of exponent *n* is constrained by the initial output power. If exponent *n* exceeds this limitation at the initial time, then the output power of the converter with a high SoC may exceed its rated power, thereby causing a fault. The lower limit of exponent *n* is determined by minimizing the SoC error within the acceptable range in the preset duration. The equalization rate slows down when exponent *n* decreases; hence, the rate should be ensured to meet design requirements [11]. The limitation of the equalization rate is explained in detail in [11].

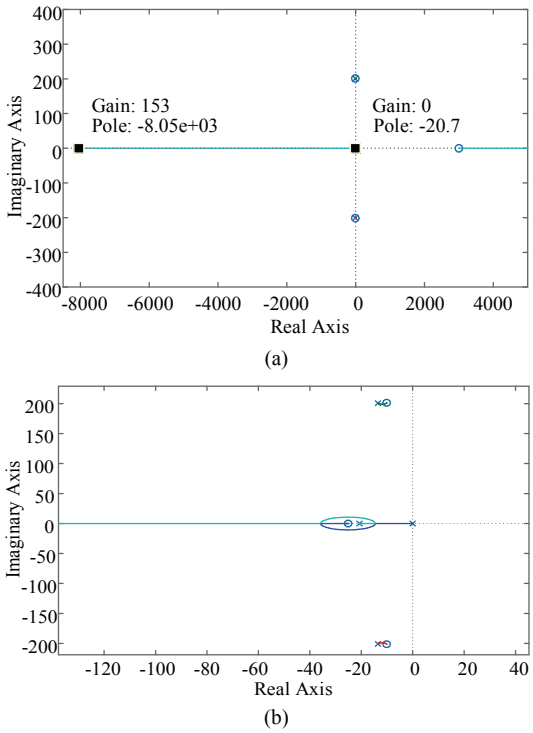


Fig. 8. Root locus of the system with different λ values: (a) Root locus, (b) Local enlarged view.

4) Stability Analysis after Introducing the Compensation Coefficient:

As shown in Fig. 4, $G_{u_{\mathrm{dc}}i_{\mathrm{L1}}}(s)$, $G_{u_{\mathrm{dc}}i_{\mathrm{L2}}}(s)$, and $G_{u_{\mathrm{dc}}i_{\mathrm{L3}}}(s)$ are the transfer functions from the DC bus voltage to the inductance current. Therefore, the DC bus voltage can be expressed as

$$u_{\mathrm{dc}} = G_{u_{\mathrm{dc}}i_{\mathrm{L1}}}(s) \times i_{\mathrm{1ref}} \,. \tag{14}$$

When (14) is substituted into (1) and $\lambda = \mathrm{SoC}_i^{\,n} / r^n$, the following is derived when (3)–(6) are considered:

$$i_{\mathrm{ref}} = (k_{\mathrm{up}} + \frac{k_{\mathrm{ui}}}{s}) \cdot \lambda \cdot (u_{\mathrm{dcref}} - G_{u_{\mathrm{dc}}i_{\mathrm{L}}} \cdot i_{\mathrm{ref}}) \,. \tag{15}$$

Then, (15) can be rewritten as

$$\frac{i_{\mathrm{ref}}}{u_{\mathrm{dcref}}} = \frac{(k_{\mathrm{up}} + \frac{k_{\mathrm{ui}}}{s}) \cdot \lambda}{1 + G_{u_{\mathrm{dc}}i_{\mathrm{L}}} \cdot \lambda \cdot (k_{\mathrm{up}} + \frac{k_{\mathrm{ui}}}{s})} \,. \tag{16}$$

Therefore, the open-loop transfer function of the system $G(s)H(s)$ can be expressed as

$$G(s)H(s) = G_{u_{\mathrm{dc}}i_{\mathrm{L}}} \cdot \lambda \cdot (k_{\mathrm{up}} + \frac{k_{\mathrm{ui}}}{s}) \,, \tag{17}$$

where

$$G_{u_{dc}i_{L1}}(s)=\frac{-L_1^2I_{L1}C_{dc}s^2+[(1-D_4)L_1C_{dc}U_{dc}-\frac{I_{L1}L_1^2}{R}]s+\frac{(1-D_4)L_1U_{dc}}{R}}{L_1C_{dc}^2U_{dc}s^2+[\frac{2L_1C_{dc}U_{dc}}{R}+3(1-D_4)I_{L1}L_1C_{dc}]s+\frac{3(1-D_4)I_{L1}L_1}{R}+\frac{L_1U_{dc}}{R^2}}.$$

Stability analysis based on root locus can be conducted according to (17). The system parameters are provided in Table 1. Fig. 8 shows the root locus of the system with different λ values. As shown in Fig. 8, when $0<\lambda<153$, the system meets the stability requirements. When n = 4 and n = 6 are used as examples, the values of r satisfy the following expressions:

$$\begin{cases}\mathrm{SoC}_i/r\le 3.5 & \mathrm{n}=4\\ \mathrm{SoC}_i/r\le 2.3 & \mathrm{n}=6\end{cases}. \tag{19}$$

B. Control Scheme for Charging Power Distribution

Fig. 9 shows the control structure of charging power distribution based on the nth order of the SoC. In the two-stage charging process, two energy storage modules are assumed to be connected in parallel to the DC side. The charging power of the two modules can be derived by disregarding the influence of power correction on the control system.

The reference value of converter 1 for current control can be expressed as

$$i_{1\mathrm{ref}}=\frac{(P_C-\overline{m_1}U_{b1}I_{b1})\cdot\frac{1}{\mathrm{SoC}_1^{\,n}}}{3\sum_{i=1}^{2}\frac{1}{\mathrm{SoC}_i^{\,n}}\cdot U_{b1}}. \tag{20}$$

The reference value of converter 2 for current control can be expressed as

$$i_{2\mathrm{ref}}=\frac{(P_C-\overline{m_2}U_{b2}I_{b2})\cdot\frac{1}{\mathrm{SoC}_2^{\,n}}}{3\sum_{i=1}^{2}\frac{1}{\mathrm{SoC}_i^{\,n}}\cdot U_{b2}}, \tag{21}$$

where m_i is shown as

$$m_i=\begin{cases}1\\0\end{cases}. \tag{22}$$

When the ith module operates normally in the constant current charging stage, the value of m_i should be set as $m_i=1$. When the ith module operates in the constant voltage charging stage or exits work, the value of m_i should be set as $m_i=0$.

In charging mode, if the SoC of the battery is within the normal operating range, then the voltage values of the battery are close to one another and can be approximated as

$$u_{b1}=u_{b2}. \tag{23}$$

The charging power of the battery in module1 can be expressed as

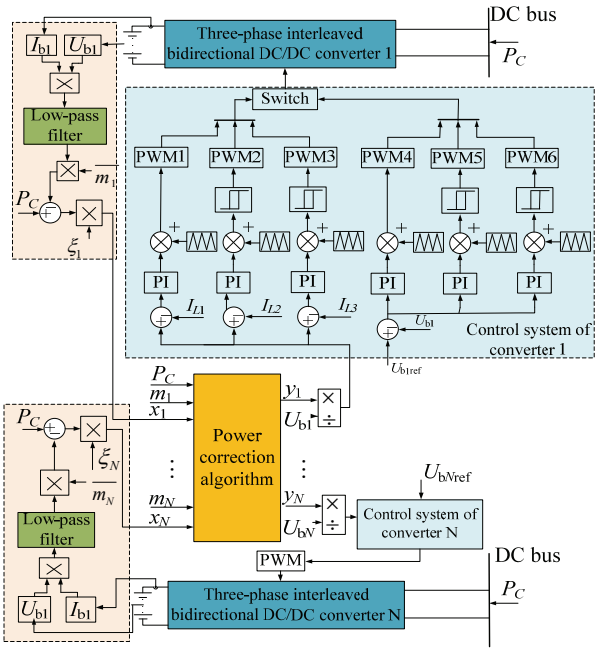


Fig. 9. Overall control diagram of charge power distribution.

$$P_1=3i_{1\mathrm{ref}}u_{b1}. \tag{24}$$

The charging power of the battery in module2 can be expressed as

$$P_2=3i_{2\mathrm{ref}}u_{b2}. \tag{25}$$

From (20) to (25), P_1 and P_2 can be derived as

$$\frac{P_1}{\mathrm{SoC}_2^{\,n}}=\frac{P_2}{\mathrm{SoC}_1^{\,n}}. \tag{26}$$

This conclusion is extended to the following:

$$\frac{P_1}{\frac{1}{\mathrm{SoC}_1^{\,n}}}=\frac{P_2}{\frac{1}{\mathrm{SoC}_2^{\,n}}}=\cdots=\frac{P_N}{\frac{1}{\mathrm{SoC}_N^{\,n}}}. \tag{27}$$

Therefore, when the BESS is operating in charge mode, the power of the battery is inversely proportional to the nth order of the SoC. The battery with high SoC receives less power. Finally, each module achieves equal charging power with a rapid rate. Modules in the constant voltage charging stage should exit the power distribution mode.

Similar to the discharging mode, the power distribution control for the charging process can be divided into two modes according to the comparison between the charging power of BESS P_C and the rated power of BESS P_E.

1) $P_C \ge P_E$:

Each module charges with the rated power.

2) $P_C < P_E$:

When the battery is in constant current charging state, charging power is distributed by the SoC. However, the assigned power P_i of a module exceeds the rated power. The assigned power can be derived as

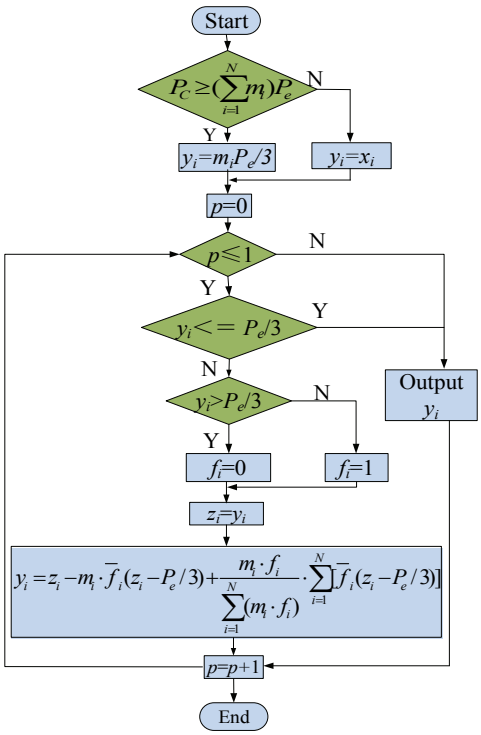


Fig. 10. Flowchart of the power correction algorithm.

$$P_i = P_C \cdot \frac{m_i \cdot \frac{1}{\mathrm{SoC}_i^{\,n}}}{\sum_{i=1}^{N}(m_i \cdot \frac{1}{\mathrm{SoC}_i^{\,n}})} \qquad i = 1, 2, \cdots N \,. \tag{28}$$

To prevent the assigned power from exceeding the rated power of each module, this study presents a power correction algorithm. The process is illustrated in Fig. 10. The specific process is described as follows.

Step 1: Whether P_C is greater than or equal to $(\sum_{i=1}^{N} m_i)P_e$, where P_e is the rated charging power of each module, is determined. If $P_c \geq (\sum_{i=1}^{N} m_i)P_e$, then $y_i = m_i \cdot P_e/3\,, i = 1,2,\cdots N$; else, $y_i = x_i, i = 1,2,\cdots N$.

Step 2: The initial value p = 0 is given. If $\mathrm{p} \leq 1$, then the next step is performed; otherwise, $y_i (i = 1,2,\cdots N)$ is outputted, and the correction process ends.

Step 3: Whether y_i is less than or equal to $P_e/3$ is determined. If $y_i \leq P_e/3$, then correcting the power is unnecessary. $y_i, i = 1,2,\cdots N$ is outputted, and the correction process ends; otherwise, the next step is performed.

Step 4: If $y_i > P_e/3$, then variable $f_i = 0 (i = 1,2,\cdots N)$; otherwise, let variable $f_i = 1 (i = 1,2,\cdots N)$.

Step 5: The values of y_i to z_i are assigned, and the parameters are substituted into the following formula to obtain the corrected power value:

$$y_i = z_i - m_i \cdot \overline{f}_i(z_i - P_e/3) + \frac{m_i \cdot f_i}{\sum_{i=1}^{N}(m_i \cdot f_i)} \cdot \sum_{i=1}^{N}[\overline{f}_i(z_i - P_e/3)] \,.$$

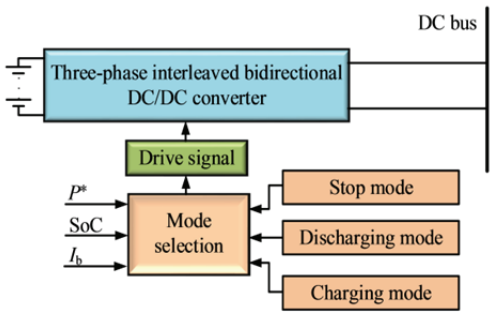


Fig. 11. Operating modes of the BESS.

Step 6: Let $\mathrm{p} = \mathrm{p} + 1$, and return to Step 2.

The corrected power value is used as the input variable of the control system to realize constant current control. When the SoC reaches the limit value, the module that enters constant voltage charging mode exits power distribution mode, whereas the other modules continue to operate in distribution mode.

To make the BESS work in normal operation during the charging process, the control parameters in the charging state should be limited.

(1) Limitation of battery SoC in each module

When SoC_i does not exceed 90%, the module operates in constant current charging mode; when SoC_i exceeds 90%, the module operates in constant voltage charging mode and exits power distribution mode.

(2) Limitation of equalization rate

Similar to discharging mode, the selection of exponent n depends on the requirements of the equalization rate of power [12].

C. Power Distribution Control Scheme for Charging and Discharging Switching Processes

In this study, the power distribution control scheme in charging and discharging transition is designed further. Fig. 11 shows its control structure. The operating mode of the BESS is determined by power command P^*, the SoC, and the current I_b of the battery. When the discharging direction is positive, the specific methods for switching are as follows.

1) $P^* > 0$ *:*

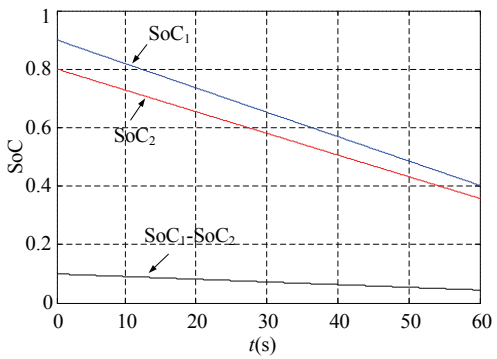
If $\mathrm{SoC} > \mathrm{SoC}_{\min}$, then the BESS discharges with the power distribution control scheme in discharging mode. When the battery reaches the discharging limit $\mathrm{SoC} = \mathrm{SoC}_{\min}$, then the BESS stops working.

2) $P^* < 0$ *:*

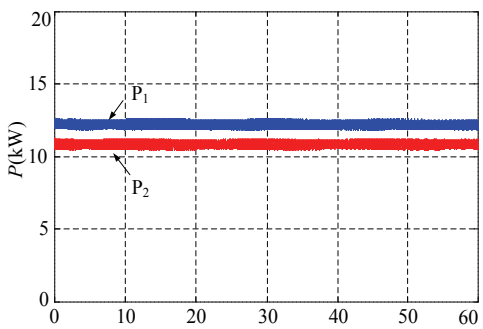
If $\mathrm{SoC} < \mathrm{SoC}_{\mathrm{cv}}$, then the BESS charges with the power distribution control scheme in charging mode. If $\mathrm{SoC} = \mathrm{SoC}_{\mathrm{cv}}$, then the BESS works in constant voltage mode. If $\mathrm{SoC} = \mathrm{SoC}_{\max}$, then the battery finishes charging and the BESS stops power distribution.

TABLE I
SYSTEM PARAMETERS

Parameter	Value
$SoC_{1,t=0}$/%	90
$SoC_{2,t=0}$/%	80
Battery rated voltage U_b/V	200
DC bus reference voltage U_{dcref}/V	700
DC bus side capacitance C_{dc}/uF	2000
Inductance for energy storage L/mH	2
Switching frequency/kHz	10
Load resistance/Ω	24.5
Load power/kW	20



(a)



(b)

Fig. 12. Waveforms of the SoC and power based on traditional proportional distribution: (a) SoC waveform, (b) Power waveform.

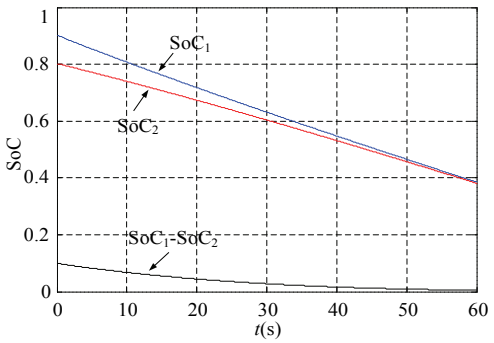
IV. SIMULATION VERIFICATION

A. Simulation of the Control Scheme for Discharge Power Distribution

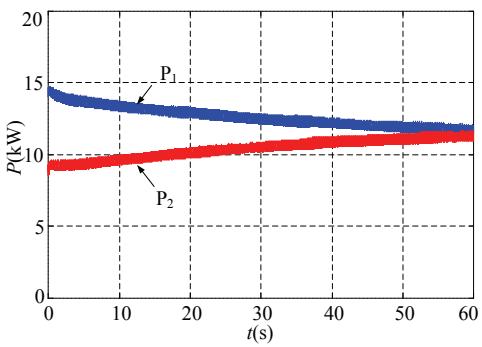
A MATLAB/Simulink model is established to verify the theoretical analysis. The system parameters of this simulation are provided in Table I.

Fig. 12 shows the SoC and power waveforms with the traditional proportional distribution method-based SoC. The results show that the SoC and output power of each energy storage module gradually converge at a slow rate.

Simulations are performed in the case of two modules



(a)



(b)

Fig. 13. Waveforms of the SoC and output power when n = 4: (a) SoC waveform, (b) Power waveform.

connected in parallel to evaluate the performance of the discharging power distribution method based on the nth order of the SoC. Exponent n is set as 4 and 6. The model parameters are provided in Table 1. The comparison of Figs. 13 and 14, shows that the proposed method is remarkably faster than the traditional proportional distribution method, and a faster dynamic process of power sharing equalization is achieved with a larger exponent n. This result is in accordance with the theoretical analysis.

From (1) and (2), when a compensation coefficient does not exists, the SoC (0<SoC<1) gradually decreases with the discharging of the battery, thereby increasing the tracking error of the current reference, which causes the DC bus voltage to drop (Fig. 15). To maintain DC bus voltage stability and strengthen the control of the voltage loop over DC bus voltage, a DC bus voltage compensation coefficient r is introduced. SoC_i^n/r^n is the correction parameter of the current reference value, and $SoC_i^n/r^n \geq 1$. The steady-state error decreases by multiplying this correction parameter, and then the bus voltage stabilizes. Fig. 16 shows that the DC bus voltage can remain stable after adding the compensation coefficient.

In the discharging process of the BESS, some modules may exit the system due to battery or inverter failure or other reasons. A module can reconnect with the system once the system returns to its normal state. Fig. 17 shows the transient operation characteristics of the system when a certain module

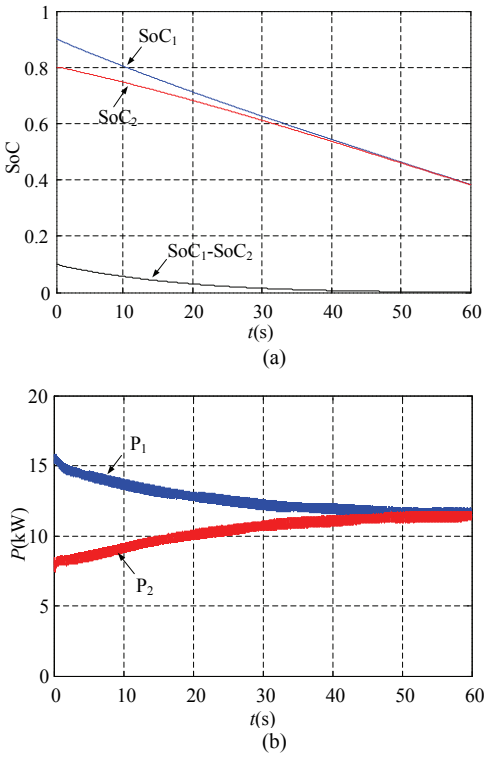


Fig. 14. Waveforms of the SoC and output power when n = 6: (a) SoC waveform, (b) Power waveform.

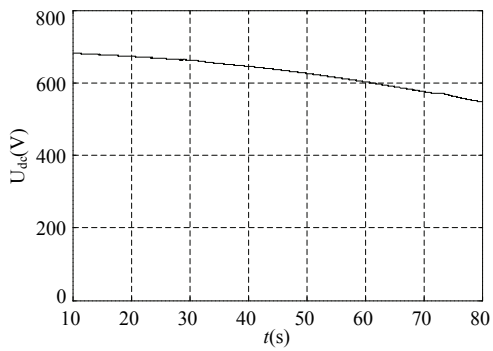


Fig. 15. Bus voltage before adding the compensation coefficient.

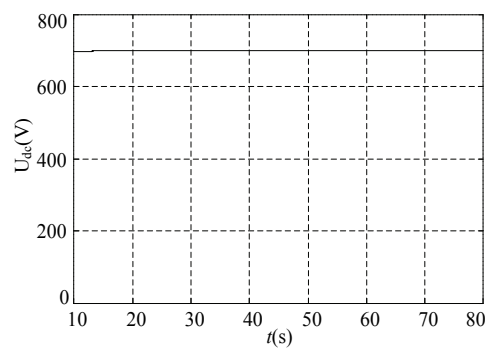


Fig. 16. Bus voltage after adding the compensation coefficient.

is cut off and then reconnected. The results indicate that the output power of the three energy storage modules tend to be equal in normal operation mode. At 20 s, module 3 is cut off,

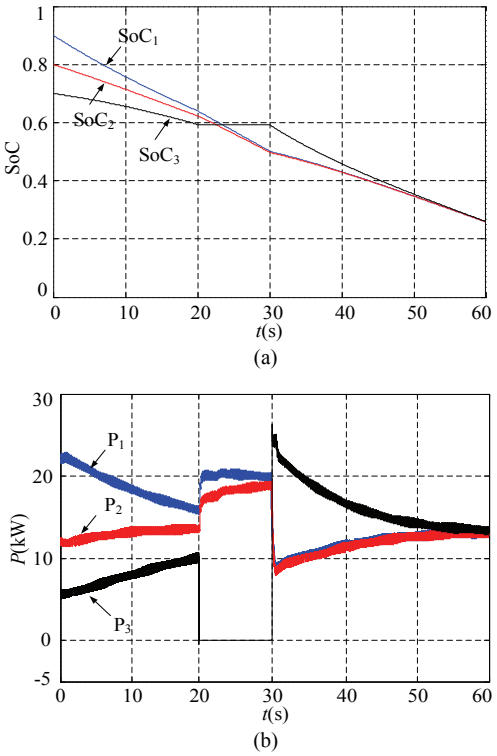


Fig. 17. Waveforms of the SoC and power when multiple modules are parallel with the transient operation: (a) SoC waveform, (b) Power waveform.

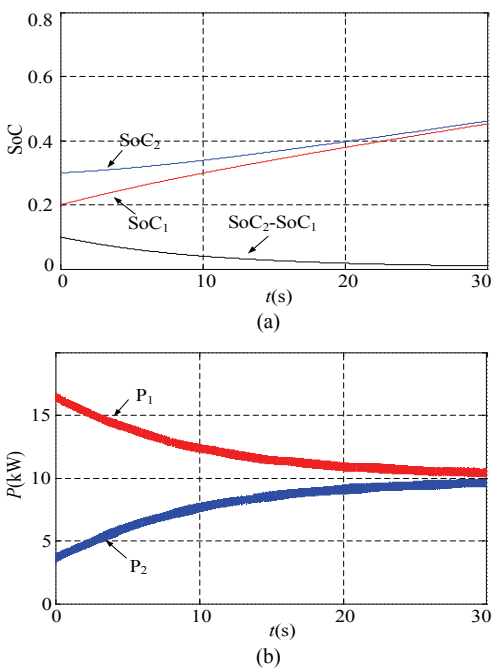


Fig. 18. Waveforms of the SoC and charging power when n = 4: (a) SoC waveform, (b) Power waveform.

and load power is supplied by modules 1 and 2. During this process, modules 1 and 2 can still realize power distribution using the proposed control method. At 30 s, module 3 is reconnected with the system, and the three converters can

TABLE II
SYSTEM PARAMETERS

Parameter	Value
$SoC_{1,t=0}$/%	20
$SoC_{2,t=0}$/%	30
Charging power/kW	20

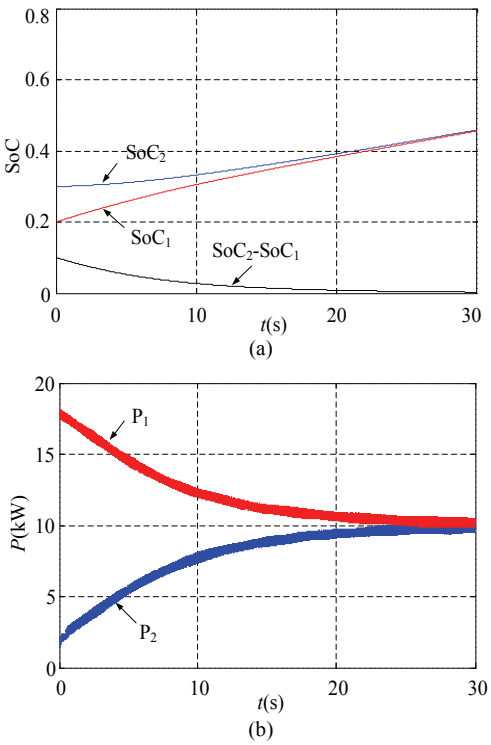


Fig. 19. Waveforms of the SoC and charging power when n = 6: (a) SoC waveform, (b) Power waveform.

redistribute power dynamically. The results indicate that the output powers of the three converters tend to be equal, and they satisfy the design requirements for the control system.

B. Simulation of the Control Scheme for Charge Power Distribution

Simulations are performed in the case of two modules connected in parallel to evaluate the performance of the charging power distribution method. Table 2 provides the system parameters.

Figs. 18 and 19 reflect the SoC of the battery and power changes of the BESS when exponent n is set as 4 and 6, respectively. This finding indicates that the distribution rate of charging power is positively correlated to exponent n.

Similar to the discharging process, some modules may be cut off or reconnected during the charging process. Fig. 20 shows the transient operation characteristic of the BESS. The charging powers of the three energy storage modules in normal operation gradually become equal when the proposed control method is used. At 20 s, module 3 is cut off, and load power supply comes from modules1 and 2. During this

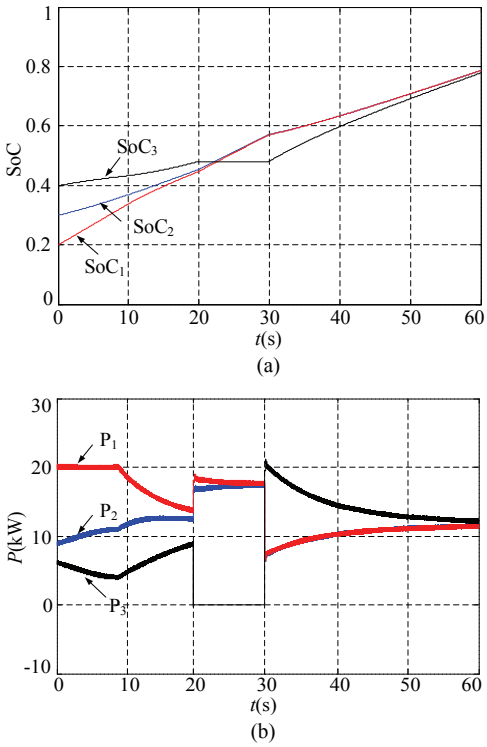


Fig. 20. Waveforms of the SoC and power when multiple modules are parallel with the transient operation: (a) SoC waveform, (b) Power waveform.

TABLE III
SYSTEM PARAMETERS

Parameter	Value
$SoC_{1,t=0}$/%	73.5
$SoC_{2,t=0}$/%	64.5
$SoC_{3,t=0}$/%	57
Resistance of inductance R/Ω	0.2
Load power (0–6 s)/kW	45
Load power (6–16 s)/kW	35
Charging power (16–26 s)/kW	30
Charging power (26–36 s)/kW	40
Load power (36–56 s)/kW	40

process, modules1 and 2 can still realize power distribution using the proposed control method. At 30 s, module 3 is reconnected with the system, and the three converters can redistribute power dynamically. The results show that the output powers of the three converters tend to be equal, thereby satisfying the design requirements for the control system.

C. Simulation of Power Distribution Control Scheme for the Charging and Discharging Switching Processes

Simulations are performed in the case of the three modules connected in parallel to evaluate the performance of the power distribution method in the charging and discharging switching processes. The parameters are provided in Table 3.

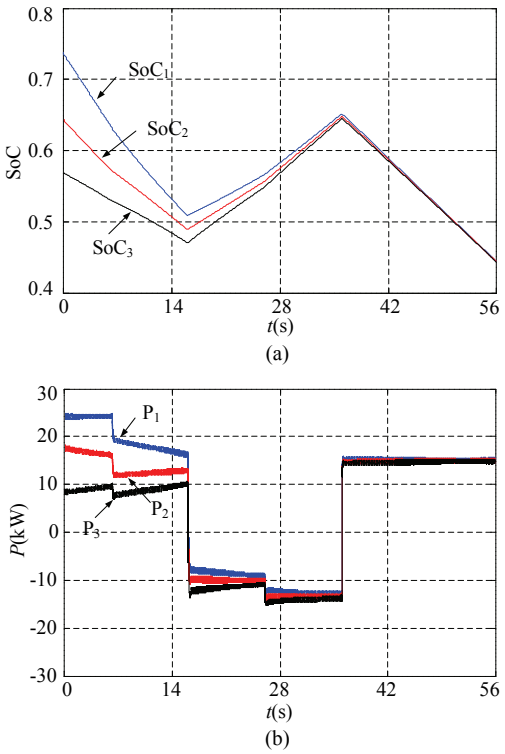


Fig. 21. Waveforms of the SoC and power when the energy storage modules are in charging and discharging states: (a) SoC waveform, (b) Power waveform.

Fig. 21 shows the SoC of the battery and the power of the BESS. The BESS can track charging and discharging powers during the processes of conversion of load power, operation mode, and charging power.

V. Conclusion

A power distribution control scheme based on the *n*th order of the SoC is proposed to achieve dynamic SoC balance and to increase the power equalization rate of energy storage modules in a BESS. Ultimately, the SoCs of the studied battery sets tend to be equal. Charging and discharging operation modes are considered. The voltage compensation coefficient ensures the stability of the bus voltage during the discharging process. The proposed power correction algorithm can guarantee that the power assigned to each module will not exceed the rated power during the charging process.

References

[1] A. Riccardo, C. Egidio, D. Elia, and T. Paolo, "Overview on recent developments in energy storage: Mechanical, electrochemical and hydrogen technologies," *Energy Convers. Manag.,* Vol. 132, No. 15, pp. 372-387, Jan. 2017.

[2] R. Hemmati and H. Saboori, "Emergence of hybrid energy storage systems in renewable energy and transport applications – A review," *Renewable and Sustainable Energy Reviews,* Vol. 65, pp.11-23, Nov. 2016.

[3] X. S. Zhou, Y. T. Lin, and Y. J. Ma, "The overview of energy storage technology," in *Proc. ICMA*, pp. 43-48, 2015.

[4] K. C. Divya, and J. Ostergaard, "Battery energy storage technology for power systems – An overview," *Electric Power Syst. Res.,* Vol. 79, No. 4, pp. 511-520, Apr. 2009.

[5] M. T. Lawder, B. Suthar, P. W. C. Northrop, S. De, C. M. Hoff, O. Leitermann, M. L. Crow, S. Santhanagopalan, and V. R. Subramanian, "Battery energy storage system (BESS) and battery management system (BMS) for grid-scale applications," in *Proc. IEEE*, pp. 1014-1030, 2014.

[6] J. Li, S. Xu, and D. Hui, "A review of hundred MW level energy storage power station's multi-parallel PCS's stability analysis and control strategy," in *Proc. CSEE*, pp. 4034-4046, 2016.

[7] Y. W. Sun, J.M. Liu, Y. G. Li, C. Fu, and Y. Wang, "A coordinative control strategy for power electronic transformer based battery energy storage systems," *J. Power Electron.*, Vol. 17, No. 6, pp. 1625-1636, Nov. 2017.

[8] K. Jin and C. Liu, "A novel PWM high voltage conversion ratio bidirectional three-phase DC/DC converter with Y-Delta connected transformer," *IEEE Trans. Power Electron.*, Vol. 31, No. 1, pp. 81-88, Jan. 2016.

[9] A. A. Abosnina and G. Moschopoulos, "Three-phase DC-DC PWM boost converter for renewable energy applications," in *Proc. INTELEC*, pp. 447-454, 2017.

[10] O. Palizban and K. Kauhaniemi, "Power sharing for distributed energy storage systems in AC microgrid: Based on state-of-charge," in *Proc. APPEEC*, 2015.

[11] K. A. Wang, X. J. Wu, F. J. Deng, and F. Liu, "A dynamic power distribution strategy for large-scale cascaded photovoltaic systems," *J. Power Electron.*, Vol. 17, No. 5, pp. 1317-1326, Sep. 2017.

[12] B. Zhao, Q. Yu, L. Wang, and Y. Xiao, "Parallel grid-connected system of non-master-slave and current-sharing battery energy storage," *Autom. Electric Power Syst.*, Vol. 36, No. 21, pp. 108-117, Nov. 2012.

[13] L. M. Tolbert, F. Z. Peng, T. Cunnyngham, and J. N. Chiasson, "Charge balance control schemes for cascade multilevel converter in hybrid electric vehicles," *IEEE Trans. Ind. Electron,* Vol. 49, No. 5, pp. 1058-1064, Oct. 2002.

[14] Y. Jin, Q. Song, and W. Liu, "Large scaled cascaded battery energy storage system with charge/discharge balancing," *Electric Power Autom. Equipment*, Vol. 31, No. 3, pp. 6-11, Mar. 2011.

[15] Y. Xu, X. Xiao, Y. Sun, and Y. Long, "Large-capacity cascaded bipolar BESS and its control strategy," *Electric Power Autom. Equipment*, Vol. 36, No. 8, pp. 103-109, Aug. 2016.

[16] H. Kakigano, A. Nishino, Y. Miura, and T. Ise, "Distribution voltage control for DC microgrid by converters of energy storages considering the stored energy," *in Proc. ECCE*, pp. 2851-2856, 2010.

[17] L. Maharjan, T. Yamagishi, and H. Akagi, "Active-power control of individual converter cells for a battery energy storage system based on a multilevel cascade PWM converter," *IEEE Trans. Power Syst,* Vol. 27, No. 3, pp. 1099-1107, Mar. 2012.

[18] S. Anand, B. G. Fernandes, and J. Guerrero, "Distributed control to ensure proportional load sharing and improve voltage regulation in low-voltage DC microgrids," *IEEE Trans. Power Electron*, Vol. 28, No. 4, pp. 1900-1912, Apr. 2013.
[19] F. Tang, J. Jiang, W. Dan, X. Zhou, and J. Mguerrero, "Active power coordinated control considering SoC of battery energy storage system," *Autom. Electric Power Syst*., Vol. 39, No. 22, pp. 30-36, Nov. 2015.
[20] X. Lu, K. Sun, J. M. Guerrero, J. C. Vasquez, and L. Huang, "State-of-Charge balance using adaptive droop control for distributed energy storage systems in DC microgrid applications," *IEEE Trans. Ind. Electron,* Vol. 61, No. 6, pp. 2804-2815, Jun. 2014.
[21] X. Lu, K. Sun, J. M. Guerrero, J. C. Vasquez, and L. Huang, "Double-quadrant State-of-Charge based droop control method for distributed energy storage systems in autonomous DC microgrids," *IEEE Trans. Smart Grid*. Vol. 6, No. 1, pp. 147-157, Jan. 2015.
[22] X. D. Guo, B. M. Ge, D. Q. Bi, and X. Y. Yang, "Control method of parallel vanadium batteries operating in energy stored wind farm system," *Advanced Technol. Electrical Eng. Energy*, Vol. 32, No. 2, pp. 34-39, Apr. 2013.
[23] Y. S. Lin, K. W. Hu, T.H. Yeh, and C. M. Liaw, "An electric-vehicle IPMSM drive with interleaved front-end DC/DC converter," *IEEE Trans. Veh. Technol.*, Vol. 65, No.5, pp. 4493-4504, May. 2015.
[24] C. M. Lai, Y. C. Lin, and D. Lee, "Study and implementation of a two-phase interleaved bidirectional DC/DC converter for vehicle and DC-microgrid systems," *Energies*, Vol. 8, No. 9, pp. 9969-9991, Sep. 2015.
[25] Y. F. Wang, L. K. Xue, C. S. Wang, P. Wang, and W. Li, "Interleaved high conversion ratio bidirectional DC-DC converter for distributed energy storage systems circuit generation, analysis, and design," *IEEE Trans. Power Electron*., Vol. 31, No. 8, pp. 5547-5561, Aug. 2016.

Bing Xie was born in Shenyang, China. He obtained his B.S. and M.S. in Agricultural Electrification and Automation from Shenyang Agricultural University, Shenyang, China in 2008 and 2013, respectively. He is currently working toward a Ph.D. in the School of Electrical Engineering and Automation, Harbin Institute of Technology, Harbin, China. His current research interests include the modeling and control of bidirectional converters and battery energy storage systems.

Jianze Wang was born in China. He obtained his B.S., M.S., and Ph.D. in Electrical Engineering from Harbin Institute of Technology, Harbin, China, in 1993, 1996, and 1999, respectively. He has been with the Department of Electrical Engineering, Harbin Institute of Technology, where he is currently a research professor, since 2007. His current research interests include power electronics, multilevel converters, and digital signal processor-based power quality control systems.

Yu Jin was born in Heilongjiang, China. He obtained his B.S. in Electrical Engineering from Harbin Institute of Technology, Harbin, China in 2011. He is currently working toward a Ph.D. in the School of Electrical Engineering and Automation, Harbin Institute of Technology, Harbin, China. His current research interests include the control strategy and analysis of stability of cascaded H-bridge/module multilevel converter STATCOM.

Yanchao Ji was born in China. He obtained his B.S. and M.S. in Electrical Engineering from Northeast Electric Power University, Jilin, China in 1983 and 1989, respectively, and his Ph.D. in Electrical Engineering from North China Electric Power University, Beijing, China in 1993. He has been with the Department of Electrical Engineering, Harbin Institute of Technology, Harbin, China, where he is currently a professor, since 1993. His current research interests include power converter topologies and flexible AC transmission system devices.

Chong Ma was born in Dalian, China. She obtained her B.S. and M.S. in Electrical Engineering and Agricultural Electrification and Automation from Shenyang Agricultural University, Shenyang, China in 2010 and 2013, respectively. She has been with the State Grid Fushun Electric Power Supply Company, Fushun, China, where she is currently an engineer, since 2013. Her current research interests include power system relay protection and power electronics applications.