JPE 18-4-24

https://doi.org/10.6113/JPE.2018.18.4.1223
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

Mitigation of Voltage Unbalances in Bipolar DC Microgrids Using Three-Port Multidirectional DC-DC Converters

Taha Ahmadi*, Esmaeel Rokrok†, and Mohsen Hamzeh**

†,*Department of Electrical and Electronics Engineering, Lorestan University, Lorestan, Iran
**School of Electrical and Computer Engineering, College of Engineering, University of Tehran, Tehran, Iran

Abstract

In this paper, a new three-port multidirectional DC-DC converter is proposed for integrating an energy storage system (ESS) to a bipolar DC microgrid (BPDCMG). The proposed converter provides a voltage-balancing function for the BPDCMG and adjusts the charge of the ESS. Thanks to the multi-functional operation of the proposed converter, the conversion stages of the system are reduced. In addition, the efficiency and weight of the system are improved. Therefore, this converter has a significant capability when it comes to use in portable BPDCMGs such as electric DC ships. The converter modes are analyzed and small-signal models of the converter in each of the independent modes are extracted. Finally, comprehensive simulation studies are carried out and a BPDCMG laboratory prototype is implemented in order to verify the performance of the proposed voltage balancer using the burst mode control scheme.

Key words: Bipolar DC microgrid, Line voltage unbalance rate, Multidirectional converters, Three-port converters (TPCs), Voltage balancer

I. INTRODUCTION

DC microgrids, when compared to AC microgrids, have received a lot of attention in the pursuit of operational solutions for new structure energy delivery problems. There are many power quality issues encountered with DC microgrids such as DC voltage drop, voltage oscillations, circulating current and voltage fluctuations. These issues have been carefully considered and have been discussed in previous studies [1], [2]. DC microgrids are categorized into two types [3]: unipolar-type and bipolar-type [4]. Unipolar DC microgrids have one voltage level in a two-wire DC distribution network. On the other hand, BPDCMG type microgrids have two voltage levels in a three-wire DC distribution network (positive, neutral, and negative). BPDCMGs are more reliable due to the possibility of supplying loads under abnormal operating conditions such as the loss of one polarity. As a result, in Intel and IBM data centers, power distributions of ± 190V or ± 200V have been utilized, in order to increase the reliability of the power supplies [5]. A BPDCMG can also increase the power transmission capability and overall efficiency of systems due to their lower current levels. In addition to the advantages of the BPDCMG, it also has some challenges. In fact, when loads are connected to the upper and lower terminals, they may have different powers. Therefore, the voltage of the terminals may drift from the rated value, which results in a voltage imbalance in BPDCMGs [6]. To quantify this voltage imbalance, the line voltage unbalances rate equation (LVUR) is utilized [7].

$$LVUR_{DC}\% = \frac{\text{voltagePole deviation}}{\text{avg pole voltage}} \times 100 = \frac{|V_1 - V_2|}{\frac{V_1 + V_2}{2}} \times 100 \quad (1)$$

Where V_1 and V_2 are the positive and negative buses voltages. The voltage unbalance and voltage drop are closely

Manuscript received Nov. 9, 2017; accepted Feb. 13, 2018
Recommended for publication by Associate Editor Kai Sun.
†Corresponding Author: rokrok.e@lu.ac.ir
Tel: +98-66-33120005, Lorestan University
*Dept. of Electrical and Electronics Engineering, Lorestan University, Iran
**School of Electr. and Comp. Eng., College of Eng., Univ. of Tehran, Iran

© 2018 KIPE

related to the power quality in distribution systems. In [8], a technique for voltage regulation in BPDCMGs that employs neutral to line drop compensation is used to restrain the LVUR. This method uses the neutral current and neutral line equivalent impedance to solve the neutral line potential fluctuation. In [9]-[12], the effects of an imbalanced voltage in the BPDCMG are presented and various interlink converters (IC) have been proposed to mitigate them. In [5], various voltage balancer circuits have been proposed. The IC structure is composed of a voltage balancer in series with a voltage-source inverter (VSI). However, these circuits tend to only balance the voltage at one end of the BPDCMG. A number of disadvantages can be found in these papers. 1) There is a reduction of system reliability (which is one of the main features of BPDCMGs) due to supplying loads using a single converter. 2) Due to a series connection of the VSI and the voltage balancer, the power of the voltage balancer should be equal to that of the VSI. 3) In the island mode, when the IC is disconnected from the power grid, the voltage balancer control system should be switched to the island mode, which causes significant voltage transients [13]. 4) In a BPDCMG with a long feeder length, these methods cannot bring the neutral line current to zero. A new structure has been proposed in [6] to compensate for these issues. In this structure, each of the distribution generator (DG) units provides the voltage-balancing function in addition to the interlink converter connected to the BPDCMG. Although this topology improves voltage balancing, due to the increasing number of converters, the system efficiency (which is also another main advantage of bipolar DC microgrids) is decreased.

To overcome the above-mentioned problems, an interleaved dc-dc converter was introduced in [7] to mitigate the unbalanced voltage. In [14], the concept of the BPDCMG was introduced. In this configuration, it is assumed that the voltage control units are distributed on the positive and negative buses. Therefore, a new configuration for the two-layer control strategy is applied on the IC converter in order to balance and manage the power. The authors of [15] focused on comparing single half-bridge and three phase half-bridge current redistributors. A new half-bridge voltage, which can adjust the unequal voltage between the positive and the negative terminals, is described in [16]. In [17], a method is introduced to mitigate the voltage unbalance and to reduce the power loss due to the neutral current in a BPDCMG by using a static load transfer switch. The advantage of these methods is that there is no need to have active sources as the compensator. In this regard, due to the fact that batteries play an important role in BPDCMGs, it is possible to achieve a new structure for the battery converter in order to mitigate unbalanced voltage in addition to charging and discharging the battery. Therefore, the benefits of this new converter are: 1) enhanced loadability of the BPDCMG due to the ability of transferring the loads of one terminal to another terminal; 2) a reduction in the number of converters by integrating the voltage balancing converter and the battery converter; 3) reductions in the current of the neutral line and its associated power losses, while the IC converters cannot eliminate the neutral line current for a BPDCMG with a long feeder length, due to the fact that they only attempt to balance the voltage at one end of the BPDCMG [7]; 4) the possibility of balancing the voltage in the island condition of the BPDCMG by disconnecting the interlink converter.

Multi-port bi-directional DC-DC converters have attracted special interest in applications where multiple energy sources are used [18]. In [19], a family of non-isolated DC-DC three-port converters (TPCs) for integrating renewable-energy sources (RESs) and energy storage systems into a DC bus has been proposed. In [20], a multi-port converter to integrate the energies of a PV panel, a fuel cell and a battery to supply local loads has been introduced. In [21], a three-port DC-DC boost converter has been introduced. The introduced converter interfaces two unidirectional input power ports and a bidirectional port for a battery. This converter can supply a load, charging or discharging a battery by the sources connected to the ports either individually or simultaneously. Since multiple voltages are required in some applications, several studies have been done for different types of single-input multiple-output converters [22]. In [23], a single-inductor dual-output boost converter has been presented. This topology can be extended to have multiple outputs and can be applied to buck, flyback and other kinds of converters. In [24], based on the flyback converter, a new three-port dc-dc converter to integrate PV and battery systems to feed loads connected to the converter has been proposed. The flyback converter has many advantaged, such as a high output voltage range, isolation of the ports voltages and a cost effective structure [25]. As can be seen, although a lot of investigation have been done on TPCs, these topologies are mostly designed to integrate multiple energy sources at certain polarities for consuming loads at other polarities and cannot transfer power from all three of the polarities to each other. Therefore, solutions for integrating batteries and BPDCMGs are still farily limited. Within this context, this paper focuses on the voltage balancing of a BPDCMG while proposes a new isolated three-port multidirectional converter by integrating a battery system with a BPDCMG, which has the ability to balance the positive and negative terminal voltages, in addition to charging and discharging the battery. The proposed three-port multidirectional converter is based on the three-port flyback converter.

II. Description of the Proposed Three-Port Multidirectional Converter

The structure of a BPDCMG is shown in Fig. 1. In the BPDCMG, loads can be connected between the positive and negative terminals, the positive and neutral terminals, and the

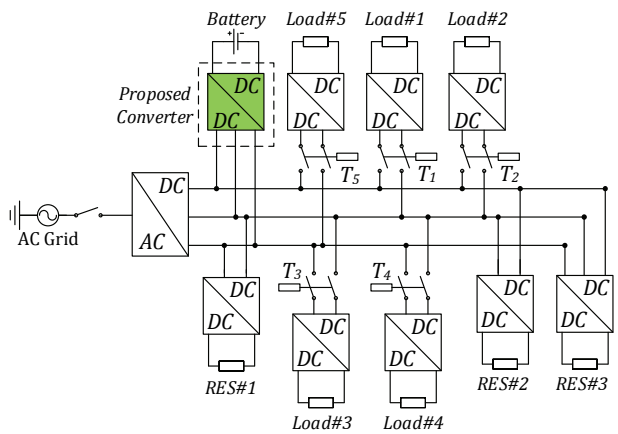


Fig. 1. Typical isolated BPDCMG with the proposed converter.

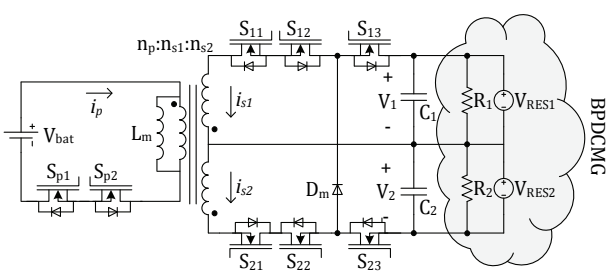


Fig. 2. Proposed three-port multidirectional converter for integrating a battery system to a BPDCMG.

negative and neutral terminals. Since the last two cases may cause voltage imbalances between the upper and lower buses, it is necessary to utilize a voltage balancing strategy. Therefore, the proposed three-port multidirectional converter is integrated into the BPDCMG to balance the voltages of the positive and negative terminals.

The proposed three-port multidirectional converter is depicted in Fig. 2. As can be seen in this figure, in the primary side of the transformer, V_{bat}, i_P and L_m stand for the ESS voltage, ESS output current and magnetization inductance. Dual secondary windings are available on the other side of the transformer. In this side, i_{s1} and i_{s2} are the currents of the secondary windings, C_1 and C_2 denote the output voltage filter capacitors, R_1 and R_2 are the equivalent load resistors of the BPDCMG, v_1 and v_2 are the output DC voltages, n_p, n_{s1} and n_{s2} denote for the primary, secondary and tertiary turns numbers.

The proposed converter was analyzed under the island operating mode of the BPDCMG. In this mode, the interplay of the battery and the RESs has a considerable role. Usually, the proposed three-port multidirectional converter operates under constant-voltage mode control, and causes additional power losses such as switching loss and conduction loss [26]. To increase the system efficiency and reliability, the proposed three-port multidirectional converter operates under the burst mode or with the skip mode control method. The burst control mode operates using the cycle-skipping method

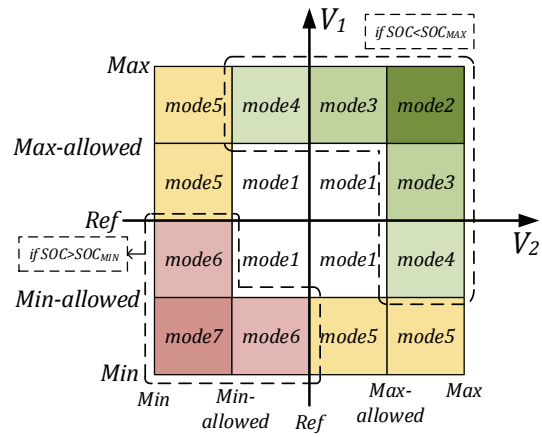


Fig. 3. Operation modes of the proposed converter.

to reduce the switching loss in a low power switching converter and to increase the operational efficiency. During cycle skipping, each skip of the switching can be started at the minimum-allowed voltage value and stopped at the maximum-allowed-voltage value [27].

Based on the burst control scheme, a similar strategy can be employed for the proposed converter in low-voltage bipolar DC microgrids. Fig. 3 shows the seven operation modes of the proposed converter for operating in the BPDCMG. To simplify the analysis of the proposed converter, it is assumed that the indexes '*I*' and '*J*' are defined as: $I \neq J \in \{1,2\}$.

A. Mode 1: Natural Balance Mode (NBM)

Based on the idea of burst mode, a two-dimensional burst mode control scheme was considered for the proposed converter. As shown in Fig. 3, when V_I and V_J are inherently kept between $V_{min\text{-}allowed}$ and $V_{max\text{-}allowed}$, the proposed converter does not operate and the battery is isolated.

B. Mode 2: Dual Input Single Output-Charging of the Battery (DISO-C)

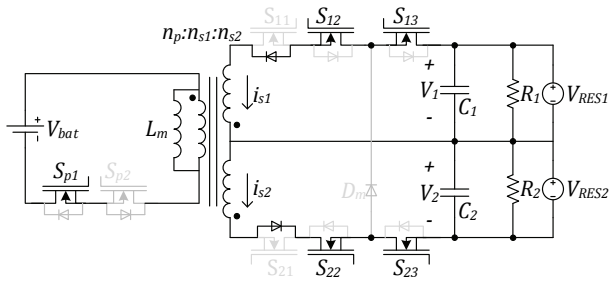
When $V_{max-allowed} < V_I, V_J < V_{max}$, the RESs generation potential is more than the load demands at any two terminals. In this condition, if the battery does not reach its maximum state of charge (SOC), it is charged by the redundant power of both the negative and positive terminals. The operation states of this mode are defined as follows (see Fig. 4):

State I: S_{12}, S_{13}, S_{22}, S_{23} and S_{p1} are turned ON. Therefore, L_m absorbs energy from V_1 and V_2.

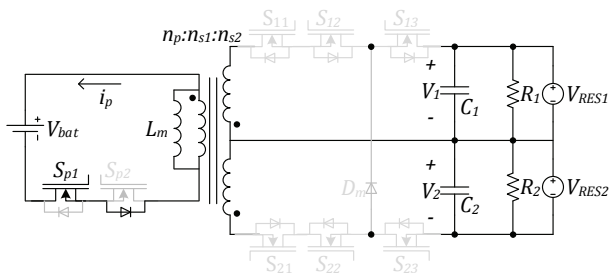
State II: S_{P1} stays ON and the absorbed energy is sent to the battery by D_{P2}.

C. Mode 3: Single Input Single Output-Charging of the Battery (SISO-C)

When $V_{ref} < V_J < V_{max-allowed}$, $V_{max-allowed} < V_I < V_{max}$ and the battery does not reach its maximum SOC, it is charged by the redundant power of terminal *'I'*. The states of this mode are defined as follows (see Fig. 5):

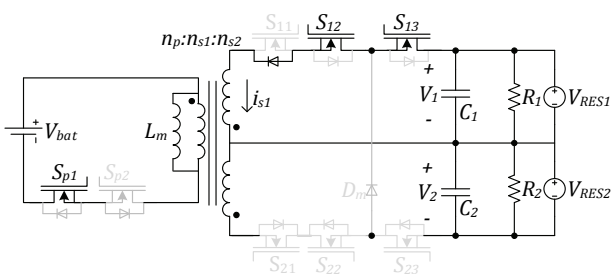


(a)

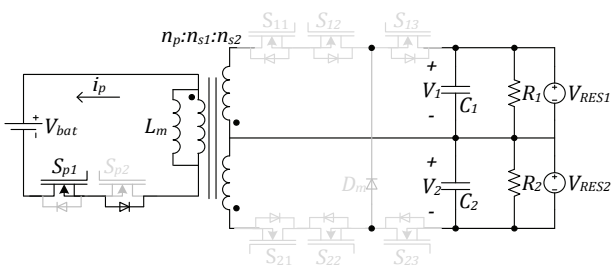


(b)

Fig. 4. States of mode 2: (a) State I; (b) State II.



(a)



(b)

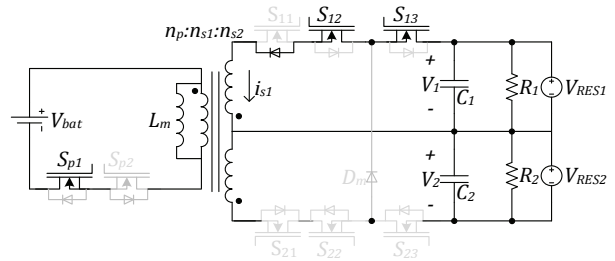
Fig. 5. States of mode 3, assuming I=1: (a) State I; (b) State II.

State I: S_{I3}, S_{I2} and S_{p1} are ON. The transformer absorbs energy from V_I.

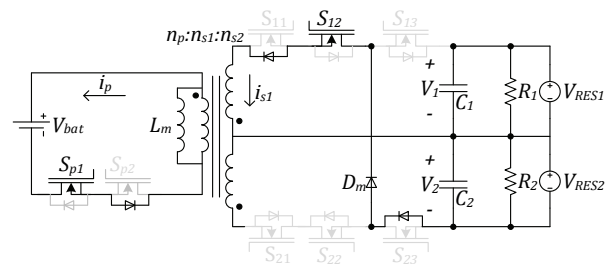
State II: S_{p1} stays ON. The transformer sends energy to charge the battery through the forward-biased D_{sp2}.

D. Mode 4: Single Input Dual Output-Charging of the Battery and Transferring of Redundant Power (SIDO-C)

When $SOC < SOC_{max}$, $V_{max-allowed} < V_I < V_{max}$ and $V_{min-allowed} < V_J < V_{ref}$, the redundant power of terminal *'I'* is transferred to both the battery and terminal *'J'*. The states of this mode are defined as follows (see Fig. 6):

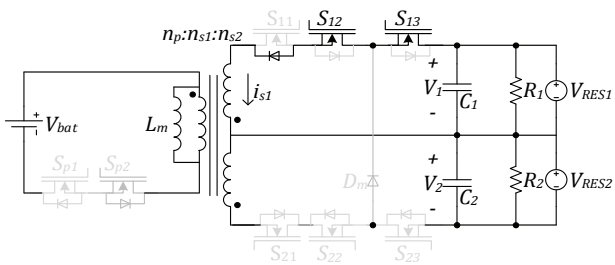


(a)

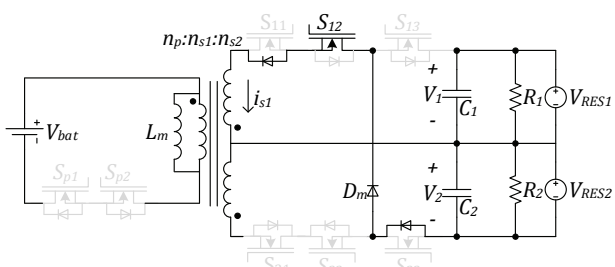


(b)

Fig. 6. States of mode 4, assuming I=1: (a) State I; (b) State II.



(a)



(b)

Fig. 7. States of mode 5, assuming I=1: (a) State I; (b) State II.

State I: S_{I3}, S_{I2} and S_{p1} are turned ON. The transformer absorbs energy from V_I.

State II: S_{p1} and S_{I2} stay ON. Therefore, the transformer sends power to charge the battery through the forward- biased D_{sp2} and terminal *'J'* through S_{I2}, D_{I1}, D_{J3} and D_m.

E. Mode 5: Single Input Single Output-Buck-Boost (SISO-B)

When $V_{max-allowed} \le V_I \le V_{max}$ and $V_{min} \le V_J \le V_{min-allowed}$, the battery is isolated from the BPDCMG. Under this condition, the proposed converter operates as a bidirectional buck-boost converter and transfers power from bus *'I'* to bus *'J'*. The states of this mode are defined

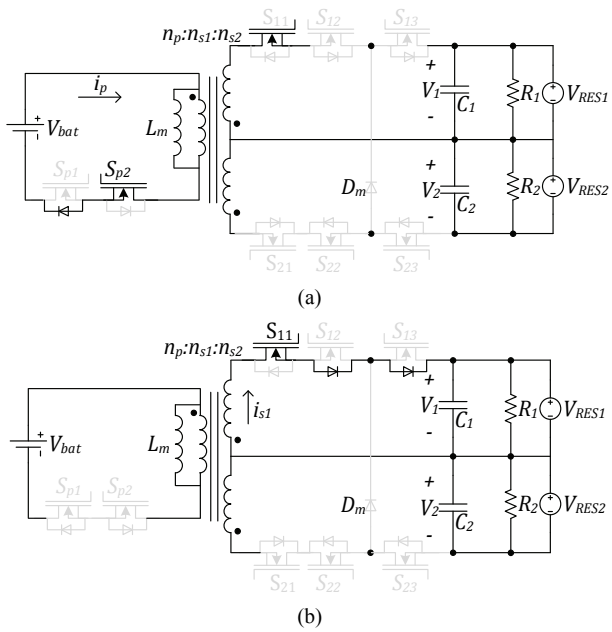


Fig. 8. States of mode 6, assuming I=1: (a) State I; (b) State II.

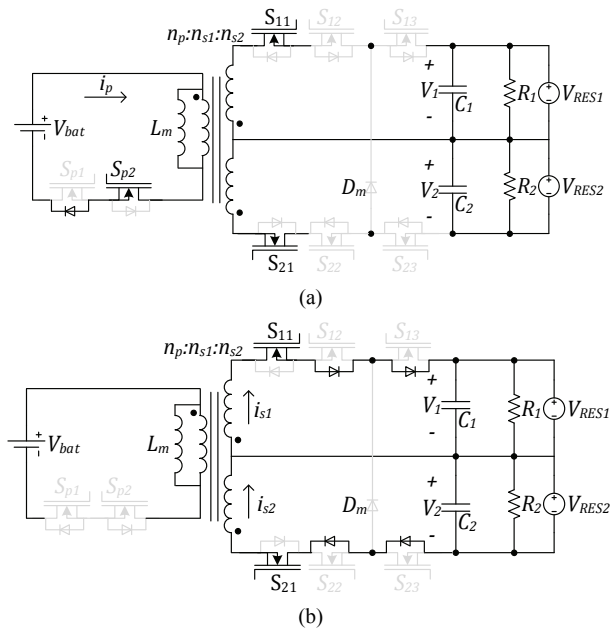


Fig. 9. States of mode 7: (a) State I; (b) State II.

as follows (see Fig. 7):

State I: S_{I2} and S_{I3} are turned ON. Therefore, the magnetizing inductor current through the transformer increases linearly.

State II: When S_{I3} is turned OFF, the transformer magnetizing inductor current continues to discharge through S_{I2}, D_{I1}, D_{J3} and D_m on the load R_J.

F. Mode 6: Single Input Single Output-Discharging of the Battery (SISO-D):

When $V_{min-allowed} \leq V_I \leq V_{ref}$, $V_{min} \leq V_J \leq V_{min-allowed}$ and $SOC \geq SOC_{min}$, the proposed converter starts to compensate the bus *'J'* voltage through discharging the battery (under the assumption that the battery can supply that amount of required power). The operation states of this mode are defined as follows (see Fig. 8):

State I: S_{J1} and S_{p2} are turned ON. The transformer magnetizing inductor current increases linearly through the battery.

State II: When S_{P2} is turned OFF, the transformer magnetizing inductor current continues to discharge through S_{J1}, D_{J2} and D_{J3}.

G. Mode 7: Single Input Dual Output-Discharging of the Battery (SIDO discharge):

When $V_{min} \leq V_I, V_J \leq V_{min-allowed}$ and $SOC \geq SOC_{min}$, to balance the upper and lower terminal voltages, the battery discharges through the buses according to the load requirements, independently. The operation states of this mode are defined as follows (see Fig. 9):

State I: S_{P2}, S_{I2} and S_{21} are ON. Therefore, L_m absorbs energy form V_{Bat}. C_1 and C_2 are discharged through R_1 and R_2.

State II: S_{I2} and S_{22} stay ON and the absorbed energy is sent to R_1 and R_2 by the transformer.

III. Average Small-Signal Model of the Proposed Converter

Fig. 10 shows a control block diagram of the proposed converter. To adjust the transient response and to meet the small steady-state error, the duty cycle to the output voltage small-signal transfer function is acquired using the average state-space method.

This transfer function is employed to obtain the frequency response of the proposed converter system. A current and voltage controller is used to improve the dynamic and steady-state behavior of the system. These equations are written for power transmission from the battery to R_1. Therefore, the state-space equations for the two states of mode 6 are derived and averaged over one switching cycle. The state variables are the voltages of the C_1 (V_1), and the inductor current (i_{Lm}). The input vector is the source voltage, which in this mode is the battery voltage (V_b).

In reference to Fig. 8(a), the state-space equation obtained from the equivalent circuit of the shoot-through state is:

$$\frac{dx}{dt} = A_1 x + B_1 u \tag{2}$$

Where:

$$x = [V_1 \quad i_{Lm}]', u = V_b$$

$$A_1 = \begin{bmatrix} \frac{-1}{R_1 C_1} & 0 \\ 0 & 0 \end{bmatrix} \quad B_1 = \begin{bmatrix} 0 \\ \frac{1}{L_m} \end{bmatrix}$$

In addition, the state-space equation in the non-shoot-through state (Fig. 8(b)) is:

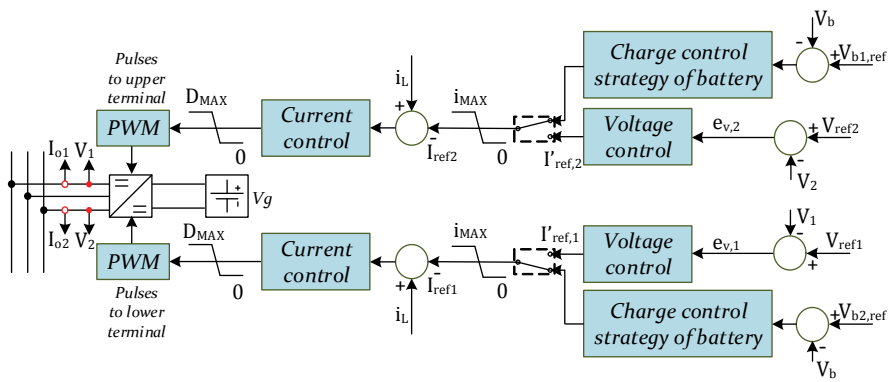


Fig. 10. Control block diagram of the proposed converter.

$$\frac{dx}{dt} = A_2 x + B_2 u \tag{3}$$

Where:

$$A_2 = \begin{bmatrix} \frac{-1}{R_1\, C_1} & \frac{N_p}{N_{s1} * C_1} \\ -\frac{N_p}{N_{s1} * L_m} & 0 \end{bmatrix} \quad B_2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$$

Averaging the state-space equations (2) and (3) over one switching cycle leads to:

$$\frac{dx}{dt} = A_{ave} x + B_{ave} u \tag{4}$$

$$A_{ave} = DA_1 + (1 - D)A_2 \tag{5}$$

$$B_{ave} = DB_1 + (1 - D)B_2 \tag{6}$$

To deduce the small-signal model of the proposed converter, (6) are perturbed (denoted by hat) around their steady-state values (denoted by capital) and the system is linearized. The small ac variations are $\hat{x}, \hat{y}$ and $\hat{d}$, which in turn cause the small ac variations *x(t)*, *y(t)* and *d(t)*, respectively. After some mathematical operations and neglecting the second-order ac terms, because of their non-considerable magnitudes, the linear small-signal model is obtained as:

$$\begin{cases} \dot{\hat{x}} = A\hat{x} + B\hat{u} + [(A_1 - A_2)X + (B_1 - B_2)U]\hat{d} \\ \hat{y} = C\hat{x} \end{cases} \tag{7}$$

Where $C = [1\ 0]'$. Therefore, the transfer function in the s-domain is represented by:

$$\begin{cases} s\hat{x}(s) = A\hat{x}(s) + B\hat{u}(s) + [(A_1 - A_2)X + (B_1 - B_2)U]\hat{d}(s) \\ \hat{y}(s) = C\hat{x}(s) \end{cases} \tag{8}$$

Since in the proposed converter, the number of turns of the transformer in each winding is equal, the transfer function of the output voltage (y) versus the inductance current (i_L), $G_v(s)$ and the inductance current (i_L) versus the duty cycle (d), $G_i(s)$ by the substituting the parameters shown in Table I are obtained as (9) and (10).

$$G_v(s) = \frac{\hat{y}(s)}{\hat{i}_L(s)} = -\frac{s - 40000}{8 \times (2s + 75)} \tag{9}$$

$$G_i(s) = \frac{\hat{i}_L(s)}{\hat{d}(s)} = \frac{400 \times (2s + 75)}{s^2 + 25s + 500000} \tag{10}$$

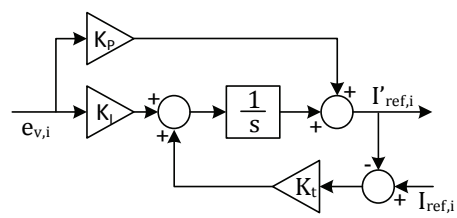


Fig. 11. Bumpless transfer that switches smoothly between two control systems.

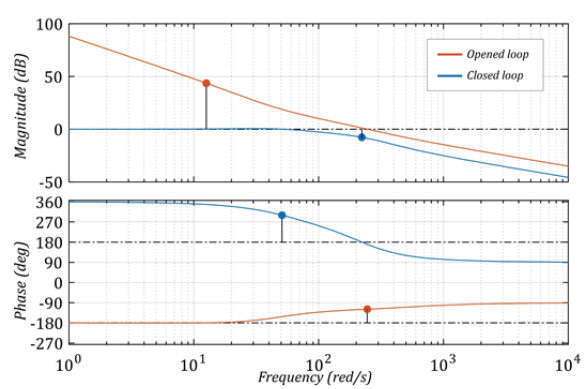


Fig. 12. Bode diagram of plant transfer functions with and without compensation.

In Fig. 12, the reference voltage is obtained by the droop control. In order to reduce the steady state error and to improve the overall stability of the system, an appropriate closed-loop controller is designed so that the controller provides a sufficient phase margin and bandwidth. Therefore, the transfer function of the voltage control system ($G_{cv}(s)$) and current control system ($G_{cc}(s)$) in Fig. 10 are represented by (11) and (12).

$$G_{cv}(s) = 0.036 + \frac{(1.2609 + \text{bumpless transfer term})}{s} \tag{11}$$

$$G_{cc}(s) = 0.283 + \frac{101.28}{s} \tag{12}$$

Due to the same numbers of the proposed converter transformer in the primary, secondary and tertiary, this method is similar in the other modes of power transfer to load.

TABLE I
SYSTEM PARAMETER VALUES

Parameter	Value
Inductor L_m	2.5 *mH*
Capacitor C_1 and C_2	200 μF
Duty cycle D	0.5
Load R_{load}	200 Ω
Transformer winding turns N_P=N_{s1}=N_{s2}	1
Battery	2000 *Ah*, 400 *V*
Reference voltage (V_{ref})	400 *V*
Maximum voltage (V_{max})	408 *V*
Minimum voltage (V_{min})	392 *V*
Maximum-allowed voltage ($V_{max\text{-}allowed}$)	404 *V*
Minimum-allowed voltage ($V_{min\text{-}allowed}$)	396 *V*
Inductor current upper limit (i_{MAX})	10 *A*
Duty cycle upper limit (D_{MAX})	0.8

In order to avoid the kicks in the control signal caused by setpoint changes from the voltage control and battery charge control strategy, a bumpless transfer has been used. Using the model introduced in [28] and [29], as shown in Fig. 11, bumpless transfer is achieved by adding ($I_{ref,i} - I'_{ref,i}$) to the integral coefficient term of $G_{cv}(s)$. Where $I'_{ref,i}$ is the output value of the voltage control block, the index i represents the bus number and K_t is a constant coefficient that is related to the reverse of the reset time.

With the parameters mentioned above, a Bode diagram of the open-loop and closed-loop control system is shown in Fig. 12. By analyzing the amplitude-frequency characteristic and phase-frequency response curves in the Bode diagram, it can be seen that the designed controller provides a good stability margin for the system.

IV. SIMULATION RESULTS

In order to verify performance of the proposed converter, computer simulations studies were carried out in Matlab-Simulink software. The parameters of proposed converter are listed in Table I.

It is assumed that, RES_1 and RES_2 are able to product a maximum power of 2kW. Simulation waveforms of the voltages (V_1, V_2 and V_{bat}), the inductor current (i_L) and the converter modes under different load currents are shown in Fig. 13. As analyzed previously, these simulations were carried out in seven different operational modes.

A. 0~0.01: DISO-C Mode

During 0~0.01, the load currents connected to the upper and lower terminals are 400 Ω. As a result, the RESs inject a constant current to support the local loads while the extra generated power is used to charge the battery. In this scenario, the RESs have the ability to continuously charge the battery. Therefore, V_1 and V_2 stay between V_{max} and $V_{max\text{-}allowed}$. As a result, the converter operates in mode 2.

B. 0.01~0.02: SISO-C Mode

When reducing R_2 to 80Ω, the value of V_2 decreases and stays between $V_{min\text{-}allowed}$ and $V_{max\text{-}allowed}$. Therefore, the system changes to mode 3. In this mode, the redundant power transferred from the positive terminal charges the battery. Because RES_1 does not have the ability to continuously charge the battery, V_1 is decreased. After V_1 reaches $V_{max\text{-}allowed}$, the converter changes to mode 1. At this time, the converter does not work and i_L become zero. Then V_1 begins to increase during a burst-mode switching period, where the positive terminal voltage satisfies the condition of $V_1 < V_{max\text{-}allowed}$. After that, when V_1 reaches $V_{max\text{-}allowed}$ again, the converter operates in mode 3.

C. 0.02~0.03: SIDO-C Mode

With a further reduction in R_2 (R_2= 57Ω), the value of V_2 decreases and stays between $V_{min\text{-}allowed}$ and $V_{max\text{-}allowed}$, while the value of V_1 stays between V_{max} and $V_{max\text{-}allowed}$. In this condition, the redundant power of the positive bus is transferred to charge the battery and to regulate the negative bus voltage. Similar to mode 3, the operational mode changes to mode 1 during the burst mode switching period.

D. 0.03~0.04: SISO-B Mode

When the reduction of R_2 continues to 40Ω (R_1 stays at 400Ω), the redundant power-generated potential of the RES_1 is enough to supply the R_1 and R_2 load demand. In this condition, the proposed converter changes to mode 5. Therefore, the upper bus only compensates the voltage of the negative bus. Then, V_2 begins to increase to the allowed voltage lower limit ($V_{min\text{-}allowed}$). After that, the operation mode changes to mode 1 until V_2 is reached V_{min} again.

E. 0.04~0.05: SISO-D Mode

When R_1 is reduced to 80Ω (R_2 stays at 40Ω), the value of V_1 decreases and stays between $V_{min\text{-}allowed}$ and V_{ref}. Therefore, the proposed converter starts to compensate the negative bus voltage through discharging the battery. In this condition, the proposed converter operates in mode 6. Similar to the previous conditions, the operational mode changes to mode 1 during the burst mode switching period.

F. 0.05~0.06: SIDO-D Mode

With a greater reduction in R_1 (R_1=40Ω, R_2=40Ω), both of the bus voltages stay between V_{min} and $V_{min\text{-}allowed}$. Therefore, the battery discharges on both buses to increase the voltages V_1 and V_2. Finally, these voltages come back to the allowed values during the droop control. Then, V_1 and V_2 begin to increase to the allowed voltage lower limit ($V_{min\text{-}allowed}$). Similar to the previous conditions, the operational mode changes to mode 1.

G. 0.06~0.07: NBM Mode

When R_1 = 80Ω, R_2 = 80Ω, the voltages V_1 and V_2 naturally tend to stay balanced without control. Eventually they stay

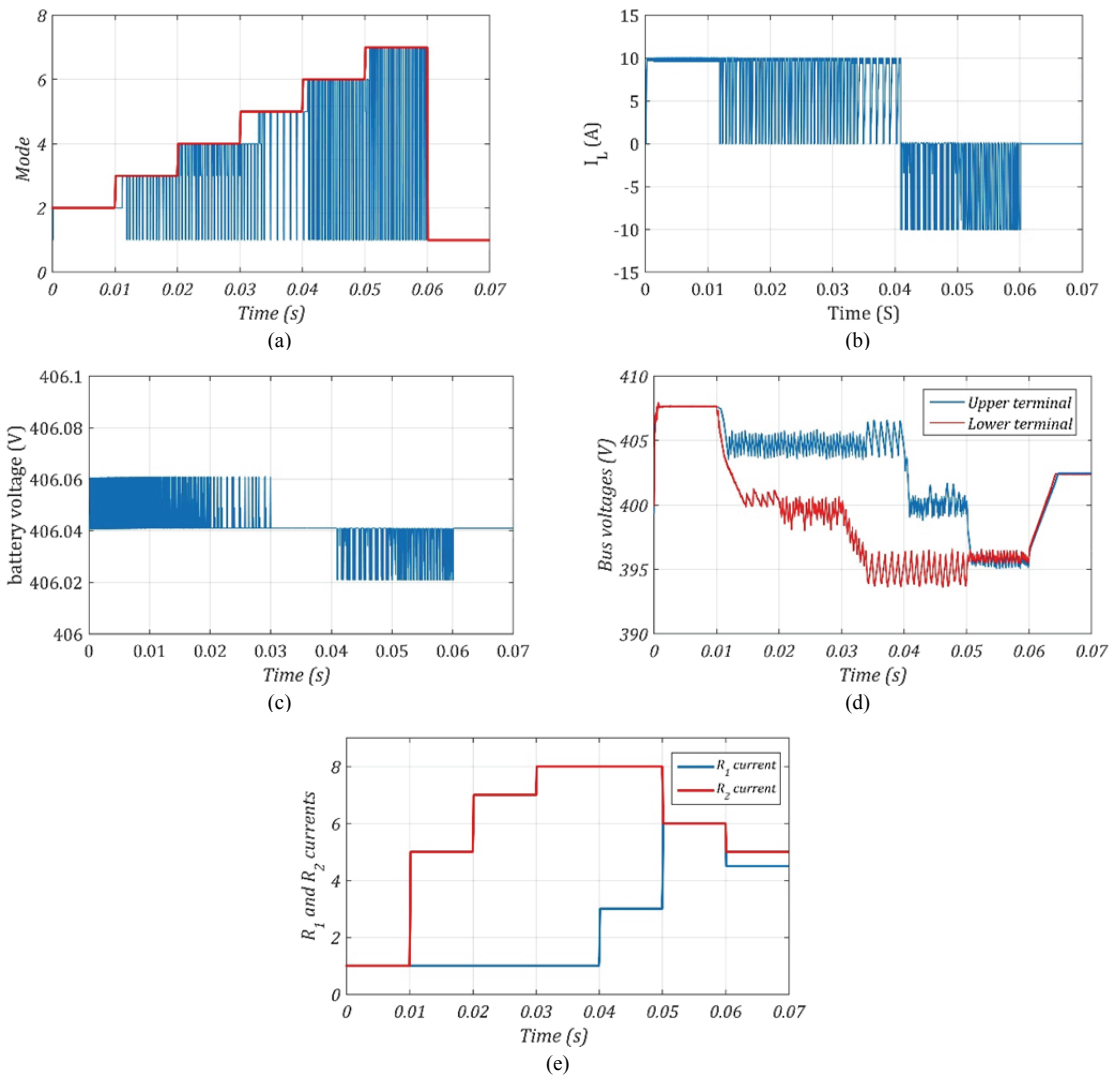


Fig. 13. Simulation results: (a) Modes; (b) Inductor current; (c) Voltage of the battery; (d) Output voltage of the negative and positive terminals; (e) Load currents.

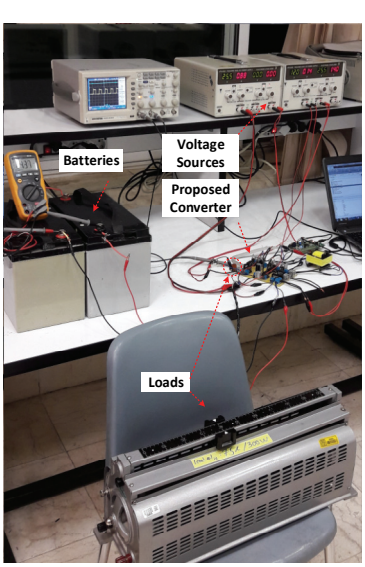


Fig. 14. Photograph of the proposed converter prototype.

equal. Since V_1 and V_2 stay between $V_{min\text{-}allowed}$ and $V_{max\text{-}allowed}$, the balancer does not operate and changes to mode 1. In this mode, the inductor current is constantly zero.

V. Experimental Results

In order to verify the proposed converter, a low voltage and low power (24V-50W) experimental setup of the proposed converter, shown in Fig. 14, is designed and implemented. The experimental testbench includes two 24V DC input voltage sources with a maximum current of 2A, the proposed three-port multidirectional converter, two cascaded VRLA 12V batteries and loads. The converter parameters are listed in Table II.

When $R_1 = R_2 = 47\Omega$ (loads of less than 2A), the voltage source power generations is more than the load demands in both buses. Therefore, the proposed converter operates in mode 2 and the battery can be charged with the positive and

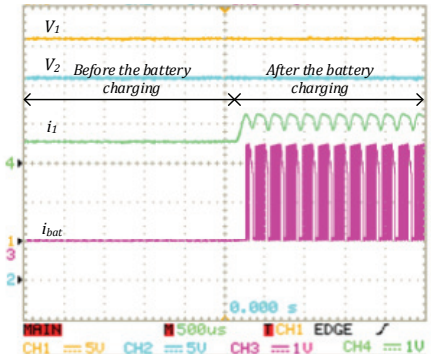


Fig. 15. Voltages of R_1 and R_2, the output current of the positive voltage source and the battery charging current in mode 2.

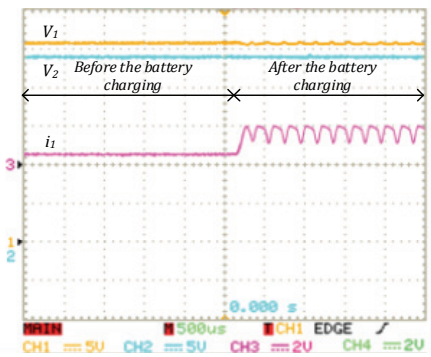


Fig. 16. Voltages of R_1 and R_2 and the output current of the positive voltage source in mode 3.

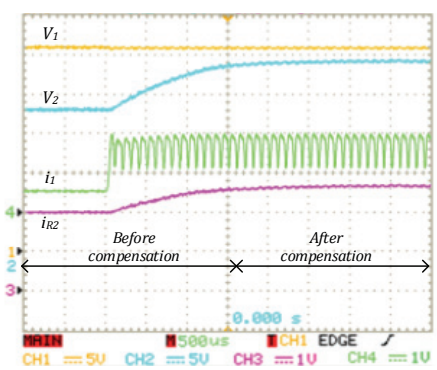


Fig. 17. Voltages of R_1 and R_2, the output current of the positive voltage source and the current of R_2 in mode 4.

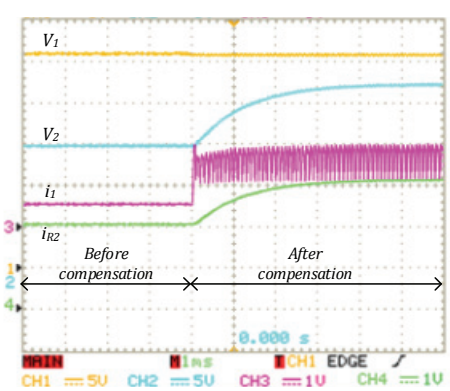


Fig. 18. Voltages of R_1 and R_2, the output current of the positive voltage source and the current of R_2 in mode 5.

TABLE II
MAIN PARAMETERS OF THE EXPERIMENTAL SETUP

Parameter	Value
$N_P=N_{s1}=N_{s2}$	15
Transformer wire size	AWG 18
Transformer core size	EE 55
Reference voltage (V_{ref})	24*V*
Maximum voltage (V_{max})	26*V*
Minimum voltage (V_{min})	21*V*
Maximum-allowed voltage ($V_{max\text{-}allowed}$)	25*V*
Minimum-allowed voltage ($V_{min\text{-}allowed}$)	23*V*
Battery	12*V*-100*AH*
Battery fully charged voltage	13.06 *V*
Switching Frequency	10*kHz*
Inductor L_m	*0.288 μH*
Capacitor C_1 and C_2	220 *μF*
Duty cycle upper limit (D_{MAX})	0.8
Inductor current upper limit (i_{MAX})	2.5*A*

negative buses. Under this condition, the voltages of R_1 and R_2, the output current of the positive voltage source and the battery charging current are shown in Fig. 15. It should be noted that the current waveform of the negative voltage source has not been shown due to its similarity to the current waveform of the positive voltage source.

By changing R_2 to 12Ω, the negative voltage source delivers 2A to R_2. At this moment, the maximum possible power is taken from the negative voltage source. Under this condition, the proposed converter operates in mode 3. Therefore, the redundant power transferred from the positive terminal charges the battery. The voltage of R_1 and R_2 and the current of the positive voltage source are shown in Fig. 16.

When R_2=9Ω (load demand of more than 2A) and R_1 = 47Ω (load demand of less than 2A), the redundant power of the positive bus has the ability to regulate the negative bus voltage and to charge the battery. Under this condition, the system operates in mode 4. Fig. 17 shows the R_1 and R_2 voltages, the output current of the positive voltage source and the current of R_2 before and after compensation. From Fig. 17, it can be seen that *LVUR* is reduced from 35.8% (before compensation) to 6.6% (after compensation).

When the reduction of R_2 continues to 7.2Ω (R_1 stays at 47Ω), the power-generation potential of the positive voltage source is more than the R_1 load demand. Under this condition, the proposed converter operates in mode 5. The upper bus only considers compensating the voltage of the negative bus. Fig. 18 shows the R_1 and R_2 voltages, the output current of the positive voltage source and the current of R_2 before and after compensation. Under this condition *LVUR* is reduced from 54.3% (before compensation) to 13.4% (after compensation).

With a decrease in R_1 (R_1 = 11.75Ω, R_2 = 7.2Ω), the voltage sources generations are no longer enough to supply the loads. Therefore, the proposed converter operates in mode 6 and the battery can participate to compensate the lower bus voltage. In this mode, the battery compensates the lower bus

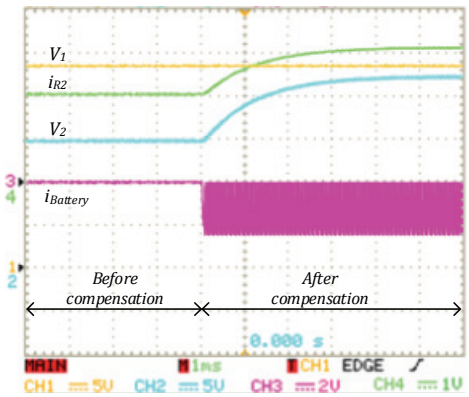


Fig. 19. Voltages of R_1 and R_2, the current of R_2 and the battery discharging current in mode 6.

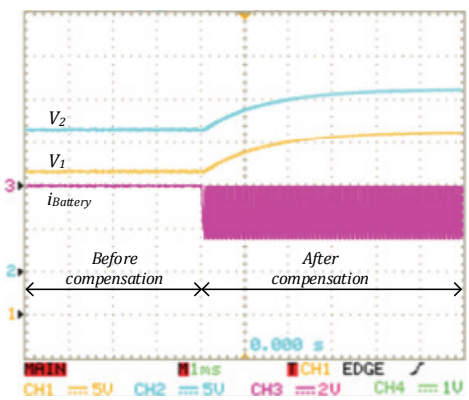


Fig. 20. Voltages of R_1 and R_2 and the battery discharging current in mode 7.

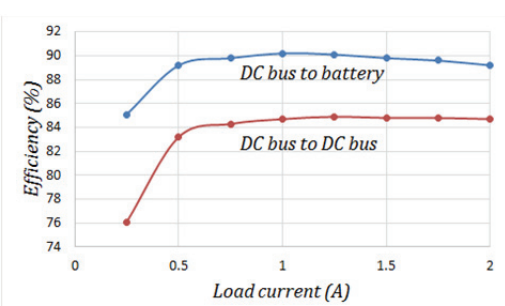


Fig. 21. Conversion efficiencies of the DC bus to battery and DC bus to DC bus modes.

voltage. The voltage of R_1 and R_2, the current of the battery and the current of R_2 before and after compensation are shown in Fig. 19.

When, R_1 and R_2 are 8.2Ω, the amount of power generated by the voltage sources in order to provide the available loads is not enough. In this case, the battery compensates the positive and negative bus voltages through the proposed converter. The voltage of R_1 and R_2, the current of the battery and the current of R_2 before and after compensation are shown in Fig. 20.

The conversion efficiencies of representative operation modes are shown in Fig. 21. The duty cycle is adjusted to meet different load current levels, and the input voltages are kept the same during the measurements. Although the converter has many switches, since some of the switches always remain in the ON state during the switching time, the conduction loss is small and the proposed converter can still achieve a high conversion rate. The efficiencies of the proposed converter are in the range of 76.1%-90.2%, which verifies the good performances of the proposed converter in different operation states. The blue line depicts the power transfer efficiency from the DC bus to the battery which is the efficiency curve of battery charging/discharging modes (mode 2, mode 3, mode 6 and mode 7). The red line depicted the power transfer efficiency from one DC bus to the other DC bus (mode 5). Since the efficiency curve of mode 4 can be represented by a combination of the two curves, this curve can be placed between the two curves, depending on the amount of current being shared between the battery and the other DC bus.

VI. Conclusion

In this paper, a new three-port multidirectional converter with a burst-time control scheme has been proposed for bipolar DC microgrids. The structure of the proposed three-port multidirectional converter mitigated the bus voltage unbalancing and enhanced the system efficiency thanks to the fact that it can be used instead of several converters due to its multi-mode operation. A small-signal model was developed to study its stability and to design the outer voltage and inner current controller. The operation principles of the proposed converter were presented in seven modes. Finally, simulation and experimental results verified that the proposed converter has the ability to balance bus voltages with unbalanced loads.

References

[1] L. M. Saublet, R. Gavagsaz-Ghoachani, J. P. Martin, B. Nahid-Mobarakeh, and S. Pierfederici, "Bifurcation analysis and stabilization of DC power systems for electrified transportation systems," *IEEE Trans. Transport. Electrific.,* Vol. 2, No. 1, pp. 86-95, Mar. 2016.

[2] C. Subramani and K. Ramanand, "A brief review on electric spring: Analysis, control and applications," *J. Circuits, Syst. Comp.,* Vol. 27, No. 5, p. 1830002, May 2017.

[3] T. Dragičević, X. Lu, J. C. Vasquez, and J. M. Guerrero, "DC microgrids – Part II: A review of power architectures, applications, and standardization issues," *IEEE Trans. Power Electron.,* Vol. 31, No. 5, pp. 3528-3549, May 2016.

[4] H. Kakigano, Y. Miura, and T. Ise, "Low-voltage bipolar-type DC microgrid for super high quality distribution," *IEEE Trans. Power Electron.,* Vol. 25, No. 12, pp. 3066-3075, Dec 2010.

[5] F. Wang, Z. Lei, X. Xu, and X. Shu, "Topology deduction and analysis of voltage balancers for DC microgrid," *IEEE J. Emerg. Sel. Topics Power Electron.,* Vol. 5, No. 2, pp.

672-680, Jun. 2017.

[6] S. D. Tavakoli, J. Khajesalehi, M. Hamzeh, and K. Sheshyekani, "Decentralised voltage balancing in bipolar dc microgrids equipped with trans-z-source interlinking converter," *IET Renew. Power Gener.,* Vol. 10, No. 5, pp. 703-712, May 2016.

[7] P. Prabhakaran and V. Agarwal, "Mitigation of voltage unbalance in a low voltage bipolar DC microgrid using a boost-SEPIC type interleaved DC-DC compensator," in *2016 IEEE 2nd Annual Southern Power Electronics Conference, SPEC*, 2016.

[8] T. H. Jung, G. H. Gwon, C. H. Kim, J. Han, Y. S. Oh, and C. H. Noh, "Voltage regulation method for voltage drop compensation and unbalance reduction in bipolar low-voltage DC distribution system," *IEEE Trans. Power Del.,* Vol. 33, No. 1, pp. 141-149, Feb 2018.

[9] W. M. dos Santos, T. A. Pereira, C. Knaesel, H. R. Mamede, and D. C. Martins, "Modeling and control of the new DC-DC step-up converter to bipolar DC microgrid," in *Telecommunications Energy Conference (INTELEC), 2014 IEEE 36th International*, pp. 1-8, 2014.

[10] H. R. Mamede, W. M. dos Santos, and D. C. Martins, "A new DC-DC power converter derived from the TAB for bipolar DC microgrids," in *Energy Conversion Congress and Exposition (ECCE), IEEE,* pp. 6217-6222, 2015.

[11] P. Prajof and V. Agarwal, "Novel boost-SEPIC type interleaved DC-DC converter for low-voltage bipolar dc microgrid-tied solar pv applications," in *2015 IEEE 42nd Photovoltaic Specialist Conference, PVSC 2015*, 2015.

[12] M. Ferrera, S. Litrán, E. Durán, and J. Andújar, "A SEPIC-Cuk converter combination for bipolar DC microgrid applications," in *Industrial Technology (ICIT), 2015 IEEE International Conference on*, pp. 884-889, 2015.

[13] S. D. Tavakoli, G. Kadkhodaei, M. Mahdavyfakhr, M. Hamzeh, and K. Sheshyekani, "Interlinking converters in application of bipolar dc microgrids," in *Power Electronics, Drive Systems & Technologies Conference (PEDSTC), 2017 8th*, pp. 37-42, 2017.

[14] J. Ma, M. Zhu, Q. Li, and X. Cai, "From voltage balancer to interlinking converter; A shift of operation concept for distributed bipolar DC system," in *IECON 2017 - 43rd Annual Conference of the IEEE Industrial Electronics Society*, pp. 1166-1171, 2017.

[15] T. D. Mai, T. Verschelde, and J. Driesen, "Comparative study of current redistributor's topologies for mitigating unbalanced currents in bipolar DC microgrids," in *2017 IEEE Second International Conference on DC Microgrids (ICDCM)*, pp. 242-247, 2017.

[16] H. J. Kim and B. M. Han, "Operation analysis of bipolar DC distribution system with new half-bridge voltage balancer," in *2015 IEEE International Conference on Building Efficiency and Sustainable Technologies*, pp. 62-67, 2015.

[17] G.-H. Gwon, C.-H. Kim, Y.-S. Oh, C.-H. Noh, T.-H. Jung, and J. Han, "Mitigation of voltage unbalance by using static load transfer switch in bipolar low voltage DC distribution system," *Int. J. Electrical Power & Energy Syst.,* Vol. 90, pp. 158-167, Sep. 2017.

[18] Z. Rehman, I. Al-Bahadly, and S. Mukhopadhyay, "Multiinput DC–DC converters in renewable energy applications–An overview," *Renew. Sustain. Energy Rev.,* Vol. 41, No. 8, pp. 521-539, Jan. 2015.

[19] T. Cheng and D. D.-C. Lu, "Three-Port Converters with a Flexible Power Flow for Integrating PV and Energy Storage into a DC Bus," *J. Power Electron.,* Vol. 17, No. 6, pp. 1433-1444, Nov. 2017.

[20] M. Jafari, Z. Malekjamshidi, and J. Zhu, "Design, analysis and control of a magnetically-coupled multi-port multi-operation-mode residential micro-grid," in *2017 20th International Conference on Electrical Machines and Systems (ICEMS)*, pp. 1-6, 2017.

[21] F. Nejabatkhah, S. Danyali, S. H. Hosseini, M. Sabahi, and S. M. Niapour, "Modeling and control of a new three-input DC-DC boost converter for hybrid pv/fc/battery power system," *IEEE Trans. Power Electron.,* Vol. 27, No. 5, pp. 2309-2324, May 2012.

[22] B. Wang, L. Xian, and K. J. Tseng, "Dynamic model predictive voltage control for single-input dual-output flyback converter," in *2016 IEEE 11th Conference on Industrial Electronics and Applications (ICIEA)*, pp. 1212-1217, 2016.

[23] M. Dongsheng, K. Wing-Hung, T. Chi-Ying, and P. K. T. Mok, "Single-inductor multiple-output switching converters with time-multiplexing control in discontinuous conduction mode," *IEEE J. Solid-State Circuits,* Vol. 38, No. 1, pp. 89-100, Jan. 2003.

[24] Y. Hu, W. Xiao, W. Cao, B. Ji, and D. J. Morrow, "Three-port DC-DC converter for stand-alone photovoltaic systems," *IEEE Trans. Power Electron.,* Vol. 30, No. 6, pp. 3068-3076, Jun. 2015.

[25] J. Dong, G. Chen, Y. Deng, K. Wang, and X. He, "A family of integrated dual-output DC-DC converters: Synthesis methodology and performance analysis," in *2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*, pp. 342-347, 2016.

[26] C. Liu, D. Zhu, J. Zhang, H. Liu, and G. Cai, "A Bidirectional dual buck-boost voltage balancer with direct coupling based on a burst-mode control scheme for low-voltage bipolar-type DC microgrids," *J. Power Electron.,* Vol. 15, No. 6, pp. 1609-1618, Nov. 2015.

[27] M. Evzelman and R. Zane, "Burst mode control and switched-capacitor converters losses," in *Applied Power Electronics Conference and Exposition (APEC), 2016 IEEE*, pp. 1603-1607, 2016.

[28] G. Herbst, "Practical active disturbance rejection control: Bumpless transfer, rate limitation, and incremental algorithm," *IEEE Trans. Ind. Electron.,* Vol. 63, No. 3, pp. 1754-1762, Mar. 2016.

[29] K. J. Astrom, *Control System Design*, 2002.

Taha Ahmadi was born in Tehran, Iran, in 1987. He received his B.S. degree in Electrical Engineering from the Shahrood University of Technology, Shahrud, Iran, in 2010; and his M.S. degree in Electrical Engineering from Mazandaran University, Babolsar, Iran, in 2012. He is presently working towards his Ph.D. degree in Electrical Engineering at Lorestan University, Khoramabad, Iran. His current research interests include distribution generation, microgrid control and the application of power electronics in power distribution systems.

Esmaeel Rokrok was born in Khoramabad, Iran, in 1972. He received his B.S., M.S. and Ph.D. degrees in Electrical Engineering from the Isfahan University of Technology, Isfahan, Iran, in 1985, 1997 and 2010, respectively. He is presently working as an Assistant Professor in the Department of Electrical Engineering, Lorestan University, Khoramabad, Iran. His current research interests include power system control and dynamics, dispersed generation, microgrids, power electronics and robust control.

Mohsen Hamzeh received his B.S. and M.S. degrees in Electrical Engineering from the University of Tehran, Tehran, Iran, in 2006 and 2008, respectively. He received his Ph.D. degree in Electrical Engineering from the Sharif University of Technology, Tehran, Iran, in 2012. Since 2010, he has been a Senior Research Engineer with SGP Company, Tehran, Iran. He joined the Department of Electrical and Computer Engineering, Shahid Beheshti University, Tehran, Iran, in 2013, where he is presently working as an Assistant Professor. His current research interests include renewable energies, microgrid control and the application of power electronics in power distribution systems.