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Three-Phase Four-Wire Inverter Topology with Neutral Point Voltage Stable Module for Unbalanced Load Inhibition

Chunwei Cai[†,**], Pufeng An[*,***], Yuxing Guo[*,**], and Fangang Meng[*]

[†,*]School of Information and Electrical Engineering, Harbin Institute of Technology, Weihai, China
[**]Shandong Institute of Ship Building Technology, Weihai, China
[***]Suzhou Inovance Technology Co., Ltd, Suzhou, China

Abstract

A novel three-phase four-wire inverter topology is presented in this paper. This topology is equipped with a special capacitor balance grid without magnetic saturation. In response to unbalanced load and unequal split DC-link capacitors problems, a qusi-full-bridge DC/DC topology is applied in the balance grid. By using a high-frequency transformer, the energy transfer within the two split dc-link capacitors is realized. The novel topology makes the voltage across two split dc-link capacitors balanced so that the neutral point voltage ripple is inhibited. Under the condition of a stable neutral point voltage, the three-phase four-wire inverter can be equivalent to three independent single phase inverters. As a result, the three-phase inverter can produce symmetrical voltage waves with an unbalanced load. To avoid forward transformer magnetic saturation, the voltages of the primary and secondary windings are controlled to reverse once during each switching period. Furthermore, an improved mode chosen operating principle for this novel topology is designed and analyzed in detail. The simulated results verified the feasibility of this topology and an experimental inverter has been built to test the power quality produced by this topology. Finally, simulation results verify that the novel topology can effectively improve the inhibition of an inverter with a three-phase unbalanced load while decreasing the value of the split capacitor.

Key words: Energy transfer, Qusi-full-bridge, Three-phase four-wire inverter, Unbalanced load, Voltage balance

I. INTRODUCTION

Distributed generation systems are drawing more attention due to the increasing demand for sustainable energy. These systems usually works in stand-alone operation or grid-connected operation. In particular, stand-alone operation is more economical than grid-connected in remote areas. However, in practical applications, the loads connected to the power supply are not necessarily balanced [1]-[3]. As an important part of a distributed power supply, the three-phase inverter is supposed to have ability to supply an unbalanced load in stand-alone operation and provide a regulated ac voltage [4].

There are three main topologies to improve the power quality of a three-phase inverter under an unbalanced load. A three-phase combined inverter consists of three single phase inverters. The inverter can work well even if one of its phase experiences a failure [5], [6]. Although the control method is simple and each of the phases works under independent control, the redundant circuit structure increases the cost and volume. When compared to the three-arm inverter topology, three-phase four-leg circuit topology feeds a three-phase unbalanced load better due to the increase of the bridge arm, the midpoint of the arm and the three-phase loads neutral point are connected to a common point so that the negative-sequence current path can be controlled by dual current controllers, and the topology is simple [7]-[9]. However, this topology has a potential electromagnetic compatibility problem

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[†]Corresponding Author: caichunwei@hit.edu.cn
Tel: +86-631-5687800, Fax: +86-631-5687028, HIT
[*]School of Information and Electrical Eng., Harbin Inst. of Tech., China
[**]Shandong Institute of Ship Building Technology, China
[***]Suzhou Inovance Technology Co., Ltd, China

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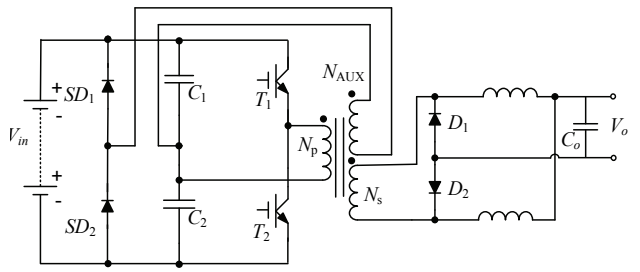


Fig. 1. Half-bridge converter.

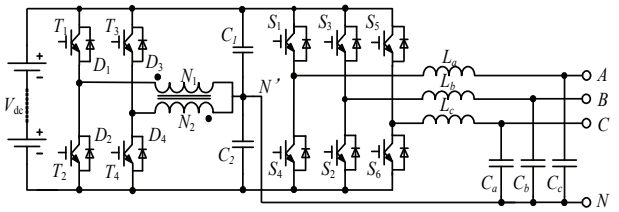


Fig. 2. Novel neutral point voltage stable three-phase four-wire inverter topology.

for the neutral point which is subjected to high frequency voltage transitions [10]. In addition, the control method for the fourth leg is complex, and it cannot be independently controlled. The corresponding controller is also difficult to design as discussed in literature [11]. When compared with the four-leg structure, the split dc-link capacitor three-phase inverter can also achieve a three-phase four-wire structure, providing a loop for the neutral current, which effectively improve the inverter's ability to feed unbalanced loads, and the neutral point is clamped at half of the bus voltage by two split DC-link capacitors [12]. If the neutral point voltage is stable, the split dc-link capacitor three-phase inverter can be equivalent to three single-phase half-bridge inverters, which can decouple the three-phase inverter [13]. In this way, the three-phase can be controlled independently so that the output voltage asymmetry problem caused by an unbalanced load can be effectively inhibited. However, for this split dc-link capacitor three-phase inverter, the existence of the division of the capacitor voltage problem caused by the neutral current flowing into the capacitor or the difference between the two capacitors limits the range of applications, and a higher capacitance is necessary with an increase in the load unbalanced degree [14].

To maintain the balanced voltage of the two capacitors, an adequate capacitor voltage balance circuit is necessary. The topology proposed in [14] is an attractive option. However, the system instability requires a complex control algorithm. Applying the topology described in [15] to a three-phase inverter can enhance the unbalanced load feeding capacity of the inverter. The half-bridge converter is shown in Fig. 1.

However, the magnetization current in the half bridge structure is kept positive or negative in every half cycle of the mid-line current when connecting a three-phase four-wire inverter. If the magnetization current rises too much, the transformer core has saturation. The higher the saturation of the core, the greater the distortion of the magnetic potential.

As a result, the temperatures of the transformer winding and core are increased, and the transformer is burned in the worst-case scenario. Hence, the transformer magnet core must be reset in each control cycle, as long as the magnetization current keeps positive and negative amplitude and waveform symmetry in each control cycle [16]. Therefore, the topology needs to be optimized and improved. In this paper, based on a qusi-full-bridge DC/DC topology, a novel neutral point voltage stable three-phase inverter is proposed. Utilizing a simple control method, the ability of the split dc-link capacitor three-phase inverter to feed an unbalanced load can be improved. The novel topology can inhibit the voltage ripple of the split dc-link capacitor, reduce the windings current and avoid the core saturation risk.

II. Novel Topology and Operation Mode Analysis

A. Novel Topology Description

In order to avoid the core saturation problem of directly applying a DC/DC topology to three phase four wire inverters in [15], another two power switches are used to replace the series diodes. Applying a qusi-full-bridge module, a novel neutral point voltage stable three-phase four-wire inverter topology is obtained. The structure of the novel topology is shown in Fig. 2.

In Fig. 2, V_{dc} is the input bus voltage, T_1~T_4 are the power switches for the qusi-full-bridge DC/DC module, C_1 and C_2 are the split dc-link capacitors, N_1 and N_2 are the primary and secondary windings, and S_1~S_6 are the power switches for the three-phase inverter. When compared with the former structure, the safety and characteristics of this inverter are improved without an increased cost. In addition, the proposed qusi-full-bridge module works in the PWM mode.

B. Operation Mode Analysis

Depending on the neutral point voltage drift direction, the operation principle of this novel topology can be described case by case as below. Case 1: when the neutral point voltage drops below half of the DC bus voltage. Case 2: when the neutral point voltage rise to more than half of the DC bus voltage. There are 4 intervals in one cycle. The operation principle for each case is only analyzed in one cycle. In the same part, these intervals are the same.

Fig. 3 shows key theoretical waveforms in the steady state for a qusi-full-bridge module. The time base is chosen as one cycle before the neutral point voltage cross zero (t_0-t_4) and one cycle after the neutral point voltage cross zero (t_4-t_8). V_{ge1} ~ V_{ge4} are waveforms of the control signals of the power switches T_1 ~ T_4; V_{N1} and V_{N2} are voltage waveforms of the

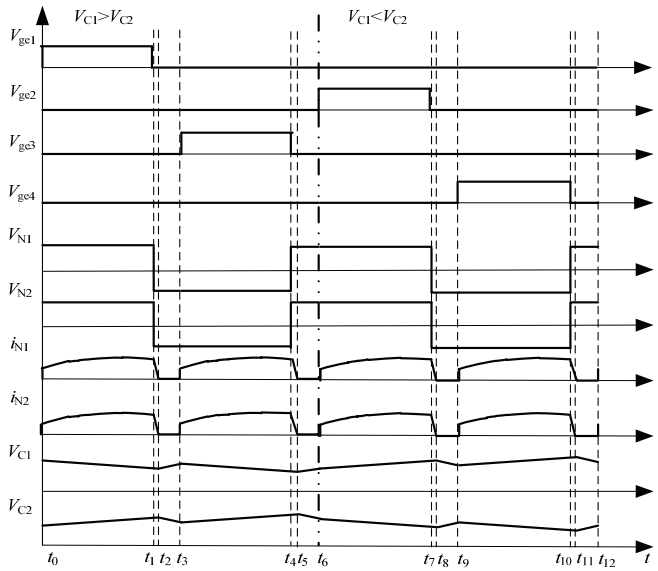


Fig. 3. Key waveforms in the steady state for a qusi-full-bridge module.

primary and secondary winding of the HF transformer; i_{N1} and i_{N2} are current waveforms of the primary and secondary winding of the HF transformer; and V_{C1} and V_{C2} are voltage waveforms of the two split dc-link capacitors.

When the neutral point voltage drops blow half the DC bus voltage (t_0-t_4), the energy of the upper capacitor C_1 is transferred to the lower capacitor C_2 to realize the equalization of the upper and lower capacitor voltages. During this period, the two upper switches T_1 and T_3 alternately conduct, and the two lower switches T_2 and T_4 remain off.

The transformer N_1 winding and the N_2 winding alternately serve as the primary wilding of the transformer. Similarly, when the neutral point voltage rises to over half of the DC bus voltage (t_0-t_4), the two upper switches T_2 and T_4 alternately conduct, and the two lower switches T_1 and T_3 remain off.

Fig. 4 shows the circuit operating mode for every interval. For convenience, the three-phase inverter arms and loads can be equivalent to two resistive loads in series.

Interval 1 (t_0-t_1) the operating mode is shown in Fig. 4(a). The switch T_1 conducts and the switches T_2 to T_4 are kept off. In current loop1 (C_1^+-T_1-N_1-C_1^-), the primary side (winding N_1) current i_{N1} of the transformer is formed, and the capacitor C_1 is discharged. The voltage of the winding N_1 is:

$$V_{N1} = V_{C1} - V_{T1} \tag{1}$$

Where V_{T1} is the conduct voltage of the switch T_1, and V_{C1} is the voltage of the capacitor C_1.

Current loop2 (N_2-C_2-D_4-N_2) is formed on the secondary winding, the capacitor C_2 is charged, and the voltage of the winding N_2 is:

$$V_{N2} = V_{C2} + V_{D4} \tag{2}$$

Since the winding turns ratio of the transformer is 1:1, the voltage difference between V_{C1} and V_{C2} is:

$$V_{C1} - V_{C2} = V_{T1} + V_{D4} \tag{3}$$

The voltage difference between V_{C1} and V_{C2} in the steady state is the sum of the conduction voltage drop of the switch T_1 and the conduction voltage drop of the diode D_4. Since the values of V_{T1} and V_{D4} are small, the system can achieve reliable operation, the difference between the values V_{C1} and V_{C2} becomes very small, and the neutral point voltage only fluctuates in a small range. Therefore, the neutral point voltage can be controlled stably.

Interval 2 (t_1-t_2) is the transformer leakage inductance freewheeling stage. The operation mode is shown in Fig. 4(b). The switches $T_1 \sim T_4$ are off. The winding currents i_{N1} and i_{N1} are reduced to 0 through circuit loop3 (N_1-C_2-D_2-N_1) and circuit loop4 (N_2-C_2-D_4-N_2), or until the switch T_3 is turned on.

Interval 3 (t_2-t_3) is the stage where the capacitors are out of control. The operation mode is shown in Fig. 4(c). The winding currents i_{N1} and i_{N1} remain zero. During intervals 1 and 2, C_2 is charging. Then the voltage of point N' is higher than that of point N. Therefore, in this interval, C_2 is recharging through loop6, and C_1 is charging through loop5.

Interval 4 (t_3-t_4) the operating mode is shown in Fig. 4(c). The switch T_3 turns on, and the switches T_1, T_2 and T_4 are kept off. In loop5 (C_1^+-T_3-N_2-C_1^-), the winding N_2 serve as the primary side of the transformer, and the voltage of the winding N_2 is:

$$V_{N2} = V_{C1} - V_{T3} \tag{4}$$

In the secondary side of the transformer (winding N_1), the capacitor C_2 is charged through current loop6 (N_1-C_2-D_2-N_1), and the secondary winding voltage is:

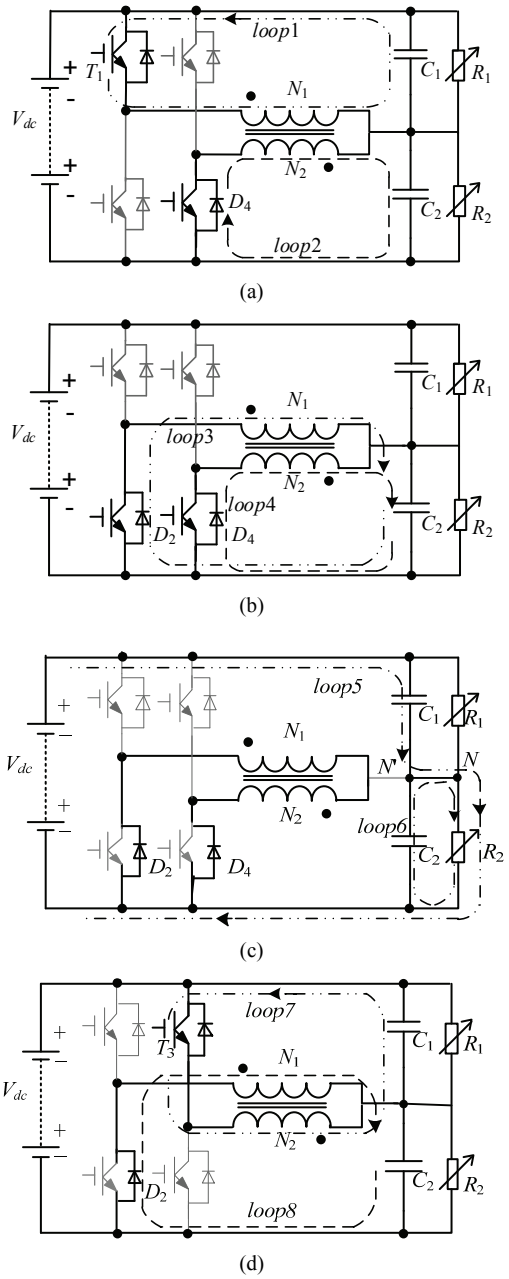


Fig. 4 Equivalent circuits for the interval operation modes: (a) Interval 1, (b) Interval 2 and interval 5, (c) Interval 3 and interval 6, (d) Interval 4.

$$V_{N1} = V_{C2} + V_{D2} \tag{5}$$

Since the transformer winding turn ratio is 1:1, the voltage difference can be expressed as:

$$V_{C1} - V_{C2} = V_{T3} + V_{D2} \tag{6}$$

The voltage difference between V_{C1} and V_{C2} is limited within the sum of the conduction voltage drop of the switch T_3 and the conduction voltage drop of the diode D_2. Because the values are small, the voltage difference between V_{C1} and V_{C2} is small.

Interval 5 (t_4-t_5) is still the freewheeling stage. The operating mode is shown in Fig. 4(b), and it is the same as interval 2.

Interval 6 (t_5-t_6) is still the stage where the capacitors are working free. Its operating mode is shown in Fig. 4(c), and it is the same as interval 3.

Similarly, when the voltage of C_1 is lower than the voltage of C_2, through the alternately conduction of the two lower arms switches T_2 and T_4, the transformer windings N_1 and N_2 alternately serve as the transformer primary side, and the lower capacitor C_2 energy is transferred to the upper capacitor C_1, to achieve upper and lower capacitor voltage equalization. In this mode, the two upper switches T_1 and T_3 remain in the off state. The analysis procedure is the same as the above.

III. Modulation Strategy Design

According to the operation modal analysis of the circuit, the transformer winding needs to serve alternatively as the primary winding by control, and the final design of the modulation strategy is shown in Fig. 5.

In Fig. 5, V_{C2} represents the voltage value of the lower capacitor, and V_{ref} is half of the DC bus voltage. The drift direction of the neutral point voltage is detected by the sign bit which is obtained by comparing 0V with the deviation signal.

The sign bit is used to select the working mode, and for deciding whether the upper switches or the lower switches of the two arms alternately turn on or off. When the sign bit is a low level signal, the upper capacitor voltage is larger than the lower capacitor voltage, and the switches T_1 and T_3 alternately turn on, while T_2 and T_4 remain off. On the other hand, when the sign bit is a high level signal, the lower capacitor voltage is higher than the upper capacitor voltage, and the switches T_2 and T_4 alternately turn on, while T_1 and T_3 remain off.

The PWM signal is divided to control the two upper switches or lower switches so they are alternately conducting. The dead time is designed to prevent the two switches on the same bridge from directly conducting.

To design the logic function for each of the switch controls, a truth table has been drawn in Table I. The control signals G_1、G_2、G_3 and G_4 are written as output signals.

The sign bit A, the divided PWM signal B and the original PWM signal C are written as input signals. The digital logic operation module synthesizes the input signals to obtain the control signals of the four switches.

As can be seen from the table, the logic function for each switch control signal can be expressed as:

$$G_1 = \overline{A} \cdot \overline{B} \cdot C \tag{14}$$

$$G_2 = A \cdot B \cdot C \tag{15}$$

$$G_3 = \overline{A} \cdot B \cdot C \tag{16}$$

$$G_4 = A \cdot \overline{B} \cdot C \tag{17}$$

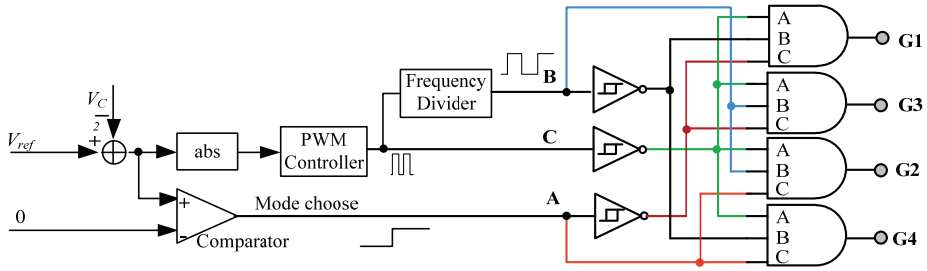


Fig. 5. Modulation strategy diagram for a quasi-full-bridge module.

TABLE I
TRUTH TABLE FOR THE LOGIC SIGNAL

Input signal			Output signal			
A	B	C	G_1	G_2	G_3	G_4
0	0	0	0	0	0	0
0	0	1	1	0	0	0
0	1	0	0	0	0	0
0	1	1	0	0	1	0
1	0	0	0	0	0	0
1	0	1	0	0	0	1
1	1	0	0	0	0	0
1	1	1	0	1	0	0

IV. SIMULATION AND EXPERIMENT RESULTS

A. Simulation Results

The proposed topology has been simulated in Simulink. The two split DC-link capacitors are set as unequal. Firstly, a dc/dc converter like the one in Fig. 4 is built in Matlab. The main parameters are shown in Table II. The operating frequency of the dc/dc converter is 40kHz.

Fig. 6 shows the relationships among the trigger signals of the power switches T_1 and T_2, the voltage and current of the capacitors C_1 and C_2, and the transformer current. When the switches T_1 and T_2 are both turned off, the winding currents i_{N1} and i_{N2} are reduced to zero. Then the current i_{C2} becomes negative and the current i_{C1} becomes positive. Therefore, in this interval, the capacitor C_1 is charging and the capacitor C_2 is recharging, which is in agreement with Fig. 3.

Fig. 7 shows voltage and current waveforms of the split-capacitors when the initial voltage of the upper capacitor is higher than the initial voltage of the lower capacitor. The higher capacitor is discharged, and the voltage of lower capacitor is rising. Then the voltages are close to each other.

Then an inverter like the one in Fig. 2 is built. The DC side parameters are same as those in Table II, and the ac parameters are shown in Table III.

The switching frequency of the inverter is 18kHz. The simulation results are shown as follows.

Fig. 8(a) shows the novel neutral point voltage stable three-phase four-wire inverter output voltage and current waveforms. The three-phase peak voltage are 120.2V, 120.4V and 120.0V,

TABLE II
SIMULATION PARAMETERS

Components	Parameters
Split DC-link capacitor C_1	360μF
Split DC-link capacitor C_2	480μF
HF Transformer	Linear Transformer: $V_{n1}=V_{n2}$, $R_{n1}=R_{n2}$, $L_{n1}=L_{n2}$
Load resistance	$R_1=50\Omega$, $R_2=25\Omega$
Initial voltage of capacitors	$V_{C1}=160V$, $V_{C2}=130V$

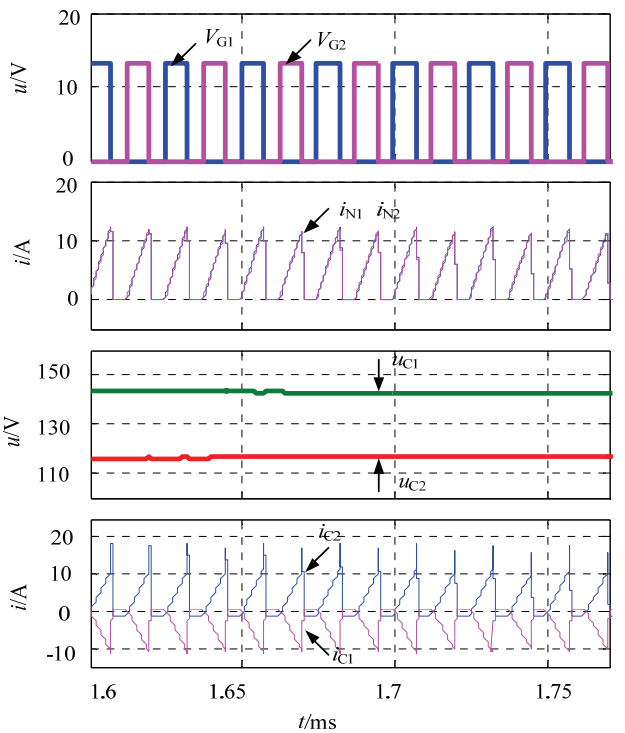


Fig. 6. Simulation waveforms in a switching cycle when $V_{C1}>V_{C2}$.

due to the tolerance of the neutral voltage. There is basically no distortion in the voltage or current waveforms, and the voltage asymmetry rate is about 0.1%. The voltage amplitude and THD values have been greatly improved and enhanced the three-phase inverter ability in terms of the inhibition of unbalanced loads.

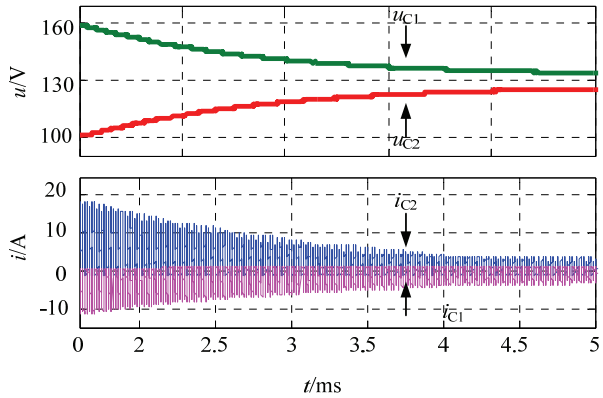


Fig. 7. Simulation results when $u_{C1}>u_{C2}$.

TABLE III
SIMULATION PARAMETERS

Components	Parameters
Output filter inductor L_f	1000μH, 10A
Output filter inductor C_f	20μF
Three-phase load resistance	24Ω, 56Ω, 124Ω

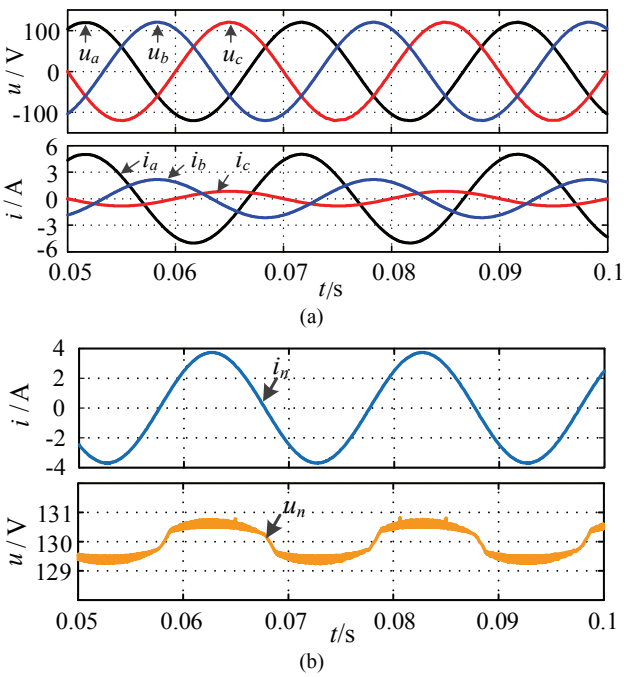


Fig. 8. Simulation waveforms of the proposed topology: (a) Voltage and current waveforms of three-phase loads, (b) Mid-line current and neutral point voltage waveforms.

Fig. 8(b) shows mid-line current and neutral point voltage waveforms. The neutral point voltage has been suppressed to within 0.5V when the mid-line current is about 4A, and the basic voltage is controlled to half of the bus voltage, 130V. From output waveforms of the novel neutral point voltage stable three-phase four-wire inverter topology, it can be seen that the novel topology can keep the neutral point voltage

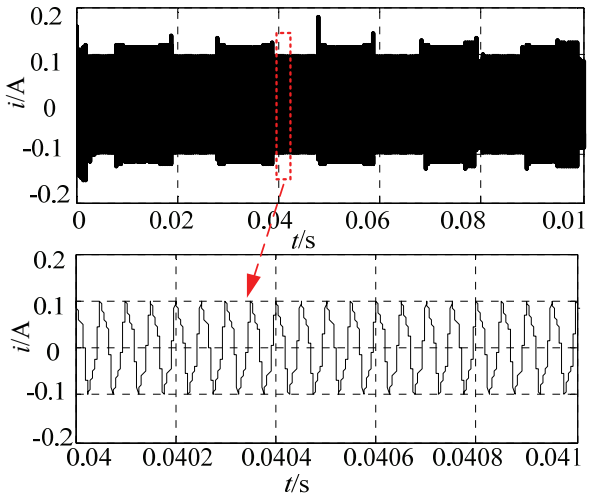


Fig. 9. Magnetizing current of simulation transformer.

stable under the conditions of an unbalanced load and an unequal split DC-link capacitor.

Fig. 9 shows a magnetization current waveform of the HF transformer for the novel topology. It can be seen from this figure that the magnetization current fluctuation range is ± 0.1A, and that the current amplitude in the positive and negative is symmetrical. Therefore, the character of the transformer magnetic current is improved, the transformer can get reset reliably on a high frequency. Thus, it can avoid core saturation and reduce the reactive power loss.

B. Experiment Results

To further verify the characteristic of the novel topology, a novel neutral point voltage stable three-phase four-wire inverter prototype has been built, as shown in Fig. 10.

The main parameters are shown in Table IV, and are the same as those of the simulations.

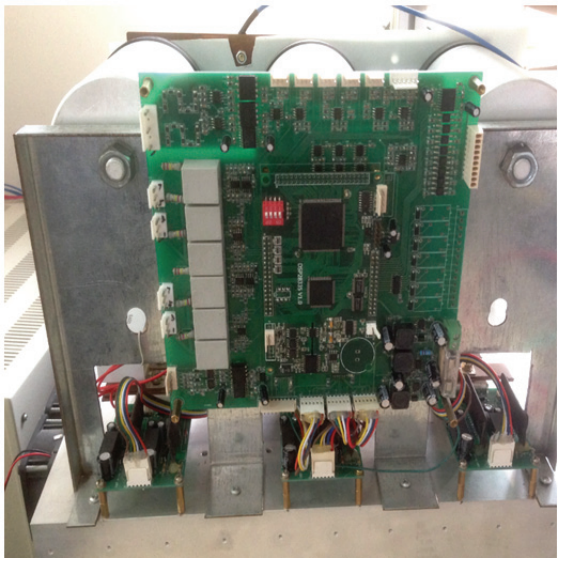
The experiment results are given as follows.

Fig. 11 shows the relationships between the transformer voltage and the trigger signals waveforms of the three power switches T_1,T_2 and T_3 in detail. This is in agreement with Fig. 3. The trigger signals of T_1 and T_3 are complementary, and the trigger signal of T_2 remains zero. In addition, the voltage of the transformer is symmetrical.

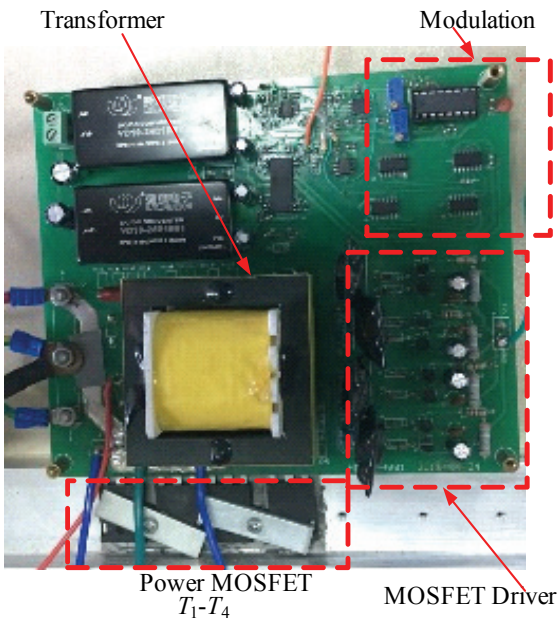
Fig. 12 shows a neutral voltage waveform and a transformer secondary winding voltage waveform. It can be see that when the neutral point voltage is zero, the full-bridge neutral point voltage stability control module does not work, and the transformer winding voltage is kept zero.

Fig. 13 shows the relationships between the neutral voltage fluctuation and the trigger signals waveforms of the two power switches T_2 and T_4. When the neutral point voltage fluctuates in the positive direction, only the switches T_2 and T_4 work alternately.

Fig. 14 shows the relationships between the neutral point voltage and the trigger signals waveforms of the power



(a)



(b)

Fig. 10. Novel neutral point voltage stable three-phase four-wire inverter prototype: (a) Three-phase four-wire inverter prototype, (b) Neutral point voltage stable module.

TABLE IV
PARAMETERS OF THE LABORATORY PROTOTYPE

Components	Parameters
Power IGBT T_1,T_2, T_3,T_4	IKW40T120
Split DC-link capacitor C_1	120μF capacitor,3 capacitors in parallels
Split DC-link capacitor C_2	120μF capacitor,4 capacitors in parallels
HF Transformer	EE55 ferrite core, Primary windings turns:n_1=28; secondary turns n_2=28;Leakge inductance referred to the primary L_{leak}=6μH

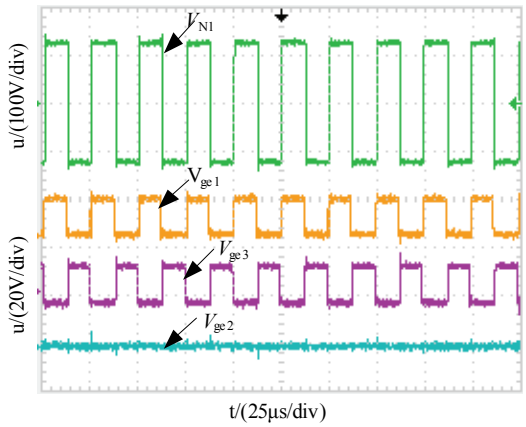


Fig. 11. Experimental waveforms in a switching cycle when V_{C1}>V_{C2}.

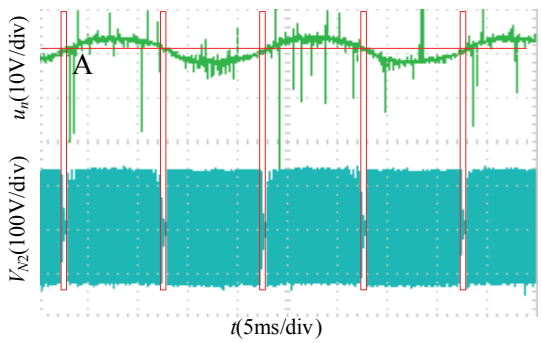


Fig. 12. Neutral voltage and transformer secondary winding voltage waveforms.

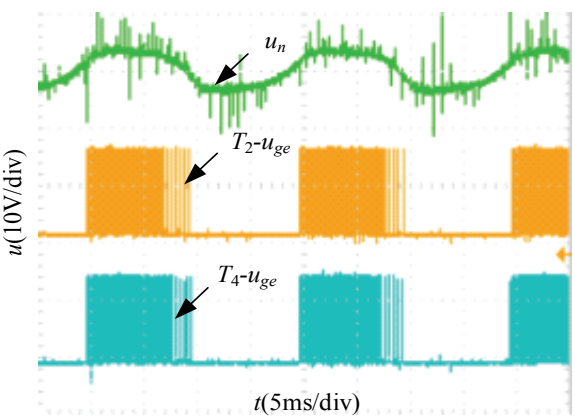


Fig. 13. Neutral point voltage and trigger signals of the power switches T_2 and T_4 waveforms.

switches T_1 and T_2. With neutral point voltage fluctuation direction changes, the two switches in the same bridge work separately, and the operation mode is the same as modulation strategy design.

Fig. 15 shows output waveforms of the novel neutral point stable three-phase four-wire topology, where the switching frequency is 18kHz. Figure 15(a) shows a three-phase load voltage waveform. The voltage amplitude is about 120V, 117V and 122V. The three-phase voltage amplitude are close

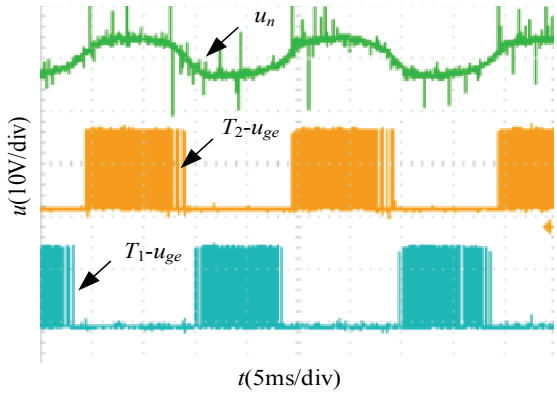


Fig. 14. Neutral point voltage and trigger signals of the power switches T_1 and T_2 waveforms.

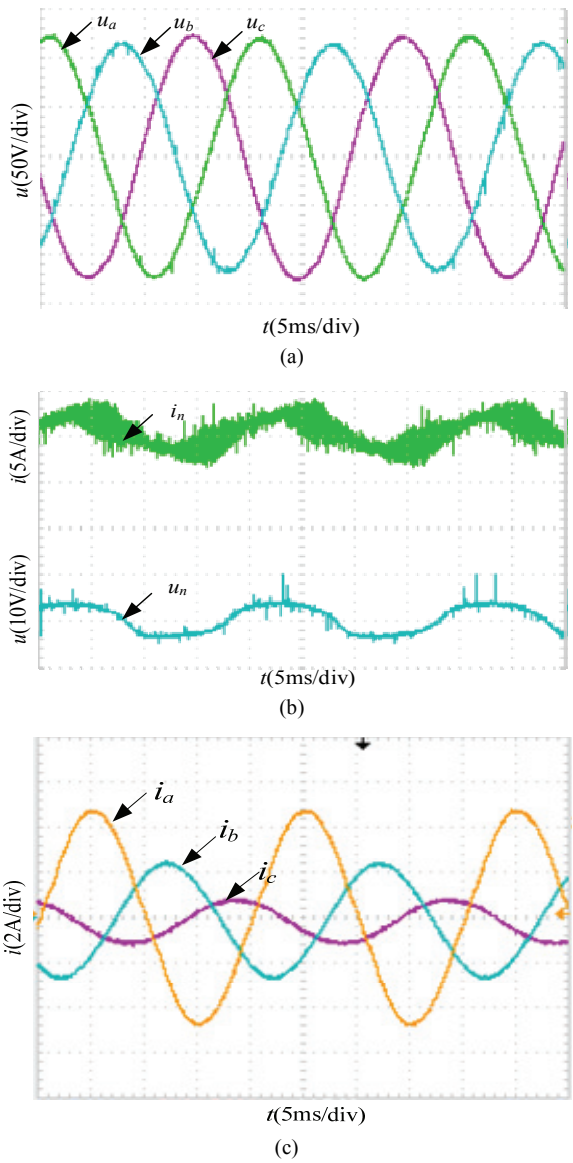


Fig. 15. Experimental waveforms of the proposed topology: (a) Voltage waveforms of a three-phase load, (b) Mid-line current and neutral point voltage waveforms, (c) Current waveforms of a three-phase load.

to equal. The maximum phase voltage amplitude and the minimum phase voltage amplitude difference is about 5V, and it accounts for 1.9% of the bus voltage. The modulation strategy is shown in Fig. 5. A certain error of the neutral voltage is permitted to reduce the switching times. As a result, the magnitudes of the voltages may be a little different. The three-phase voltage phase is 120 degrees. Therefore, the three-phase voltage output is basically in the balanced state, with a three-phase voltage asymmetry rate of about 2.41%. Figure 15(b) shows mid-line current and neutral point voltage waveforms. It can be seen that the novel neutral point voltage is stable. The three-phase four-wire inverter, the mid-line current and the neutral point voltage are basically in the same phase. This indicates that the neutral point voltage is not influenced by split DC-link capacitors. Under the condition that the mid-line current amplitude is about 3A, the neutral point voltage fluctuation has been obviously limited, and the amplitude of the neutral point voltage ripple is about 4V. The voltage fluctuation relative to the bus voltage is 1.5%. Figure 15(c) shows a three-phase current waveform. The three-phase current amplitudes were about 4A, 2A and 0.8A. It can be seen from this figure that the three-phase current phase is basically symmetrical. According to the vector analysis, the vector sum of the three-phase current is about 2.8A, which is close to the middle line current. This indicates that the neutral current does not flow through the split capacitor. The efficient is 86% in this condition due to the additional loss of the qusi-full-bridge module.

V. Conclusions

A novel neutral point voltage stable three-phase four-wire inverter is proposed in this paper. By balancing the energy of two split-DC link capacitors, the capability of feeding an unbalanced load for a stand-alone operation three-phase four-wire inverter is improved. The operation mode for the novel topology is analyzed in detail, and a corresponding modulation strategy is put forward. The novel topology has the following characteristics.

1) The novel topology can keep the neutral point voltage stable, the output harmonic content is small, and three-phase AC voltages are symmetrical.

2) Reducing the split capacitor capacitance with an unbalanced load required a split capacitor capacity, which effectively reduces the inverter size and helps reduce cost. Meanwhile, the influence caused by the unequal split DC-link capacitors can be diminished.

3) In each switching cycle, the two windings of the transformer alternately serve as the primary side, and the current positive and negative current symmetry, to avoid magnetic saturation, which improves the stability and reliability of the proposed inverter.

4) Realization of a modular design. The controls of the

three-phase inverter and the qusi-full-bridge module are independent.

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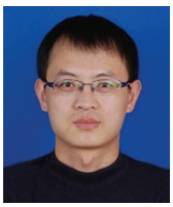
Chunwei Cai was born in Shandong, China, in 1977. He received his B.S. and M.S. degrees in Control Theory and Control Engineering from Shandong University, Jinan, China, in 2001 and 2004, respectively. He received his Ph.D. degree in Electrical Engineering from the Harbin Institute of Technology, Harbin, China, in 2013. In 2006, he became a Lecturer at the Harbin Institute of Technology, Weihai, China, where he has been working as an Assistant Professor since 2014. His current research interests include power converters, inverters and wireless power transfer systems.

Pufeng An was born in Shandong Province, China, 1991. He received his B.S. and M.S. degrees in Electrical Engineering from the Harbin Institute of Technology, Harbin, China, in 2013 and 2015, respectively. He is presently working on the research and development of inverters Suzhou Inovance Technology Co., Ltd. His current research interests include control circuits, IGBT driving and inverter topologies.

Yuxing Guo was born in China, in 1993. He received his B.S. degree in Electrical Engineering and Automation from the Harbin University of Science and Technology, Harbin, China, in 2015. He is presently working towards his M.S. degree in Electrical Engineering in the Academy of Information and Electrical Engineering, Harbin Institute of Technology, Harbin, China. His current research interests include power electronics, electric drives and power system controlling.



Fangang Meng was born in Shandong, China, in 1982. He received his B.S. degree in Thermal Energy and Power Engineering, and his M.S. and Ph.D. degrees in Electrical Engineering from the Harbin Institute of Technology, Harbin, China, in 2005, 2007 and 2011, respectively. His current research interests include harmonic detection, stability analysis of converters and high power rectification.