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Analysis of Synchronous Rectification Discontinuous PWM for SiC MOSFET Three Phase Inverters

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Abstract

Wide band gap semiconductor devices such as SiC MOSFETs are becoming the preferred devices for high frequency and high power density converters due to their excellent performances. However, the proportion of the switching loss that accounts for the whole inverter loss is growing along with an increase of the switching frequency. In view of the third quadrant working characteristics of a SiC MOSFET, synchronous rectification discontinuous pulse-width modulation is proposed (SRDPWM) to further reduce system losses. The SRDPWM has been analyzed in detail. Based on a frequency domain mathematical model, a quantitative mathematical analysis of the harmonic characteristic is conducted by double Fourier transform. Meanwhile, a switching loss model and a conduction loss model of inverter for SRDPWM have been built. Simulation and experimental results verify the result of the harmonic analysis of the double Fourier analysis and the accuracy of the loss models. The efficiencies of the SRDPWM and the SVPWM are compared. The result indicates that the SRDPWM has fewer losses and a higher efficiency than the SVPWM under high switching frequency and light load conditions as a result of the reduced number of switching transitions. In addition, the SRDPWM is more suitable for SiC MOSFET converters.

Key words: Double Fourier analysis, Efficiency, Harmonic, Loss model, SiC MOSFET, Synchronous rectification discontinuous pulse width modulation

I. INTRODUCTION

Since the advent of the first commercial SiC MOSFET in 2010, wide-band-gap semiconductor devices have been paid more and more attention. Compared with Si material, the outstanding advantages of SiC material in terms of band gap, electron saturation drift velocity, thermal conductivity, etc. make SiC devices superior in the power electronic field, especially in high frequency, high efficiency and high power density converters [1], [2]. For medium and high power applications, the switching speed of the SiC MOSFET is significantly higher than that of the Si IGBT. Therefore, the application of SiC MOSFETs in power electronic converters can significantly increase the switching frequency of the converter, which can reduce the volume and weight of passive devices, reduce the cost of converters and improve the system power density.

Improvements in the switching speed of a power device results in an obvious increase in the switching loss proportion in the converter loss. Under favorable heat dissipation conditions, the efficiency of the entire system decrease at high switching frequencies, especially when the load power is greater. To reduce the converter switching loss, soft-switching technology is usually applied. However, this method adds additional auxiliary switching devices, passive components and gate circuits, which increases the cost and complexity of the system while reducing system reliability [3]-[7]. When compared with continuous pulse-width modulation, discontinuous pulse-width modulation (DPWM) makes the phase voltage of each phase bridge clamped to the positive or negative bus voltage alternately for one-sixth of a fundamental

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cycle (60°). At the same carrier frequency, the switching frequency of the power device can be reduced to 2/3 of the continuous pulse width modulation, which reduces the switching loss of the system and improves the efficiency of the converter. To study the application of discontinuous pulse width modulation to three-phase converters, the authors of [9] proposed a new method for unified discontinuous pulse width modulation. However, it just analyzes the harmonic distortion rate without specific quantification. The switching loss of an inverter is compared in [10] and [11]. However, they do not take into account the impact the on-state loss of the devices have on the system. In [12], the harmonic performance of DPWM is analyzed in terms of both the weighted total harmonic distortion (WTHD) and the harmonic distortion factor (HDF). However, it is only briefly analyzed as a whole, and a concrete analysis of the harmonic component is lacking. The loss differences between DPWM, SPWM and SVPWM were quantitatively analyzed in [13]. However, since the experimental object is the Si IGBT, it cannot show the advantages of DPWM at a high frequency. There is not a lot of research on the combination of SiC MOSFETs and DPWM, especially when related to the high switching frequency of SiC MOSFET. Therefore, a study of discontinuous pulse width modulation strategy based on the SiC MOSFET is more meaningful.

The SiC MOSFET has bidirectional current conduction capability. Therefore, the power device can work in synchronous rectification mode. Under this condition, current flows from the source through the SiC MOSFET channel to the drain which can improve the system conversion efficiency when compared to the diode freewheeling [14]. In this paper, the mechanism of 60° synchronous rectified discontinuous pulse width modulation (SRDPWM) is introduced. Using the double Fourier analysis in [15], the output phase bridge voltage of a three-phase inverter under SRDPWM is analyzed in detail. Combined with the synchronous rectification mode of a SiC MOSFET, loss models based on the SRDPWM of a three-phase inverter are proposed. Finally, the accuracy of the loss models is verified by experiments on a prototype, and the efficiency of different frequencies and different load powers are measured and compared.

II. Synchronous Rectification Discontinuous PWM

An increase in the switching frequency of a power device allows the harmonic component of the output voltage to move to the high frequency region, which can reduce the size and weight of the output filter and improve the density of the converter. A high breakdown voltage and a high switching frequency of wide band-gap semiconductor devices (such as SiC MOSFET) cater to this feature.

Fig. 1 shows the main topology of a SiC MOSFET three-phase voltage source inverter. Lfilter, Rload and udc are the filter inductor, load resistor and DC voltage, respectively. A basic space voltage vector diagram in the αβ coordinate is shown in Fig. 2. V1(001), V2(010), V3(011), V4(100), V5(101) and V6(110) are six nonzero basic vectors, and V0(000) and V7(111) are zero vectors. The basic space voltage diagram in Fig. 2 is based on a six-sector space vector diagram that is divided in the middle of each sector, shown as the dotted line in the figure. SVPWM can be considered to be equivalent to regular sampling SPWM with the addition of zero sequence components in sinusoidal pulse width modulation [16]. SVPWM can be manifested as follows [9]:

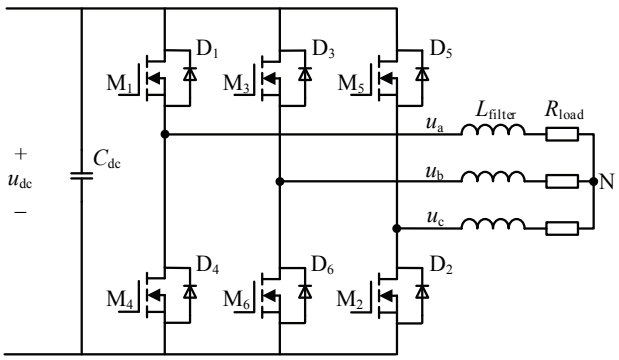


Fig. 1. Diagram of a three-phase voltage source inverter based on SiC MOSFET.

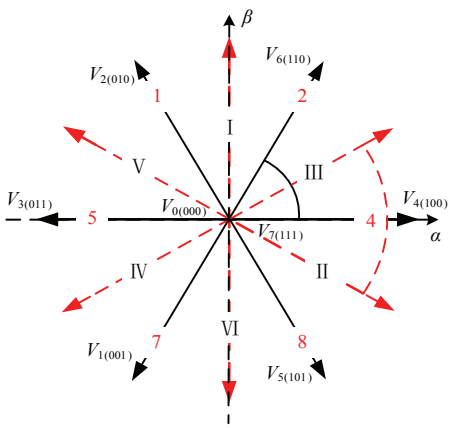


Fig. 2. Diagram of a basic space voltage vector.

$$\begin{cases} u_{\mathrm{a}}^{**} = u_{\mathrm{a}}^{*} + u_{\mathrm{zs}} \\ u_{\mathrm{b}}^{**} = u_{\mathrm{b}}^{*} + u_{\mathrm{zs}} \\ u_{\mathrm{c}}^{**} = u_{\mathrm{c}}^{*} + u_{\mathrm{zs}} \end{cases} \tag{1}$$

Where u_{a}^{*}, u_{b}^{*}, u_{c}^{*} are the three-phase sine given signals with a mutual difference of 120°. In addition, u_{a}^{**}, u_{b}^{**}, u_{c}^{**} are the modulation signals, and u_{zs} is the zero sequence duty cycle, which is generated by the following equation:

$$u_{\mathrm{zs}} = -[(1-2k_0) + k_0 \square u_{\max} + (1-k_0) \square u_{\min}] \tag{2}$$

TABLE I
EXPRESSION OF THE PHASE LEG REFERENCE VOLTAGE WAVEFORMS FOR 60° SRDPWM

60° Section	$2V_a^{**}/V_{dc}$ of A phase	$2V_b^{**}/V_{dc}$ of B phase	$2V_c^{**}/V_{dc}$ of C phase
$5\pi/6 \le \theta \le \pi$	-1	$-1-\sqrt{3}M\cos(\theta+\pi/6)$	$-1+\sqrt{3}M\cos(\theta+5\pi/6)$
$\pi/2 \le \theta \le 5\pi/6$	$-1+\sqrt{3}M\cos(\theta+\pi/6)$	+1	$+1-\sqrt{3}M\sin\theta$
$\pi/6 \le \theta \le \pi/2$	$-1-\sqrt{3}M\cos(\theta+5\pi/6)$	$-1+\sqrt{3}M\sin\theta$	-1
$-\pi/6 \le \theta \le \pi/6$	+1	$-1-\sqrt{3}M\cos(\theta+\pi/6)$	$+1+\sqrt{3}M\cos(\theta+5\pi/6)$
$-\pi/2 \le \theta \le -\pi/6$	$-1+\sqrt{3}M\cos(\theta+\pi/6)$	-1	$-1-\sqrt{3}M\sin\theta$
$-5\pi/6 \le \theta \le -\pi/2$	$+1-\sqrt{3}M\cos(\theta+5\pi/6)$	$-1+\sqrt{3}M\sin\theta$	+1
$-\pi \le \theta \le -5\pi/6$	-1	$-1-\sqrt{3}M\cos(\theta+\pi/6)$	$-1+\sqrt{3}M\cos(\theta+5\pi/6)$

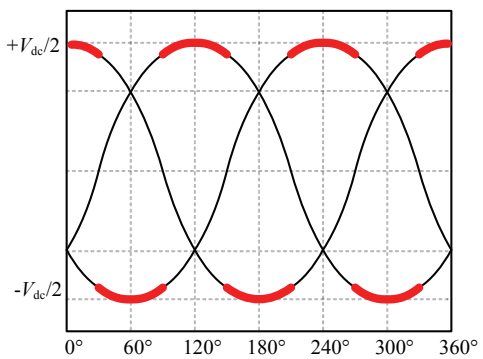


Fig. 3. Diagram of clamping at the peak voltage.

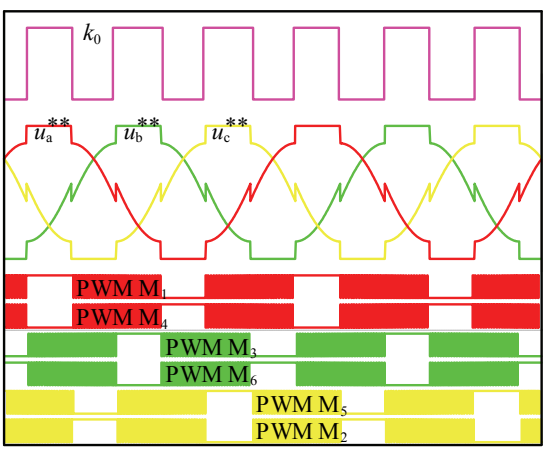


Fig. 4. Diagram of modulation waves and switch pulse waveforms of 60°SRDPWM.

Where $u_{max}=\max(u_a^*,u_b^*,u_c^*)$ and $u_{min}=\min(u_a^*,u_b^*,u_c^*)$.

k_0 is the zero vector adjustment factor. When k_0=0.5, the output PWM is SVPWM. Because of the third quadrant characteristics of SiC MOSFETs, when the lower leg is on, current flows from the source of the SiC MOSFET to the drain to achieve reverse conduction. At this point, the device operates in a synchronous rectification state with the SiC MOSFET channel freewheeling [14]. In addition, the modulation above is synchronous rectification pulse width modulation (SRPWM) [17].

When k_0 follows relation (3), the output PWM is 60° discontinuous modulation with no switching state at the phase voltage 60°peak region. In the SiC MOSFET inverter, the modulation combined with the third quadrant characteristics under the condition of equation (3) is synchronous rectification discontinuous pulse width modulation (SRDPWM). Fig. 3 shows a diagram of clamping at the peak of the phase voltage. Fig. 4 shows three-phase modulation waves and the switching pulse waveforms for each of the SiC MOSFETs when k_0 meets the condition of relation (3) and modulation index is 0.9.

$$\begin{cases} k_0 = 1 & J > 0 \\ k_0 = 0 & J < 0 \end{cases} \tag{3}$$

Where $J=\max(u_a^*,u_b^*,u_c^*)+\min(u_a^*,u_b^*,u_c^*)$.

Using the midpoint of the DC side as a reference point, the expression of the three phase leg reference voltage waveforms after standardization in a cycle are calculated and shown in Table I. Their actual waveforms correspond to the modulation waves u_a^{**}, u_b^{**} and u_c^{**} in Fig. 4.

III. HARMONIC PERFORMANCE ANALYSIS

Due to the low on-resistance characteristics of a SiC MOSFET when adopting SRDPWM, the voltage drop produced by the freewheeling current through the channel is smaller than that through the anti-parallel diode. Therefore, the output voltage waveform distortion is small and the harmonic performance can be improved.

The most well-known harmonic component analysis method was first proposed by Bowes and Bird [20]. The method used in the communication system was transformed for use in the harmonic analysis of a converter phase bridge switch. This paper uses A phase as an example to analyze its harmonic performance. According to the phase voltage modulation function in Table 1, which was output from the SRDPWM strategy, the mathematical model of the 60°SRDPWM modulation unit shown in Fig. 5 can be

TABLE II
OUTER AND INNER DOUBLE FOURIER INTEGRAL LIMITS FOR 60°SRDPWM MODULATION

i	$y_s(i)$	$y_e(i)$	$x_r(i)$	$x_f(i)$
1	$5\pi/6$	π	0	0
2	$\pi/2$	$5\pi/6$	$-\pi-(\sqrt{3}\pi M/2)\cos(y+\pi/6)$	$\pi+(\sqrt{3}\pi M/2)\cos(y+\pi/6)$
3	$\pi/6$	$\pi/2$	$-(\sqrt{3}\pi M/2)\cos(y-\pi/6)$	$(\sqrt{3}\pi M/2)\cos(y-\pi/6)$
4	$-\pi/6$	$\pi/6$	$-\pi$	π
5	$-\pi/2$	$-\pi/6$	$-(\sqrt{3}\pi M/2)\cos(y+\pi/6)$	$(\sqrt{3}\pi M/2)\cos(y+\pi/6)$
6	$-5\pi/6$	$-\pi/2$	$-\pi-(\sqrt{3}\pi M/2)\cos(y-\pi/6)$	$\pi+(\sqrt{3}\pi M/2)\cos(y-\pi/6)$
7	$-\pi$	$-5\pi/6$	0	0

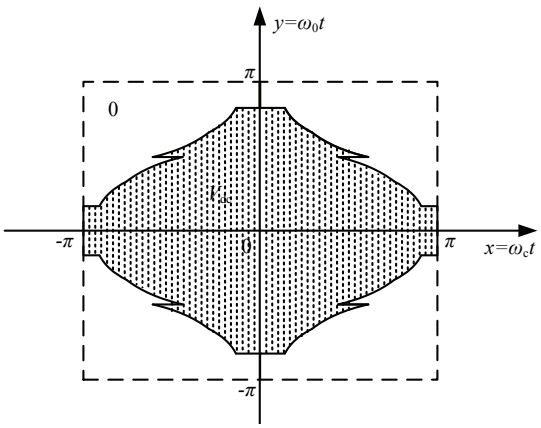


Fig. 5. Mathematic model of a 60° SRDPWM cell.

constructed. Both the x and y axes are in radians; $x=\omega_c t$, $y=\omega_0 t$. In addition, ω_c is the carrier frequency, ω_0 is the modulation frequency, and x and y are independent of each other. The value of the function f(x, y) represents the output phase bridge voltage of the inverter. In addition, the value of the function at any point in the unit can be expressed as a Fourier series.

According to the Fourier transform theory, any time-varying function can be expressed as the sum of harmonic components. In particular, for a double control variable waveform f(x, y), the Fourier harmonic component expression can be deduced as formula (4):

$$f(x,y)=\frac{A_{00}}{2}+\sum_{n=1}^{\infty}(A_{0n}\cos ny+B_{0n}\sin ny)+\sum_{m=1}^{\infty}(A_{0m}\cos mx+B_{0m}\sin mx)+\sum_{m=1}^{\infty}\sum_{\substack{n=-\infty\\(n\neq 0)}}^{\infty}[A_{mn}\cos(mx+ny)+B_{mn}\sin(mx+ny)] \quad (4)$$

where:

$$A_{mn}=\frac{1}{2\pi^2}\int_{-\pi}^{\pi}\int_{-\pi}^{\pi}f(x,y)\cos(mx+ny)\mathrm{d}x\mathrm{d}y \quad (5)$$

$$B_{mn}=\frac{1}{2\pi^2}\int_{-\pi}^{\pi}\int_{-\pi}^{\pi}f(x,y)\sin(mx+ny)\mathrm{d}x\mathrm{d}y \quad (6)$$

For facilitating the calculation, use the plural expression as follows:

$$C_{mn}=A_{mn}+\mathrm{j}B_{mn}=\frac{1}{2\pi^2}\int_{-\pi}^{\pi}\int_{-\pi}^{\pi}f(x,y)\mathrm{e}^{\mathrm{j}(mx+ny)}\mathrm{d}x\mathrm{d}y \quad (7)$$

Where m is the carrier index, and n is the fundamental wave index. The first term in equation (4) is the DC bias component, the second term is the fundamental wave and baseband harmonic component, the third term is the carrier harmonic component, and the fourth term is the sideband harmonic component.

For the SRDPWM scheme, it can be divided into seven small segments. Therefore, equation (7) can be written as:

$$C_{mn}=A_{mn}+\mathrm{j}B_{mn}=\frac{1}{2\pi^2}\sum_{i=1}^{7}\int_{y_s(i)}^{y_e(i)}\int_{x_r(i)}^{x_f(i)}V_{dc}\mathrm{e}^{\mathrm{j}(mx+ny)}\mathrm{d}x\mathrm{d}y \quad (8)$$

The limits of the outer and inner double Fourier integral above are shown in Table II (A leg).

Thus, the plural Fourier series of the A-phase leg can be obtained as:

$$\begin{aligned}C_{mn}&=A_{mn}+\mathrm{j}B_{mn}\\&=\frac{1}{2\pi^2}\left[\int_{\frac{\pi}{2}}^{\frac{5\pi}{6}}\int_{-\pi-\frac{\pi}{2}\sqrt{3}M\cos(y+\frac{\pi}{6})}^{\pi+\frac{\pi}{2}\sqrt{3}M\cos(y+\frac{\pi}{6})}V_{dc}\,\mathrm{e}^{\mathrm{j}(mx+ny)}\,\mathrm{d}x\mathrm{d}y+\right.\\&\int_{\frac{\pi}{6}}^{\frac{\pi}{2}}\int_{-\frac{\pi}{2}\sqrt{3}M\cos(y-\frac{\pi}{6})}^{\frac{\pi}{2}\sqrt{3}M\cos(y-\frac{\pi}{6})}V_{dc}\,\mathrm{e}^{\mathrm{j}(mx+ny)}\,\mathrm{d}x\mathrm{d}y+\int_{-\frac{\pi}{6}}^{\frac{\pi}{6}}\int_{-\pi}^{\pi}V_{dc}\,\mathrm{e}^{\mathrm{j}(mx+ny)}\,\mathrm{d}x\mathrm{d}y+\\&\int_{-\frac{\pi}{2}}^{-\frac{\pi}{6}}\int_{-\frac{\pi}{2}\sqrt{3}M\cos(y+\frac{\pi}{6})}^{\frac{\pi}{2}\sqrt{3}M\cos(y+\frac{\pi}{6})}V_{dc}\,\mathrm{e}^{\mathrm{j}(mx+ny)}\,\mathrm{d}x\mathrm{d}y+\\&\left.\int_{-\frac{5\pi}{6}}^{-\frac{\pi}{2}}\int_{-\pi-\frac{\pi}{2}\sqrt{3}M\cos(y-\frac{\pi}{6})}^{\pi+\frac{\pi}{2}\sqrt{3}M\cos(y-\frac{\pi}{6})}V_{dc}\,\mathrm{e}^{\mathrm{j}(mx+ny)}\,\mathrm{d}x\mathrm{d}y\right]\end{aligned} \quad (9)$$

Considering the Jacobi-Anger expansion:

$$e^{\pm j\xi\cos\theta} = J_0(\xi) + 2\sum_{k=1}^{\infty} j^{\pm k} J_k(\xi)\cos k\theta \tag{10}$$

Where $J_n(x)$ is the nth order Bessel function of x.

Equation (9) is discussed in different situations.

i When m=n=0, simplify (9) to get the DC bias component:

$$C_{00} = A_{00} + jB_{00} = V_{dc} \tag{11}$$

The DC bias component is generated due to the definition of the output switching voltage, which is defined with a negative DC bus as a reference point. The benefit of this is to simplify the mathematical calculation in the Fourier decomposition process.

ii When m=0, n>0(n≠1), equation (9) can be reduced to:

$$\begin{aligned} C_{0n} &= A_{0n} + jB_{0n} \\ &= V_{dc}\frac{(\sqrt{3}M-2)n^2+2}{\pi n(n^2-1)}(\sin\frac{n\pi}{2} - \sin\frac{n\pi}{6} - \sin\frac{5n\pi}{6}) \\ &= -V_{dc}\frac{(\sqrt{3}M-2)n^2+2}{\pi n(n^2-1)}(4\cos^2\frac{n\pi}{3} - 1)\sin\frac{n\pi}{6} \end{aligned} \tag{12}$$

It can be found that when m=0 and n≠0,1, the phase leg output voltage does not contain the even-times harmonic of the fundamental wave. Instead, it contains only 3 odd-times harmonics. Therefore, the equation above also illustrates the elimination of the 3-fold baseband harmonic components in the line-line voltage.

When n=1, $C_{01} = A_{01} + jB_{01} = MV_{dc}$. Obviously, C_{01} is the amplitude of the target reference waveform.

iii When m>0, n=0, equation (9) can be reduced to:

$$\begin{aligned} C_{m0} &= A_{m0} + jB_{m0} \\ &= \frac{2V_{dc}}{m\pi^2}[\cos m\pi\sum_{k=1}^{\infty}\frac{1}{k}\sin\frac{k\pi}{2}\sin\frac{2k\pi}{3}J_k(m\frac{\sqrt{3}\pi}{2}M) + \\ &\quad \sum_{k=1}^{\infty}\frac{1}{k}\sin\frac{k\pi}{2}\sin\frac{k\pi}{3}J_k(m\frac{\sqrt{3}\pi}{2}M)] \end{aligned} \tag{13}$$

From the equation above, it can be analyzed that when m is an odd number, C_{m0}=0; and when m is an even number, C_{m0}≠0. That is, there is only the carrier frequency when m is even.

iv When m>0, n≠0, equation (9) can be reduced to:

$$\begin{aligned} C_{mn} &= A_{mn} + jB_{mn} \\ &= \frac{4V_{dc}}{m\pi^2}\cos m\pi\left\{\frac{\pi}{6}\sin\frac{n\pi}{2}\cos\frac{n\pi}{6}J_n(m\frac{\sqrt{3}\pi}{2}M) + \right. \\ &\quad \sum_{\substack{k=1\\(k\neq -n)}}^{\infty}\frac{1}{n+k}\sin[(n+k)\frac{\pi}{6}]\sin\frac{k\pi}{2}\cos(\frac{2n\pi}{3}+\frac{k\pi}{2})\cdot \\ &\quad J_k(m\frac{\sqrt{3}\pi}{2}M) + \sum_{\substack{k=1\\(k\neq n)}}^{\infty}\frac{1}{n-k}\sin[(n-k)\frac{\pi}{6}]\sin\frac{k\pi}{2}\cdot \\ &\quad \left.\cos(\frac{2n\pi}{3}-\frac{k\pi}{2})J_k(m\frac{\sqrt{3}\pi}{2}M)\right\} + \frac{4V_{dc}}{m\pi^2}\left\{\frac{\pi}{6}\sin\frac{n\pi}{2}\cdot\right. \\ &\quad \cos\frac{n\pi}{6}J_n(m\frac{\sqrt{3}\pi}{2}M) + \sum_{\substack{k=1\\(k\neq -n)}}^{\infty}\frac{1}{n+k}\sin[(n+k)\frac{\pi}{6}]\sin\frac{k\pi}{2}\cdot \\ &\quad \cos(\frac{n\pi}{3}+\frac{k\pi}{2})J_k(m\frac{\sqrt{3}\pi}{2}M) + \sum_{\substack{k=1\\(k\neq n)}}^{\infty}\frac{1}{n-k}\sin[(n-k)\frac{\pi}{6}]\cdot \\ &\quad \left.\sin\frac{k\pi}{2}\cos(\frac{n\pi}{3}-\frac{k\pi}{2})J_k(m\frac{\sqrt{3}\pi}{2}M)\right\} \end{aligned} \tag{14}$$

It can be analyzed that when m+n is odd, C_{mn}≠0; and when m+n is even, C_{mn}=0. Namely, in terms of sideband harmonics, there are only harmonics when m±n is odd.

Based on the above analysis, the harmonic performance of a SiC MOSFET three-phase two-level inverter under the 60 ° SRDPWM scheme is as follows.

1) The amplitude of the fundamental wave of the output phase leg voltage is MV_{dc}. That is to say, the efficiency of the DC voltage of the SRDPWM is still 15% higher than that of the SPWM.

2) The output phase leg voltage contains only 3 times the odd-order harmonics.

3) There are only carrier harmonics with m even for the output phase leg voltage.

4) The output phase bridge voltage contains only the sideband harmonics with m±n odd.

IV. Power Loss Calculation of a SiC MOSFET Three-Phase Inverter

A. Conduction Loss

In the converter of a Si IGBT, current flows through the anti-parallel diode for reverse conduction. However, for a SiC MOSFET, the negative current caused by the switching behavior can flow through the channel of the device for reverse conduction outside the dead time due to the third quadrant characteristics of the SiC MOSFET. The reverse conduction of the SiC MOSFET influences the distribution of the on-state loss of the switching devices in the inverter. Thus, the conduction loss model needs to be reestablished for SiC MOSFET three-phase two-level inverters.

TABLE III
DUTY CYCLE OF SRDPWM

Sector	Duty cycle (δ_1)	Duty cycle (δ_2)
$-\pi/6 \le \theta \le \pi/6$	1	0
$\pi/6 \le \theta \le \pi/3$	$(1+e_1-e_3)/2$	$(1-e_1+e_3)/2$
$\pi/3 \le \theta \le \pi/2+\varphi$	$(1+e_2+e_3)/2$	$(1-e_2-e_3)/2$
$-\pi/6 \le \theta \le -\pi/3$	$(1-e_1+e_2)/2$	$(1+e_1-e_2)/2$
$-\pi/3 \le \theta \le -\pi/2+\varphi$	$(1-e_2+e_3)/2$	$(1+e_2-e_3)/2$

The third quadrant characteristic of a SiC MOSFET operating in the synchronous rectification mode is different from the forward conduction characteristic. Therefore, it is necessary to calculate the on-state loss separately. In the calculation, the dead time is not taken into account. The on-state situation of the SiC MOSFET needs to be known for separately calculating the conduction loss of each section because the SRDPWM scheme has discontinuous modulation. When the current is positive (flowing out of the phase leg), the sector that the reference voltage vector passes through is shown in I, II, III, IV of Fig. 2 (namely sector 2, 4, 8). Table III shows the duty cycles of both δ_1 of main switches and δ_2 of the freewheeling devices in different sectors of a phase leg.

Where $e_1 = M\sin\theta$, $e_2 = M\sin(\theta+\pi/3)$, $e_3 = M\sin(\theta-\pi/3)$.

The average forward conduction loss of a SiC MOSFET in a fundamental cycle is $P_{\text{forw\_M}_1}^{\text{SRDPWM}}$:

$$\begin{aligned}P_{\text{forw\_M}_1}^{\text{SRDPWM}} = \frac{1}{2\pi}\cdot\Bigg\{&\int_{-\frac{\pi}{6}}^{\frac{\pi}{6}}\frac{V_{\text{DSN}}}{I_{\text{DN}}}I_{\text{m}}^2\cos^2(\omega t-\varphi)\mathrm{d}\omega t+\\&\int_{\frac{\pi}{6}}^{\frac{\pi}{3}}\frac{V_{\text{DSN}}}{I_{\text{DN}}}I_{\text{m}}^2\cos^2(\omega t-\varphi)\delta_1\mathrm{d}\omega t+\\&\int_{\frac{\pi}{3}}^{\frac{\pi}{2}+\varphi}\frac{V_{\text{DSN}}}{I_{\text{DN}}}I_{\text{m}}^2\cos^2(\omega t-\varphi)\delta_1\mathrm{d}\omega t+\\&\int_{-\frac{\pi}{3}}^{-\frac{\pi}{6}}\frac{V_{\text{DSN}}}{I_{\text{DN}}}I_{\text{m}}^2\cos^2(\omega t-\varphi)\delta_1\mathrm{d}\omega t+\\&\int_{-\frac{\pi}{2}+\varphi}^{-\frac{\pi}{3}}\frac{V_{\text{DSN}}}{I_{\text{DN}}}I_{\text{m}}^2\cos^2(\omega t-\varphi)\delta_1\mathrm{d}\omega t\Bigg\}\end{aligned}\tag{15}$$

The average conduction loss of the complementary freewheeling SiC MOSFET in a fundamental cycle is $P_{\text{fre\_M}_4}^{\text{SRDPWM}}$:

$$\begin{aligned}P_{\text{fre\_M}_4}^{\text{SRDPWM}} = \frac{1}{2\pi}\cdot\Bigg\{&\int_{\frac{\pi}{6}}^{\frac{\pi}{3}}\frac{V_{\text{SDN}}}{I_{\text{DN}}}I_{\text{m}}^2\cos^2(\omega t-\varphi)\delta_2\mathrm{d}\omega t+\\&\int_{\frac{\pi}{3}}^{\frac{\pi}{2}+\varphi}\frac{V_{\text{SDN}}}{I_{\text{DN}}}I_{\text{m}}^2\cos^2(\omega t-\varphi)\delta_2\mathrm{d}\omega t+\\&\int_{-\frac{\pi}{3}}^{-\frac{\pi}{6}}\frac{V_{\text{SDN}}}{I_{\text{DN}}}I_{\text{m}}^2\cos^2(\omega t-\varphi)\delta_2\mathrm{d}\omega t+\\&\int_{-\frac{\pi}{2}+\varphi}^{-\frac{\pi}{3}}\frac{V_{\text{SDN}}}{I_{\text{DN}}}I_{\text{m}}^2\cos^2(\omega t-\varphi)\delta_2\mathrm{d}\omega t\Bigg\}\end{aligned}\tag{16}$$

Where V_{DSN} is the rated drain-source voltage for position conduction, V_{SDN} is the rated drain-source voltage for reverse conduction, I_{N} is the rated current, φ is the power factor angle, and I_{m} is the on-state current amplitude.

After further calculation:

$$\begin{aligned}P_{\text{forw\_M}_1}^{\text{SRDPWM}} = \frac{V_{\text{DSN}}}{I_{\text{DN}}}\cdot I_{\text{m}}^2\cdot\Bigg[&\frac{1}{6}+\frac{\sqrt{3}}{16\pi}\cos 2\varphi+\\&M\left(-\frac{1}{4\pi}+\frac{\sqrt{3}}{3\pi}\cos\varphi-\frac{1+2\sqrt{3}}{24\pi}\cos 2\varphi\right)\Bigg]\end{aligned}\tag{17}$$

$$\begin{aligned}P_{\text{fre\_M}_4}^{\text{SRDPWM}} = \frac{V_{\text{SDN}}}{I_{\text{DN}}}\cdot I_{\text{m}}^2\cdot\Bigg[&\frac{1}{12}-\frac{\sqrt{3}}{16\pi}\cos 2\varphi-\\&M\left(-\frac{1}{4\pi}+\frac{\sqrt{3}}{3\pi}\cos\varphi-\frac{1+2\sqrt{3}}{24\pi}\cos 2\varphi\right)\Bigg]\end{aligned}\tag{18}$$

B. Switching Loss

The switching energy of a SiC MOSFET has the relationship of a quadratic function with the drain current and of a exponential function with the ratio between the drain-source voltage and the test voltage. The switching energy can be expressed as:

$$E_{\text{switch}}^{\text{SRDPWM}} = (A_0 + B_0\cdot i_{\text{c}} + C_0\cdot i_{\text{c}}^2)\cdot\left(\frac{V_{\text{DS}}}{V_{\text{base}}}\right)^{K_{\text{vds}}}\tag{19}$$

Where A_0, B_0 and C_0 are the current-dependent switching energy function coefficients obtained by the double pulse test, V_{base} is the drain-source voltage of the experimental test, and K_{vds} is the correction factor of the drain-source voltage.

According to the switching energy model, the average switching loss of the SiC MOSFET in a fundamental cycle is:

$$\begin{aligned}P_{\text{switch}}^{\text{SRDPWM}} = &\frac{f_{\text{c}}}{2\pi}\cdot\left(\frac{V_{\text{DS}}}{V_{\text{base}}}\right)^{K_{\text{vds}}}\cdot\\&\Bigg\{\int_{-\frac{\pi}{2}}^{-\frac{\pi}{6}}[A_0+B_0I_{\text{m}}\cos(\omega t)+C_0(I_{\text{m}}\cos(\omega t))^2]\mathrm{d}\omega t+\\&\int_{\frac{\pi}{6}}^{\frac{\pi}{2}}[A_0+B_0I_{\text{m}}\cos(\omega t)+C_0(I_{\text{m}}\cos(\omega t))^2]\mathrm{d}\omega t\Bigg\}\\=&f_{\text{c}}\cdot\left(\frac{V_{\text{DS}}}{V_{\text{base}}}\right)^{K_{\text{vds}}}\cdot\left(\frac{A_0}{3}+\frac{B_0}{2\pi}I_{\text{m}}+\frac{4\pi-3\sqrt{3}}{24\pi}C_0I_{\text{m}}^2\right)\end{aligned}\tag{20}$$

Where f_c is the carrier frequency.

Based on the analysis above, the total losses of the SiC MOSFET three-phase two-level inverter for the SRDPWM scheme are:

$$P_{\text{total}}^{\text{SRDPWM}} = 6(P_{\text{forw\_M}_1}^{\text{SRDPWM}} + P_{\text{fre\_M}_4}^{\text{SRDPWM}} + P_{\text{switch}}^{\text{SRDPWM}}) \quad (21)$$

V. Simulation and Experimental Analysis

In order to verify the previous conclusion of the double Fourier analysis, simulations of a three-phase two-level inverter are carried out by MATLAB. The modulation index M is 0.9 and the carrier ratio N is 50. According to equation (8), it is possible to obtain the theoretical harmonic spectrum. Fig. 6 and Fig. 7 show a harmonic spectrum comparison of the inverter phase leg output voltages between the simulation and the theoretical calculation for the 60° SRDPWM modulation scheme. Table IV gives the theoretical calculation relative amplitude of the main harmonic, the MATLAB simulation relative amplitude and the experimental relative amplitude (using the fundamental amplitude for the unit amplitude).

An analysis of Fig. 6, Fig. 7 and Table IV shows that the simulation result and theoretical result are basically the same. With the SRDPWM scheme, the output phase leg voltage mainly contains the fundamental wave, even times the carrier harmonics and their sideband harmonics. In addition, it only contains odd harmonic in the sideband harmonics of the even times carrier harmonics, which can verify the correctness of the theoretical analysis. However, there are still some errors in the amplitude. The main difference is the sideband harmonic of the carrier harmonics. The main reason for this difference is the small truncation error of the simulation or the calculation error which MATLAB cannot determine. The double Fourier analysis can effectively avoid the effects of step size, accuracy and noise, to calculate the harmonic component size of the PWM waveform more accurately.

In this paper, a 10 kW prototype of a SiC MOSFET three-phase two-level inverter and its testing platform were built, as shown in Fig. 8. The main switching devices are a SiC MOSFET half-bridge module from CREE (CAS300M17BM2) and a TekDPO3014 oscilloscope. The other measuring instruments are: differential voltage probe (Pico TAO42), current probe (Tektronix TCP0030A), power analyzer (Yokogawa WT1800) and harmonic analyzer (FLUKE 435). The parameters of the experiment are shown in Table V. The load is a variable power resistance box and the DC-link voltage is given by a programmable DC voltage source. Fig. 9 shows a switching pulse of the A-phase high-side MOSFET and a waveform of the output three-phase AC voltage. Taking the A-phase bridge as an example, it can be seen that the switching pulse PWM M1 of the SiC MOSFET is clamped at a high level during the 60° range of the peak output voltage of the A-phase bridge, while the low-side switching pulse of the A-phase bridge is clamped at a low level. Thus, the two switches of this phase do not operate during the above stage and there is no switching loss.

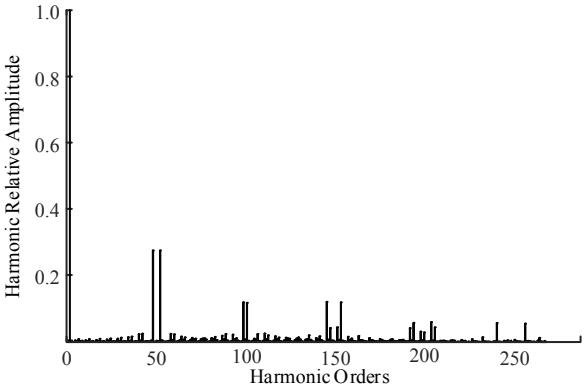


Fig. 6. Simulated spectrum of the phase leg voltage for the SRDPWM modulation.

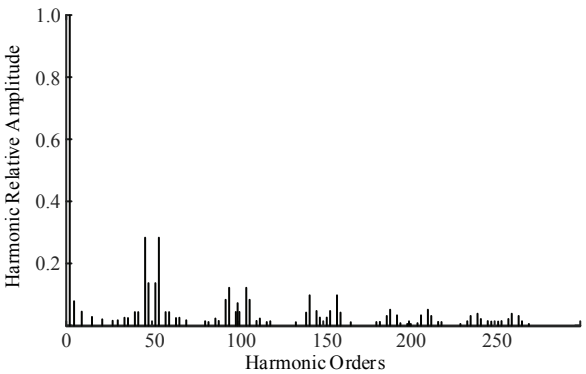
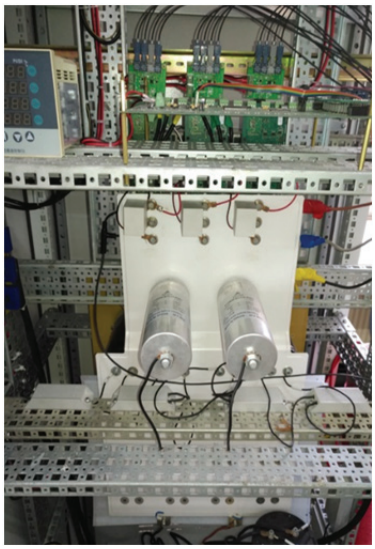


Fig. 7. Theoretical spectrum of the phase leg voltage for the SRDPWM modulation.

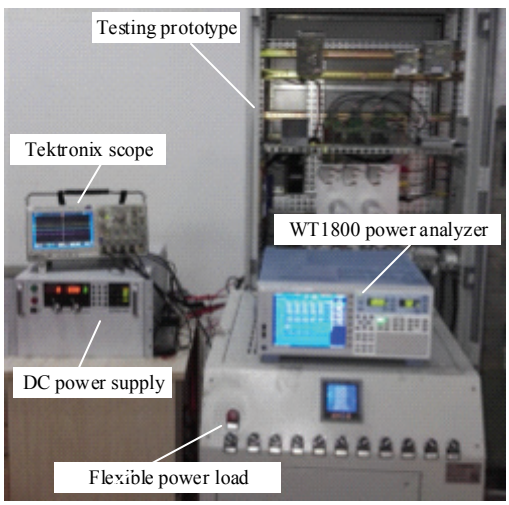
TABLE IV
Comparison of the Phase Leg Voltage Relative Amplitude

Harmonic orders	Phase-leg voltage relative amplitude		
	Theory	Simulation	Experiment
48	0.3330	0.3343	0.3238
52	0.3330	0.3339	0.3174
99	0.1213	0.1375	0.1373
101	0.1213	0.1356	0.1217
148	0.05674	0.05045	0.05252
152	0.05674	0.05233	0.05127

Fig. 10 shows an efficiency analysis of the theoretical loss and the experimental measured loss of the SiC MOSFET three-phase two-level inverter for the SRDPWM modulation scheme at a power of 9kW. It can be seen from the figure that the results of both are very close. However, there are still some errors, and the average error rate is 0.7%. The main reason for the errors is that: in the experiment, dead time is added to avoid shoot-through failures, and the loss caused by this dead time is not taken into account in the loss models.



(a)



(b)

Fig. 8. Prototype of a SiC MOSFET three-phase two-level inverter and its testing platform: (a) Testing prototype, (a) Testing prototype.

TABLE V
PARAMETERS OF THE EXPERIMENT

Parameter	Value
DC-link voltage	600V
Load power	0~10kW
Filter inductance	0.7mH
Switching frequency	5~40kHz
Modulation index	0.9
Dead time	250ns

During the dead time, current flows through the anti-parallel diode of the SiC MOSFET. After the dead time ends, it commutates with the SiC MOSFET channel for freewheeling. The losses during this period are shown as follows:

$$P_{\text{fre}}^{\text{SRDPWM}} = P_{\text{fre\_D}}^{\text{SRDPWM}} + P_{\text{sw\_D}}^{\text{SRDPWM}} + P_{\text{fre\_M}_4}^{\text{SRDPWM}} \quad (22)$$

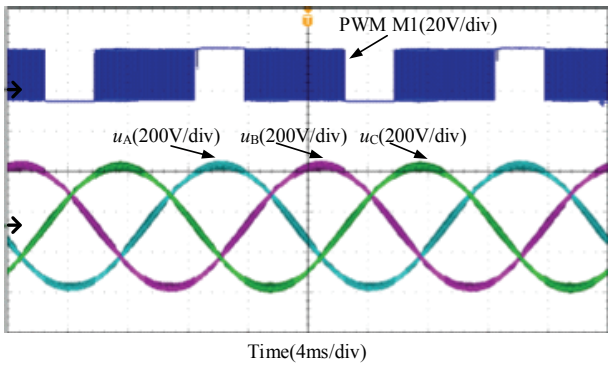


Fig. 9. Waveforms of the switching pulse of the A-phase high-side MOSFET and the output three-phase AC voltage for SRDPWM.

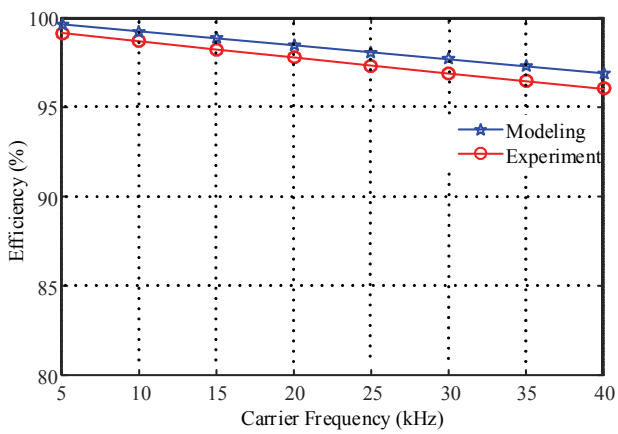


Fig. 10. Comparison of the theoretical calculation efficiency and the experimental efficiency for SRDPWM modulation.

Where $P_{\text{fre\_D}}^{\text{SRDPWM}}$ is the loss of the diode freewheeling, and $P_{\text{sw\_D}}^{\text{SRDPWM}}$ is the switch loss of the diode in the process of current commutation.

In the loss model, since the dead-time is ignored, the diode freewheeling is replaced by SiC MOSFET channel freewheeling, and the diode losses $P_{\text{fre\_D}}^{\text{SRDPWM}}$ are much larger than the SiC MOSFET channel losses. At the same time, the diode switching losses $P_{\text{sw\_D}}^{\text{SRDPWM}}$ are not calculated during the current commutation between the diode and the SiC MOSFET channel.

On the other hand, loss is also generated in the main circuit of the inverter, including the bus parasitic inductance, switching device lead inductance, parasitic capacitance and so on. Due to rapid changes in the current and voltage (di/dt, du/dt), large voltages and currents are induced on these parasitic parameters, as shown in equations (23) and (24), which results in additional losses. These two aspects lead to a deviation between the theoretical calculation efficiency of the loss model and the experimental measured efficiency.

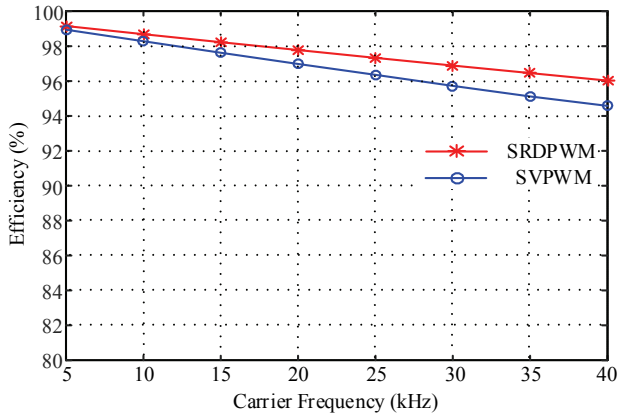


Fig. 11. Experimental efficiency comparison of SRDPWM and SVPWM under different carrier frequencies.

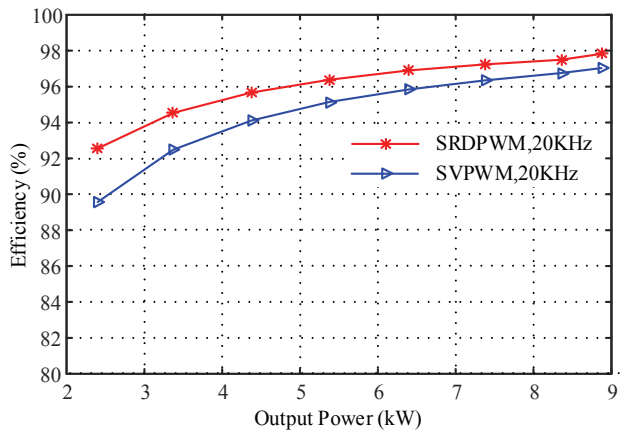


Fig. 12. Experimental efficiency comparison of SRDPWM and SVPWM under different powers.

$$U_L = L\frac{di_L}{dt} \tag{23}$$

$$I_C = C\frac{du_c}{dt} \tag{24}$$

Where L and C are the parasitic inductance and parasitic capacitance in the main circuit of the inverter.

Fig. 11 shows an experimental measured efficiency comparison of SRDPWM and SVPWM at different carrier frequencies. As can be seen in the figure, with an increase of the carrier frequency, the SRDPWM scheme is more dominant in efficiency. In addition, the higher the frequency, the more obvious the advantage. When the carrier frequency is 40 kHz, the efficiency increases by 1.448%. The improvement of the carrier frequency causes the switching loss of the power devices to gradually dominate the overall losses of the inverter. In the SRDPWM modulation scheme, the output phase leg voltages are clamped to the positive or negative DC bus voltages in a modulation cycle for 120°, and the clamped position is within 60°of the output current peak. As a result, the switching loss of the SiC MOSFET is greatly reduced. When compared with SVPWM modulation, SRDPWM greatly improves the efficiency of the inverter, especially at a high switching frequency. In addition to improving the efficiency of the inverter, the volume and weight of the passive components are reduced, which reduces the cost of the inverter. At the same time, there is no change in the gate driving circuit for both SRDPWM and SVPWM. Therefore, SRDPWM can increase the efficiency and power density of the system more effectively.

Fig. 12 shows a comparison of the efficiency of SRDPWM and SVPWM under different power conditions. It can be seen that the efficiency of the SRDPWM scheme in the light load condition is significantly higher than that of the SVPWM scheme. It can also be seen that the efficiencies of the two modulation schemes are gradually getting closer with an increase of the load power. This is because the switching losses of the devices occupy the dominant position of the inverter loss at a light load. In addition, when the load power increases, the device on-state losses related to the square of the current dominate again. Therefore, the SRDPWM modulation strategy is more suitable for use with a light load and a high switching frequency.

VI. Conclusion

In this paper, a synchronous rectifier discontinuous pulse width modulation (SRDPWM) strategy suitable for SiC MOSFETs is proposed for SiC MOSFET three-phase two-level inverters from the point of view of reducing the switching loss of the SiC MOSFET under high frequency operation. The following conclusions are obtained from the output harmonics and inverter losses.

1) The SRDPWM modulation method is achieved by using a double Fourier analysis, and its frequency domain mathematical model is established. The harmonic characteristics are analyzed quantitatively. The expressions of the harmonics are obtained and compared with simulation and experimental results. On the other hand, it is concluded that the double Fourier analysis for SRDPWM is superior to the simulation.

2) Based on the synchronous rectification mode of a SiC MOSFET, the switching loss and on-state loss model of a SiC MOSFET two-level inverter under the SRDPWM modulation strategy are established. The model results are verified by a 10kW experimental prototype. The average error rate of the model and experimental results is 0.7%.

3) Through an experimental data analysis, the device switching losses can be significantly reduced with the SRDPWM modulation scheme in SiC MOSFET-based converters and this effect is more obvious with a higher switching frequency. This modulation strategy is more suitable for the condition of light loads and high switching frequencies.

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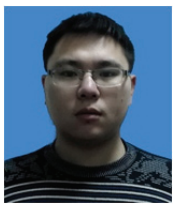

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