JPE 18-5-14

https://doi.org/10.6113/JPE.2018.18.5.1448
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

Dual-model Predictive Direct Power Control for Grid-connected Three-level Converter Systems

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Abstract

Many researchers devote themselves to develop model-predictive direct power control (MPDPC) so as to accelerate the response speed of the grid-connected systems, but they are troubled its large computing amount. On the basis of MPDPC, dual MPDPC (DMPDPC) is presented in this paper. The proposed algorithm divides the conventional MPDPC into two steps. In the first step, the optimal sector is obtained, which contains the optimal switching state in three-level converters. In the second step, the optimal switching state in the selected sector is searched to trace reference active and reactive power and balance neutral point voltage. Simulation and experiment results show that the proposed algorithm not only decreases the computational amount remarkably but also improves the steady-state performance. The dynamic response of the DMPDPC is as fast as that of the MPDPC.

Key words: Active and reactive power, Computing amount, Model predictive control, Neutral point voltage, Three-level converter

I. INTRODUCTION

Three-level (TL) converters are widely utilized in industrial applications as a result of harmonic reduction [1]-[5]. From a topological perspective, TL converters are divided into diode neutral point clamped (DNPC) [6-8], active neutral point clamped (ANPC) [9], [10], and T-type neutral point clamped (TNPC) [1], [2], [11] converters. The unequal loss distribution among the power switches is the fatal flaw of DNPC [9]. ANPC selects different switching states of "O" to achieve loss balance [9], but it intensifies the algorithm complexity. TNPC has no problem of loss distribution in power switches and is taken as an example to express the algorithm proposed in this paper [11].

On account of the fast dynamic response of model predictive control (MPC), many scholars have made great contributions to perfect it [13]-[19].

Manuscript received May 20, 2017; accepted Apr. 11, 2018
Recommended for publication by Associate Editor Jaehong Kim.
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Several MPC algorithms are provided to control grid-connected TL converter systems [13]-[20], and they can be classified into two types: one is model-predictive current control, which controls internal current by selecting the proper right switching state to guarantee its high dynamic and static performance [13]-[15], and the other is model-predictive direct power control (MPDPC). In MPDPC, instantaneous active and reactive power is regulated by selecting the optimal switching state of converters [16]-[19]. In Reference [13], the MPC is proposed to modulate grid current, balance the neutral point (NP) voltage, and reduce the switching frequency of TL converters by selecting the optimal switching state. However, this algorithm costs 27 times cycle computation in TL converters to search the switching state, thereby wasting the considerable computing resources of the main microchip. To improve the computing efficiency of MPC for two-level and TL converters, a simplified finite-control-set MPC with equivalent transformation and a specialized sector distribution method is given in Reference [14] to control the grid current of TL converters. A hierarchical model predictive voltage control strategy based on g-h coordinate space vector modulation is provided in Reference [15]. These approaches can save substantial computing resources, but they cannot assist in improving the steady-state or dynamic performance

of the converters. In Reference [18], the switching state of TL converters is selected based on symmetrical bounds, which have a relationship with the instantaneous active and reactive power and NP voltage; if the parameters of TL converters become out of bounds, then the switching state is changed to return it within bounds. This approach can minimize the switching frequency and reduce the computational burden. In Reference [19], on the basis of symmetrical bounds, the power slope of switching states is considered to further decrease the computational burden and switching frequency. These approaches reduce computational burden but sacrifice the steady-state performances of TL converters, such as active and reactive power ripple, NP voltage ripple, and current total harmonic distortion (THD).

On the basis of the advantages of the algorithms mentioned above, a dual MPDPC (DMPDPC) is proposed in this paper. The DMPDPC cannot only reduce the computational amount greatly but can also improve the steady-state performance of converters. For instance, the proposed DMPDPC can have a lower current THD and smaller NP voltage and active and reactive power ripples than those of the MPDPC.

The rest of this paper is organized as follows: The problem of a large calculation amount when TL converter applies the conventional MPDPC is illustrated in detail in Section II. The DMPDPC is proposed and explained in Section III. The advantage of the DMPDPC is analyzed in Section IV. In Section V, the simulation and experiments are established to verify the effectiveness and superiorities of the DMPDPC. The conclusion is provided in Section VI.

II. PROBLEM STATEMENT

In Fig. 1, the grid-phase voltage and current are expressed as e_{abc} and i_{abc}, respectively, and the output voltage of the TL converter is u_{abc}. The effect on grid-phase current caused by resistance is less than that related to inductance in the AC filter of the grid-connected TL converter system; therefore, the resistance influence is neglected. In terms of the relationship between the grid-phase current and voltage, the derivatives of active and reactive power in static αβ coordinates are [16], [17]

$$\begin{cases} \dfrac{dP}{dt}=\dfrac{3}{2}\left\{e_\alpha[\dfrac{(u_\alpha-e_\alpha)}{L}+\omega i_\beta]+e_\beta[\dfrac{(u_\beta-e_\beta)}{L}-\omega i_\alpha]\right\} \\ \dfrac{dQ}{dt}=\dfrac{3}{2}\left\{e_\beta[\dfrac{(u_\alpha-e_\alpha)}{L}+\omega i_\beta]-e_\alpha[\dfrac{(u_\beta-e_\beta)}{L}-\omega i_\alpha]\right\} \end{cases}, \tag{1}$$

where (e_α, e_β) is the grid-phase voltage, (i_α, i_β) represents the grid-phase current, and (u_α, u_β) denotes the output voltage of the TL converter. L is the inductance of the AC filter. ω is the angular speed. P is the active power, and Q is the reactive power. When v_i works and the output voltage vector of the TL converter is $u_i(u_{\alpha i},u_{\beta i})$, Eq. 1 is rewritten as [17]

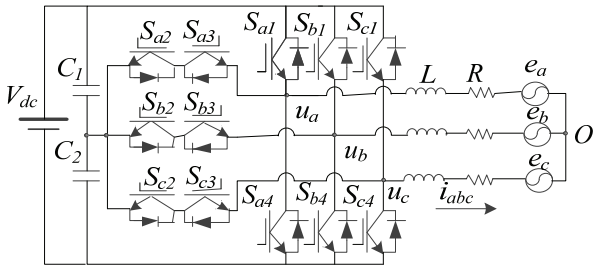


Fig. 1. Topology of the three-phase grid-connected TL converter system.

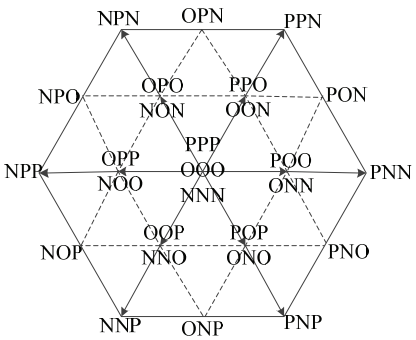


Fig. 2. TL converter space vector diagram.

$$\begin{cases} f_{pi}=\dfrac{dP}{dt}\Big|u_\alpha=u_{\alpha i} \quad u_\beta=u_{\beta i} \\ f_{qi}=\dfrac{dQ}{dt}\Big|u_\alpha=u_{\alpha i} \quad u_\beta=u_{\beta i} \end{cases}. \tag{2}$$

The active power and reactive power at the time instant k+1 are

$$\begin{cases} P(k+1)=f_{pi}T_s+P(k) \\ Q(k+1)=f_{qi}T_s+Q(k) \end{cases}, \tag{3}$$

where k is the current sampling instant, and k+1 is the next one. T_s is the sampling period, and T_s=t(k+1)-t(k). The 27 vectors in Fig. 2 are substituted into Eq. 3. The active and reactive power of each one in the next sampling instant can be predicted. When the ith vector works, the predictive equations are obtained as

$$\begin{cases} P_i^p(k+1)=f_{pi}T_s+P(k) \\ Q_i^p(k+1)=f_{qi}T_s+Q(k) \end{cases}. \tag{4}$$

As shown in Fig. 1, the voltage difference of the two DC-link capacitors is [14], [18], [19]

$$\frac{du_o}{dt}=\frac{1}{C}\left|S_{iabc}\right|^T i_{abc}, \tag{5}$$

where u_o is the voltage difference between the two capacitors, and u_o=u_{c2}-u_{c1}. S_{iabc} is the ith switching state of the TL converter, and $|S_{iabc}|$=$\{|S_a|,|S_b|,|S_c|\}^T$; $S_i(i=a,b,c)\in\{-1,0,1\}$. i_{abc}

is the grid-phase current of the connected system, and $i_{abc}=\{i_a,i_b,i_c\}^{\mathrm{T}}$. C is the capacitance of C_1 and C_2. The voltage difference at time instant $k+1$ can be predicted by [14], [18], [19]

$$u_{oi}^{p}(k+1)=\frac{T_s}{C}\left|S_{iabc}\right|^{T} i_{abc}+u_o(k). \tag{6}$$

Only the NP voltage balance and the performance of active and reactive power of the grid-connected TL converter system are considered due to the space limitation of this paper. The other performances, such as common mode voltage and switching frequency reduction, can be acquired with the similar method mentioned above. The reference voltage difference among the DC-link capacitors is always equal to 0; therefore, the cost function is

$$\begin{aligned} J=&[P_{ref}-P_i^p(k+1)]^2+[Q_{ref}-Q_i^p(k+1)]^2\\ &+\lambda\left|u_{oi}^{p}(k+1)\right|, \end{aligned} \tag{7}$$

where P_{ref} is the reference active power, and Q_{ref} is the reference reactive power. For clarity, Eqs. 4, 6, and 7 are summarized, and the MPDPC is

$$\begin{cases} P_i^p(k+1)=f_{pi}T_s+P(k)\\ Q_i^p(k+1)=f_{qi}T_s+Q(k)\\ u_{oi}^{p}(k+1)=\dfrac{T_s}{C}\left|v_{abc}\right|^{T} i_{abc}+u_o(k)\\ J=[P_{ref}-P_i^p(k+1)]^2+[Q_{ref}-Q_i^p(k+1)]^2\\ \qquad +\lambda\left|u_{oi}^{p}(k+1)\right|\\ switch(k)=\arg\min(J)\quad i=0\sim 24 \end{cases}. \tag{8}$$

The zero vectors include three switching states (PPP, OOO, and NNN) with the same gradient of active and reactive power and without effect on NP voltage. Thus, OOO is selected to replace the others because of its less common mode voltage. Only 25 different switching states exist in the MPDPC. The MPDPC procedures are given as follows to track reference power and balance the NP voltage. The 25 switching states are substituted into the predictive model successively, and the active and reactive power and voltage difference among the DC-link capacitors at time instant $k+1$ are obtained. The optimum switching state is selected according to Eq. 7 to control the switches in the TL converter. The schematic in accordance with Eq. 8 is given in Fig. 3 to express the algorithm clearly [14].

The flow diagram of the MPDPC shown in Fig. 4 is gained according to the schematic in Fig. 3. To select the most optimal switching state, 25 times is required to calculate the power predictive model (Eq. 4), the capacitor voltage difference predictive model (Eq. 6), and the cost function (Eq. 7) in each control period. We need substantial computing

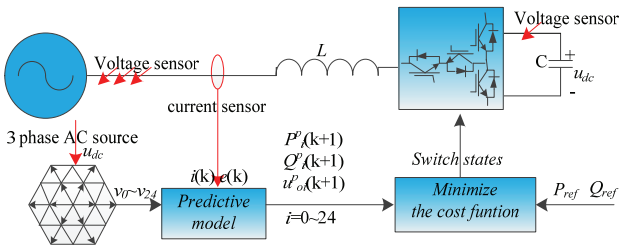


Fig. 3. Schematic of the MPDPC scheme.

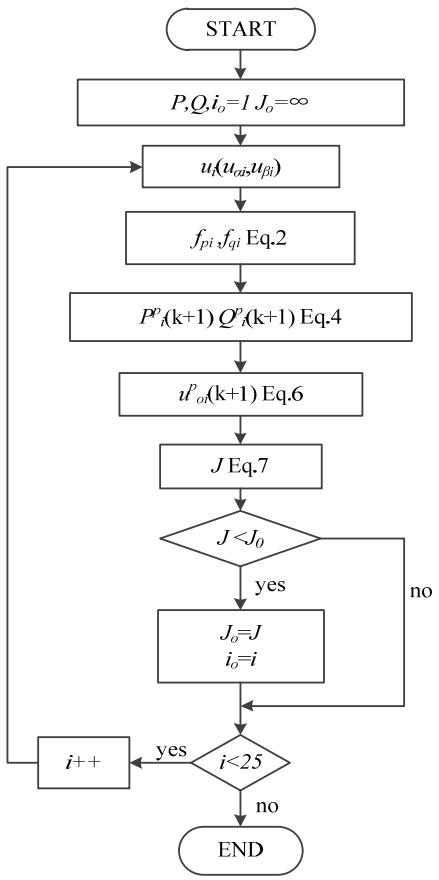


Fig. 4. Flow diagram of the MPDPC.

resources to accomplish this algorithm. Other computational tasks, such as analog-to-digital conversion and serial asynchronous communication, make the calculation of the MPDPC difficult to accomplish. Therefore, a simplified apporach to reducing the MPDPC complexity needs to be proposed.

III. DMPDPC

As shown in Fig. 5, a virtual vector $\tilde{v}$ exists. When the vector $\tilde{v}$ works in the TL converter, the output voltage is $\tilde{u}(\tilde{u}_\alpha,\tilde{u}_\beta)$, and the predictive active and reactive power at time instant $k+1$ is equal to the reference active and reactive power. According to Eqs. 4 and 2, the derivatives of active and reactive power of $\tilde{v}$ are expressed as

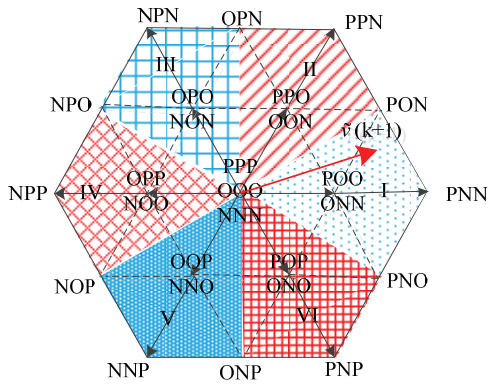


Fig. 5. TL converter space vector sector diagram.

$$\begin{cases} \dfrac{d\tilde{P}}{dt} = \dfrac{P_{ref} - P(k)}{T_s} \\ \dfrac{d\tilde{Q}}{dt} = \dfrac{Q_{ref} - Q(k)}{T_s} \end{cases}. \tag{9}$$

Eqs. 9 and 1 can be combined and converted to

$$\begin{cases} \dfrac{P_{ref} - P(k)}{T_s} = \dfrac{3}{2}\left\{ \begin{array}{l} e_\alpha[\dfrac{(\tilde{u}_\alpha - e_\alpha)}{L} + \omega i_\beta] \\ \quad + e_\beta[\dfrac{(\tilde{u}_\beta - e_\beta)}{L} - \omega i_\alpha] \end{array} \right\} \\ \dfrac{Q_{ref} - Q(k)}{T_s} = \dfrac{3}{2}\left\{ \begin{array}{l} e_\beta[\dfrac{(\tilde{u}_\alpha - e_\alpha)}{L} + \omega i_\beta] \\ \quad - e_\alpha[\dfrac{(\tilde{u}_\beta - e_\beta)}{L} - \omega i_\alpha] \end{array} \right\} \end{cases}. \tag{10}$$

Substituting Eq. 10 into Eq. 7 leads to

$$\begin{aligned} J = & \frac{2L^2}{9T_s^2U_m^2}[(\tilde{u}_\alpha - u_{\alpha i})^2 + (\tilde{u}_\beta - u_{\beta i})^2] \\ & + \lambda \left| u_{oi}^{\,p}(k+1) \right|, \end{aligned} \tag{11}$$

where U_m is the maximum value of grid voltage. Without considering the effect of NP voltage, Eq. 11 shows that the cost function is determined by the distance between $\tilde{v}$ and the alternative vector v_i.

The space vector diagram of the TL converter is divided into six sectors based on the location of $\tilde{v}$. As shown in Fig. 5, the center of each sector is the short vector. When v_{s1} (POO/ONN) works in the TL converter and is the center of sector I, its output voltage is u_{s1} ($u_{s1\alpha}$, $u_{s1\beta}$). The location of $\tilde{v}$ is estimated by

$$J' = \frac{2L^2}{9T_s^2U_m^2}[(\tilde{u}_\alpha - u_{si\alpha})^2 + (\tilde{u}_\beta - u_{si\beta})^2]. \tag{12}$$

Combining Eqs. 10 and 12 leads to

$$J' = [P_{ref} - P_i^p(k+1)]^2 + [Q_{ref} - Q_i^p(k+1)]^2. \tag{13}$$

TABLE I
SWITCH STATES IN EACH SECTOR

Sector	Switch States
I	OOO POO ONN PNO PNN PON
II	OOO PPO OON PON PPN OPN
III	OOO OPO NON OPN NPN NPO
IV	OOO OPP NOO NPO NPP NOP
V	OOO OOP NNO NOP NNP ONP
VI	OOO POP ONO ONP PNP PNO

The output voltages that correspond to the six short vectors are substituted into Eq. 13. As shown in Fig. 5, if $\tilde{v}$ is located in sector I and v_{s1} works, then the cost function J' could yield a minimum value because $\tilde{v}$ is nearest to v_{s1}. Therefore, the sector can be obtained by Eq. 13.

The switching states in each sector are shown in Table I. Six switching states exist in each sector and the adjacent sectors share two switching states. The TL converter aims to make its active and reactive power trace the reference power; consequently, the weight factor λ is small. The NP voltage could be modulated by selecting different switching states of short vector. Thus, when the cost function Eq. 7 is the minimum, the selected switching state must be in the same sector that contains $\tilde{v}$.

The equations used to select the sector in the first step are given as

$$\begin{cases} P_{si}^p(k+1) = f_{pi}T_s + P(k) \\ Q_i^p(k+1) = f_{qi}T_s + Q(k) \\ J' = [P_{ref} - P_i^p(k+1)]^2 + [Q_{ref} - Q_i^p(k+1)]^2 \\ sector(k) = \arg\min(J') \quad i = 0 \sim 5 \end{cases}. \tag{14}$$

The six short vectors are substituted into Eq. 14, and the sector with the least cost function J' is selected. The second step is to obtain the optimal switching state, and the equations are presented as

$$\begin{cases} P_i^p(k+1) = f_{pi}T_s + P(k) \\ Q_i^p(k+1) = f_{qi}T_s + Q(k) \\ u_{oi}^p(k+1) = \dfrac{T_s}{C}\left| v_{abc} \right|^T i_{abc} + u_o(k) \\ J = [P_{ref} - P_i^p(k+1)]^2 + [Q_{ref} - Q_i^p(k+1)]^2 \\ \qquad + \lambda \left| u_{oi}^p(k+1) \right| \\ switch(k) = \arg\min(J) \quad i = 0 \sim 5 \end{cases}. \tag{15}$$

The six switching states in the selected sector in the first step are substituted into Eq. 15, and the switching state with the least cost function J is utilized to control the switches of the TL converter. The switching state makes the active and reactive power trace the reference power and balances the NP voltage simultaneously.

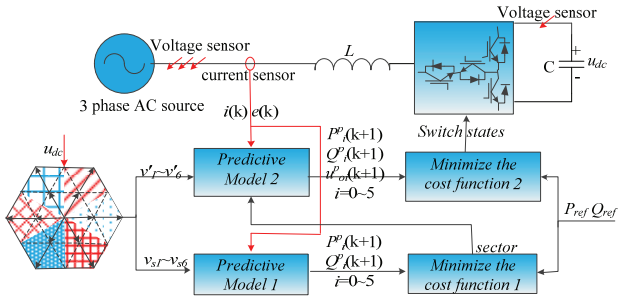


Fig. 6. Schematic of the DMPDPC scheme.

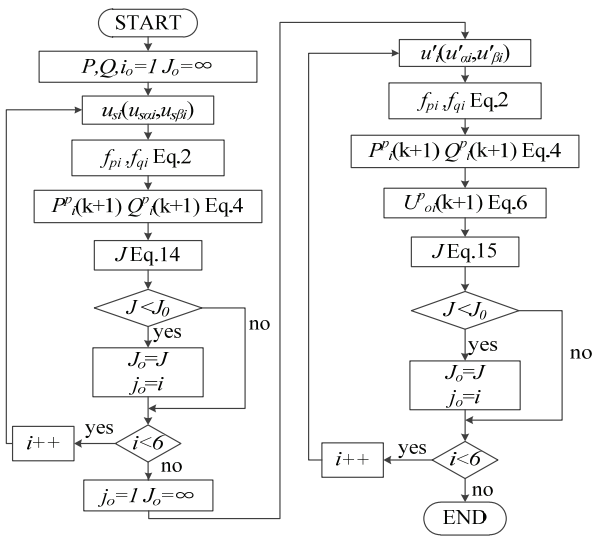


Fig. 7. Flow diagram of the DMPDPC.

The schematic of the DMPDPC shown in Fig. 6 is obtained in accordance with Eqs. 15 and 14. The procedures are summarized as follows: First, six short vectors are substituted into the predictive model, and the sector number is gained through Eq. 14. Second, the switching states of the selected sector are substituted into the predictive model, and the optimal switching state, which makes the active and reactive power of the TL converter trace the reference power and balance the NP voltage, is obtained through Eq. 15.

The flow diagram of the digital signal processor (DSP), as shown in Fig. 7, is built according to the schematic of the DMPDPC. We need to calculate Eqs. 15 and 14 six times to obtain the optimal switching state. Therefore, the DMPDPC improves computing efficiency and reduces the times of cycle computation from 25 to 12. The computational burden of Eq. 13 is less than that of Eq. 7, thereby further reducing the computing cost.

IV. Analysis

At the time instant k in Fig. 8, the sampling of grid voltage and current is finished. The active and reactive power with considering t_{d1} delay are $P^p_i(k+1+t_d/T_s)$ and $Q^p_i(k+1+t_d/T_s)$, respectively. The accuracy predictive equations (Eq. 4) are rewritten as

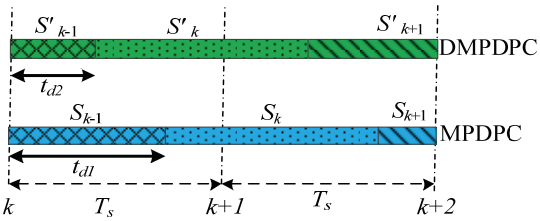


Fig. 8. Operations of the MPDPC and the DMPDPC with t_{d1} ,t_{d2} delay time.

TABLE II
System Parameters

Parameter	Value
Filter inductance	6 mH
DC-link capacitor	1000 μF
DC-link voltage	350 V
Grid line voltage	220 V
Grid frequency	50 Hz
Sampling frequency	10 kHz
Dead time	3 μs
Reference active power	3 kW
Reference reactive power	0 kVar

$$\begin{cases} P_i^p(k+1+\dfrac{t_{d1}}{T_s}) = f_{pi}T_s + P(k+\dfrac{t_{d1}}{T_s}) \\ Q_i^p(k+1+\dfrac{t_{d1}}{T_s}) = f_{qi}T_s + Q(k+\dfrac{t_{d1}}{T_s}) \end{cases}. \quad (16)$$

As for the DMPDPC, the accuracy predictive equations are

$$\begin{cases} P_i^p(k+1+\dfrac{t_{d2}}{T_s}) = f_{pi}T_s + P(k+\dfrac{t_{d2}}{T_s}) \\ Q_i^p(k+1+\dfrac{t_{d2}}{T_s}) = f_{qi}T_s + Q(k+\dfrac{t_{d2}}{T_s}) \end{cases}. \quad (17)$$

In the MPC, Eq. 4 is regarded as the approximate equation of Eqs. 17 and 16 without considering the delay time. In Fig. 8, the active power and reactive power calculated by the sampling grid current and voltage are $P(k)$ and $Q(k)$, respectively. t_{d2} is less than t_{d1}. Thus, the calculation errors between $P(k)$, $Q(k)$ and $P(k+t_{d2}/T_s)$, $Q(k+t_{d2}/T_s)$ in the DMPDPC are less than those of the MPDPC. The performance of the DMPCP is also better than that of the MPDPC [21].

V. Simulation and Experiments

Simulation platforms based on MATLAB/Simulink and experiment desktops are built to validate the effectiveness of the proposed approach. The simulation and experiment parameters are shown in Table II. The results are tested in two aspects. First, the active and reactive power ripple, AC current THD, and NP voltage ripple of the DMPDPC are

lower than those of the MPDPC. Second, the DMPDPC needs less computing resources.

A. Simulation Results

With the assumption that the MPDPC and the DMPDPC have the same delay time, the simulation results, including the current THD and the active and reactive power ripple, of the two algorithms are the same. As shown in Fig. 9, the performance of the TL converter is affected directly by the delay time. Fig. 9(a) indicates that the current THD has a negative relationship with the delay time. Fig. 9(b) shows that the delay time increases the ripple of active and reactive power. The current THD must satisfy the demand of industrial applications. Reducing delay time is a smart decision to improve the performance of the TL converter. In accordance with the results of the following experiment, the delay time of the DMPDPC is 0.038167 ms, which is shorter than the 0.091573 ms of the MPDPC, i.e., the DMPDPC effectively improves the steady-state performance of the TL converter, such as the current THD and active and reactive power ripple.

Fig. 10 shows the waveforms of output line voltage, grid-phase current, active and reactive power, and DC-link capacitor voltages in the TL converter when the reference active power with the MPDPC increases from 0 kW to 3 kW. As shown in Figs. 10(b–c), the settling time of active power is 3 ms, and the overshoot of active power and grid-phase current is eliminated, which means that the dynamic response of the TL converter is fast. However, an obvious distortion occurs in the output line voltage of the TL converter, as shown in Fig. 10(a). The grid-phase current THD of Fig. 10(b) is obtained by Fourier harmonic analysis as 7.6%. As shown in Fig. 10(c), the ripples of active and reactive power are 700 W and 1,000 Var, respectively. The NP voltage ripple in Fig. 10(d) is 6 V.

Fig. 11 provides the dynamic response of the TL converter, including output line voltage, grid-phase current, active and reactive power, and DC-link capacitor voltage, when the reference of active power in the TL converter with the DMPDPC suddenly increases by 3 kW. Unlike the MPDPC, the DMPDPC not only overcomes its static response shortcoming but also has a rapid dynamic response similar to the MPDPC. The settling time of the DMPDPC is approximately 3 ms, and the overshoot of grid-phase current and active power is removed, as shown in Figs. 11(b–c). Moreover, the distortion of output line voltage in the TL converter is obviously reduced, as shown in Fig. 11(a), and the current THD in Fig. 11(b) is decreased from 7.6% to 6.49%. The active and reactive power ripples are 300 W and 400 Var, respectively, which are lower than the ones with MPDPC. The NP voltage ripple is approximately 2 V, which means the DMPCPC is more capable of reducing the NP voltage ripple.

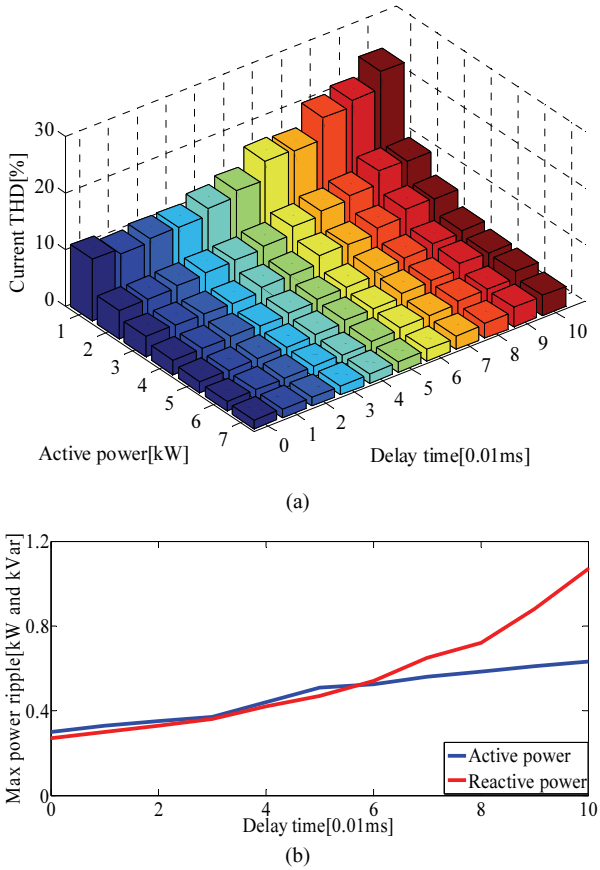


Fig. 9. AC current THD and max active and reactive power ripple of the converter with different delay time and output active power. (a) AC current THD. (b) Max active and reactive power ripple.

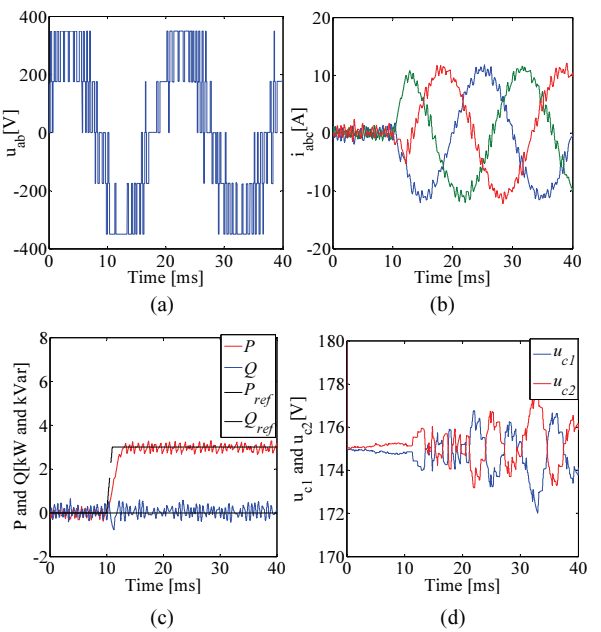


Fig. 10. Dynamic response of the TL converter based on the MPDPC: (a) Output line voltage of the TL converter, (b) Grid line current, (c) Active and reactive power, (d) DC-link capacitor voltages.

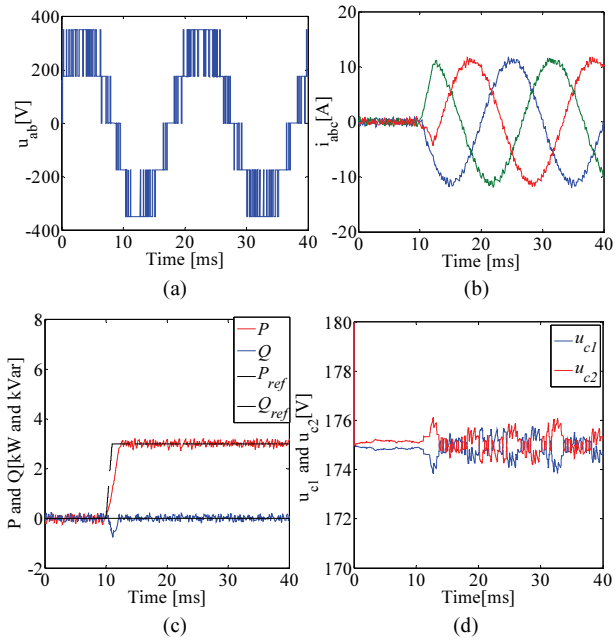


Fig. 11. Dynamic response of the TL converter based on the DMPDPC: (a) TL converter output line voltage, (b) Grid line current, (c) Active and reactive power, (d) DC-link capacitor voltages.

B. Experimental Results

As shown in Fig. 12, the hardware experimental platform of the TL converter is composed of control, sampling, driver, and power boards with power switches of IKW50N60T produced by Infineon. Their functions are as follows. In the control board, the algorithm of DPC is accomplished by a DSP (TMS320F28335), and a complex programmable logic device (EPM570T144C5) decodes the information transmitted from the general purpose input/output of TMS320F28335 for switching states. The sampling board transforms phase current, line voltage, and DC-link voltage into voltage signals to be compatible with the input interface of control board. The switching states from the control board are turned into gate signals by a driver board to turn on/off power switches. The main circuit of the TL converter is placed on the power board installed on the radiator.

When the MPDPC is applied, it requires the main control microchip (TMS320F28335) 13,736 instruction cycles obtained by CCS6.0 to achieve the optimal switching state, and the computing time of the MPDPC is estimated by

$$t_c = t_{soc} N, \tag{17}$$

where t_{osc} is the instruction cycle of TMS320F28335, t_{osc}=6.67 ns[20], and N refers to the instruction cycles spent in executing the MPDPC. They are substituted into Eq. 10, and the computing time of the MPDPC is generated as 0.091573 ms. The TMS320F28335 needs approximately 5,725 instruction cycles to finish the DMPDPC, and the computing time of the DMPDPC is 0.038167 ms.

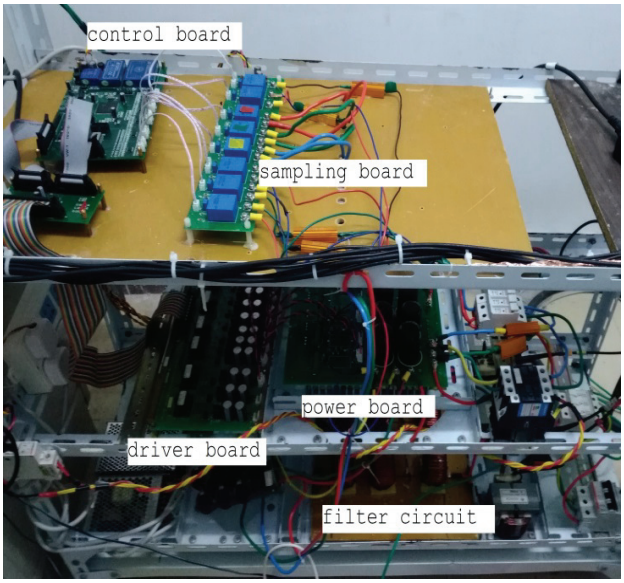


Fig. 12. Hardware experimental platform.

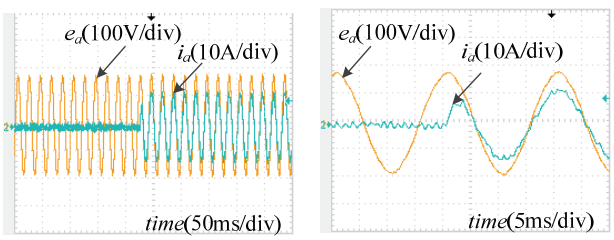
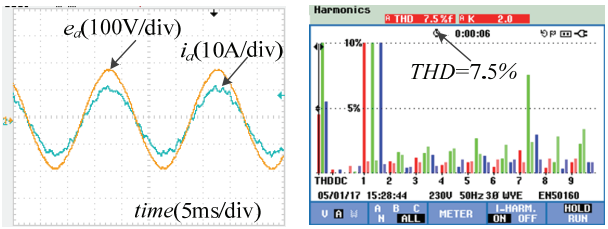


Fig. 13. Dynamic response of grid-phase voltage e_a and current i_a in the TL converter with the MPDPC: (a) Selected by 50 ms, (b) Selected by 5 ms.

Table II shows that the sampling interval of the grid-connected system is 0.1 ms, which is also the control period. Therefore, 91.57% of the computing resources are allocated to deal with the MPDPC, and the rest are used to sample the grid-phase voltage, phase current, and DC-link voltage. The computing resources are insufficient to execute serial asynchronous communication in practical applications. As shown in Fig. 9, the delay time occupied by the calculation of the MPDPC deteriorates the AC current and increases the ripple of active and reactive power. If the TL converter applies the DMPDPC, then only 38.16% of the computing resources is needed to finish the algorithm, thereby addressing the problem of insufficient computing resources.

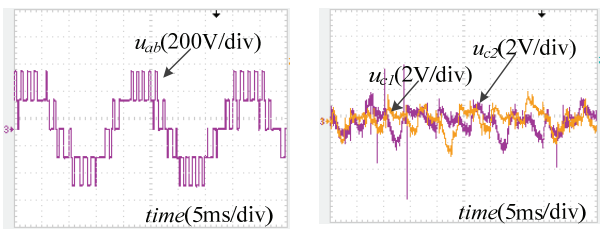
The waveforms of phase voltage and current when the reference of active power is changed from 0 W to 3 kW are given in Fig. 13(a). To clearly observe the process of altering, the waveforms are zoomed in only in the selected 5 ms period, as shown in Fig. 13(b). Fig. 13 validates that the settling time of the MPDPC is short, and overshoot of current is eliminated.

Fig. 14(a) gives the waveforms of the phase voltage and current of the TL converter in steady state. The grid current



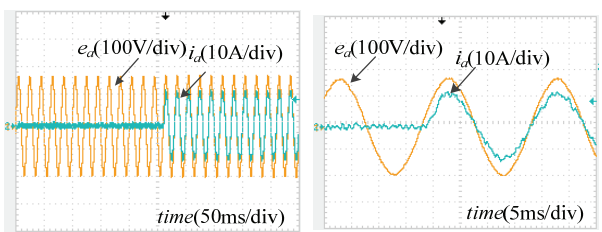
(a) (b)

Fig. 14. Waveforms of phase voltage e_a and current i_a and harmonic analysis of TL converter with the MPDPC in steady state: (a) Grid-phase voltage and current, (b) Grid current spectrum.



(a) (b)

Fig. 15. Waveforms of the output line voltage u_{ab} and DC-link capacitor voltage with the MPDPC: (a) Output line voltage, (b) DC-link capacitor voltages in the AC model of oscilloscope.



(a) (b)

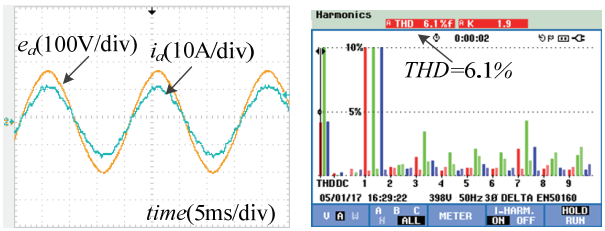
Fig. 16. Dynamic response of grid-phase voltage e_a and current i_a in the TL converter with the DMPDPC: (a) Selected by 50 ms, (b) Selected by 5 ms.

spectrum is shown in Fig. 14(b). The root mean square (RMS) of the grid line voltage and current is measured by Fluke430 as 220.3 V and 8.2 A, respectively. The active power and reactive power are 3108 W and 59.9 Var, respectively, i.e., the power factor is close to 1.

Fig. 15(a) shows distortion in the output line voltage resulting from the delay time of the calculation, and Fig. 15(b) gives the NP voltage ripple as 4 V.

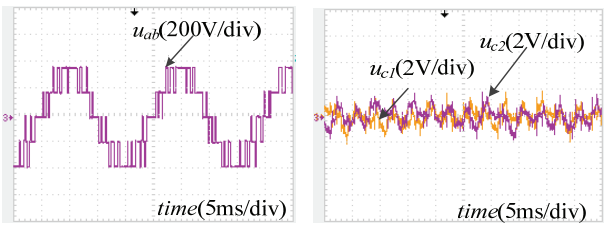
The waveforms of grid-phase voltage and current when the reference active power is changed from 0 W to 3 kW are shown in Fig. 16. Unlike Fig. 13, Fig. 16 shows that the dynamic response of the DMPDPC is as fast as that of the MPDPC.

The RMS of the grid line voltage and current in the TL converter with the DMPDPC is also measured by Fluke435 as 220.0 V and 8.1 A, respectively. The active power and reactive power are 3,102 W and 36.6 Var, respectively. Figs. 17(a–b) show that the DMPDPC reduces the current THD from 7.5% to 6.1%.



(a) (b)

Fig. 17. Waveforms of grid-phase voltage e_a and current i_a and harmonic analysis of the TL converter with the DMPDPC in steady state: (a) Grid-phase voltage and current, (b) Grid current spectrum.



(a) (b)

Fig. 18. Waveforms of the output line voltage u_{ab} and NP voltage of the TL converter with the DMPDPC: (a) Output line voltage, (b) DC-link capacitor voltages in the AC model of oscilloscope.

Fig. 18 shows that the DMPDPC reduces the distortion of output line voltage in the TL converter and the DMPDPC and the NP voltage ripple from 4 V to 2 V.

The simulation and experiment results imply that the dynamic response of the DMPDPC is as fast as that of the MPDPC, but the static performance of the TL converter with the DMPDPC is better than the other as a result of the reduced delay time in steady state.

VI. Conclusion

The DMPDPC is proposed in this paper to reduce the computational burden and improve the steady-state performance of a TL converter on the basis of the MPDPC. Simulation and experimental platforms are established to test the effectiveness of the proposed approach. The simulation and experiment results demonstrate that the proposed algorithm decreases the computational amount by 58.32% and extends the application of the MPDPC. The TL converter with the DMPDPC has lower current THD, less distortion of line voltage, and smaller ripple of active and reactive power and ripple of NP voltage than those of the TL converter with the MPDPC.

In the TL converter, the DMPDPC provides a solution for the MPDPC with fixed switching frequency burdened by a large calculation amount.

Acknowledgment

This work was supported by the Guangdong Science and Technology Foundation of China (2015A010106018) and the

Distinguished Young Teacher Project of the Education Department of Guangdong Province (YQ2015156).

REFERENCES

[1] C. Jian, W. Zheng, W.Yibo, and M. Cheng, "Analysis and control of NPC-3L inverter fed dual three-phase PMSM drives considering their asymmetric factors," *J. Power Electron.*, Vol. 17, No. 6, pp. 1500-1511, Nov. 2017.

[2] Y. Yao, L. Kang, and Z. Zhang, "A novel modulation method for three-Level inverter neutral point potential oscillation elimination," *J. Power Electron.*, Vol. 18, No. 2, pp. 445-455, Mar. 2018.

[3] H. Yap, R. Mohd Amran Mohd, and H. Mohd Khair, "A simplified synchronous reference frame for indirect current controlled three-level inverter-based shunt active power filters," *J. Power Electron.*, Vol. 16, No. 5, pp. 1964-1980, Sep. 2016.

[4] E. Kantar and A. M. Hava, "Optimal design of grid-connected voltage source converters considering cost and operating factors," *IEEE Trans. Ind. Electron.,* Vol. 63, No. 9, pp. 5336-5347, Sep. 2016.

[5] L. Zhang, K. Sun, and Y. Fang, "An optimized common mode voltage reduction PWM strategy for T-type three-phase three-level photovoltaic grid-tied inverter," in *Proc. ECCE*, pp. 1623-1627, 2013.

[6] P. Chaturvedi, S. Jain, and P. Agarwal, "Carrier-based neutral point potential regulator with reduced switching losses for three-Level diode-clamped inverter," *IEEE Trans. Ind. Electron.*, Vol. 61, No. 2, pp.613-624. Feb. 2014.

[7] M. Gnanasundari, M. Rajaram, and S. Balaraman, "Natural balancing of the neutral point potential of a three-level inverter with improved firefly algorithm" *J. Power Electron.*, Vol. 16, No. 4, pp. 1306-1315, Jul. 2016.

[8] J. Pou, R. Pindado, D. Boroyevich, and P. Rodriguez, "Evaluation of the low-frequency neutral-point voltage oscillations in the three-level inverter," *IEEE Trans. Ind. Electron.,* Vol. 52, No. 6, pp. 1582-1588, Dec. 2015.

[9] Y. Jiao, S. Lu, and F. C. Lee, "Switching performance optimization of a high power high frequency three-level active neutral point clamped phase leg," *IEEE Trans. Power Electron.*, Vol. 29, No. 7, pp. 3255-3266, Aug. 2013.

[10] Y. Jiao and F. C. Lee, "New modulation scheme for three-level active neutral-point-clamped converter with loss and stress reduction," *IEEE Trans. Ind. Electron.*, Vol. 62, No. 9, pp. 5468-5479, Feb. 2015.

[11] M. Schweizer and J. W. Kolar, "Design and implementation of a highly efficient three-level T-type converter for low-voltage applications," *IEEE Trans. Power Electron.*, Vol. 28, No. 2, pp. 899-907, Feb. 2013.

[12] P. Acuña, L. Morán, M. Rivera, R. Aguilera, R. Burgos, and V. G. Agelidis, "A single-objective predictive control method for a multivariable single-phase three-level NPC converter-based active power filter," *IEEE Trans. Ind. Electron.*, Vol.62, No.7, pp.4598-4607, Jan. 2015.

[13] R. Vargas, P. Cortes, U. Ammann, J. Rodriguez, and J. Pontt, "Predictive control of a three-phase neutral-point clamped inverter," *IEEE Trans. Ind. Electron.*, Vol. 40, No. 9, pp. 2697-2740, Aug. 2007.

[14] C. Xia, T. Liu, T. Shi, and Z. Song, "A simplified finite-control-set model-predictive control for power converters," *IEEE Trans. Ind. Informat.*, Vol. 10, No. 2, pp. 991-1002, May 2014.

[15] Z. Gong, P. Dai, X. Wu, F. Deng, D. Liu, and Z. Chen, "A hierarchical model predictive voltage control for NPC/H-Bridge converters with a reduced computational burden," *J. Power Electron.*, Vol. 17, No. 1, pp. 136-148, Jan. 2017.

[16] Y. Zhang, Y. Peng, and C. Qu, "Model predictive control and direct power control for PWM rectifiers with active power ripple minimization," *IEEE Trans. Ind. Appl.,* Vol. 52, No. 6, pp. 4909-4918, Nov./Dec. 2016.

[17] S. Vazquez, A. Marquez, R. Aguilera, D. Quevedo, J. I. Leon, and L. G. Franquelo, "Predictive optimal switching sequence direct power control for grid-connected power converters," *IEEE Trans. Ind. Electron.*, Vol. 62, No. 4, pp. 2010-2020, Apr. 2015.

[18] J. Scoltock, T. Geyer, and U. K. Madawala, "Model predictive direct power control for grid-connected NPC converter," *IEEE Trans. Ind. Electron.*, Vol. 62, No. 9, pp. 5319-5328, Sep. 2015.

[19] B. S. Riar, J. Scoltock, and U. K. Madawala, "Model predictive direct slope control for power converters," *IEEE Trans. Power Electron.*, Vol. 32, No. 3, pp. 2278-2289, Mar. 2017.

[20] Texas Instruments Incorporated http://www.ti.com.cn/cn/lit/ds/symlink/tms320f28332.pdf?keyMatch=f28335&tisearch=Search-CN-TechDocs, Mar. 2011.

[21] G. Mirzaeva, G. Goodwin, and C. Townsend, "Dealing with linear and nonlinear time delays under model predictive control of power electronic inverters," in *Proc. ICA-ACCA*, pp. 1-8, 2016.

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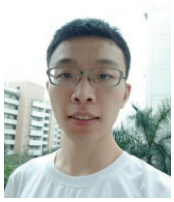

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