

Deadbeat and Hierarchical Predictive Control with Space-Vector Modulation for Three-Phase Five-Level Nested Neutral Point Piloted Converters

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Abstract

To achieve a fast dynamic response and to solve the multi-objective control problems of the output currents, capacitor voltages and system constraints, this paper proposes a deadbeat and hierarchical predictive control with space-vector modulation (DB-HPC-SVM) for five-level nested neutral point piloted (NNPP) converters. First, deadbeat control (DBC) is adopted to track the reference currents by calculating the deadbeat reference voltage vector (DB-RVV). After that, all of the candidate switching sequences that synthesize the DB-RVV are obtained by using the fast SVM principle. Furthermore, according to the redundancies of the switch combination and switching sequence, a hierarchical model predictive control (MPC) is presented to select the optimal switch combination (OSC) and optimal switching sequence (OSS). The proposed DB-HPC-SVM maintains the advantages of DBC and SVM, such as fast dynamic response, zero steady-state error and fixed switching frequency, and combines the characteristics of MPC, such as multi-objective control and simple inclusion of constraints. Finally, comparative simulation and experimental results of a five-level NNPP converter verify the correctness of the proposed DB-HPC-SVM.

Key words: Capacitor voltage balancing control, Deadbeat control, Five-level, model predictive control, Nested neutral point piloted, Space-vector modulation, Stacked multicell converter

I. INTRODUCTION

Multilevel converters have been widely applied to the grid integration of renewable energy sources, motor drives and other fields [1]-[3]. Stacked multicell converters (SMCs) are presented in [4]-[10], which stack several flying capacitor (FC) converters together. When compared to FC converters, SMCs require less energy storage in the capacitors and have

lower switching losses. In [9] and [10], a five-level SMC is described as a five-level nested neutral point piloted (NNPP) converter that is nested by the two modular structures of the phase-leg of a three-level neutral point piloted (NPP) converter.

In order to balance the capacitor voltages for the SMC, some capacitor voltage balancing methods based on pulse width modulation (PWM) are presented in [8]-[10]. In [9], a space vector pulse width modulation (SVPWM) for five-level NNPP converters is proposed to achieve the decoupling control strategies of capacitor voltages and reduce the common-mode voltage. The conventional proportional-integral (PI) controllers with PWM schemes are one of the most common solutions to control power converters. However, the performance of PI controller is closely related to the controller parameters, bandwidth and stability of the controller. Moreover, the dynamic response is slow, especially for cascade PI control.

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In order to address the problems of the conventional PI+PWM, some advanced control strategies are proposed. These strategies include as direct torque control (DTC) [11], direct power control (DPC) [12], deadbeat control (DBC) [13]-[15], and model predictive control (MPC) [16]-[22].

MPC is one of the most promising controllers for power electronic converters [16]-[27]. MPC has the advantages of simple concept, a fast dynamic response, multi-objective control, and easy inclusion of nonlinearities and constraints [18]-[27]. Finite control set MPC (FCS-MPC) takes advantage of the inherent discrete nature of power electronic converters to generate the control signals without an external modulator [18]-[27]. However, traditional FCS-MPC has some disadvantages. These disadvantages include high sampling frequency, high computational burden, complex weighting factor design, and variable switching frequency.

In multilevel converters, the number of candidates of switching states for FCS-MPC increases geometrically with the increase of the output levels [27]. Therefore, the improved FCS-MPC is still an open issue to be investigated to reduce the computational burden [21]. In order to address the issue of the high computational burden in the conventional FCS-MPC, some improved MPC strategies with a reduced computational burden have been proposed in [22]-[24], [27].

In [25], a traditional FCS-MPC for five-level SMC is proposed to achieve the multi-objective control of the load currents and floating-capacitor voltages, which results in a high computational burden. In [26], an improved FCS-MPC is proposed to reduce the computational burden by using the redundancies and separating the whole problem in two different FCS-MPC problems. However, the FCS-MPC strategies in [25] and [26] do not discuss the dc-link capacitor voltages or the switching principle, while resulting in unwanted switching transitions and a variable switching frequency. In [27], a fast FCS-MPC based on switching principle is proposed to reduce the computational cost and avoid the unwanted switching transitions. However, the fast FCS-MPC requires high sampling frequency and complex weighting factor design, and leads to variable switching frequency.

In order to solve the problem of a variable switching frequency and to reduce the ripples of the control variables in the conventional FCS-MPC, some improved predictive control strategies have been proposed in [28]-[33]. These strategies include PWM-based MPC [28], MPC with duty cycle optimization (DCO) [29]-[31] and DBC [14], [32], [33]. In [28], model predictive direct power control (MP-DPC) with modulation function optimization is proposed to achieve zero steady-state errors and a fast dynamic response. In [29], a dead-beat predictive direct power control (DB-DPC) strategy with an improved voltage-vector sequences is presented. This method eliminates the steady-state power errors. An improved two-vector-based model predictive torque control (MPTC) without a weighting factors is presented in [30] to reduce

both torque and flux ripples. In [31], a predictive duty cycle control is proposed to achieve zero steady-state average error and a fast dynamic response. However, the online optimizing algorithm is complicated and has a high computational burden.

According to a predictive model, DBC calculates the required reference voltage vector in order to track the desired reference values of the control variables, which is an inverse-model-based solution. DBC has the advantages of zero steady-state error, a fast dynamic response and easy digital implementation [13]-[15], [32], [33]. However, DBC requires an external modulator and multi-objective control is not easy to implement. In [32], advanced deadbeat direct torque and flux control (A-DB-DTFC) is presented to improve steady-state and transient-state performances by adopting two improved deadbeat methods. In [33], DBC for permanent-magnet synchronous motor (PMSM) drives is proposed to reduce the current and torque ripples.

This paper focuses on the multi-objective optimal control problem (MOOCP) for five-level NNPP converters, including the output currents, floating-capacitor voltage balance, dc-link capacitor voltage balance, and system constraints. A deadbeat and hierarchical predictive control with space-vector modulation (DB-HPC-SVM) is presented to improve the steady-state and dynamic performances. When compared to FCS-MPC in [27], the proposed DB-HPC-SVM does not require high sampling frequency and complex weighting factor design, and achieves fixed switching frequency. According to a system predictive model, the deadbeat reference voltage vector (DB-RVV) is calculated by DBC, which achieves zero steady-state error and a fast dynamic response. According to the fast space-vector modulation (SVM) principle proposed in [9], three basic voltage vectors adjacent to DB-RVV are selected and the corresponding duty cycles are calculated. To solve the problem of a high computational burden, this paper presents a hierarchical MPC. In the first stage, MPC with simple logical judgment is proposed to balance the floating-capacitor voltages. In the second stage, MPC based on optimal switching sequence (OSS) is proposed to control the dc-link capacitor voltages. Comparative simulation and experimental results under dynamic and steady-state conditions are presented to validate the proposed DB-HPC-SVM.

II. SWITCHING PRINCIPLE AND MATHEMATICAL MODEL

A. Five-Level NNPP Converter

A three-phase five-level NNPP converter is shown in Fig. 1. In this paper, x represents phases (a , b , and c). If $V_{dc} = 4E$, the reference voltages of the dc-link capacitors C_1 and C_2 are $2E$, and the reference voltages of floating capacitors C_{fx1} and C_{fx2} are E . The switches S_{x11} and S_{x12} , S_{x15} and S_{x16} , S_{x21} and S_{x22} , and S_{x25} and S_{x26} are two power semiconductor devices

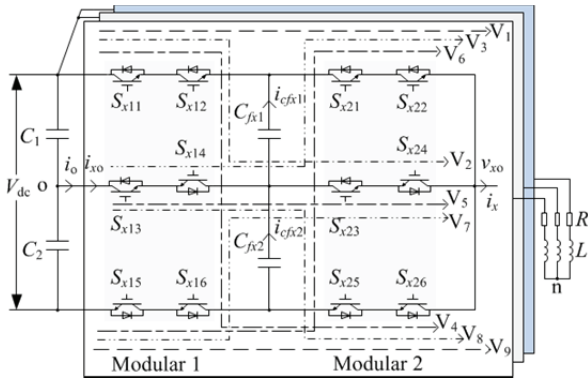


Fig. 1. Three-phase five-level NNPP converter.

 TABLE I
 SWITCH COMBINATIONS OF FIVE-LEVEL NNPP CONVERTER

V_n	S_{x11}	S_{x21}	S_{x13}	S_{x23}	v_{xo}	i_{cfx1}	i_{cfx2}	i_{xo}
V_1	1	1	1	1	$2E$	0	0	0
V_2	1	0	1	1	E	$-i_x$	0	0
V_3	0	1	1	1	E	i_x	0	i_x
V_4	1	0	1	0	0	$-i_x$	$-i_x$	0
V_5	0	0	1	1	0	0	0	i_x
V_6	0	1	0	1	0	i_x	i_x	0
V_7	0	0	0	1	$-E$	0	i_x	0
V_8	0	0	1	0	$-E$	0	$-i_x$	i_x
V_9	0	0	0	0	$-2E$	0	0	0

connected in series. The directions of the instantaneous currents i_o , i_{xo} , i_{cfx1} , i_{cfx2} and i_x are shown in Fig. 1.

The switch combination is defined as $(S_{x11} S_{x21} S_{x13} S_{x23})$, where 1 and 0 represent the turn-on and turn-off statuses, respectively. Five output voltage levels for each phase are generated by nine distinct switch combinations V_1 - V_9 , which are listed in Table I. The output voltage level of each phase is described as the switch variable S_x . The output voltage levels $-2E$, $-E$, 0 , E and $2E$ are represented by 0, 1, 2, 3 and 4 respectively. Moreover, Fig. 1 shows circuit diagrams for all of the work modes of a five-level NNPP converter, which are represented by the switch combinations V_1 - V_9 .

B. Switching Principle

In order to ensure safe operation, the output phase voltage of a multilevel converter should switch between adjacent output levels in a switching process. Moreover, the output phase voltage will be clamped to other unwanted voltage levels during the dead-time period if improper switching operation modes are applied [9], [27]. Therefore, the switching operation of a five-level NNPP converter should meet the switching principle [9], [27]:

1) S_{x11} (S_{x12}) and S_{x14} , S_{x15} (S_{x16}) and S_{x13} , S_{x21} (S_{x22}) and S_{x24} , and S_{x25} (S_{x26}) and S_{x23} operate in the complementary mode in order to avoid a short-circuit between the dc-link capacitors and the floating capacitors.

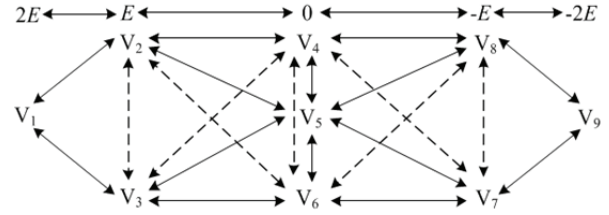


Fig. 2. Switching operation modes of a five-level NNPP converter.

2) S_{x11} , S_{x12} , S_{x15} and S_{x16} as well as S_{x21} , S_{x22} , S_{x25} and S_{x26} should not simultaneously turn on.

3) Switching operation is implemented between adjacent output levels to avoid a high voltage level jump.

4) Switch combinations should follow specific switching operation modes to avoid improper freewheeling circuits and unwanted voltage levels.

Fig. 2 shows the switching operation modes of a five-level NNPP converter. As can be seen in this figure, the specific switching operation modes represented by solid lines meet the above switching principle. In addition, the other switching operation modes represented by dashed lines may lead to high output voltage level jumps.

C. Mathematical Model

According to the topology, the output phase voltage is:

$$v_{xo} = S_{x11}V_{c1} + (S_{x21} - S_{x11})V_{cfx1} + (S_{x13} - 1)V_{c2} + (S_{x23} - S_{x13})V_{cfx2} \quad (1)$$

where V_{c1} , V_{c2} , V_{cfx1} and V_{cfx2} are the voltages of the capacitors C_1 , C_2 , C_{fx1} and C_{fx2} , respectively.

To ensure that the power electronic switching devices work in the safe operating area (SOA), floating-capacitor voltages and dc-link capacitor voltages should be stabilized at their reference voltages [9]. If the capacitor voltages are balanced, v_{xo} can be simplified as:

$$v_{xo} = (S_{x11} + S_{x21} + S_{x13} + S_{x23} - 2)E \quad (2)$$

According to the topology, the instantaneous currents of floating capacitors can be represented by:

$$i_{cfx1}(t) = (S_{x21} - S_{x11})i_x(t) \quad (3)$$

$$i_{cfx2}(t) = (S_{x23} - S_{x13})i_x(t) \quad (4)$$

The total instantaneous current of the dc-link neutral point for three-phase is:

$$i_o(t) = \sum_{x=a}^c [(S_{x13} - S_{x11})i_x(t)] \quad (5)$$

The continuous-time models of the floating-capacitor voltages are:

$$i_{cfx1}(t) = (S_{x21} - S_{x11})i_x(t) = -C_{fx1} \frac{dV_{cfx1}(t)}{dt} \quad (6)$$

$$i_{cfx2}(t) = (S_{x23} - S_{x13})i_x(t) = -C_{fx2} \frac{dV_{cfx2}(t)}{dt} \quad (7)$$

The continuous-time models of the dc-link capacitor voltages are:

$$\begin{cases} i_o(t) = \sum_{x=a}^c [(S_{x13} - S_{x11})i_x(t)] = 2C_1 \frac{dV_{c1}(t)}{dt} \\ i_o(t) = \sum_{x=a}^c [(S_{x13} - S_{x11})i_x(t)] = -2C_2 \frac{dV_{c2}(t)}{dt} \end{cases} \quad (8)$$

The duty cycles of the switches S_{x11} , S_{x21} , S_{x13} and S_{x23} in a sampling period T_s are described as D_{x11} , D_{x21} , D_{x13} and D_{x23} . The average currents of three-phase floating capacitors and dc-link neutral point at the k -th sampling instant are:

$$i_{cfx1}(k) = [D_{x21}(k) - D_{x11}(k)]i_x(k). \quad (9)$$

$$i_{cfx2}(k) = [D_{x23}(k) - D_{x13}(k)]i_x(k). \quad (10)$$

$$i_o(k) = \sum_{x=a}^c \{ [D_{x13}(k) - D_{x11}(k)]i_x(k) \}. \quad (11)$$

In one-step prediction, the discrete-time models of the floating-capacitor voltages and dc-link capacitor voltages are:

$$\begin{cases} V_{cfx1}(k+1) = -\frac{T_s}{C_{fx1}}i_{cfx1}(k) + V_{cfx1}(k) \\ V_{cfx2}(k+1) = -\frac{T_s}{C_{fx2}}i_{cfx2}(k) + V_{cfx2}(k) \end{cases} \quad (12)$$

$$\begin{cases} V_{c1}(k+1) = \frac{T_s}{2C_1}i_o(k) + V_{c1}(k) \\ V_{c2}(k+1) = -\frac{T_s}{2C_2}i_o(k) + V_{c2}(k) \end{cases} \quad (13)$$

For the sake of simplicity, a three-phase five-level NNPP converter feeds the RL load. According to Kirchhoff's voltage law (KVL), continuous-time models of the load currents in the abc coordinate system can be represented by:

$$v_{xn}(t) = v_{xo}(t) - v_{no}(t) = Ri_x(t) + L \frac{di_x(t)}{dt}. \quad (14)$$

where $x = a, b, c$, and $v_{no}(t)$ is the common-mode voltage:

$$v_{no}(t) = \frac{v_{ao}(t) + v_{bo}(t) + v_{co}(t)}{3}. \quad (15)$$

In the dq coordinate system, the continuous-time models of load currents are:

$$\begin{cases} v_d(t) = Ri_d(t) + L \frac{di_d(t)}{dt} - \omega Li_q(t) \\ v_q(t) = Ri_q(t) + L \frac{di_q(t)}{dt} + \omega Li_d(t) \end{cases} \quad (16)$$

where $v_d(t)$, $v_q(t)$, $i_d(t)$ and $i_q(t)$ are the coordinates of output voltages and currents in the dq coordinate system, and ω is the angular frequency.

Fig. 3 shows a block diagram of a conventional PI+SVM based on the dq coordinate system. The fast SVM algorithm for a five-level NNPP converter proposed in [9] is used and the floating-capacitor voltage balance and the dc-link capacitor

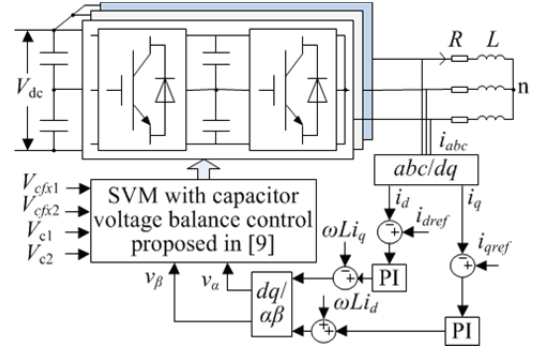


Fig. 3. Block diagram of a conventional PI+SVM.

voltage balance methods are based on the PWM scheme. The floating-capacitor voltages are balanced by selecting appropriate switch combinations for each phase. The dc-link capacitor voltages are balanced by dynamically selecting a seven-segment switching sequence and introducing a regulatory factor [9].

The output current derivative is substituted by a forward Euler approximation. In the abc coordinate system, the discrete-time models of the output currents are:

$$i_x(k+1) = A[v_{xo}(k) - v_{no}(k)] + Bi_x(k). \quad (17)$$

where $A = T_s/L$, $B = 1-RA$ and T_s is the sampling period.

In the $\alpha\beta$ coordinate system, the discrete-time models of output currents are:

$$\begin{cases} i_\alpha(k+1) = Av_\alpha(k) + Bi_\alpha(k) \\ i_\beta(k+1) = Av_\beta(k) + Bi_\beta(k) \end{cases} \quad (18)$$

where $v_\alpha(k)$, $v_\beta(k)$, $i_\alpha(k)$ and $i_\beta(k)$ are the coordinates of the output voltages and currents at the instant k in the $\alpha\beta$ coordinate system.

III. DB-HPC-SVM FOR A FIVE-LEVEL NNPP CONVERTER

In addition to output current control, five-level NNPP converters also suffer from dc-link capacitor voltage balance control and three-phase floating-capacitor voltage balance control problems. Therefore, the control system of a five-level NNPP converter is a multi-objective control system. It can be seen from Table I that nine distinct switch combinations V_1 - V_9 generate the five output voltage levels for each phase. Therefore, the number of three-phase candidate switch combinations used in the enumeration process of conventional FCS-MPC is 9^3 , which greatly increases the computational burden.

This paper proposes DB-HPC-SVM for a five-level NNPP converter. When compared to the FCS-MPC strategies in [25]-[27], the proposed DB-HPC-SVM reduces the steady-state ripples of the control variables and achieves a fixed switching frequency. When compared to the conventional PI+SVM, the proposed DB-HPC-SVM has the advantages of

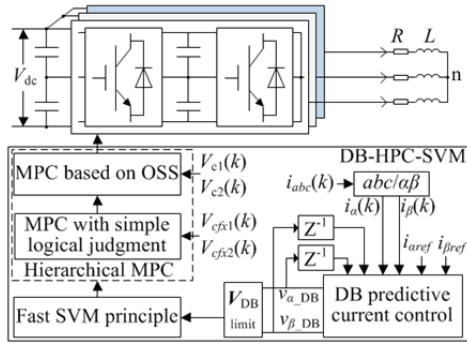


Fig. 4. Block diagram of the proposed DB-HPC-SVM.

a fast dynamic response and easy inclusion of constraints. In [9], in order to reduce the common-mode voltage, the number of redundant switching states is reduced to four or five in a small sector. Therefore, the number of seven-segment switching sequences used to balance the dc-link capacitor voltages are reduced to one or two, which may reduce the dynamic response of the capacitor voltages. Moreover, the capacitor voltage balance methods proposed in [9] are implemented based on the measured voltage and current values at the instant k , and the control actions are applied at the instant $k+1$, which results in a delay problem. In the proposed DB-HPC-SVM, all of the candidate five-segment switching sequences are enumerated by a cost function to balance the capacitor voltages. The number of five-segment switching sequences is always larger than that of the seven-segment switching sequences in [9], which may result in a fast voltage balance capability. Unlike [9], the proposed hierarchical MPC balances the capacitor voltages according to the predictive values of the capacitor voltage and current, which eliminates the delay effects and achieves a fast dynamic response for the capacitor voltages.

Fig. 4 shows a block diagram of the proposed DB-HPC-SVM. As shown in this figure, the proposed DB-HPC-SVM has three main steps.

1) According to the system predictive model, calculate the DB-RVV by means of DBC to track the reference currents.

2) According to the fast SVM principle, determine the three adjacent basic voltage vectors that synthesize the DB-RVV and calculate the corresponding duty cycles.

3) Determine the finite control subset of the hierarchical MPC, which is composed of all of the candidate switching sequences in the optimal small sector. Then select the OSC and OSS by the hierarchical MPC to balance the capacitor voltages.

The stability of the predictive control in power converters is still an open topic of research [13, 21, 33]. In [13], the stability and robustness of deadbeat current controllers are enhanced by using delay compensation and an adaptive load model. In [33], it is demonstrated that model predictive direct current control guarantees stability and provides robustness under parameter uncertainties.

In the proposed DB-HPC-SVM, the DB-RVV is calculated based on the system predictive model to achieve zero steady-state error of the output currents. DB-RVV is the continuous variable and is always synthesized by the candidate switching sequences. Moreover, only switching sequences that synthesize the DB-RVV are considered in the hierarchical MPC. Then the OSC and OSS are selected from the candidate switching sequences to balance the capacitor voltages. Therefore, the proposed DB-HPC-SVM guarantees practical stability. In order to address the parameter sensitivity issue of the deadbeat controller, the novel adaptive self-tuning load model proposed in [13] and the repetitive-control-based observer proposed in [14] can be used.

A. DBC

In multilevel converters, the number of candidate voltage vectors increases exponentially with the number of output voltage levels. The conventional FCS-MPC enumerates all candidates to minimize the cost function at every sampling interval, which leads to high computational burden. This paper uses DBC to calculate the DB-RVV directly instead of selecting the optimal voltage vector (OVV) in the voltage vector selection process. This avoids enumerating all of the candidate voltage vectors in the FCS-MPC.

In general, the control strategies require massive calculations, which introduces the time delay during execution. According to the Lagrange extrapolation formula, the future reference values of the output currents at the instant $k+2$ can be estimated as:

$$i_x^*(k+2) = 6i_x^*(k) - 8i_x^*(k-1) + 3i_x^*(k-2). \quad (19)$$

where $i_x^*(k+2)$, $i_x^*(k)$, $i_x^*(k-1)$ and $i_x^*(k-2)$ are the reference values of the currents at the instants $k+2$, k , $k-1$ and $k-2$, respectively.

The discrete-time models of the output currents at the instant $k+2$ in the $\alpha\beta$ coordinate system can be predicted:

$$\begin{cases} i_{\alpha}(k+2) = A v_{\alpha}(k+1) + B i_{\alpha}(k+1) \\ i_{\beta}(k+2) = A v_{\beta}(k+1) + B i_{\beta}(k+1) \end{cases} \quad (20)$$

In theory, as long as the required reference voltage vector is within the converter output capacity, zero steady-state error of the output current can be achieved at the instant $k+2$. By making the output currents at the instant $k+2$ equal to the desired reference values, the required reference voltage vector applied at the instant $k+1$ is described as the deadbeat reference voltage vector $V_{DB}(k+1)$ and is calculated from (18)-(20).

$$\begin{bmatrix} v_{\alpha_DB}(k+1) \\ v_{\beta_DB}(k+1) \end{bmatrix} = \frac{1}{A} \begin{bmatrix} i_{\alpha}^*(k+2) \\ i_{\beta}^*(k+2) \end{bmatrix} - B \begin{bmatrix} v_{\alpha}(k) \\ v_{\beta}(k) \end{bmatrix} - \frac{B^2}{A} \begin{bmatrix} i_{\alpha}(k) \\ i_{\beta}(k) \end{bmatrix}. \quad (21)$$

where $v_{\alpha_DB}(k+1)$ and $v_{\beta_DB}(k+1)$ are the coordinates of $V_{DB}(k+1)$ at the instant $k+1$ in the $\alpha\beta$ coordinate system, $i_{\alpha}^*(k+2)$ and $i_{\beta}^*(k+2)$ are the future reference values of the output currents at the instant $k+2$ in the $\alpha\beta$ coordinate system.

The maximal output voltage capacity of a power electric converter is generally restricted by the dc-link voltage. In this paper, DB-RVV is generated by using the fast SVM principle. Therefore, the output voltage of the converter should follow:

$$\sqrt{v_{\alpha_DB}^2(k+1) + v_{\beta_DB}^2(k+1)} \leq V_{dc} / \sqrt{3}. \quad (22)$$

B. Fast SVM Principle

In this paper, all of the candidate switching sequences that synthesize DB-RVV are obtained by using the fast SVM principle based on the gh coordinate system proposed in [9]. This SVM principle is easily implemented by addition and subtraction calculations without the need for a complex sector judgment or a large number of trigonometric calculations.

Fig. 5 shows the first big sector of a five-level space vector diagram. The small sector which contains DB-RVV is described as the deadbeat optimal small sector. The duty cycles of the three adjacent basic voltage vectors in the deadbeat optimal small sector are calculated as D_1 , D_2 and D_3 . All of the redundant switching states in the deadbeat optimal small sector can be obtained by using the fast SVM principle. Thus, all of the candidate switching sequences for the hierarchical MPC are derived.

As shown in Fig. 5, there are seven redundant switching states in the deadbeat optimal small sector for $V_{DB}(k+1)$. In order to reduce the switching losses, the five-segment switching sequence is adopted in this paper. There are five candidate switching sequences in the deadbeat optimal small sector for $V_{DB}(k+1)$, as listed in Table II.

Moreover, due to the redundancy of the switch combinations for each phase, each switching sequence has several different three-phase switching operation modes to generate three-phase control signals. According to the switching operation modes in Fig. 2, the number of three-phase switching operation modes for each switching sequence can be obtained, which is described as N . Taking $V_{DB}(k+1)$ as an example, the number N for each switching sequence is listed in Table II. According to the duty cycles of each voltage vector in the switching sequence and the specific switching operation mode for each phase, the corresponding duty cycles of each switch can be calculated.

C. Hierarchical MPC

In order to reduce the computational burden, this paper presents the hierarchical MPC, which is divided into two stages: MPC with a simple logical judgment and MPC based on OSS. In the first stage, according to the redundancy of the switch combination, the floating-capacitor voltages are

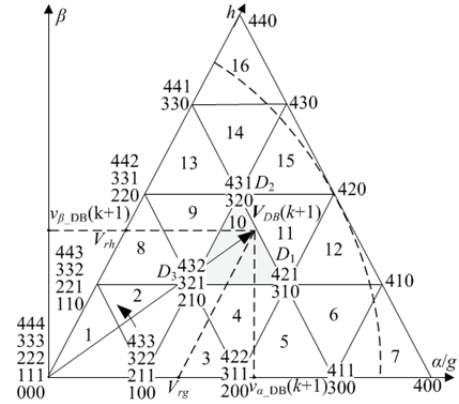


Fig. 5. First big sector of a five-level space vector diagram.

TABLE II
FIVE-SEGMENT CANDIDATE SWITCHING SEQUENCES

Switching sequences	N	$i_o(k+1)$ in one case
210-310-320-310-210	4*4*1	$-i_c(k+1)*(D_3+D_1+D_2)$
310-320-321-320-310	1*4*2	$-i_c(k+1)*(D_1+D_2)$
320-321-421-321-320	2*1*2	$-i_c(k+1)*D_2 - i_a(k+1)*D_1$
321-421-431-421-321	2*4*1	$-i_a(k+1)*(D_1+D_2)$
421-431-432-431-421	1*4*4	$-i_a(k+1)*(D_1+D_2+D_3)$

balanced by selecting the OSC for each phase. In the second stage, according to the redundancy of the switching sequence, the control objectives of the dc-link capacitor voltages and the switching constraints are evaluated in a cost function to obtain OSS. Therefore, the computational burden is significantly reduced without sacrificing the fast dynamic response.

The average currents of floating capacitors and dc-link neutral point at the instant $k+1$ are calculated as:

$$i_{cfx1}(k+1) = [D_{x21}(k+1) - D_{x11}(k+1)]i_x(k+1). \quad (23)$$

$$i_{cfx2}(k+1) = [D_{x23}(k+1) - D_{x13}(k+1)]i_x(k+1). \quad (24)$$

$$i_o(k+1) = \sum_{x=a}^c \{ [D_{x13}(k+1) - D_{x11}(k+1)]i_x(k+1) \}. \quad (25)$$

Discrete-time models of the floating-capacitor voltages and dc-link capacitor voltages at the instant $k+2$ are represented by:

$$\begin{cases} V_{cfx1}(k+2) = -\frac{T_s}{C_{fx1}}i_{cfx1}(k+1) + V_{cfx1}(k+1) \\ V_{cfx2}(k+2) = -\frac{T_s}{C_{fx2}}i_{cfx2}(k+1) + V_{cfx2}(k+1) \end{cases} \quad (26)$$

$$\begin{cases} V_{c1}(k+2) = \frac{T_s}{2C_1}i_o(k+1) + V_{c1}(k+1) \\ V_{c2}(k+2) = -\frac{T_s}{2C_2}i_o(k+1) + V_{c2}(k+1) \end{cases} \quad (27)$$

Moreover, extra switching control between two adjacent

switching sequences is added to the cost function to reduce the switching transitions. The number of the switches that change between two adjacent sampling periods is calculated by using the last three-phase switch combinations at the instant k and the first three-phase switch combinations at the instant $k+1$. The number of extra switching transitions between two adjacent switching sequences is:

$$F_{num} = \sum_{x=a}^c (|S_{x11}(k+1) - S_{x11}(k)| + \dots). \quad (28)$$

In the FCS-MPC strategies in [25]-[27], the control objectives of the output currents, dc-link capacitor voltages and three-phase floating-capacitor voltages and system constraints are included in a cost function to achieve multi-objective control. All of the three-phase candidate switch combinations are evaluated by the cost function in [25]. The cost function for the conventional FCS-MPC is:

$$\begin{aligned} g_1 = & |i_{\alpha}^*(k+2) - i_{\alpha}(k+2)| + |i_{\beta}^*(k+2) - i_{\beta}(k+2)| \\ & + W_{dc} |V_{c1}(k+2) - V_{c2}(k+2)| + W_{fs} F_{num} \\ & + W_{cf} \sum_a^c \sum_{i=1}^2 |V_{cfxi}(k+2) - V_{cref}| \end{aligned} \quad (29)$$

where W_{dc} , W_{cf} and W_{fs} are the weighting factors, $V_{cref} = V_{dc}/4$.

However, the complexity of the weighting factor design for different control variables is significantly increased. In general, the different natures of the control variables hinder the design of the weighting factors [21]. Moreover, the conventional FCS-MPC requires an exhaustive exploration of all the possible states by using (29), which significantly increases the computational burden. In [27], the number of candidate switch combinations is reduced from 9^3 to 4^3 by using switching principle.

In this paper, the output currents are controlled by DBC, and all of the candidate switching sequences are obtained by using the fast SVM principle. The control variables in this stage are reduced to capacitor voltages and system constraints. Moreover, the finite control subset of MPC is a component of the candidate switching sequences. All of the candidate switching sequences can be evaluated by the cost function as follows:

$$\begin{aligned} g_2 = & |V_{c1}(k+2) - V_{c2}(k+2)| + W_{fs} F_{num} \\ & + W_{cf} \sum_a^c \sum_{i=1}^2 |V_{cfxi}(k+2) - V_{cref}| \end{aligned} \quad (30)$$

According to the switching operation modes in Fig. 2, the maximum number of reasonable switching operation modes between adjacent output voltage levels is 4. In a five-segment switching sequence, there are two phases to change the output voltage level and there is a phase to maintain the output voltage level. Therefore, the maximum number of three-phase switching operation modes for each switching sequence is 4^2 , which increases the computational burden.

In order to address the problems of a high computational

burden and a complex weighting factor design in the conventional FCS-MPC with a cost function (30), a hierarchical MPC is proposed to control the floating-capacitor voltages and the dc-link capacitor voltages by using different MPC methods.

As listed in Table I, a five-level NNPP converter has the redundant switch combinations to generate the same output voltage level. In order to simplify the switching operation, V_5 is chosen to generate the output level of 0 in this paper. The switch combinations V_2 and V_3 have opposite effects on the voltage of the floating capacitor $C_{f\alpha 1}$, and the switch combinations V_7 and V_8 have the opposite effects on the voltage of the floating capacitor $C_{f\alpha 2}$.

Since the floating-capacitor voltages for each phase are only related to the switch combinations corresponding to the single-phase output voltage level, the floating-capacitor voltages for each phase can be independently balanced. Moreover, because the number of redundant switch combinations used in this paper is only two, the cost function can be replaced by a simple logical judgment method. Unlike the method in [9], in order to compensate the digital implementation delay, the OSC applied at the instant $k+1$ for each phase is selected by a simple logical judgment based on predictive values at the instant $k+1$. Therefore, in the first stage, MPC with a simple logical judgment for each phase is adopted in this paper, which avoids the three-phase unified control and reduces the computational burden.

According to the predictive values of the floating-capacitor voltages and the output currents at the instant $k+1$, the OSC for each phase is determined by a simple logical judgment as follow. If $[V_{cf\alpha 1}(k+1) - V_{cref}]i_x(k+1) > 0$, V_3 is chosen to generate the output level E . When the opposite is true, V_2 is chosen. If $[V_{cf\alpha 2}(k+1) - V_{cref}]i_x(k+1) > 0$, V_7 is chosen to generate the output level $-E$. When the opposite is true, V_8 is chosen.

After the OSC for each phase is selected by the simple logical judgment, each switching sequence has only one three-phase switching operation mode to generate the three-phase control signals. As a result, the maximum number of three-phase switching operation modes for each switching sequence is reduced from 4^2 to 1. The corresponding duty cycles of each switch at the instant $k+1$ can be calculated. According to (25) and (27), the dc-link capacitor voltages at the instant $k+2$ can be predicted.

Since there are several redundant switching states for a multilevel converter to generate the same basic voltage vector, different five-segment switching sequences can be obtained to synthesize the same DB-RVV in the deadbeat optimal small sector.

As listed in Table II, five candidate switch sequences in the deadbeat optimal small sector can be applied to synthesize $V_{DB}(k+1)$ at the instant $k+1$. If V_8 is selected to generate the voltage level $-E$ and V_3 is selected to generate the voltage

TABLE III
MAIN PARAMETERS OF THE SIMULATION MODEL

Parameter	Value
dc-link voltage	5000V
Dc-link capacitors	4700 μ F
Floating capacitors	2200 μ F
Switching frequency	2kHz
Fundamental frequency	50Hz
RL load	10 Ω , 30mH

level E for three phases by using the MPC with a simple logical judgment, the neutral-point current $i_o(k+1)$ for each candidate switch sequence in this case is listed in Table II.

According to the redundancy of the switching sequence, the dc-link capacitor voltages are balanced by using the MPC based on the OSS. All of the five-segment candidate switching sequences are evaluated by the cost function and the switching sequence minimizing the cost function is selected as the OSS.

Moreover, in order to reduce the switching losses, an extra switching control between two adjacent switching sequences is added to the cost function. The cost function for the MPC in the second stage is:

$$g_3 = |V_{c1}(k+2) - V_{c2}(k+2)| + W_{fs} F_{num}. \quad (31)$$

When compared with the conventional FCS-MPC with a cost function (30), the hierarchical MPC reduces the computational burden and avoids a complex weighting factor design.

IV. SIMULATION RESULTS

To evaluate the proposed DB-HPC-SVM, a three-phase five-level NNPP converter simulation model is constructed using MATLAB software. Comparative simulation results between the conventional PI+SVM, the conventional FCS-MPC with a cost function (29) and the proposed DB-HPC-SVM are presented. The main parameters of the simulation model are listed in Table III. The output reference currents in the dq coordinate system are $i_{dref} = 35.35$ A and $i_{qref} = 91.91$ A. Then they are changed to $i_{dref} = 35.35$ A and $i_{qref} = 183.82$ A at 0.15 s.

To ensure fairness, the sampling frequency f_s for the conventional FCS-MPC is chosen as 10 kHz. By using the branch and bound techniques, the weighting factors in the conventional FCS-MPC are as follows: $W_{cf} = 0.3$, $W_{dc} = 0.4$, and $W_{fs} = 1.8$. The switching frequency band is mainly distributed between 1 kHz and 3 kHz. The PI controller parameters are as follows: $K_p = 2.0$, $K_i = 150$ and $f_s = 2$ kHz. In the proposed DB-HPC-SVM, the control parameters are as follows: $W_{fs} = 0.5$ and $f_s = 2$ kHz.

Fig. 6 shows comparative simulation results of the line voltage and three-phase output currents between three different

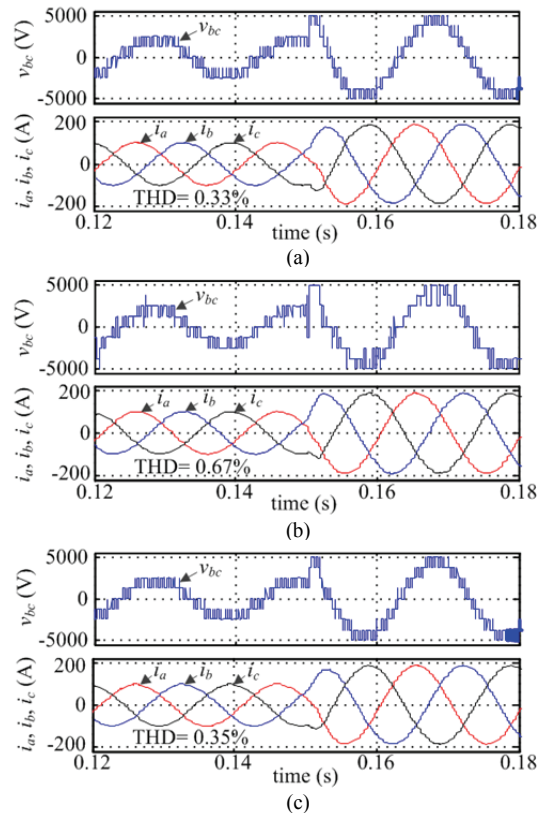


Fig. 6. Simulation results for different control strategies under dynamic conditions: (a) Conventional PI+SVM; (b) Conventional FCS-MPC; (c) Proposed DB-HPC-SVM.

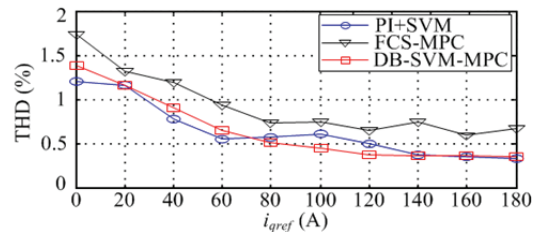


Fig. 7. Plots of current THD versus i_{qref} for three control strategies.

control strategies under dynamic conditions. As shown in Fig. 6(a)-(c), the output current THDs for the three different control strategies when $i_{dref} = 35.35$ A and $i_{qref} = 183.82$ A are 0.33%, 0.67% and 0.35%. It can be clearly observed from Fig. 6 that the dynamic response times for three different control strategies are 8 ms, 2 ms and 3 ms.

As can be observed from Fig. 6(a) and (c), the proposed DB-HPC-SVM obtains similar steady-state current ripples when compared to the conventional PI+SVM, while achieving a fast dynamic response. As can be observed from Fig. 6(b) and (c), the proposed DB-HPC-SVM reduces the steady-state current ripples and current THD when compared to the conventional FCS-MPC, while achieving a fast dynamic response. Nevertheless, the dynamic response time for the proposed DB-HPC-SVM is a little larger than that for the conventional FCS-MPC. This can be explained by the higher

sample frequency of the FCS-MPC. Comparative simulation results show that the proposed DB-HPC-SVM combines the advantages of DBC, SVM, and MPC to improve both the steady-state and dynamic performances.

Moreover, as shown in Fig. 6(b), the output voltage for the conventional FCS-MPC shows a high output voltage level jump and unwanted switching transitions, especially under dynamic conditions. It can be seen from Fig. 6(a) and (c) that the proposed DB-HPC-SVM and the conventional PI+SVM avoid high output voltage level jumps and unwanted switching transitions.

To evaluate the steady-state performance of the three control strategies, the output current quality is evaluated in term of the THD. Fig. 7 shows plots of the current THD versus i_{qref} for the three control strategies when $i_{dref} = 35.35$ A. It can be seen from Fig. 7 that the proposed DB-HPC-SVM provides a lower current THD when compared to the conventional FCS-MPC. This can be explained by the fact that the DBC achieves zero steady-state error of the output currents. Moreover, the proposed DB-HPC-SVM and the conventional PI+SVM present similar current THDs in most of the i_{qref} range. Therefore, the proposed DB-HPC-SVM maintains similar steady-state performance of the output current with the PI+SVM. Simulation results show that the proposed DB-HPC-SVM maintains the advantages of zero steady-state error and a fast dynamic response.

In order to verify the steady-state tracking performance of the three different control strategies, Fig. 8 shows comparisons of the tracking error of i_b between the three different control strategies when $i_{dref} = 35.35$ A and $i_{qref} = 183.82$ A. As can be seen from Fig. 8(a)-(c), the steady-state tracking error of i_b for the conventional FCS-MPC is the largest, and the proposed DB-HPC-SVM and the conventional PI+SVM provide similar steady-state tracking performance.

To verify the improved harmonic spectrum of the proposed DB-HPC-SVM, Fig. 9 shows a FFT analysis of the line voltage for the three different control strategies when $i_{dref} = 35.35$ A and $i_{qref} = 183.82$ A. It can be seen from Fig. 9(a) that the harmonic spectrum for the conventional PI+SVM is mainly concentrated around the switching frequency f_s and its multiples. As shown in Fig. 9(b), the conventional FCS-MPC results in a variable switching frequency and a spread spectrum. Moreover, the line voltage contains some low-order harmonics that are not easily eliminated by an output filter. As shown in Fig. 9(c), the proposed DB-HPC-SVM improves the generated waveforms harmonic spectrum with a fixed switching frequency.

One of the main contributions of the proposed DB-HPC-SVM is its ability to achieve a fixed switching frequency. As shown in Fig. 9, although the proposed DB-HPC-SVM provides a higher voltage THD than the conventional FCS-MPC, the proposed DB-HPC-SVM improves the harmonic spectrum with a fixed switching frequency and eliminates

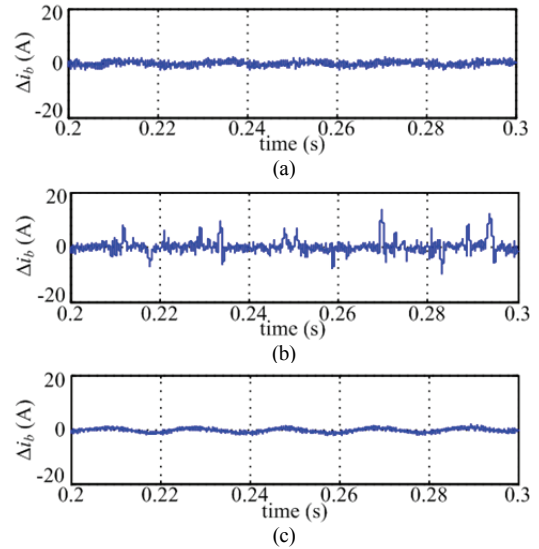


Fig. 8. Tracking error of i_b for different control strategies: (a) Conventional PI+SVM; (b) Conventional FCS-MPC; (c) Proposed DB-HPC-SVM.

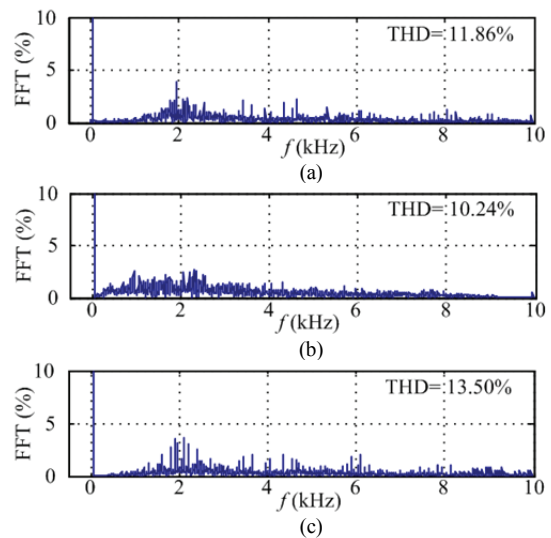


Fig. 9. FFT analysis of the line voltage for different control strategies: (a) Conventional PI+SVM; (b) Conventional FCS-MPC; (c) Proposed DB-HPC-SVM.

low-order harmonics. The increment of the THD is mainly caused by the harmonics around the switching frequency, which are easy to filter. Moreover, the line voltage THD for the proposed DB-HPC-SVM is higher than that for the conventional PI+SVM. This can be explained by the fact that all of the five-segment switching sequences are dynamically selected by the MPC and require fewer switching transitions in a switching period. However, the seven-segment switching sequence used in [9] is generally predefined and requires higher switching transitions in a switching period.

Fig. 10 shows comparative simulation results of the capacitor voltages for different control strategies. As shown in Fig. 10, all three control strategies can balance the three-

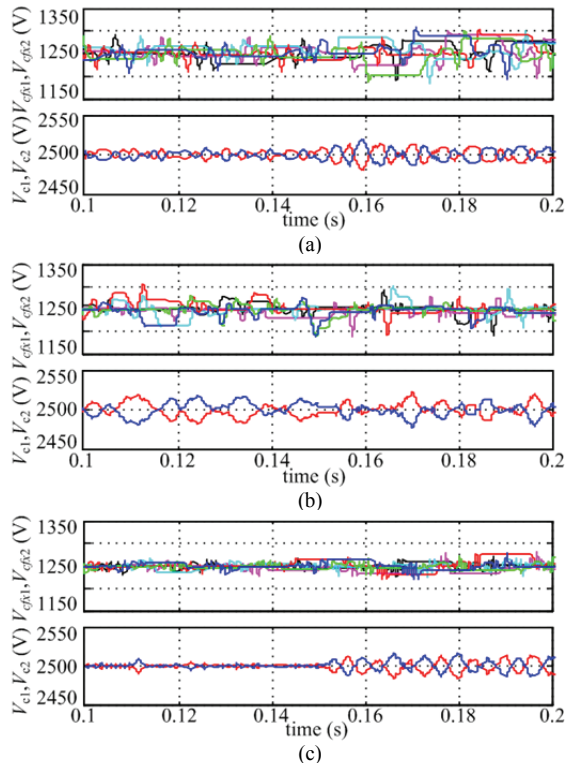


Fig. 10. Simulation results of capacitor voltages for different control strategies: (a) Conventional PI+SVM; (b) Conventional FCS-MPC; (c) Proposed DB-HPC-SVM.

phase floating-capacitor voltages and dc-link capacitor voltages under steady-state and dynamic conditions.

As can be seen from Fig. 10(a), the fluctuation amplitude of the floating-capacitor voltages for the conventional PI+SVM is maximal and the dc-link capacitor voltage ripples are average. As shown in Fig. 10(b), by using the conventional FCS-MPC, the fluctuation amplitude of the floating-capacitor voltages is average and the dc-link capacitor voltage ripples are maximal. As shown in Fig. 10(c), the fluctuation amplitudes of the floating-capacitor voltages and the dc-link capacitor voltages are minimal using the proposed DB-HPC-SVM. Comparative simulation results show that the proposed DB-HPC-SVM reduces the capacitor voltage ripples. On the one hand, the predictive values of the floating-capacitor voltages and output currents at the instant $k+1$ are used in the MPC with a simple logical judgment to balance the floating-capacitor voltages. On the other hand, the dc-link capacitor voltages at the instant $k+2$ are predicted in the MPC based on OSS to compensate the control delay. Moreover, the proposed DB-HPC-SVM avoids the complex weighting factor design and the interaction effect between different control variables.

V. EXPERIMENTAL RESULTS

An experimental setup of a five-level NNPP converter shown in Fig. 11 has been constructed to verify the proposed

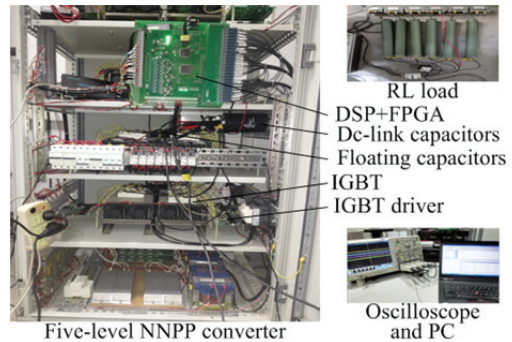


Fig. 11. Experimental setup of a five-level NNPP converter.

TABLE IV
MAIN PARAMETERS FOR THE EXPERIMENTAL SETUP

Parameter	Value
dc-link voltage	200V
Dc-link capacitors	6800 μ F
Floating capacitors	3400 μ F
Switching frequency	2kHz
Fundamental frequency	50Hz
RL load	5 Ω , 15mH

DB-HPC-SVM. The proposed DB-HPC-SVM has been implemented by the control system which contains a DSP (TI TMS320F28335) and a FPGA (ACTEL A3P250). Table IV shows the main experimental parameters. In order to keep the capacitor voltage fluctuations within an allowable range, the capacitance of the floating capacitors and dc-link capacitors required in a low voltage system is greater than that in simulation. In a low-voltage experimental setup, the parameters of the RL load are designed to generate one-tenth the output currents of the simulation with a similar modulation index.

Since the conventional FCS-MPC has a high computational burden and is not easy to implement, experimental results of the conventional FCS-MPC are not presented. Comparative experimental results between the conventional PI+SVM and the proposed DB-SVM-MPC are presented. The PI controller parameters are as follows: $K_p = 1.2$, $K_i = 70$ and $f_s = 2$ kHz. In the proposed DB-SVM-MPC, the control parameters are as follows: $W_{is} = 0.5$ and $f_s = 2$ kHz. The output reference currents in the dq coordinate system are as follow: $i_{dref} = 3.535$ A, and i_{qref} changes from 9.191 A to 18.382 A under dynamic conditions.

A. Steady-state Performance

Fig. 12 shows a comparisons of the phase voltage, line voltage, dc-link voltage and output current between the conventional PI+SVM and the proposed DB-HPC-SVM under steady-state conditions, when $i_{dref} = 3.535$ A and $i_{qref} = 18.382$ A. As shown in Fig. 12, the line voltages and output currents for both control strategies have similar steady-state performances. The proposed DB-HPC-SVM achieves zero

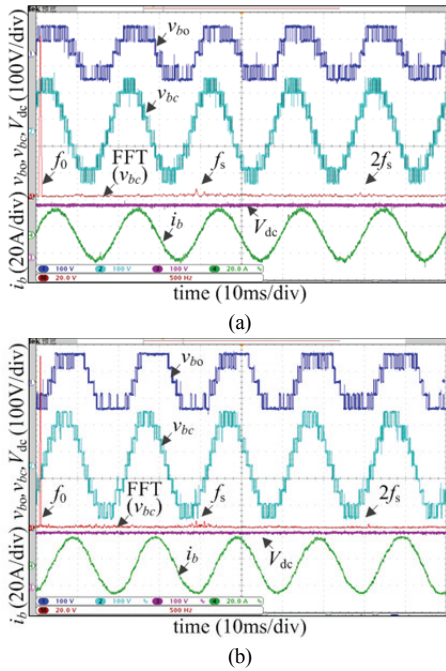


Fig. 12. Experimental results for different control strategies under steady-state conditions: (a) Conventional PI+SVM; (b) Proposed DB-HPC-SVM.

steady-state error of the output currents, which is consistent with the simulation results. Moreover, the results of the phase voltage for the proposed DB-HPC-SVM show that the output voltage level does not change during several switching periods, which reduces the switching losses. On the one hand, two phases change the output voltage level, while one phase maintains the same output voltage level in every five-segment switching sequence. On the other hand, the extra switching control in the MPC based on OSS reduces the switching transitions between two adjacent switching sequences. However, the results of the phase voltage for the PI+SVM show that the number of switching transitions for the seven-segment switching sequence used in [9] is larger than that of the proposed DB-HPC-SVM. Therefore, the proposed DB-HPC-SVM also combines the characteristic of easy inclusion of constraints, such as extra switching control.

Moreover, as shown in Fig. 12, an FFT analysis of the line voltages for both control strategies is also presented. It can be seen from Fig. 12(a) that the harmonic spectrum for the conventional PI+SVM is mainly concentrated around the switching frequency f_s . As shown in Fig. 12(b), the proposed DB-HPC-SVM also combines the advantage of a fixed switching frequency and eliminates low-order harmonics, which is one of the main contributions of the proposed DB-HPC-SVM.

B. Dynamic Performance

Fig. 13 shows comparative experimental results of the line voltage and three-phase output currents between the conventional PI+SVM and the proposed DB-HPC-SVM

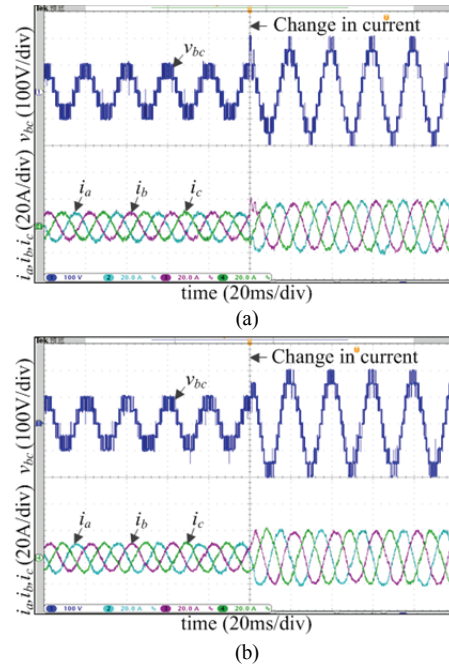


Fig. 13. Experimental results for different control strategies under dynamic condition: (a) Conventional PI+SVM; (b) Proposed DB-HPC-SVM.

under dynamic conditions. It is clearly observed from Fig. 13 that the dynamic response times of the output currents for the conventional PI+SVM and the proposed DB-HPC-SVM are 8 ms and 3 ms, respectively. These results are consistent with the simulation results. Moreover, the proposed DB-HPC-SVM presents a fast dynamic response without current overshoot, while the current overshoot of the conventional PI+SVM is about 10%. As can be observed from Fig. 13(a) and (b), the proposed DB-HPC-SVM achieves a fast dynamic response when compared to the conventional PI+SVM, while obtaining similar steady-state current ripples.

Moreover, as shown in Fig. 13, both the conventional PI+SVM and the proposed DB-HPC-SVM avoid high output voltage level jumps and unwanted switching transitions under steady-state and dynamic conditions.

Fig. 14 shows comparative experimental results of the capacitor voltages between the conventional PI+SVM and the proposed DB-HPC-SVM under dynamic condition. As shown in Fig. 14, both control strategies can balance the three-phase floating-capacitor voltages and dc-link capacitor voltages under steady-state and dynamic conditions.

As can be seen from Fig. 14, the dynamic response times of the capacitor voltages for the conventional PI+SVM and the proposed DB-HPC-SVM are 80 ms and 40 ms, respectively. Therefore, the floating-capacitor voltages and the dc-link capacitor voltages for the proposed DB-HPC-SVM have faster dynamic responses when compared to the capacitor voltages for the conventional PI+SVM. Moreover, the fluctuation amplitude of the floating-capacitor voltages for the conventional PI+SVM is larger than that for the proposed

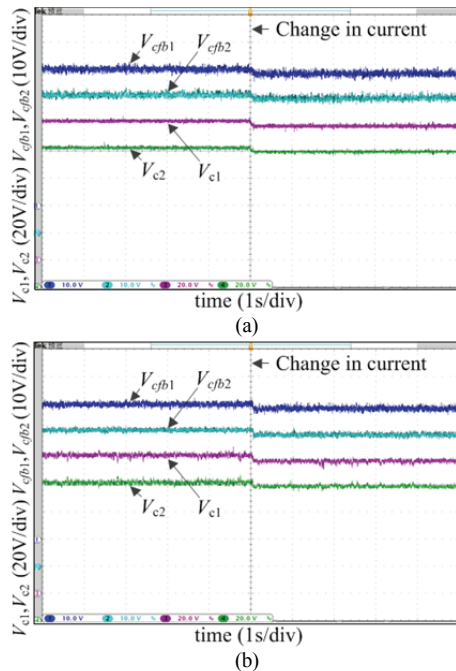


Fig. 14. Experimental results of capacitor voltages for different control strategies under dynamic conditions: (a) Conventional PI+SVM; (b) Proposed DB-HPC-SVM.

DB-HPC-SVM, while the dc-link capacitor voltages for both of the control strategies present similar steady-state ripples. When compared with the capacitor voltage balance methods in [9], the proposed DB-HPC-SVM balances the capacitor voltages by using the predictive values of the capacitor voltage and current, which compensates the control delay.

The comparative experimental results above show that the proposed DB-HPC-SVM combines the advantages of DBC, fast SVM and MPC to improve both the steady-state and dynamic performance.

VI. CONCLUSIONS

In this paper, DB-HPC-SVM is presented to achieve a fast dynamic response, balance capacitor voltages, and reduce steady-state current ripples. Unlike the exhaustive exploration in FCS-MPC, the voltage vector selection process is simplified by using DBC to obtain DB-RVV, which achieves zero steady-state current error and a fast dynamic response. The fast SVM principle is used to obtain all of the candidate switching sequences that synthesize the DB-RVV. In order to reduce the computational burden and the complexity of the weighting factor design, a hierarchical MPC is proposed to balance the capacitor voltages. The OSC for each phase is selected by the MPC with a simple logical judgment and the OSS is selected by minimizing the cost function of the MPC. The proposed DB-HPC-SVM combines the advantages of DBC, fast SVM and MPC. When compared with the conventional PI+SVM, the proposed DB-HPC-SVM has a fast dynamic response. When compared with the conventional

FCS-MPC, the proposed DB-HPC-SVM improves steady-state performances, such as a fixed switching frequency and a lower steady-state ripple. Comparative results verify the feasibility and validity of the proposed DB-HPC-SVM under different conditions.

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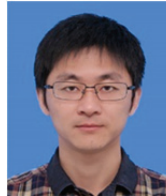
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