JPE 18-6-26

https://doi.org/10.6113/JPE.2018.18.6.1901
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

Improved Circuit Model for Simulating IGBT Switching Transients in VSCs

Naushath Mohamed Haleem†, Athula D. Rajapakse*, and Aniruddha M. Gole*

†,*Department of Electrical and Computer Engineering, University of Manitoba, Winnipeg, Canada

Abstract

This study presents a circuit model for simulating the switching transients of insulated-gate bipolar transistors (IGBTs) with inductive load switching. The modeling approach used in this study considers the behavior of IGBTs and freewheeling diodes during the transient process and ignores the complex semiconductor physics-based relationships and parameters. The proposed circuit model can accurately simulate the switching behavior due to the detailed consideration of device–circuit interactions and the nonlinear nature of model parameters, such as internal capacitances. The developed model is incorporated in an IGBT loss calculation module of an electromagnetic transient simulation program to enable the estimation of switching losses in voltage source converters embedded in large power systems.

Key words: Electromagnetic Transient Program, Insulated-gate bipolar transistor, Insulated-gate bipolar transistor modeling, Switching loss, Voltage source converter

I. INTRODUCTION

Voltage source converters (VSCs) are widely applied in power systems due to their several advantages, including the absence of commutation failures, independent control of active and reactive power, and fast dynamic response [1]. An insulated-gate bipolar transistor (IGBT) is a power electronic switch that is used in VSC applications in the range of a few kilowatts to hundreds of megawatts [2]. Switching losses constitute a remarkable portion of power losses in two-level VSCs that operate at high switching frequencies. They represent a serious concern even in multi-level modular converters (MMCs) that operate at low switching frequencies because of the large number of switches operating in a cycle. The instantaneous power dissipated during a switching transient could increase to several megawatts in large capacity IGBTs used in power systems [3], and the losses are dependent on the characteristics of the IGBT and on the gate drive and stray inductances in the circuit. The thermal management systems of converters are designed and manufactured with relatively low safety margins due to economic reasons [4]. Therefore, the switching loss component should be accurately estimated in designing the cooling systems for IGBTs in VSCs.

Power systems with embedded power electronic converters are typically simulated through electromagnetic transient (EMT) simulation programs [5]. In these programs, IGBT devices are represented as simple switches, and switching losses are impossible to determine [4]. The losses in large power electronic systems operating under realistic conditions can be assessed when a switch model could be modified in such a way that its losses can be estimated [5]. The accurate estimation of switching losses and corresponding thermal stresses of IGBT switches in converters can aid in the identification of failure risks at the design stage and can appropriately refine thermal management systems. During the operational stage, loss estimation facilities can perform simulations to help identify the regions that are safe for converter operation.

The three key requirements of an estimation model for IGBT switching losses in a circuit simulation program are as follows: (i) manageable level of model complexity, (ii) accessibility to model parameters, and (iii) accurate estimation of switching losses. The techniques used in different research papers that developed models of IGBT switching losses can be broadly classified as (i) empirical models that fit appropriate curves to actual loss measurements [6]-[9], (ii) circuit models that

Manuscript received Aug. 12, 2017; accepted Jul. 17, 2018
Recommended for publication by Associate Editor Sang-Won Yoon.
†Corresponding Author: umnausha@myumanitoba.ca
Tel: +1-2044801403, University of Manitoba
*Dept. of Electr. & Computer Eng., University of Manitoba, Canada

simulate the waveforms of switching transients [10]-[14], and (iii) semiconductor physics-based dynamic models that employ partial differential equations for modeling internal fields and charge distributions [15], [16].

In empirical modeling, the total device power losses or switching energy losses estimated from experimental measurements conducted under certain test conditions are fitted as load current functions because the supply voltage is fixed for two-level converters [12], [13]. Empirical models only require a few model parameters and minimal computational effort. However, the reliance on switching loss variations versus load current characteristics specified in data sheets [13], [15] or on measurements obtained from particular test circuits hinders the use of these models as generic design tools because under such condition, the impact of the gate drives and stray inductances of actual converters is ignored.

Semiconductor physics-based models, which use partial differential equations of time and space to model the dynamic behavior of switching devices, should be simulated at small time steps. In addition, they are generally more complex than circuit models are. A major drawback of physics-based models is the need for a large number of inaccessible and unfamiliar parameters [15], [16].

Circuit models use basic circuit elements to mimic the transient behavior of switching devices and their interactions with gate drives and external circuits. These models estimate the transient trajectories of terminal voltages and currents and use them to estimate energy losses. These models are suitable as design tools because external factors such as stray inductances and gate drive characteristics can be incorporated. Circuit models that rely on Simulation Program with Integrated Circuit Emphasis (SPICE)-like library components of bipolar junction transistors (BJT) and metal-oxide-semiconductor field-effect-transistors (MOSFET) [10] cannot be directly implemented in EMT programs. Any circuit model that calculates switching transient waveforms should be solved in small time steps (several nanoseconds). Therefore, the circuit models of IGBTs cannot be incorporated in large power system simulations conducted in EMT simulation programs without severely increasing the computational time. Nevertheless, a combination of lookup tables and circuit models can be used with pre- and post-switching IGBT voltages and currents obtained through EMT simulations running with an ideal switch model [5].

This study presents a circuit model that simulates the switching behavior of IGBTs during different phases. An approximated circuit model that mimics the important process of each phase is utilized. The proposed model considers the gate drive performance and stray inductances of PCBs. An accurate prediction of collector-to-emitter voltage changes is conducted by mimicking the nonlinear nature of switching capacitances. Furthermore, a systematic model parameter extraction process is implemented. The electro-thermal behavior of an IGBT in a VSC can be simulated by using a thermal model of the IGBT and by considering the temperature dependency of model parameters, as proposed in [5].

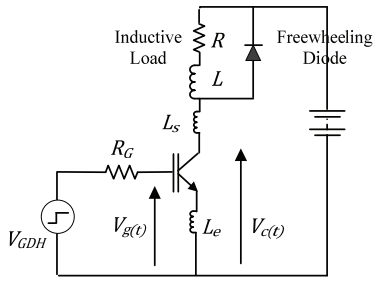

Fig. 1. Unit cell of a VSC.

II. Outline of the Modeling Approach

A. Transient Behavior of Turn-on Switching Event

Although six pairs of switches (IGBT and antiparallel diode) are required in a three-phase VSC, the switches connected to each phase operate independently. One of the antiparallel diodes provides a conductive path for continuous inductive load currents when an IGBT is off. During a turn-on transition, the load current is transferred from a freewheeling diode to the IGBT in the opposite arm of the same phase. An opposite condition occurs during the turn-off transition. Given the independent nature of each arm, the circuit shown in Fig. 1 can be used to characterize the switching behavior of a VSC. The circuit in Fig. 1 is referred to as the unit switching cell (unit cell). Stray inductance L_s is the total series inductance of a high current path, excluding the stray inductance L_e in the gate-to-emitter loop.

The load current remains nearly constant during a switching event. Therefore, the inductive load can be conveniently replaced with a constant and independent current source to simplify the circuit.

B. Circuit Model of Switching Device

The regular behavior of an IGBT is generally characterized by a BJT driven by a MOSFET [11]. However, in the circuit modeling of switching behavior, an IGBT is represented by using a controlled source, inter-electrode switching capacitances, and terminal inductances, as shown in Fig. 2.

Inter-electrode capacitances C_{ge}, C_{gc}, and C_{ce} are referred to as the gate-to-emitter capacitance, Miller capacitance, and collector-to-emitter capacitance, respectively.

Inductances L_c and L_e are the stray inductances of the metallic connections to the collector and emitter terminals, respectively. The resistance of the metallic connections to the gate terminals is represented by R_{G_int}. The circuit model of an IGBT is a lumped parameter model that imitates the variations of terminal voltages and currents during a switching event. A set of ordinary differential equations can

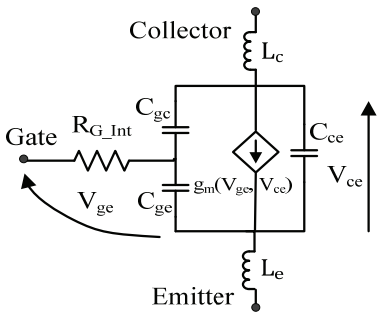

Fig. 2. IGBT circuit model.

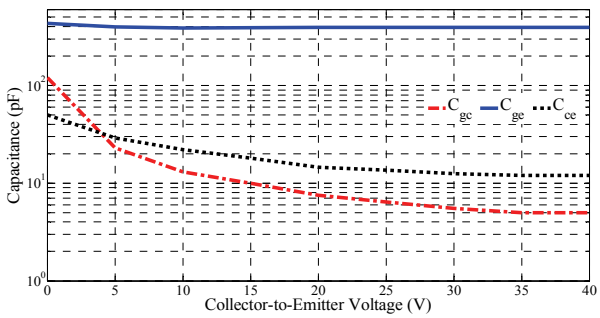

Fig. 3. Variation of switching capacitances with collector voltage [17].

be derived to describe the circuit that involves the IGBT model, its gate drive, and the converter power circuit. Consequently, the computational effort required to solve a circuit model is lower than that required to solve a semiconductor physics-based model. Inter-electrode capacitances are nonlinear because the amount of their stored charge per unit voltage varies with the collector voltage. Fig. 3 depicts the typical variations of the inter-electrode capacitances of an IGBT with the collector voltage.

The capacitances remain constant at their lowest values at high collector voltages. However, the capacitance values are large at low collector voltages. The typical capacitances versus collector voltage curves provided in device data sheets are measured at a zero gate-to-emitter voltage.

The coupling between the gate-to-emitter voltage and collector current is described by [13] as

$$I_C = g_{m0} (V_{ge} - V_T)^2 \quad (1)$$

where V_{ge} is the gate-to-emitter voltage, V_T is the threshold gate-to-emitter voltage of the IGBT, and g_{mo} is the transconductance, which is constant. Equation (1) is valid at a high collector voltage [13].

The behavior of an IGBT is determined on the basis of its internal dynamics and its interactions with the rest of the components in the circuit. Therefore, the stray inductances of circuits, freewheeling diode behavior, and gate drive characteristics are important to accurately model switching transients. The switching process of an IGBT within a unit cell shown in Fig. 1 follows several distinct phases [15]. The

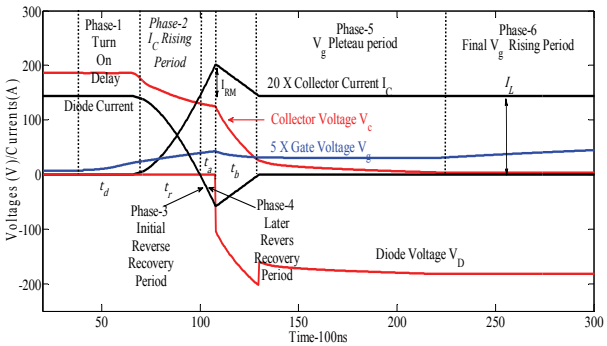

Fig. 4. Turn-on transient of an IGBT in a unit cell.

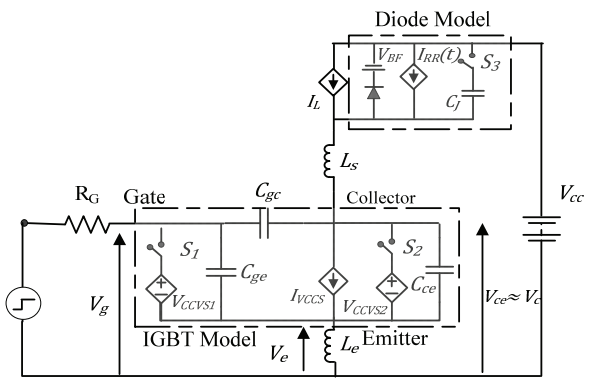

Fig. 5. Circuit model of the unit cell.

influence of a particular circuit component in several phases can be insignificant and can lead to simplifications that can be valuable in analyzing the circuit and determining model parameters. The variable nature of inter-electrode capacitances is essential to accurately calculate the trajectories of currents and voltages during switching transients. The response of an IGBT is slower than that of a diode. Hence, an IGBT greatly influences loss calculations. Instead of applying complex semiconductor physics-based diode models, an approximate model can be used to model diodes. A description of the modeling approach for turn-on and turn-off switching transients is presented in the next two sections.

III. Modeling of the Turn-on Switching Transient

A. Transient Behavior of Turn-on Switching Event

As previously described, the load current is transferred from the freewheeling diode to the IGBT during a turn-on switching event. The typical voltage and current waveforms observed during a turn-on transient are shown in Fig. 4.

The turn-on transient passes through six distinct phases [4], as indicated in Fig. 4. On the basis of the above discussion, the circuit model in Fig. 5 is proposed for the unit cell in this study. This model approximates the behavior of the IGBT at each phase with consideration of the dominant processes that occur within the IGBT and between the IGBT and other unit

cell elements.

The model in Fig. 5 accounts for the different behavior of the model in Fig. 2 during the above phases.

The model in Fig. 5 uses time-invariant values for the passive components themselves. Any time variance is accounted for by the additional controlled voltage source V_{CCVS2}, which accounts for C_{gc}'s dependence on V_{cg} during phases 4 and 5. Current controlled voltage source V_{CCVS1} is used to imitate the behavior of V_{ge} during phases 4 and 5. The voltage source that represents gate drive V_{GD} can have two values. The positive voltage applied to turn on the IGBT is represented as V_{GDP}, and the negative (or zero) voltage applied to turn off the IGBT is represented as V_{GDN}.

Current source $I_{RR}(t)$ shown in Fig. 5 mimics the reverse recovery behavior of the freewheeling diode. Capacitor C_J represents the dynamic behavior of the diode. Inductance L_s shown in Fig. 5 is the sum of the IGBT collector stray inductance L_c and the total series path inductance of the converter up to the reservoir capacitor, except for L_e. The induced EMF across stray inductance L_e causes gate voltage V_g to differ from gate-to-emitter voltage V_{ge} with the rapid variation of collector current I_c. However, the externally measurable quantity V_g is equal to V_{ge} when I_c does not vary rapidly. Furthermore, collector-to-emitter voltage V_{ce} is approximately equal to externally measurable collector voltage V_c because the induced EMF across L_e is remarkably smaller than that of V_{ce}. In this study, the measured voltages are constantly expressed in terms of the circuit ground, except for the diode voltage.

B. Modeling the Switching Phases

The modeling of the six switching phases is achieved by suitably controlling the switches and current sources in the equivalent circuit in Fig. 5. The switch states and current source equations for modeling all the six phases are given in Table I.

1) Pre-Switching Condition

Prior to the start of the turn-on switching event, the collector of the IGBT model is located at supply voltage V_{cc}, and the gate terminal is located at the saturation voltage of the gate driver output. The load current is transported by the diode that is in the conduction state, and source currents I_{VCCS} and I_{RR} are zero.

2) Phase 1: Turn-on Delay Period

This turn-on transient starts with the change of gate driver output voltage V_{GD} due to the application of a gate pulse. The finite rise time of the gate drive is modeled by using a linear ramp to approximate the initial rise of V_{GD}. V_{GD} remains at its high value (V_{GDP}) after the linear increase. Positive gate drive voltage V_{GDP} charges input capacitance C_{ies} ($C_{ge}+C_{gc}$) through gate resistance R_G that causes gate voltage V_g to gradually rise, as shown in Fig. 4 [15]. No substantial change is observed in the main IGBT voltage and current (V_{ce} or I_c) because gate-to-emitter voltage V_{ge} is still below threshold voltage V_T. The load current largely remains in the diode, and the controlled source currents I_{VCCS} and I_{RR} are zero. Hence, switch S_1 in the circuit shown in Fig. 5 is kept open in this phase. Fixed capacitances are used for C_{ge} and C_{gc} because no variation of inter-terminal capacitances is observed when V_{ce} is fixed. Phase 1 of the turn-on transient terminates when V_{ge} reaches threshold voltage V_T. The final values of the voltages and currents at the end of a given phase are assigned as the initial values of the next phase.

TABLE I
CONDITIONS AT EACH PHASE IN TURN-ON TRANSIENT

Phase	S_1	S_2	S_3	I_{VCCS}	I_{RR}
1	open	open	closed	0A	0A
2	open	open	closed	Eqn. (1)	0A
3	open	open	closed	Eqn. (1)	$I_c(t)$-I_L
4	closed	closed	closed	I_L+I_D (t)	I_D (t)
5	closed	closed	closed	I_L	0A
6	open	closed	closed	I_L	0A

3) Phase 2: Period of Rising Collector Current

Phase 2 begins with the conduction of IGBT, and collector current I_c rises with the increase of gate voltage V_{ge} according to (1). This transfer characteristic is modeled via voltage controlled current source I_{VCCS} shown in Fig. 5. Rising I_c induces voltages across stray inductances L_s, thereby causing V_{ce} to drop below V_{cc}. This variation of V_{ce} requires the depletion of some stored charges within C_{ce}. In addition, Miller capacitor C_{gc} returns the variation of V_c to the gate side. Furthermore, the induced EMF across emitter stray inductance L_e reduces the net voltage applied to the capacitive charging circuit at the gate side. Therefore, L_e provides a negative feedback that delays the turn-on switching transient. Capacitors C_{ge}, C_{gc}, and C_{ce} are considered constant in Phase 2 because V_{ce} still remains high and the variations of these capacitor values are insignificant (Fig. 3).

4) Phase 3: Initial Reverse Recovery Period

Phase 3 starts when I_c rises to load current I_L. At this point, the freewheeling diode begins to turn off, and device current I_c overshoots beyond I_L due to the reverse recovery current of the diode. The reverse recovery current of a power diode is the current caused by the depletion of stored charges in the lightly doped base region [18]. The increase of I_c is still governed by rising V_g (V_{ge}) on the basis of the relationship in (1). Given the negligible voltage across the diode (forward bias) [19], the rate of change of IGBT collector current I_c is still governed by V_{ge} and remains relatively unchanged from the previous phase 2 [5]. Current I_c minus I_L is the reverse recovery current of the diode and is injected to the circuit via

current source I_{RR} in Fig. 5. This initial phase of reverse recovery continues until I_{RR} reaches its maximum value I_{RM}. Maximum reverse recovery current I_{RM} is approximately determined by (2) [14].

$$I_{RM} = \sqrt{2\tau I_L \frac{dI_c}{dt}} \tag{2}$$

where τ is the carrier lifetime of the diode. The slope of I_c is determined during Phase 2 to enhance the estimation accuracy of I_{RM}.

5) Phase 4: Collector Voltage Falling Period

In the start of Phase 4, the diode starts to gain a reverse voltage, and its reverse recovery current begins to decrease. Switch S_3 is closed, and diode current I_D is entirely modeled by current source I_{RR} as a linearly decreasing function of time. The IGBT remains in the active region, and I_c (=I_{RR}+I_L) and V_{ge} are related through (1). Thus, a small drop in V_g is observed with the decrease of I_c, as shown in Fig. 4. The value of V_{ge} in Phase 4 is determined by using (3), which is derived from (1). In the circuit, V_{ge} is assigned with the value in (3) via current controlled voltage source V_{CCVS1}.

$$V_{ge} = V_T + \sqrt{I_L / g_{m0}} \tag{3}$$

The variation of the magnitude of V_{ge} is considerably smaller than that of V_{cg}; hence, the decrease in V_{ce} is approximately equal to the decrease in the voltage across Miller capacitor C_{gc}. Therefore, V_{ce} is mainly determined by the amount of stored charge within C_{gc}. Current I_{Miller}, which discharges C_{gc}, can be calculated by (4) [14].

$$I_{Miller}(t) = \frac{V_{GDP} - V_{ge}(t)}{R_G} - C_{ge}\frac{dV_{ge}}{dt} \tag{4}$$

The nonlinearity of C_{gc} cannot be ignored during this phase due to the remarkable drop of V_{ce} (Fig. 3). As capacitor C_{gc} is used as a function of V_{cg}, the capacitor discharging equation can be expressed as (5)

$$I_{Miller}(t) = C_{gc}(V_{cg})\frac{dV_{cg}}{dt} - V_{cg}\frac{dC_{gc}(V_{cg})}{dV_{cg}}\frac{dV_{cg}}{dt} \tag{5}$$

Equation (5) can be written in the form of (6).

$$I_{Miller}(t) = \left[C_{gc}(V_{cg}) - V_{cg} f(V_{cg})\right]\frac{dV_{cg}}{dt} \tag{6}$$

Therefore, the variation of V_{cg} can be simplified to (7), with the quantities in the square brackets replaced by C_{gc}', which can be pre-calculated and stored as a function of V_{cg} in a lookup table.

$$\frac{dV_{cg}}{dt} = I_{Miller}(t) / C_{gc}'(V_{cg}) \tag{7}$$

where

$$C_{gc}'(V_{cg}) = C_{gc}(V_{cg}) - V_{cg}\frac{dC_{gc}(V_{cg})}{dV_{cg}} \tag{8}$$

During the simulation of Phase 4, (7) is numerically integrated by using backward Euler algorithm to determine V_{cg}. During Phases 4 and 5 of the turn-on switching event (Fig. 4), the change of V_{ce} is large relative to the change in V_{ge}. Therefore, the variation of V_{cg} is approximated by the variation of V_{ce} to simplify the model. Nonlinear parameter C_{gc}' is expressed as a function of V_{ce} (because the variation of V_{cg} closely follows that of V_{ce}) and is obtained from a lookup table during numerical integration. An unequally spaced lookup table is used because the rate of change of C_{gc}' is small at large V_{ce} values. Therefore, few samples are sufficient at large V_{ce} values. The estimation of C_{gc}' is explained in Section V. In the circuit, the computed value of V_{cg} should be injected via a controlled voltage source connected between the gate and the collector. However, the same effect can be achieved by injecting (V_{cg} + V_{ge}) through a controlled source connected between the collector and emitter. This approach results in a stable circuit and is represented by using V_{CCVS2}, which is inserted to the IGBT circuit model shown in Fig. 5 by closing S_2. Phase 4 ends when I_c reaches I_L and diode current I_D becomes zero at the end of this phase.

6) Phase 5: Gate Voltage Plateau Period

I_c remains constant at I_L in Phase 5. The value of V_{ge} (V_g) remains constant, as determined by (3), because the IGBT remains in the active region. Collector-to-emitter voltage V_{ce} slowly decreases, and the decreasing rate of V_{ce} gradually drops. Therefore, V_{ge} is calculated using (3) and is enforced in the circuit with the aid of V_{CCVS1}. On the basis of (4), I_{Miller} is fixed during this phase because V_{ge} is constant. Therefore, the variation of V_{ce} is determined in the same way as that in Phase 4 from (7), but a constant I_{Miller} is used and enforced using V_{CCVS2}. Phase 5 ends when V_{ce} drops to the saturation voltage. All switches remain at the same position, similar to the case in Phase 4.

7) Phase 6: Final Gate Voltage Rising Period

In Phase 6, the IGBT enters a region where relationship (1) no longer holds. Gate voltage V_g starts to increase from the gate voltage plateau and moves toward V_{GDP} at a rate determined by the charging of C_{ge}+C_{gc} through R_G [15]. Therefore, S_1 is opened. V_{ce} is maintained at saturation voltage $V_{ce(sat)}$ by using V_{CCVS2}.

IV. Modeling of Turn-off Switching Transient

A. Transient Behavior Of Turn-off Switching Event

During the turn-off event, the load current is transferred from the IGBT to the freewheeling diode. The transient can be divided into four phases [4] (Fig. 6). Similar to the case in the turn-on transient, the four phases in the turn-off transient are simulated by using the equivalent circuit in Fig. 5 with different switch states and current sources (Table II).

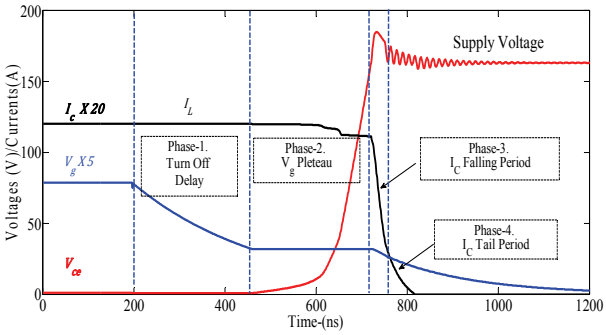

Fig. 6. Turn-off transient of the IGBT in the unit cell.

TABLE II
CONDITIONS AT EACH PHASE IN TURN-OFF TRANSIENT

Phase	S_1	S_2	S_3	I_{VCCS}	I_{RR}
1	open	open	closed	I_L	0A
2	closed	closed	closed	I_L	0A
3	open	open	closed	*Eqn. (1)*	0A
4	open	open	closed	*Eqn. (9)*	0A

B. Modeling the Switching Phases

1) Pre-Switching Condition

The gate terminal of the IGBT is located at positive gate drive voltage V_{GDP}, and the collector terminal is located at saturation voltage $V_{ce(sat)}$. I_c remains equal to I_L, and the voltage across C_J is equal to V_{cc}.

2) Phase 1: Turn-off Delay Period

Phase 1 begins when the gate drive voltage starts to change from V_{GDP} to V_{GDN}. This change may be modeled as a ramp-down when gate driver dynamics is to be considered. Negative gate voltage source V_{GDN} causes C_{ge} and C_{gc} to discharge and causes V_g to gradually drop (Fig. 6). In this phase, switches S_1 and S_2 are kept open. The finite output resistance of the gate drive can be added to R_G. This phase is completed when V_{ge} plateaus at the value given by (3).

3) Phase 2: Gate Voltage Plateau Period during Turn-off

In Phase 2, V_{ce} starts to increase, and V_g remains constant at its plateau value at the end of Phase 1. I_c remains constant. However, I_c slightly decreases during the latter part of the phase when the variation of V_{ce} is rapid (Fig. 6). The variation of V_{ce} is governed by the charging of Miller capacitance. Therefore, the variation of V_{ce} is calculated in a way similar to that done in Phase 5 of the turn-on switching transient and is enforced in the circuit using VCCS2. The instantaneous voltage across the diode is $V_{cc}-V_{ce}$, where V_{cc} is the supply voltage. The drop in I_c at the end of the phase is due to the release of stored charges in diode junction capacitance C_J[5]. For simplicity and ease of parameter extraction, C_J is modeled as a fixed capacitor. The next phase starts when V_{ce} reaches V_{cc}.

4) Phase 3: Collector Current Falling Period

The load current transfer from the IGBT to the diode starts in this phase, and a rapid fall in IGBT current I_c is observed. A simultaneous decrease in V_{ge} occurs with the decrease in I_c. An overshoot in V_{ce} is observed with the decrease in I_c due to the voltages induced across stray inductances L_s and L_e. The decrease in I_c is modeled by using (1) and is injected via controlled current source I_{VCCS}. The induced EMF across L_e resists the change in I_c, similar to the case in phases 2 and 3 of the turn-on switching transient. Fixed capacitance values are used in the simulation of this phase because V_{ce} is sufficiently high. The voltage and current variations in the diode are the responses to V_{ce} and I_c variations determined by the IGBT.

5) Phase 4: Collector Current Tail Period

In this phase, the rate of decrease in I_c declines, and I_c follows a near-exponential decay [20]. Collector-to-emitter voltage V_{ce} undergoes several oscillations, and V_g decreases toward V_{GDN}. The gradually decaying I_c is modeled by using (9) and is injected via controlled current source I_{VCCS} [21].

$$I_{C\ Tail}\ (t) = I_{Tail}\ e^{-t/\tau_{Tail}} \tag{9}$$

Time constant τ_{Tail} and amplitude I_{Tail} for a given IGBT can be determined by using test waveforms. The gate voltage change is determined by the discharging of C_{ies} through R_G. This phase ends when the gate voltage reaches V_{GDN}.

V. MODEL PARAMETERS

The parameters of the model in Fig. 5 are available in the manufacturer's datasheets and test waveforms. The capacitors are challenging because their values are voltage dependent [8]. [11] used four different values of C_{ge} for the different phases of the turn-on and turn-off transients. The model proposed in the current work follows the recommendation in [11] to simplify the modeling. These values are obtained by sampling the full characteristics (derived below) at suitable intervals.

Typically, datasheets present the variations of switching capacitances with V_{ce} measured at zero V_{ge}. However, switching capacitances remarkably change when a gate voltage is applied [22]. Therefore, an accurate estimation of capacitances can be achieved by extracting them from the measured switching transient waveforms. A systematic procedure to obtain all the required parameters from two test waveforms (turn-on and turn-off) is described below. Consider the turn-on switching transient shown in Fig. 7 with various quantities used in the equations. C_{ge} is estimated by considering two points on the measured V_g trajectory during Phase 1 with the decay of the initial oscillation of V_g. The ramp up of the gate drive voltage is expressed as

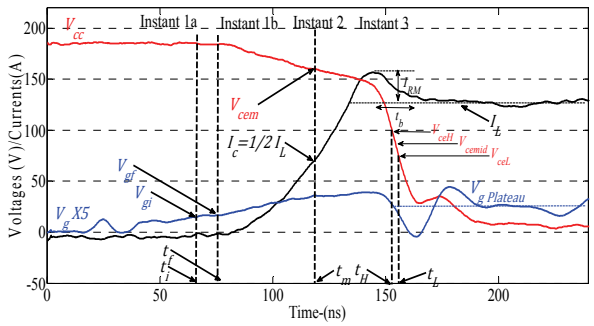

Fig. 7. IGBT turn-on transient measurement at V_{cc} = *185 V*, I_L = *6.5 A*, and R_G = *150* Ω.

$$C_{ge} = \left(\frac{t_f - t_i}{R_G}\right) \times \frac{1}{ln\left|\frac{V_{GDP} - V_{gi}}{V_{GDP} - V_{gf}}\right|} \tag{10}$$

where V_{gi} and V_{gf} are the gate voltages measured at time instants t_i and t_f (Fig. 7).

Although (10) ignores the effect of C_{gc}, accuracy does not suffer considerably because C_{ge} is greater than C_{gc} during Phase 1 and V_{ce} is fixed. Stray inductance L_s is estimated by applying (11) to an instant in which the trajectory of I_c is stable, such as ½ I_L.

$$L_s = \frac{V_{L_s}}{dI_c/dt} = \frac{(V_{cc} - V_{cem})}{dIc/dt\big|_{t=t_m}} \tag{11}$$

Alternatively, stray inductances L_s and L_e can be estimated by simulating the printed circuit board with the aid of finite element modeling-based simulation tools. Gain constant g_{mo} required for (1) and (3) is estimated by applying (12) to average V_g during the gate voltage plateau phase.

$$g_{m0} = \frac{I_L}{\left(V_{g\_Plateau} - V_T\right)^2} \tag{12}$$

Once g_{mo} is known, the emitter stray inductance L_e can be determined by considering the gate circuit during I_c rising period in Phase 2. Given the instant when I_c = ½ I_L (i.e., at t = t_m in Fig. 7), L_e is obtained as

$$L_e = \frac{\left(V_g\right)_{t=t_m} - \left(V_T + \sqrt{\frac{I_L}{2g_{m0}}}\right)}{dI_c/dt\big|_{t=t_m}} \tag{13}$$

Forward carrier lifetime τ of the diode is estimated by using (2) with dI_c/dt at t = t_m and then applying (14).

$$\tau = \frac{I^2_{RM}}{2I_L \, dI_c/dt\big|_{t=t_m}} \tag{14}$$

Later reverse recovery period t_b at different I_L and dI_c/dt values is given in the manufacturer's datasheets. A lookup table can be created to determine t_b at a given I_L and dI_c/dt. The datasheet value of C_{ce} is adequate because the impact of C_{ce} on the transient is small. The measurements in Phase 1 and the known parameters are related to Miller capacitance C_{gc} as

$$C_{gc}\frac{dV_{cg}}{dt} = \left(\frac{V_{GDP} - V_{ge}}{R_G}\right) - C_{ge}\frac{dV_{ge}}{dt} \tag{15}$$

However, (15) cannot be applied to determine C_{gc} because the sloped estimation of V_g in this period is challenging due to noises. Alternatively, the value of C_{gc} during high V_{ce} can be determined by using a trial and error approach, in which the model response at a trial C_{gc} value is compared with the measured V_g trajectory. The value of C_{gc} substantially increases during Phase 4 with the decrease of V_{ce}. A set of values for C_{gc}' in (7) is required to synthesize the variations of V_{ce} during Phases 4 and 5. C_{gc}' at a given V_{ce} is estimated from (16) by approximating the derivative of V_{ce} in (7) from nearby points (t_H V_{ce_H}), (t_L, V_{ce_L}) with V_{ce_mid} = ½(V_{ce_H} + V_{ce_L}), as marked in Fig. 7.

$$C_{gc}'\big|_{Vce\_mid} \cong -I_{Miller}\big|_{Vce\_mid}\frac{(t_H - t_L)}{(V_{ce\_H} - V_{ce\_L})} \tag{16}$$

Estimating the time rate of V_{ge} from measurements is difficult. The estimation of the current value of variable capacitance C_{ge} increases the effort required for parameter extraction. Therefore, the complexity of parameter extraction can be reduced when $[I_{\text{Miller}}]_{\text{Vce\_mid}}$ is assigned to the current injection from the gate drive and by compensating for the error through the fitting variation of V_{ce} to the current value of I_{Miller}. The set of values obtained for C_{gc}' from a test waveform can be used at any other operating points, as described in the Results and Discussion section. Consider that the conditions at the gate side slightly differ during the turn-off transient and that the variations of C_{ge} and C_{ce} are ignored. In such a case, another set of values for C_{gc}' should be determined to accurately simulate the turn-off switching transient. Doing so requires the same application of (16) to Phase 2 of the turn-off measurements. Two other capacitance values are estimated for C_{ge} (at high and low V_{ce}) to simulate the turn-off transient, as presented in [11]. The first capacitance value is utilized in Phase 1, and the second capacitance value is used in the remaining periods. The two capacitance values can be estimated by applying a capacitive charging equation (10) with initial voltages.

VI. Results and Discussion

Various test measurements were conducted by using the test circuit in Fig. 1 with IGBTs from different manufacturers.

The test circuit consisted of an inductive load with 0.5 ms time constant.

Although the IGBT/diode temperatures were uncontrolled, visible temperature changes were avoided by leaving the test devices turned off for a long period after a few consecutive short on–off pulses. One set of measurements from each IGBT/diode combination was used to extract the model parameters. The remaining measurements were used for model verification. Only the results of the IGBT model IRG6I320UPBF and freewheeling diode ISL9R1560P2 are presented due to space limitations. The estimated parameters of the IGBT, diode, and circuit layout parameters are shown in Appendix 1.

The estimated and measured turn-on transient waveforms at two different voltage–current combinations (different from the waveforms used for parameter extraction) are compared in Figs. 8 and 9. The model was simulated through PSCAD/EMTDC with a time step of 0.05 ns. The plots showed a good match between the measured and simulated turn-on transient trajectories of V_c and I_c, except for the high-frequency oscillations in the gate voltage during the gate voltage plateau. These oscillations begin when the sign of dI_c/dt suddenly changes at the peak of reverse recovery current and involve the voltage induced on L_e. Several differences were observed between the estimated gate voltage and the observed gate voltage at the conducting phases of turn-on transient, and they were due to the underestimation of L_e. The estimated diode reverse recovery voltage was inaccurate because a simplified diode model was used. Nevertheless, these oscillations on V_g exerted a minimal effect on the switching loss estimation, and the model predicted the average switching behavior with a reasonable accuracy level.

The estimated and measured turn-off transient waveforms at two dissimilar operating points are compared in Figs. 10 and 11. They showed good agreement with each other. A good agreement between the measured and the simulated waveforms can be obtained when the nonlinearity of the Miller capacitor is considered.

The effects of nonlinear C_{gc} during Phases 4 and 5 of the turn-on transient and Phase 2 of the turn-off transient are represented in the model by using source V_{CCVS2}, with its voltage computed from (7). However, capacitance C_{gc} during these phases was observed in the circuit. This condition helped preserve the initial condition across C_{gc} for the next phase and did not cause a remarkable error. The overshoot of V_c at turn-off transient was inaccurate because the nonlinear diffusion capacitance of the forward biased diode was ignored.

The accuracy of the models was evaluated by comparing the estimated and measured switching losses at different operating points shown in Tables III and IV.

The maximum error was less than 10%, and the error was less than 5% in most cases.

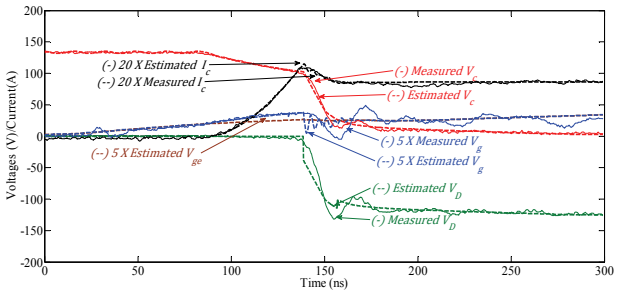

Fig. 8. Turn-on switching trajectories at $V_{cc} = 135\ V, I_L = 4.25\ A,$ and $R_G = 150\ \Omega$.

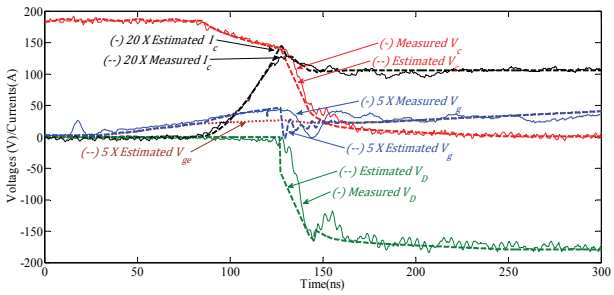

Fig. 9. Turn-on switching trajectories at $V_{cc} = 185\ V,\ I_L = 5.25\ A,$ and $R_G = 70\ \Omega$.

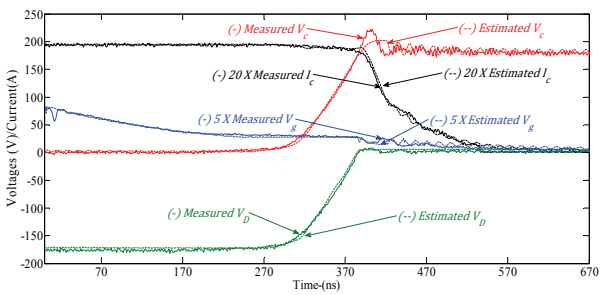

Fig. 10. Turn-off switching trajectories at V_{cc}=180V, I_L=9.75A, and R_G=70Ω.

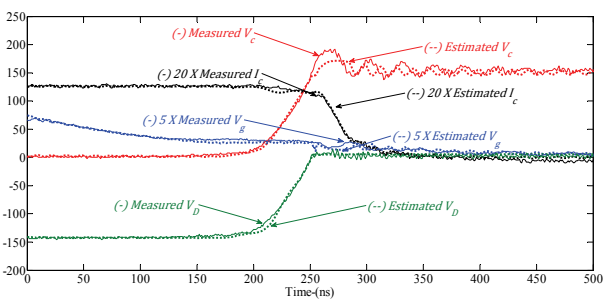

Fig. 11. Turn-off switching trajectories at $V_{cc} = 145\ V,\ I_L = 6.3\ A,$ and $R_G = 35\ \Omega$.

A. Implementation in EMT Simulation Programs

The proposed circuit model completely considers the impact of gate drive and circuit layout; this capability is a major advancement relative to the models proposed in [4], [5], [24]. Simulating the proposed circuit model is not practical as it requires considerably small simulation time steps every

TABLE III
TURN-ON SWITCHING LOSSES

V_{CC} (V)	I_L (A)	R_G (Ω)	Turn-on Energy Loss		Error (%)
			Esti. (μJ)	Meas. (μJ)	
180	6.50	150	49.9	48.6	2.7
185	4.15	150	31.2	28.6	9.1
135	4.25	150	22.5	23.4	-3.8
185	5.50	70	38.0	40.8	-6.9
153	3.20	70	27.4	26.6	3.0

TABLE IV
TURN-OFF SWITCHING LOSSES

V_{CC} (V)	I_L (A)	R_G (Ω)	Turn-on Energy Loss		Error (%)
			Esti. (μJ)	Meas. (μJ)	
175	9.75	70	174.1	168.8	3.1
180	3.25	70	48.6	48.3	0.6
140	6.00	70	74.4	80.5	7.6
180	8.75	35	109.5	104.2	5.1
145	6.30	35	53.4	54	1.1

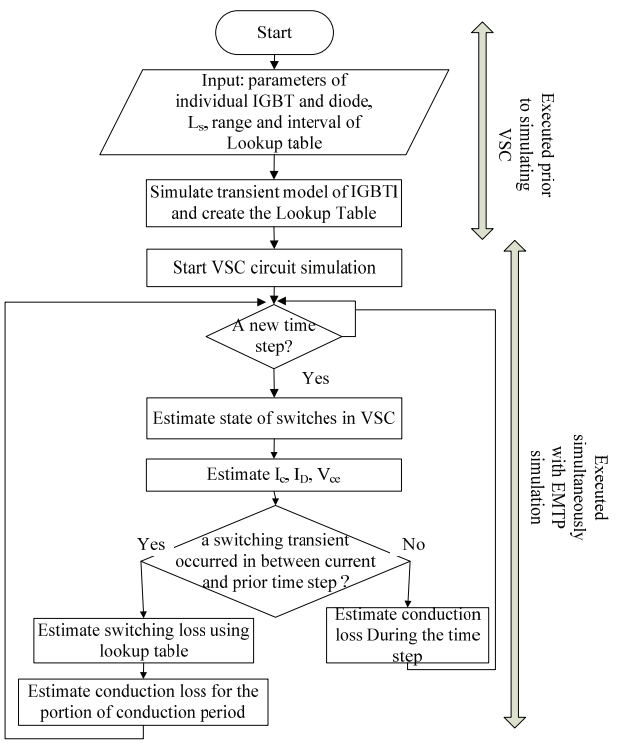

Fig. 12. Application of the model in evaluating IGBT switching losses at VSCs embedded in large power systems.

time a switching event occurs in the power circuit. As depicted in Fig. 12, a lookup table of switching losses is presented for each IGBT (and diode) as a function of I_c, and V_{ce}, (and temperature when a thermal model is integrated). In the main power circuit simulation, IGBTs and diodes are represented by using simplified (or ideal) switch models that enable the calculation of the pre- and post-switching values of I_c and V_{ce}. These values were used to retrieve the appropriate loss values from the corresponding lookup table. With this approach, any number of switches can be represented in the power circuit simulation. At the same time, IGBT parasitic and stray inductances are applicable to each IGBT, and the estimated losses are realistic because the lookup tables for the losses were computed in terms of the drive circuit.

VII. CONCLUSIONS

Simulation results and experimental measurements demonstrate that the proposed circuit model of IGBTs is capable of accurately predicting terminal currents and voltage waveforms during switching events. The proposed model improves the results of previously published research by considering the interactions between IGBT devices and circuits in a precise and transparent manner, as well as the variable nature of the parameters at different phases of transients. The circuit model of the IGBT/diode combination can be easily incorporated in circuit or power system simulation programs because the model does not rely on complex semiconductor physics-based characterization. A practical procedure for parameter extraction from transient measurements is presented. As the parameters are estimated by using a test circuit, the model can be applied to calculate the losses of a target converter circuit with the estimated stray inductances and actual gate drive characteristics.

The limitation of the proposed model includes the need to take transient measurements with a gate drive of known characteristics for parameter extraction. This limitation mainly stems from changes in a device's internal capacitances, especially C_{gc}, with V_{ge} (in addition to V_{ce}). Moreover, datasheet measurements are generally made at V_{ge} = 0. Another limitation of the model is the small time step it requires in simulating circuits. The electro-thermal behavior of VSCs can be simulated by adding two additional features to the proposed model. Model parameters g_{mo} and V_T are dependent on the junction temperature of the device. The dependency can be related by simple equations, as presented in [23]. Therefore, the proposed model can be used as a tool for designing thermal management systems by using the estimated losses to calculate the temperature change with the aid of an IGBT thermal model [5].

APPENDIX

TABLE V
C_{GC}'FOR TURN-ON TRANSIENT

V_{ce} (V)	0	10	15	20	35	45	300
C_{gc}' (pF)	800	600	225	70	58	22	15

TABLE VI
C_{GC}' FOR TURN-OFF TRANSIENT

V_{ce} (V)	0	8	15	20	35	45	300
C_{gc}' (pF)	1200	600	200	120	90	75	50

TABLE VII
CONSTANT PARAMETERS FOR IGBT AND CONVERTER

Parameter	Estimated Value	Units	Description
g_{m0}	4	A/V^2	-
V_T	4	V	-
C_{gc}	12	pF	-
C_{ce}	20	pF	-
C_{ge_ON}	1.6	nF	-
C_{ge_OFFPh1}	2.75	nF	Turn-off Phase-1
$C_{ge\_OFFPh2\text{-}4}$	1.65	nF	Turn-off Phase-2 to 4
L_s	160	nH	-
L_e	12	nH	-

REFERENCES

[1] N. Flourentzou, V. G. Agelidis, and G. D. Demetriades, "VSC-based HVDC power transmission systems: an overview," *IEEE Trans. Power Electron.*, Vol. 24, No. 3, pp. 592-602, Mar. 2009.

[2] F. Schettler, H. Huang, and N. Christl, "HVDC transmission systems using volt-age sourced converters design and applications," *Proceedings of the IEEE Power Engineering Society Summer Meeting, Seattle, Washington*, Vol. 2, pp. 715-720, Jul. 2000.

[3] H. Pang, G. Tang, and Z. He, "Evaluation of losses in VSC-HVDC transmission system," *Proceedings of the IEEE Power and Energy Society General Meeting, Pittsburgh, Pennsylvania*, pp. 1-6, Jul. 2008.

[4] A. D. Rajapakse, A. M. Gole, and P. L. Wilson, "Electromagnetic transients simulation models for accurate representation of switching losses and thermal performance in power electronic systems," *IEEE Trans. Power Del.*, Vol. 20, No. 1, pp. 319-327, Jan. 2005.

[5] A. D. Rajapakse, A. M. Gole, and R. P. Jayasinghe, "An improved representation of facts controller semiconductor losses in EMTP-type programs using accurate loss-power injection into network solution," *IEEE Trans. Power Del.*, Vol. 24, No. 1, pp. 381-389, Jan. 2009.

[6] C. Wong, "EMTP modeling of IGBT dynamic performance for power dissipation estimation," *IEEE Trans. Ind. Appl.*, Vol. 33, No. 1, pp. 64-71, Feb. 1997.

[7] S. Munk-Nielsen, L. N. Tutelea, and U. Jaeger, "Simulation with ideal switch models combined with measured loss data provides a good estimate of power loss," *2000 IEEE Industry Applications Conference*, Vol. 5, pp. 2915-2922, 2000.

[8] M. H. Naushath and A. D. Rajapakse, "A novel method for estimation of IGBT switching losses in voltage source convertors through EMT simulations," *IEEE 2nd Annual Southern Power Electronics Conference (SPEC)*, pp. 1-6, 2016.

[9] J. Qian, A. Khan, and I. Batarseh, "Turn-off switching loss model and analysis of IGBT under different switching operation modes," in *Proceedings of the 1995 IEEE IECON 21st International Conference on Industrial Electronics, Control, and Instrumentation*, Vol. 1, pp. 240-245, 1995.

[10] Y.-Y. Tzou and L.-J. Hsu, "A practical SPICE macro model for the IGBT," in International Conference on Industrial Electronics, Control, and Instrumentation, Proceedings of the IECON '93, pp. 762-766, 1993.

[11] Mihalic, K. Jezernik, K. Krischan, and M. Rentmeister, "IGBT SPICE model," *IEEE Trans. Ind. Electron.*, Vol. 42, No. 1, pp. 98-105, Feb. 1995.

[12] J.-T. Hsu and K. D. T. Ngo, "Behavioural modeling of the IGBT using the Hammerstein configuration," *IEEE Trans. Power Electron.*, Vol. 11, No. 6, pp. 746-754, Nov. 1996.

[13] H. S. Oh and M. El. Nokali, "A new IGBT behavioural model," *Solid State Electronics*, Vol. 45, No. 12, pp 2069-2075, 2001.

[14] M. Jin and M. Weiming, "Power converter EMI analysis including IGBT nonlinear switching transient model," *IEEE Trans. Ind. Electron.*, Vol. 53, No. 5, pp. 1577-1583, Oct. 2006.

[15] A. T. Bryant, L. Lu, E. Santi, J. L. Hudgins, and P. R. Palmer, "Modeling of IGBT resistive and inductive turn-on behavior," *IEEE Trans. Ind. Appl.*, Vol. 44, No. 3, pp. 904-914, Jun. 2008.

[16] A. R. Hefner, "Analytical modeling of device-circuit interactions for the power insulated gate bipolar transistor (IGBT)," *IEEE Trans. Ind. Appl.*, Vol. 26, No. 6, pp. 995-1005, Dec. 1990.

[17] IXYS Cooperation, data sheet of IXGT6N170, Available: http://ixapps.ixys.com/DataSheet/DS98990C(IXGH-T6N170A).pdf

[18] P. Leturcq, "Power semiconductor device modelling dedicated to circuit simulation," in *Power Semiconductor Devices and ICs, 1999. ISPSD '99. Proceedings., The 11th International Symposium on,* pp. 19-26, 1999.

[19] Y.-C. Liang and V. J. Gosbell, "Diode forward and reverse recovery model for power electronic SPICE simulations," *IEEE Trans. Power Electron.*, Vol. 5, No. 3, pp. 346-356, Jul. 1990.

[20] D.-S. Kuo, J.-Y. Choi, D. Giandomenico, C. Hu, S. P. Sapp, K. A. Sassaman, and R. Bregar, "Modeling the turn-off characteristics of the bipolar-MOS transistor," *IEEE Electron Device Lett.*, Vol. 6, No. 5, pp. 211-214, May 1985.

[21] M. Trivedi and K. Shenai, "Modeling the turn-off of IGBT's in hard- and soft-switching applications," *IEEE Trans. Electron. Devices*, Vol. 44, No. 5, pp. 887-893, May 1997.

[22] J. C. Joyce, "Current sharingand redistribution in high power IGBT modules," PhD Thesis, University of Cambridge, May 2001.

[23] P. Palmer, E. Santi, J. Hudgins, X. Kang, J. Joyce, and P. Eng, "Circuit simulator models for the diode and IGBT with full temperature dependent features," *IEEE Trans. Power Electron.*, Vol. 18, No. 5, pp. 1220-1229, Sep. 2003

[24] U. N. Gnanarathna, A. M. Gole, A. D. Rajapakse, S. K. Chaudhary, "Loss estimation of modular multi-level converters using electro-magnetic transients simulation," *Proceedings of Int. Conf. Power Systems Transients -2011*, pp. 1-6, 2011.

Naushath Mohamed Haleem received his B.Tech. (Eng.) degree in electronics and communications from the Open University of Sri Lanka, Sri Lanka, in 2005, and his M.Sc degree in electrical engineering from the University of Manitoba, Winnipeg, MB, Canada, in 2013. He is currently pursuing his PhD degree in electrical engineering at the University of Manitoba, Winnipeg, MB, Canada. His research interests include modeling of HVdc converters, protection of VSC-based future multi-terminal HVdc grids, and protection and control of hybrid LCC-VSC multi-terminal HVdc Systems.

Athula D. Rajapakse received his B.Sc (Eng.) degree in electrical engineering from the University of Moratuwa, Katubedda, Sri Lanka, in 1990; his M. Eng. degree in Energy (Energy Technology) from the Asian Institute of Technology, Bangkok, Thailand, in 1993; and his Ph.D. degree in quantum engineering and systems science from the University of Tokyo, Japan, in 1998. He is a professor at the University of Manitoba, Winnipeg, MB, Canada. His research interests include power system protection, grid integration of distributed and renewable energy systems, and protection of future DC grids. Dr. Rajapakse is a registered professional engineer in the province of Manitoba, Canada.

Aniruddha M. Gole received his B.Tech. degree in electrical engineering from the Indian Institute of Technology, Bombay, India, in 1978; and his Ph.D. degree from the University of Manitoba, Winnipeg, MB, Canada, in 1982. He is a distinguished professor and NSERC Industrial Research Chair in Power System Simulation at the University of Manitoba. Prof. Gole is a registered professional engineer in the province of Manitoba. He is the 2007 recipient of the IEEE Power Engineering Society Nari Hingorani FACTS Award.