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# Analysis of Switching Clamped Oscillations of SiC MOSFETs

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## Abstract

SiC MOSFETs have been used to improve system efficiency in high frequency converters due to their extremely high switching speed. However, this can result in undesirable parasitic oscillations in practical systems. In this paper, models of the key components are introduced first. Then, theoretical formulas are derived to calculate the switching oscillation frequencies after full turn-on and turn-off in clamped inductive circuits. Analysis indicates that the turn-on oscillation frequency depends on the power loop parasitic inductance and parasitic capacitances of the freewheeling diode and load inductor. On the other hand, the turn-off oscillation frequency is found to be determined by the output parasitic capacitance of the SiC MOSFET and power loop parasitic inductance. Moreover, the shifting regularity of the turn-off maximum peak voltage with a varying switching speed is investigated on the basis of time domain simulation. The distortion of the turn-on current is theoretically analyzed. Finally, experimental results verifying the above calculations and analyses are presented.

**Key words:** Analytical model, Current distortion, Maximum peak shifting, Oscillation frequency, Parasitic parameter, SiC MOSFET

## I. INTRODUCTION

Superior material's physical properties such as a wide bandgap, high heat conductivity and high saturation electron drift velocity provide more opportunities for silicon carbide (SiC) power semiconductor devices to replace silicon (Si) power semiconductor devices of the same grade in power electronic converter systems [1]. Commercial SiC field effect transistors, especially SiC MOSFETs, have been compared with conventional Si MOSFETs and IGBTs, where it is found that the former have lower switching and conduction losses, higher temperature tolerance and higher operating frequency. The superiority of device properties results in substantial system level performance improvements such as the improvement of efficiency and power density when these devices are properly applied to power electronic circuits such as photovoltaic inverters [2], electric vehicles [3] and solid state transformers [4]. However, fast switching features also introduce some undesirable phenomena. For instance, the circuit parasitic inductance and the parasitic capacitance of a device may generate a high frequency under-damped natural oscillation response.

In power electronic circuits, the main parasitic oscillation phenomena can be roughly divided into the following three types. The first type of parasitic oscillation is the shoot-through phenomenon in half-bridge configurations. An inactive switch is influenced via the displacement of the capacitive current caused by the high d$v$/d$t$ during turn on transient of the active switch. This current flows through the miller capacitance and gate resistance, introducing a voltage drop across the gate and source terminals of the inactive switch. If this drop is beyond the SiC MOSFET threshold voltage, a temporary shoot-through may be generated, leading to more switching losses and an extremely fast temperature rise or even device destruction. On the other hand, an opposite displace current is generated and the voltage drop is superposed on the negative gate bias voltage causing more stress on the SiC MOSFET gate oxide layer. Moreover, when compared to silicon devices, the SiC MOSFET has a lower threshold voltage, making it more vulnerable to the shoot-through [5]. Some effective suppression methods have been proposed to solve this problem in [6], [7]. Hence, further

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discussion is not provided in this paper. The second type of parasitic oscillation is an extreme oscillation phenomenon of repeated turning on and turning off, called self-sustained oscillation. This is common in negative feedback integrated amplifier circuits instead of power devices and is different from shoot-through. If self-sustained oscillation occurs in a power electronic circuit, the system runs into instability and the power devices may be destroyed under certain conditions. The authors of [8] and [9] adopt a small signal equivalent circuit and a negative resistance oscillator model. Furthermore, the critical condition of the self-sustained oscillation is given according to Barkhausen criterion. Results show that SiC JFETs are more likely to induce self-sustained oscillation when compared to SiC MOSFETs, due to the lower input capacitance and faster switching speed of the former. In addition, for SiC MOSFETs, self-sustained oscillation only occurs when the drain-source voltage $V_{DS}$ is lower than 100V. Thus, it does not generally appear in the actual working conditions for high rating SiC MOSFETs. The last type of parasitic oscillation is damped oscillation, which is usually called LC oscillation. This kind of phenomenon has been reported in [10]-[12]. The lower damping factor caused by a lower on-resistance and a smaller input capacitance makes SiC devices more vulnerable to parasitic resonance. Although these features reduce both conduction and switching losses of a device and provide for a more compact systems design, the influence of parasitic parameters on the SiC MOSFET gate-source voltage should be analyzed. Gate-source oscillation is briefly mentioned in [13]. An RLC circuit model is built to characterize the switching behavior in [14]. However, the actual experimental waveform is not a standard second-order underdamped oscillation. Therefore, it is not satisfactory for explaining the turn-on and turn-off transients by using the method presented in [14]. Moreover, although [14] provides a detailed approach for describing the switching oscillations after full turn-on and after full turn-off, it does not consider the parasitic capacitance $C_L$ of the inductor. The authors of [15] mentioned the maximum peak voltage shifts phenomenon. However, they only focus on the maximum peak voltage shifting of the upper switcher during the turn-on of the lower switcher, instead of the turn-on current and turn-off voltage oscillation for the lower switcher.

This paper comprehensively investigates the switching oscillation behavior of SiC MOSFETs. Both of the switching processes, turn-on and turn-off, have two distinct stages, transient and after full switching, which are characterized by switching oscillations. These stages are treated separately in this analysis since they display oscillations with different features and are triggered by different switching circuit topologies. In section II, models of all the key components of the standard double pulse test circuit are introduced. In section III, approximate calculations by the simplifying circuit are conducted to study the oscillation frequency after full turn-on and turn-off. Moreover, the turn-on current overshoot and turn-off maximum peak voltage shifting phenomenon are analyzed. In section IV, a double pulse test bench is built, and the parasitic parameters are extracted based on the experiment method. Then, distortions of the turn-on current peak and turn-off maximum peak voltage shifting are observed from experimental waveform. This verifies that these calculation and simulation are valid and reasonable. Some solutions to suppress the overshoot and oscillation are provided in Section V. Several conclusions are given in Section VI.

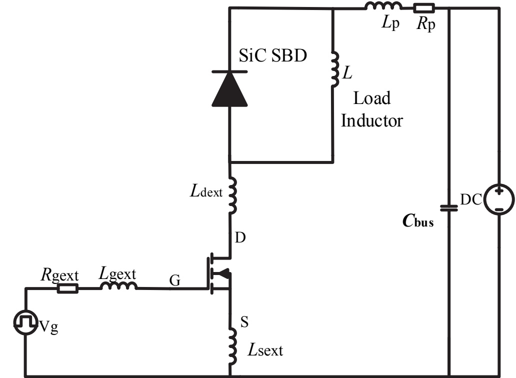

Fig. 1. Double pulse test circuit.

## II. Circuit Models

In this paper, a standard double pulse test (DPT) method is used. As shown in Fig. 1, a clamped inductive circuit is built to accurately assess and analyze the SiC MOSFET switching parasitic oscillation behavior. All of the parasitic parameters of the key components including the MOSFET, SiC SBD, load inductor, PCB trace and bus-bar capacitor, are considered.

### *A. SiC MOSFET Device*

As shown in Fig. 2, the MOSFET model includes an N-MOS, a reverse junction diode, an inner gate resistance $R_{Gint}$, three kinds of inner parasitic capacitances and three terminal parasitic inductances. The inner parasitic capacitances are composed of the gate-source capacitance $C_{GS}$, the gate-drain capacitance $C_{GD}$ and the drain-source capacitance $C_{DS}$. The three package inductances $L_{GP}$, $L_{DP}$ and $L_{SP}$ stem from the device lead and bonding wire of the gate, drain and source terminal. Although the authors of [16] suggest that $C_{GS}$ should be set to a different value depending on the polarity of $V_{GS}$, $C_{GS}$ can be regarded as constant due to the fact that $V_{GS}$ is higher than zero in the switching oscillation stage. However, $C_{GD}$ and $C_{DS}$ are non-linear with the drain-source voltage [17]. In order to simplify the analysis, two discrete values of the capacitances are adopted as shown in Fig. 3. During the turn on stage, the drain current rises firstly. Then, the drain-source voltage begins to fall. Therefore, $C_{GD}$ and $C_{DS}$ are small during turn-on current transients. Similarly, they are still small during turn-off current falling transients

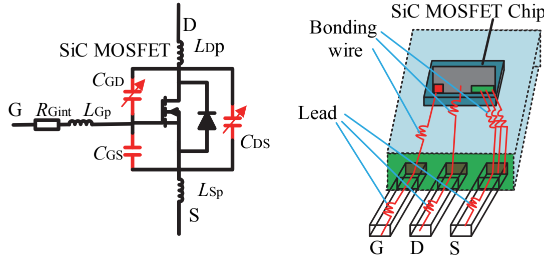


Fig. 2. Parasitic components of a SiC MOSFET device.

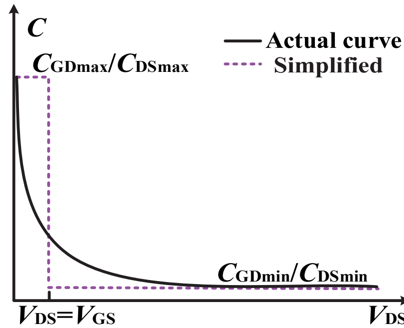


Fig. 3. Simplification of nonlinear capacitance.

since the drain-source voltage has already risen and reached a high bias voltage.

### B. SiC SBD

SiC SBD devices can be modeled as shown in Fig. 4 [17]. Similar to $C_{GD}$ and $C_{DS}$, the junction capacitance $C_D$ of a SiC SBD, which is significant for turn-on transient analysis, also varies non-linearly with a bias voltage. Therefore, two discrete values, with similar simplification to $C_{GD}$ and $C_{DS}$, are used as a trade-off between the complexity and accuracy of the analysis.

### C. Load Inductor

Although the junction capacitance of a SiC SBD is very small when compared to that of a silicon diode, there is still current overshoot due to the high d$v$/d$t$. Therefore, when an inductive load is connected in parallel with a SiC SBD, the influence of the parasitic capacitance of the load inductor on the turn-on current transient cannot be ignored. As shown in Fig. 5, the load inductor is modeled with a lumped equivalent circuit, which includes the main inductance $L$, the equivalent series resistance $R_L$ and the equivalent parallel capacitance $C_L$.

### D. Bus-Bar Capacitor and PCB Trace

During turn-off transient, a large turn-off voltage overshoot is induced across the circuit loop parasitic inductance due to d$i$/d$t$. Generally, the parasitic inductance $L_C$ of the bus-bar capacitor and the parasitic inductance $L_p$ of the interconnected PCB trace between the capacitors and the device are the dominant part of the total parasitic inductance. Similarly, the

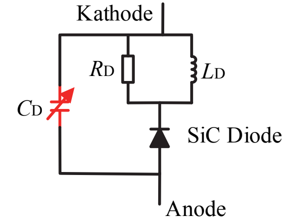


Fig. 4. Model of a SiC SBD device.

Fig. 5. Equivalent circuit of a load inductor.

bus-bar capacitor can also be modeled by a series equivalent circuit. However, the oscillation analysis in this paper pays more attention to the loop parasitic inductance. Hence, it is not necessary to model and extract the parasitic inductance of each part individually.

## III. Analysis of Switching Behaviors

Ideally, the current gradually rises until it reaches the steady-state and then remains constant during the saturation region, without considering the parasitic parameters. Actually, an undesirable oscillation occurs due to the parasitic parameters. Some studies assume that the current may change in the form of a standard second-order underdamped oscillation, and then gradually return to the steady-state value due to the parasitic capacitances and parasitic inductances of the loop. However, there are distinct oscillation behaviors between the turn-on transient and after full turn-on, and between the turn-off transient and after full turn-off. Actually, there is an abnormal phenomenon instead of an ideal second-order underdamped oscillation under different d$i$/d$t$ and d$v$/d$t$, which can be observed from the experimental switching waveforms shown in the next section.

### A. Full Turn-On Oscillation Behavior

When a SiC MOSFET fully turns on, $V_{DS}$ is approximately zero volt and $C_{DS}$ is short connected by the device. Taking into account the fact that the driver branch impedance is a lot more than reactance of the common source parasitic inductance, a simplified equivalent circuit can be developed as shown in Fig. 6 [14]. Obviously, the equivalent circuit after turning on can be seen as an RLC circuit. Hence, the switching oscillation frequency is expressed as function of the loop inductance $L_{loop}$ and total parasitic capacitance of the upper bridge $C_F$.

$$f_1 = \frac{1}{2\pi\sqrt{L_{loop}C_F}} \tag{1}$$

Where, $C_F=C_D+C_L$, $C_D=C_{Dmin}$, $L_{loop}=L_C+L_p+L_d+L_s$ and $L_d=L_{DP}+L_{dext}$, $L_s=L_{SP}+L_{sext}$.

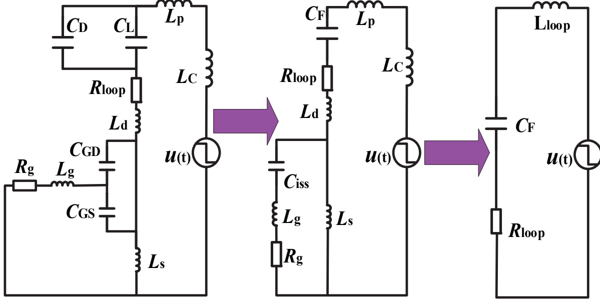


Fig. 6. Simplified equivalent circuit after full turn-on.

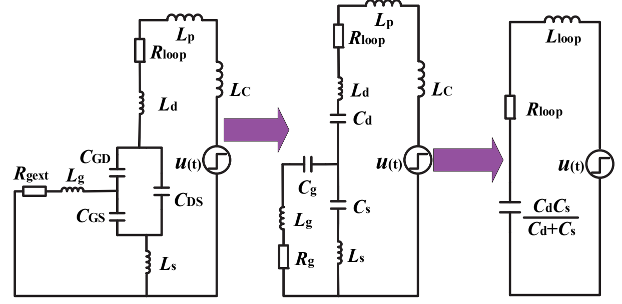


Fig. 7. Simplified equivalent circuit after full turning off.

## B. Turn-On Transient Behavior

The reverse recovery time of a SiC SBD is very short and can even be ignored [18]. Therefore, the turn-on current overshoot cannot be effectively represented by the traditional calculation formula with adopting the reverse recovery charge, snappiness factor and d$i$/d$t$ in [19]. When the SiC MOSFET turn-on current rises to the load current, the SiC SBD current drops to zero and begins entering the off-state. Then, the turn-on current keeps increasing until it reaches its peak value, due to the displacement current of the diode junction capacitance and the parasitic capacitance of the load inductor. A SiC MOSFET can be regarded as a d$i$/d$t$ constant current source during this phase and it can charge these two parasitic capacitances. The voltage of a SiC SBD can be calculated by Equ. (2) [18].

$$v_{\mathrm{F}(t)} = \frac{1}{C_{\mathrm{F}}} \int_{0}^{T} -\frac{\mathrm{d}i_{\mathrm{d}}}{\mathrm{d}t} \cdot t \cdot \mathrm{d}t \tag{2}$$

The rising slope drops to zero when the turn-on current reaches the first peak value. The energy stored in the parasitic inductance is released into the parasitic capacitance, and the inductive voltage across the loop parasitic inductance is sustained by the SiC SBD. Hence, the voltage across the SiC SBD can be expressed as:

$$v_{\mathrm{F}(t)} = -v_{\sigma} = -L_{\mathrm{loop}} \frac{\mathrm{d}i_{\mathrm{d}}}{\mathrm{d}t} \tag{3}$$

The transient time from the load current to the first peak value can be obtained by combining Equs. (2)-(3).

$$T = \sqrt{2 C_{\mathrm{F}} L_{\mathrm{loop}}} \tag{4}$$

Hence, the first peak current overshoot is:

$$\Delta i_{\mathrm{rpk}} = \frac{\mathrm{d}i}{\mathrm{d}t} \sqrt{2(C_{\mathrm{D}} + C_{\mathrm{L}}) L_{\mathrm{loop}}} \tag{5}$$

The turn-on current slope can be approximately expressed as:

$$\frac{\mathrm{d}i_{\mathrm{d}}}{\mathrm{d}t} = \frac{g_{\mathrm{fs}}\left(V_{\mathrm{GH}} - V_{\mathrm{th}}\right)}{\left[R_{\mathrm{G}}\left(C_{\mathrm{gs}} + C_{\mathrm{gdmin}}\right) + g_{\mathrm{fs}} L_{\mathrm{S}}\right]} \tag{6}$$

When the turn-on current reaches the first peak, the SiC MOSFET's $V_{\mathrm{DS}}$ starts falling rapidly, and the diode's reverse bias voltage begins rising rapidly. The high d$v$/d$t$ induces a displacement current on the parasitic capacitance of the MOSFET, the SBD and the load inductor, which then flows into the MOSFET channel. The first current overshoot might be defined as an indirectly induced displacement current. It is introduced by the displacement current of the diode junction capacitance and the parasitic capacitance of the load inductor caused by the voltage variation induced by the d$i$/d$t$ of the loop parasitic inductance. The second current overshoot, seen as a directly induced displacement current, is induced by rapid changes of $V_{\mathrm{DS}}$, leading to a current distortion during turn-on transients. The maximum d$v$/d$t$ before the SiC MOSFET is triggered on is governed empirically by Equ. (7) [20], and the second peak current overshoot is expressed as Equ. (8).

$$\left[\frac{\mathrm{d}v_{\mathrm{DS}}}{\mathrm{d}t}\right]_{\max} \approx -\frac{V_{\mathrm{GH}} - V_{\mathrm{miller}}}{R_{\mathrm{G}} C_{\mathrm{GDmin}}} \tag{7}$$

$$\Delta i_{\mathrm{cpk}} = C_{\mathrm{F}} \frac{\mathrm{d}v_{\mathrm{ds}}}{\mathrm{d}t} \tag{8}$$

## C. Full Turn-Off Oscillation Behavior

When a SiC MOSFET fully turns off, the drain current is supposed to be zero ampere and all of the load current is expected to flow through the SiC SBD. The parasitic capacitances of both the freewheeling diode and the load inductor are bypassed due to a very small forward voltage drop, which can be ignored. The Δ-Y transform expressed by Equ. (9) is used to simplify the equivalent circuit.

$$\left.\begin{aligned} C_{\mathrm{g}} &= C_{\mathrm{GS}} + C_{\mathrm{GD}} + C_{\mathrm{GS}} C_{\mathrm{GD}} / C_{\mathrm{DS}} \\ C_{\mathrm{d}} &= C_{\mathrm{GD}} + C_{\mathrm{DS}} + C_{\mathrm{GD}} C_{\mathrm{DS}} / C_{\mathrm{GS}} \\ C_{\mathrm{s}} &= C_{\mathrm{GS}} + C_{\mathrm{DS}} + C_{\mathrm{GS}} C_{\mathrm{DS}} / C_{\mathrm{GD}} \end{aligned}\right\} \tag{9}$$

$C_{\mathrm{g}}$ is far less than $C_{\mathrm{s}}$ due to the fact that $C_{\mathrm{GD}}$ is much less than $C_{\mathrm{DS}}$ and $C_{\mathrm{GS}}$. Therefore, the driver branch is large enough and can be left out. In addition, the equivalent circuit after full turn off can be simplified as the RLC circuit shown in Fig. 7. Hence, the turn-off oscillation frequency can be expressed as:

$$f_2 \approx \frac{1}{2\pi \sqrt{L_{\mathrm{loop}} C_{\mathrm{eq}}}} \tag{10}$$

$$C_{\mathrm{eq}} = \frac{C_{\mathrm{d}} C_{\mathrm{s}}}{C_{\mathrm{d}} + C_{\mathrm{s}}} \tag{11}$$

Where, $C_{\mathrm{GD}}=C_{\mathrm{GDmin}}$ and $C_{\mathrm{DS}}=C_{\mathrm{DSmin}}$.

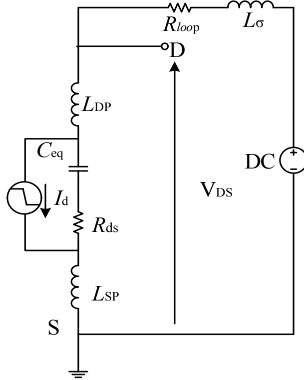


Fig. 8. Simulating model for turn-off transients.

### D. *Turn-Off Transient Behavior*

Unlike the turn-on transient, $V_{DS}$ first rises to the dc bus voltage. Then, the drain current begins falling during the turn-off transient. Similarly, the turn-off oscillation and overshoot can come from two parts of excitation. One part is the series resonance introduced by a high positive step d$v$/d$t$. The other part is the dc voltage component across the parasitic inductances induced by the d$i$/d$t$, which leads to a shift of the maximum peak voltage.

Moreover, there may not be a fixed oscillation frequency during the falling stage of $V_{DS}$ due to the nonlinearity of the parasitic capacitance. Hence, the switching behaviors during turn-off transients are very complicated. However, with variations of the turn-off speed, an abnormal phenomenon in terms of the maximum peak voltage shifting appears in the turn-off transients. To illustrate this phenomenon, this paper establishes a simple simulation model. As shown in Fig. 8, a current source with an adjustable falling time is used to reflect different turn-off speeds. $L_σ$ and $R_{loop}$ represent the power loop parasitic inductance and the stray resistance, while $L_{DP}$ and $L_{SP}$ are the terminal package parasitic inductances of a SiC MOSFET device. $C_{eq}$ is the turn-off equivalent capacitance as mentioned above. The equivalent period of oscillation can be expressed as:

$$T_{osc} = 1/f_2 \tag{12}$$

$V_{DS}$ oscillation waveforms during the turn-off period under different d$i$/d$t$ are shown in Fig. 9. It is interesting to observe that the maximum value of $V_{DS}$ shifts from the first peak to the second peak, when the current fall time $T_f$ is nearly 1.5 folds of the turn-off oscillation period $T_{osc}$. Although overshoot keeps decreasing with an increased falling time, there is still a repeated shift from the second peak to the third peak in almost 2.5 multiples of $T_{osc}$. Therefore, it is noted that there are relative maxima occurring in approximately (n+1/2)$T_{osc}$.

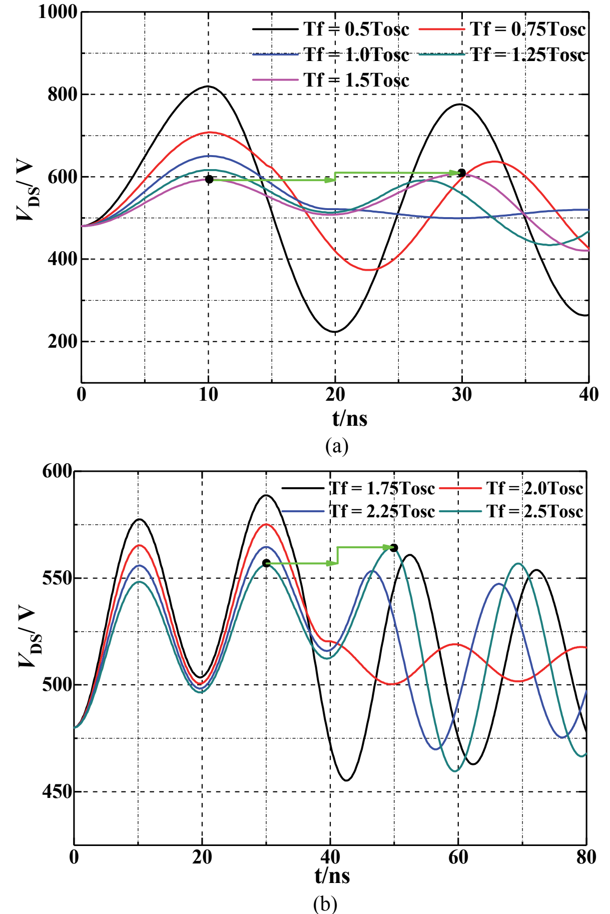


Fig. 9. Maximum peak voltage shifting with a falling time. (a) Switching waveforms under 0.5$T_{osc}$-1.5 $T_{osc}$. (b) Switching waveforms under 1.75$T_{osc}$-2.5 $T_{osc}$.

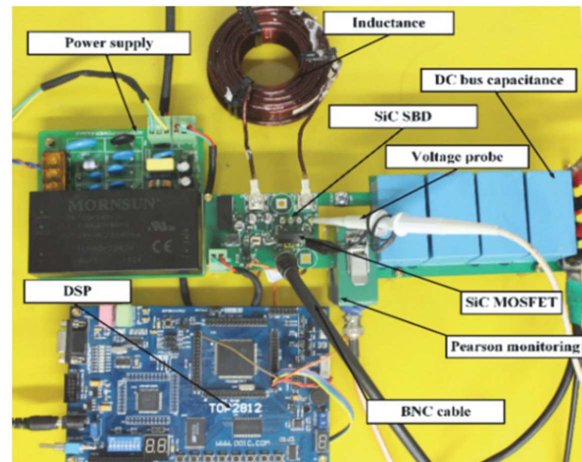


Fig. 10. Double pulse test bench.

## IV. Experimental Verification

### A. *Test Setup*

To verify the impact of the parasitic parameter on device switching behavior, a double pulse test bench is built. A 1200V/36A SiC MOSFET C2M0080120D and a 1200V/33A SiC SBD C4D20120D are available from Cree. As shown in Fig. 10, the test bench includes four parts of PCB: the digital signal processor (DSP) evaluation board 00IC TOP2812, the gate drive, the power supply and the dc bus. The DSP is used

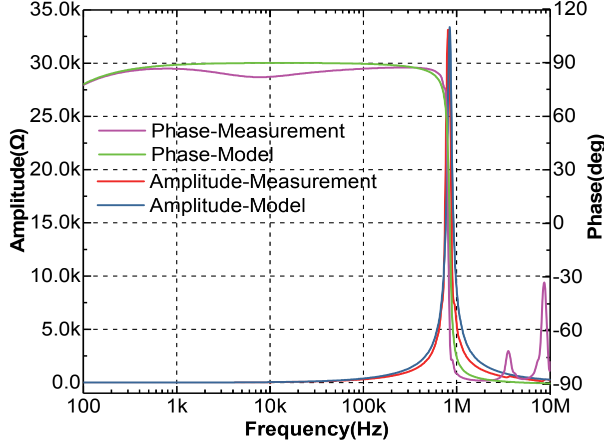

Fig. 11. The curve-fitting of the load inductor model.

TABLE I
EXPERIMENTAL PARAMETERS

| Component | Parameter | Value | Parameter | Value |
|---|---|---|---|---|
| SiC MOSFET | $C_{GS}$ | 950pF | $g_{fs}$ | 7.5 |
| | $C_{GDmin}$ | 7.6pF | $L_{DP}$ | 2.5nH |
| | $C_{DSmin}$ | 77pF | $L_{SP}$ | 6.5nH |
| | $V_{th}$ | 5.5V | $L_{GP}$ | 9.5nH |
| | $V_{mill}$ | 9V | $R_{Gint}$ | 4.6Ω |
| SiC SBD | $C_{Dmin}$ | 40pF | | |
| Load Inductor | $L$ | 570uH | $C_L$ | 108pF |
| Power loop | $V_{DD}$ | 500V | $L_{sext}$ | 3.5nH |
| | $L_{loop}$ | 100nH | $I_L$ | 20A |
| Driver loop | $V_{GH}$ | 20V | $-V_{EE}$ | -4.5V |
| | $R_{gext}$ | 37.5Ω | | |

to generate the required double pulse control signal. The ACPL-W343, internally integrated with an optical coupling isolation, has been adopted to magnify the control signal. At the same time, the power supply, based on a MORNSUN QA01C, is developed to provide positive and negative bias voltage for the gate driver. In addition, a bidirectional TVS diode is connected with gate-source terminal to protect the gate against breakdown.

### B. Parameters Extraction

The internal gate resistance $R_{g1}$, the parasitic capacitances $C_{GS}$, $C_{GD}$ and $C_{DS}$ of the SiC MOSFET, and $C_D$ of the SiC SBD can be obtained from the manufacture's datasheet. The package parasitic inductances can be extracted with measurements by an impedance analyzer [21]. The power loop parasitic inductance $L_{loop}$ may be calculated by the time domain finite element and PEEC methods. However, these require obtaining detailed models of the layout, bonding pad and connecting component, which is time-consuming. Hence, the experimental waveforms method is proposed to approximately calculate the power loop parasitic inductance $L_{loop}$. Generally, the methods of both the turn-off voltage drops and turn-off voltage overshoot can be used to evaluate the power loop inductance. The average value of the calculations by the two methods is set as the inductance in this paper.

$$L_{loop} = \frac{1}{2} \times \left[ \frac{\Delta V_{drop}}{di_r/dt} + \frac{\Delta V_{over}}{di_f/dt} \right] \tag{13}$$

The air core load inductor is modeled by the main inductance $L$ together with the series resistance $R_L$ and the parasitic capacitance $C_L$ as shown in Fig. 5. A spectrogram of this simple model is also presented in Fig. 11, where a good uniformity is obtained up to 3MHz, which is enough for a 100ns rising edge as shown in Equ. (14). The value of $C_L$ is calculated by the resonant frequency. The experimental conditions and extraction parameters are shown in Table I.

$$\text{BW} = \frac{0.25}{\min[t_r, t_f]} \tag{14}$$

### C. Oscillation Frequency of the Full Turn-on and Turn-off

In this paper, several discrete ceramic capacitors with different values are connected with the SiC SBD and SiC MOSFET in parallel to verify the relationship between the full turn-on and turn-off oscillation frequency and the parasitic capacitance. A spectral analysis of the experimental waveforms has been conducted by FFT tool. The turn-on and turn-off oscillation frequencies under different parasitic capacitances are shown in Fig. 12 and Fig. 13, which approximately agree with the results calculated based on Equ. (1) and Equ. (10), respectively. Therefore, the two equations above are effective for evaluating the oscillation frequency after full turn-on and turn-off. As shown in Table II, the relative error between turn-on oscillation frequency of the experiment and the analysis is less than 15% under different parasitic capacitances $C_F$. Similarly, the relative error between the turn-off oscillation frequency of the analysis and the experiment is less than 10% under different parasitic capacitances $C_{DS}$, as shown in Table III. Therefore, it is reasonable to evaluate the switching oscillation frequency of the full turn-on and turn-off by using this simplified method.

### D. Experimental Analysis of the Turn-On Transient

To clarify the distortion phenomenon of the turn-on transient current waveform, this paper obtains two groups of switching waveform by adjusting the values of $R_g$ and $C_{GS}$. The d$v$/d$t$ primarily depends on $R_g$ and $C_{GD}$, whereas $R_g$ and $C_{GS}$ play a more important role in the d$i$/d$t$. A smaller $R_g$ is adopted to achieve a higher d$v$/d$t$. Meanwhile, a higher d$i$/d$t$ is obtained by a lower $C_{GS}$. An experimental waveform is shown in Fig. 14. The red line with the higher d$i$/d$t$ and lower d$v$/d$t$ have almost no distortion gap. The peak difference between the indirectly induced displacement current and the directly induced displacement current is tiny. On the other hand, there is a distortion during the turn-on transient for the blue line with a lower d$i$/d$t$ and a higher d$v$/d$t$. Obviously, the directly induced displacement current has a higher peak

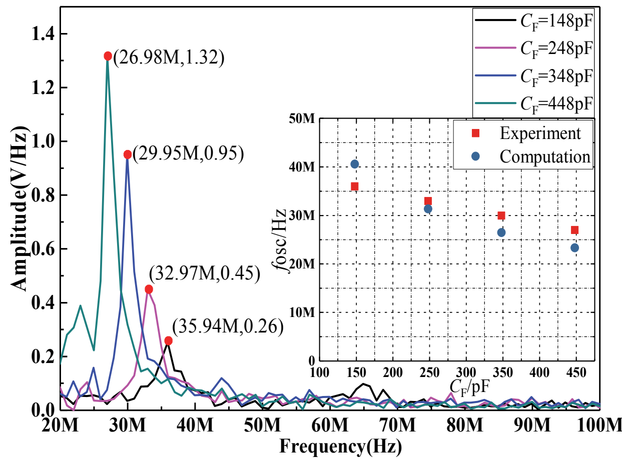


Fig. 12. Turn-on oscillation frequency under different $C_F$.

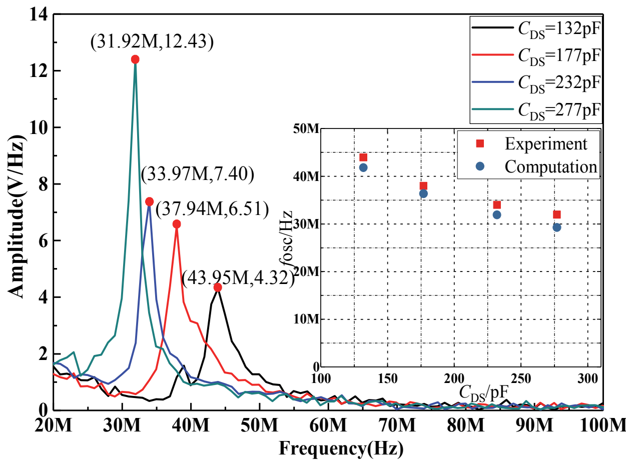


Fig. 13. Turn-off oscillation frequency under different $C_{ds}$.

TABLE II
OSCILLATION FREQUENCY AFTER FULL TURN-ON

| $C_F$(pF) | $f_{Exp}$(MHz) | $f_{Ana}$(MHz) | Error(%) |
|---|---|---|---|
| 188 | 35.94 | 40.57 | 12.87 |
| 248 | 32.97 | 31.33 | 4.95 |
| 348 | 29.95 | 26.46 | 11.67 |
| 448 | 26.98 | 23.32 | 13.58 |

TABLE III
OSCILLATION FREQUENCY AFTER FULL TURN-OFF

| $C_{DS}$(pF) | $f_{Exp}$(MHz) | $f_{Ana}$(MHz) | Error(%) |
|---|---|---|---|
| 132 | 43.95 | 41.78 | 4.94 |
| 177 | 37.94 | 36.33 | 4.25 |
| 232 | 33.97 | 31.89 | 6.13 |
| 277 | 31.92 | 29.26 | 8.34 |

value. To increase the first overshoot time $T$ while keeping d$v$/d$t$ and d$i$/d$t$ constant, several discrete inductors were inserted to change $L_d$. As shown in Fig. 15, the maximum value of the drain current always occurs at the first peak,

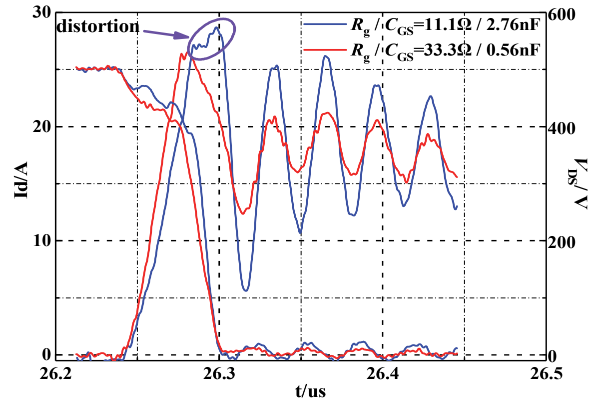


Fig. 14. Turn-on transient waveforms with two combinations.

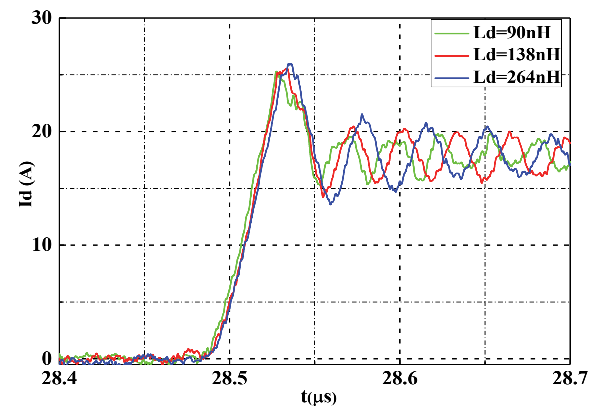


Fig. 15. Turn-on transient waveforms under different $L_d$.

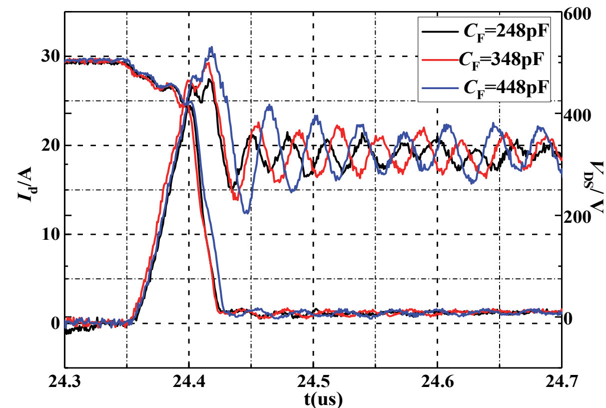


Fig. 16. Turn-on transient waveforms under different $C_F$.

which increases with a larger drain inductance. However, the maximum current occurs at the second peak when different capacitors are connected in parallel with the SiC SBD as shown in Fig. 16. Although the first peak current increase in square root multiples of $C_F$, the second current peak keeps increasing linearly. As a result, the distortion gap and oscillation amplitude increase with $C_F$.

## *E. Experimental Analysis of the Turn-Off Transient*

$R_g$ and $C_{GS}$ are two critical elements for the turn-off current falling slope d$i$/d$t$, which is approximately expressed by:

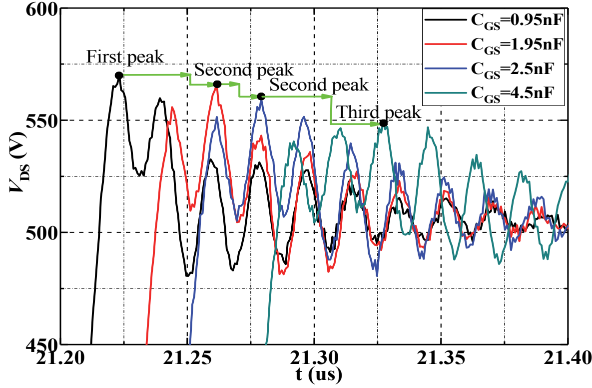


Fig. 17. Experimental waveform under different $C_{GS}$.

TABLE IV
RELATION OF CURRENT FALLING TIME AND OSCILLATION PERIOD

| $C_{GS}$(nF) | $T_{Cal}$(ns) | $T_{Exp}$(ns) | $T_{osc}$(ns) | $k_{Cal}$ | $k_{Exp}$ |
|---|---|---|---|---|---|
| 0.95 | 21.13 | 20.5 | 19 | 1.11 | 1.08 |
| 1.95 | 28.27 | 28.0 | 19 | 1.49 | 1.47 |
| 2.5 | 32.20 | 37.6 | 19 | 1.69 | 2.03 |
| 4.5 | 46.49 | 50.4 | 19 | 2.45 | 2.65 |

$$\frac{\mathrm{d}i_{d(t)}}{\mathrm{d}t} \approx -\frac{g_{fs}\left(V_{\text{mill}}+V_{\text{EE}}\right)}{\left[R_{\text{g}}\left(C_{\text{gs}}+C_{\text{gdmin}}\right)+g_{\text{fs}}L_{\text{s}}\right]} \tag{15}$$

Several different capacitors are connected in parallel with the gate-source terminal to achieve a varying current slope without affecting the d$v$/d$t$, which is also influenced by $R_g$ according to Equ. (7). The total gate-source capacitance $C_{GS}$ includes the device internal parasitic capacitance and the external paralleled capacitance. Fig. 17 shows that the shifting of the maximum peak voltage occurs when $C_{GS}$ is selected as 1.95nF and 4.5nF, respectively. As shown in Table IV, the corresponding current falling times are 28.27ns calculated by Equ. (16) and 28ns obtained by experimental tests at $C_{GS}$ =1.95nF. The multiple $k_{Cal}$ of the calculated current falling time to the oscillation period $T_{osc}$ and the multiple $k_{Exp}$ of the measured current falling time to the oscillation period $T_{osc}$ are 1.49 and 1.47, respectively. This is approximately equal to 1.5. Similarly, when $C_{GS}$ is equals to 4.5nF, the values of $k_{Cal}$ and $k_{Exp}$ are 2.45 and 2.65, which are close to the 2.5. Therefore, it is verified that the above analysis is reasonable.

Current falling time during turn-off is obtained by:

$$T_{\text{f}} = I_{\text{L}} \Big/ \frac{\mathrm{d}i_{\text{d}(t)}}{\mathrm{d}t} = \frac{I_{\text{L}}\left[R_{\text{g}}\left(C_{\text{GS}}+C_{\text{GDmin}}\right)+g_{\text{fs}}L_{\text{s}}\right]}{g_{\text{fs}}\left(V_{\text{mill}}+V_{\text{EE}}\right)} \tag{16}$$

## V. DISCUSSIONS

According to the above analysis, the full turn-on oscillation frequency and magnitude depend on the loop parasitic inductance, the parasitic capacitance of the load inductor, and the junction capacitance of the SiC SBD. In order to suppress the turn-on current overshoot, some measures must be taken in actual circuit design. One such measure is the reduction of the total parasitic capacitances of the upper bridge by using a diode with a small junction capacitance, and a load inductor with a single-layer winding. In addition, the two terminals of the load inductor should not be too close. Another measure is the controlling of the d$v$/d$t$ during turn-on transients, especially the current overshoot stage, by deploying a multi-level driver. For turn-off oscillations, the frequency and magnitude depend on the loop parasitic inductance and output capacitance of the SiC MOSFET. The miniaturization of the loop parasitic inductance is significant for reducing the turn-off voltage overshoot. Therefore, one measure for reducing oscillation during turn-off can be a round layout design for the capacitors along with a laminating bus-bar board. Another measure is to pay more attention to the converter design in order to reduce the power loop areas and to increase the trace width. Moreover, the shifting point of the maximum turn-off voltage peak should be avoided by changing the current falling time. For example, different values of $C_{GS}$ can be connected in parallel with the gate-source terminal under the condition of meeting switching speed requirements of the application.

## VI. CONCLUSIONS

This paper gives insights into the switching oscillation phenomenon during the whole switching period. After fully turning on or off, the oscillation behavior can be approximately characterized by a standard second-order underdamped circuit. It is verified that the oscillation frequency of full turn-on and turn-off depend on the parasitic capacitance of the diode, the SiC MOSFET and the loop parasitic inductance. Moreover, the complex ringing phenomena are exhibited during switching transients, including the current falling stage in the turn-off process and the drain-source voltage falling stage in the turn-on process. Either the turn-on drain current overshoot or the turn-off drain-source voltage overshoot might be induced from two aspect of the excitation source, including d$i$/d$t$ and d$v$/d$t$. During the drain current falling stage, the circuit resonance is introduced by d$i$/d$t$ excitation. The maximum voltage peak shifts backward in turn when the current fall time $T_f$ is approximately equal to (n+1/2)$T_{osc}$. During the drain-source voltage falling stage, when the d$v$/d$t$ or parasitic capacitance is high enough, the displacement current generated by the d$v$/d$t$ is superimposed on the turn-on current, resulting in a distortion gap in the turn-on current waveform.

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