

Distortion Elimination for Buck PFC Converter with Power Factor Improvement

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Abstract

A quasi-constant on-time controlled buck front end in combined discontinuous conduction mode and boundary conduction mode is proposed to improve power factor (PF). When instantaneous AC input voltage is lower than the output bus voltage per period, the buck converter turns into buck-boost converter with the addition of a level comparator to compare input voltage and output voltage. The gate drive voltage is provided by an additional oscillator during distortion time to eliminate the cross-over distortion of the input current. This high PF comes from the avoidance of the input current distortion, thereby enabling energy to be delivered constantly. This paper presents a series analysis of controlling techniques and efficiency, PF, and total harmonic distortion. A comparison in terms of efficiency and PF between the proposed converter and a previous work is performed. The specifications of the converter include the following: input AC voltage is from 90V to 264V, output DC voltage is 80V, and output power is 94W. This converter can achieve PF of 98.74% and efficiency of 97.21% in 220V AC input voltage process.

Key words: AC-DC converter, Buck, Power factor correction, Pulse assisting technique

I. INTRODUCTION

Power quality has become an important consideration in power systems. Thus, much attention has been given to converters with high power factor (PF), low input harmonics, and good efficiency [1]-[3]. Power factor correction (PFC) provides many attractive benefits, including automatic line-voltage adjustments, nearly sinusoidal input current, and improved power quality. PFC front ends are now commonly used in power supply systems, which are connected to an AC line. This AC line ensures that power equipment are in accordance with many standards, such as IEC61000-3-2 specification [4], which is used to limit harmonic current; European Code of Conduct specifications [5], which defines the minimum average efficiency of external power supplies at 25%, 50%, 75%, and 100% of full load; and Energy Star [6], which sets the minimum limit at 0.9 PF.

In a step-down situation, one approach is two-stage converter: boost PFC front end [7], [8] combined with buck DC-DC downstream. PFC circuit is employed to obtain the

sinusoidal input current to provide a high PF, whereas the DC-DC converter is used to regulate the output voltage. However, this structure has the disadvantages of low power density, high control complexity, and high cost because it includes additional PFC circuit. Single-stage [9]-[11] AC-DC converters have received much attention because of their cost effectiveness, compact size, and simple control mechanism. Another approach is buck-boost topologies, such as general buck-boost converter, fly-back converter [12], single-ended primary inductance converter (SEPIC), and Ćuk converter, which could act as step-down transformers [13]. In particular, SEPIC converter can achieve high PF and reduce output voltage stress. However, the voltage stress of switch is still relatively high. In addition, the efficiency decreases, and the cost increases.

Although buck converters are not widely used, these converters can also be used as a PFC front end [14]-[17]. Buck converter maintains high efficiency because of low average input current and root mean square (RMS) current at low input voltage. However, a buck PFC converter has difficulty achieving high PF because of its crossover distortion of input current when the input voltage is lower than output voltage. Moreover, the occurrence of input current distortion promotes total harmonic distortions (THD). Conventional buck PFC converter has difficulty passing IEC61000-3-2 standards

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because of THD.

An effective method to improve PF of the buck PFC converter is to modify the structure. Two step-down converters are proposed in [18], which include an auxiliary fly-back stage. The stage uses the same switch as a buck converter, and an additional power switch is commutated at the line frequency. The distortion of the input current can be eliminated with auxiliary fly-back converter. However, an additional diode that leads to additional losses is inserted in the power loop when these two topologies operate in buck mode. The interleaved power converter that operates at the boundary conduction mode (BCM), which is proposed in [19], can be used to recover the distortion of input current. However, the additional coupled inductor complicates the structure, which makes this structure unsuitable for such an arrangement.

In this study, a pulse-assisting buck (PAB) PFC converter is designed. The envelope of input current of the proposed buck converter is quasi-sinusoidal when buck-boost topology is turned in discontinuous mode where the drive signal is provided by additional pulse during distortion time. The predominant drawback of buck PFC can be overcome by adding discontinuous conduction mode (DCM) operation during the distortion time to make the current continuous. The DCM operation of all single-switch topologies is most suitable for low-power applications [20]. The proposed PAB converter is suitable for step-down PFC front end of an AC-DC converter.

The detailed operation principle is illustrated in Section II, the circuit parameters design considerations are presented in Section III, and the results based on a 94 W prototype are shown in Section IV. A conclusion is presented in Section V.

II. OPERATION PRINCIPLE

The output bus voltage of a conventional buck converter that is connected to a 50Hz AC source and bridge rectifier is set at a level less than the peak AC voltage at the lowest line voltage. When the instantaneous AC input voltage is greater than the output bus voltage, the PFC stage is forward biased, and the current can be drawn from the AC input. However, when the instantaneous AC input voltage falls below the bus voltage level, the diode bridge rectifiers become reverse biased, and no power can be drawn from the AC line. This condition is called crossover distortion of the input current, as shown in Fig. 1. The conduction angle can be calculated from (1).

$$t_1 = \frac{1}{100\pi} \arcsin \frac{V_o}{V_{in}}, \quad t_2 = 0.01 - t_1. \quad (1)$$

A. Preliminary

For the proposed PAB converter, the PAB converter operates in BCM, which is same as the conventional buck converter, when the instantaneous AC input voltage is higher

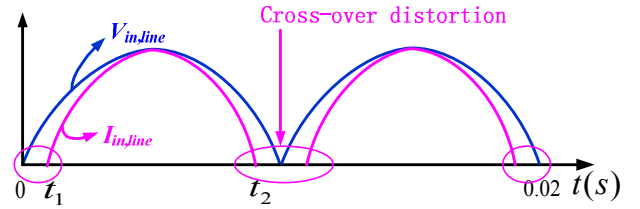


Fig. 1. Crossover distortion of the input current.

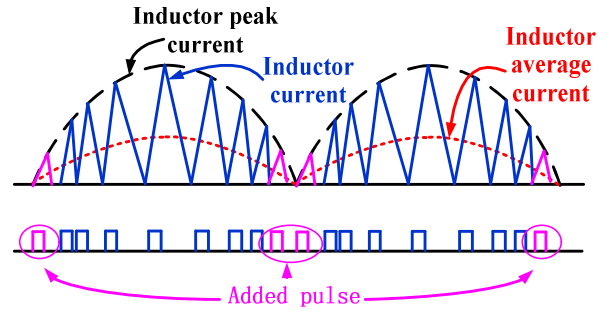


Fig. 2. Current waveform of the proposed converter.

than the output voltage [22]. When the input voltage is lower than the output voltage, the PAB converter operates in DCM, in which the gate drive voltage is provided by the PFC controller. Hence, the PF can be improved obviously and THD can be substantially eliminated based on preserving the merits of the conventional buck converter.

The current waveforms of the PAB converter are shown in Fig. 2. When the PAB buck converter operates in BCM, the positive edge of gate drive voltage is determined by zero current detection (ZCD) of the inductor current. When the converter operates in DCM during the distortion time, the turn-on instant is determined by the internal oscillator of PFC controller. The conduction of switch Q1 and Q2 in Fig. 3 is initiated by the oscillator of the controller in every beginning of a period.

B. Working Process

The converter operates in several stages during a sinusoidal period, as shown in Fig. 4.

1) *DCM*: When the magnitude of input voltage V_{in} is smaller than the output voltage V_o , the proposed converter operates in DCM. The switches Q1 and Q2 are switched on and off synchronously and controlled by internal pulse.

When Q1 and Q2 turn on, the proposed converter operates in Stage 1. The equivalent circuit is illustrated in Fig. 4(a). In this stage, inductor L is charged by V_{in} , and inductive current i_L increases during this stage.

When Q1 and Q2 turn off, the proposed converter operates in Stage 2. The equivalent circuit is illustrated in Fig. 4(b). In this stage, inductor L is discharged by V_o , and i_L decreases during this stage.

2) *BCM*: When the magnitude of V_{in} is greater than V_o , the proposed converter operates in BCM. The switch Q2 remains

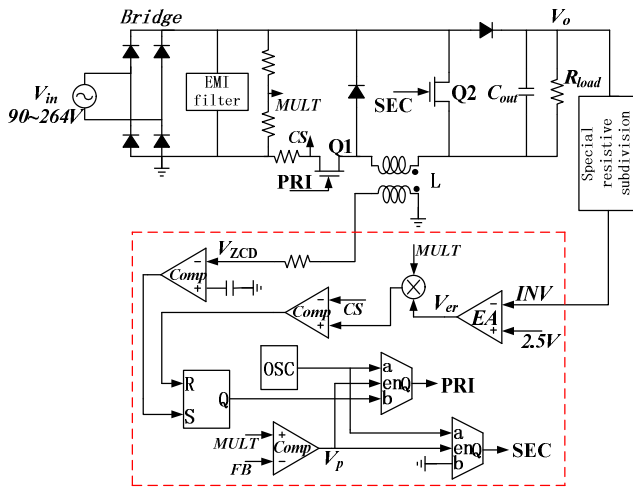


Fig. 3. Schematic of the PAB converter and its controller.

switched off, and switch Q1 is controlled by signal PRI by the PFC controller.

When Q1 turns on, the proposed converter operates in Stage 3. The equivalent circuit is illustrated in Fig. 4(c). In this stage, inductor L is charged by $V_{in}-V_o$, and i_L increases during this stage.

When Q1 turns off, the proposed converter operates in Stage 4. The equivalent circuit is illustrated in Fig. 4(d). In this stage, inductor L is discharged by V_o , and i_L decreases during this stage.

Based on the preceding analysis, the PFC controller is designed as shown in Fig. 3.

The input voltage V_{in} is detected and divided to obtain a signal $MULT$. Similarly, the output voltage V_o is represented by FB with the same ratio as that of $MULT$ representing V_{in} . Then, the control signal V_p can be calculated by comparing $MULT$ and FB . The signal V_p is high logic when $MULT$ is higher than FB and is low logic when $MULT$ is lower than FB . The control signal V_p is used to determine whether the converter operates in DCM or BCM.

The detected output signal INV is sent to the negative input of the error amplifier. The error between INV and the set reference voltage V_{ref} is amplified by the compensation networks, and then the amplified error signal V_{er} is achieved. The DC voltage signal V_{er} is applied to one input port of the multiplier, whereas another input signal of the multiplier is $MULT$. The waveform envelope of the output of the multiplier is a rectified sine wave. The output of the multiplier is used as a reference signal of the current comparator, and the output of the current comparator is used to control the peak current per cycle of the switch. When the voltage of the buck inductor is reversed, ZCD module opens the external switch. Thus, the circuit operates in BCM.

Two of the input signals of the selectors are the internal pulse and the output of the RS trigger, whereas other input signals of the selectors are the internal pulse and ground. The

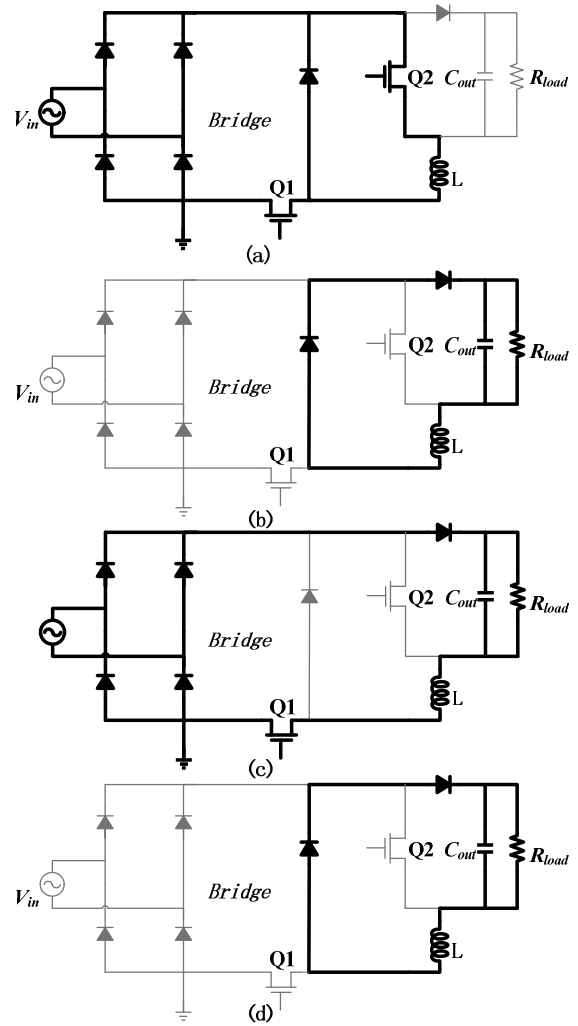


Fig. 4. Operating stages of the PAB converter.

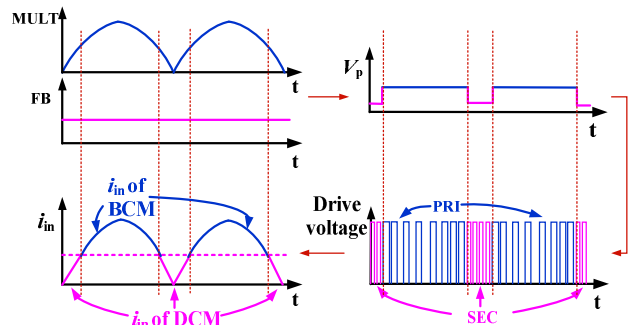


Fig. 5. Key waveforms of nodes $MULT$, FB , V_p , PRI , and SEC and i_{in} of PAB converter.

output signals PRI and SEC of the two selectors are the gate signal of Q1 and Q2, respectively.

The PAB converter operates in DCM controlled by an internal oscillator. The frequency of the internal pulse is f_s , and the duty cycle is D_0 during distortion time. The PAB converter operates in boundary mode during conduction time by using constant on-time (COT) control. The waveforms of

nodes *MULT*, *FB*, V_p , *PRI*, and *SEC* and of input current i_{in} are shown in Fig. 5.

The signal V_p determines different operation modes alternately per cycle by controlling the gate signals *PRI* and *SEC*. Different frequencies f_s of internal pulse result in the different performances of the PAB converter. The detailed optimization of frequency f_s and duty cycle D_0 during the distortion time is presented in Section III.

III. ANALYSIS OF THE PAB CONVERTER

Design considerations of the PAB converter controlled by the proposed PFC controller are presented in this section. All the calculations are based on a 94W prototypewith 90V to 264V universal AC input. The output voltage is set to 80V. The circuit described in this paper can easily obtain high PF. The following are the analyses of the input current and how the frequency and the duty cycle of internal pulse during the distortion time affect the performance of the circuit.

A. Current Analysis

According to the operating stage analysis shown in Fig.3, the characteristics of the PAB PFC converter can be derived. When the input voltage is lower than the output voltage in a half line cycle, the converter is equal to a DCM buck-boost converter. When the input voltage is higher than the output voltage, the PAB converter works like a BCM conventional buck converter. The input current in the half line cycle can be described as follows, whereas the conduct angle can be calculated from (1)

$$i_{in} = \begin{cases} D_{BCM} \cdot \frac{i_{pk,BCM}}{2}, & t_1 < t < t_2 \\ D_{DCM} \cdot \frac{i_{pk,DCM}}{2}, & (0 < t < t_1) \text{ and } (t_2 < t < 0.01) \end{cases} \quad (2)$$

where D_{BCM} and D_{DCM} are duty cycles in BCM and DCM, respectively. The peak value of the input current is $i_{pk,BCM}$ and $i_{pk,DCM}$ in BCM and DCM, respectively.

$$D_{BCM} = \frac{V_o}{V_{in} \cdot \sin(100\pi \cdot t)}, \quad D_{DCM} = D_0. \quad (3)$$

$$i_{pk,BCM} = \frac{V_{in} \cdot \sin(100\pi \cdot t) - V_o}{L} \cdot t_{on}, \quad (4)$$

$$i_{pk,DCM} = \frac{V_{in} \cdot \sin(100\pi \cdot t) \cdot D_0}{L \cdot f_s}.$$

The following is the final expression of the input current obtained by substituting (3) and (4) into (2):

$$i_{in} = \begin{cases} \frac{V_o}{V_{in} \cdot \sin(100\pi \cdot t)} \cdot \frac{V_{in} \cdot \sin(100\pi \cdot t) - V_o}{2 \cdot L} \cdot t_{on}, & t_1 < t < t_2 \\ V_{in} \cdot \sin(100\pi \cdot t) \cdot \frac{D_0^2}{2 \cdot L \cdot f_s}, & (0 < t < t_1) \text{ and } (t_2 < t < 0.01) \end{cases} \quad (5)$$

where t_{on} is the on-time of the primary switchQ2, which is nearly constant during the half line cycle. We introduce a factor, and replace D_0^2/f_s by $k \cdot t_{on}$ to simplify the calculation.

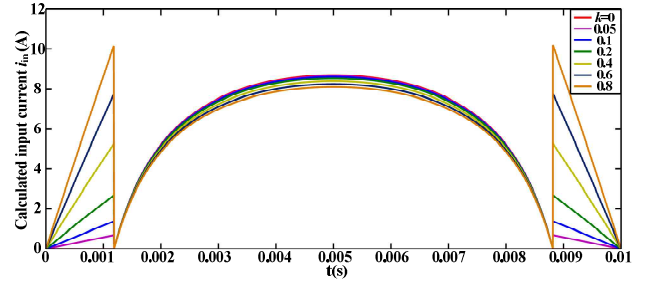


Fig. 6. Calculated input current with different factor k at 220V AC input.

We rewrite the expression of the input current as follows:

$$i_{in} = \begin{cases} \frac{V_o}{V_{in} \cdot \sin(100\pi \cdot t)} \cdot \frac{V_{in} \cdot \sin(100\pi \cdot t) - V_o}{2 \cdot L} \cdot t_{on}, & t_1 < t < t_2 \\ V_{in} \cdot \sin(100\pi \cdot t) \cdot \frac{k \cdot t_{on}}{2 \cdot L}, & (0 < t < t_1) \text{ and } (t_2 < t < 0.01) \end{cases} \quad (6)$$

According to the law of energy conservation, we can obtain the equation as follows:

$$\left(\int_0^{t_1} \frac{(V_{in} \cdot \sin(100\pi \cdot t))^2 \cdot k \cdot t_{on}}{2 \cdot L} dt + \int_{t_1}^{0.005} \frac{V_o \cdot (V_{in} \cdot \sin(100\pi \cdot t) - V_o) \cdot t_{on}}{2 \cdot L} dt \right) \cdot \eta = 0.005 \cdot P_o. \quad (7)$$

where t_{on} can be achieved as follows:

$$t_{on} = \frac{0.01 \cdot P_o}{\eta} \left/ \left(k \cdot \int_0^{t_1} \frac{(V_{in} \cdot \sin(100\pi \cdot t))^2}{L} dt + \int_{t_1}^{0.005} \frac{V_o \cdot (V_{in} \cdot \sin(100\pi \cdot t) - V_o)}{L} dt \right) \right. \quad (8)$$

Moreover,

$$k = \left(\frac{106 \cdot 0.01}{t_{on}} - \int_{t_1}^{0.005} \frac{(V_{in} \cdot \sin(100\pi \cdot t) - V_o) \cdot V_o}{L} dt \right) \left/ \int_0^{t_1} \frac{(V_{in} \cdot \sin(100\pi \cdot t))^2}{L} dt \right. \quad (9)$$

According to (6), the calculated input current in one cycle with different factor k at 220V AC input level is shown in Fig. 6. The results and discussion are shown in Section IV.

The preceding analysis indicates that the input current varies from different k and only the coefficient k in a certain range could enable the converter to meet the requirements. These conditions occur because the coefficient k is the function of D_0 and f_s . The selection of D_0 and f_s is analyzed in the next section.

B. PF Analysis and THD Analysis

A converter that maintains PF for over 0.9 must be designed in the same way as Energy Star does, which introduces a PF legislation of 0.9 at full load. From the preceding calculation, we can obtain the expression of PF as follows:

TABLE I
CALCULATED PF AND THD VERSUS k AT $V_{in} = 220V$ AC INPUT
COMPARED WITH IEC61000

k	PF	THD	MEET IEEE61000
0.02	0.9831	0.1861	YES
0.04	0.9847	0.1769	YES
0.06	0.9861	0.1683	YES
0.08	0.9874	0.1601	YES
0.1	0.9885	0.1527	YES
0.2	0.9918	0.1286	YES
0.4	0.9873	0.1608	YES
0.6	0.9699	0.2511	YES
0.9	0.9265	0.4062	NO
1	0.9091	0.4582	NO

$$PF = \frac{P_i}{V_{in} \cdot i_{rms}} \quad (10)$$

where i_{rms} is the RMS value of the input current that can be achieved as follows:

$$i_{rms} = \left(\frac{2}{0.01} \int_0^{t_1} \left(\frac{V_{in} \cdot \sin(100\pi \cdot t)}{2 \cdot L} \cdot k \cdot t_{on} \right)^2 dt + \frac{1}{0.01} \int_{t_1}^{t_2} \left(\frac{V_o \cdot V_{in} \cdot \sin(100\pi \cdot t) - V_o}{V_{in} \cdot \sin(100\pi \cdot t) \cdot 2 \cdot L} \cdot t_{on} \right)^2 dt \right)^{\frac{1}{2}} \quad (11)$$

Moreover, P_i is the input power in a cycle

$$P_i = \frac{1}{0.01} \cdot \left(2 \cdot \int_0^{t_1} \left(\frac{V_{in} \cdot \sin(100\pi \cdot t)}{2 \cdot L} \right)^2 \cdot k \cdot t_{on} dt + \int_{t_1}^{t_2} \frac{V_o \cdot (V_{in} \cdot \sin(100\pi \cdot t) - V_o)}{2 \cdot L} \cdot t_{on} dt \right) \quad (12)$$

The following expression of PF and THD are obtained by substituting (11) and (12) into (10):

$$PF = \frac{1}{0.01} \cdot \left(2 \cdot \int_0^{t_1} \left(\frac{V_{in} \cdot \sin(100\pi \cdot t)}{2 \cdot L} \right)^2 \cdot k \cdot t_{on} dt + \int_{t_1}^{t_2} \frac{V_o \cdot (V_{in} \cdot \sin(100\pi \cdot t) - V_o)}{2 \cdot L} \cdot t_{on} dt \right) / V_{in} / \left(\frac{2}{0.01} \int_0^{t_1} \left(\frac{V_{in} \cdot \sin(100\pi \cdot t)}{2 \cdot L} \cdot k \cdot t_{on} \right)^2 dt + \frac{1}{0.01} \int_{t_1}^{t_2} \left(\frac{V_o \cdot V_{in} \cdot \sin(100\pi \cdot t) - V_o}{2 \cdot L \cdot V_{in} \cdot \sin(100\pi \cdot t)} \cdot t_{on} \right)^2 dt \right)^{\frac{1}{2}} \quad (13)$$

$$THD = \sqrt{\frac{\cos^2(\varphi)}{PF^2} - 1} \quad (14)$$

According to (13) and (14), the corresponding values of PF and THD with different k at 220V and 50Hz AC input level are shown in Table I. The trend of PF and THD versus k is shown in Fig. 7.

When $k=0$, the PAB converter works as a conventional buck converter. Fig. 7 and Table I demonstrate that with the increase of k , PF increases and THD decreases. However, the value of k could not increase without limit in consideration of the distortion of the input current in a relatively large k .

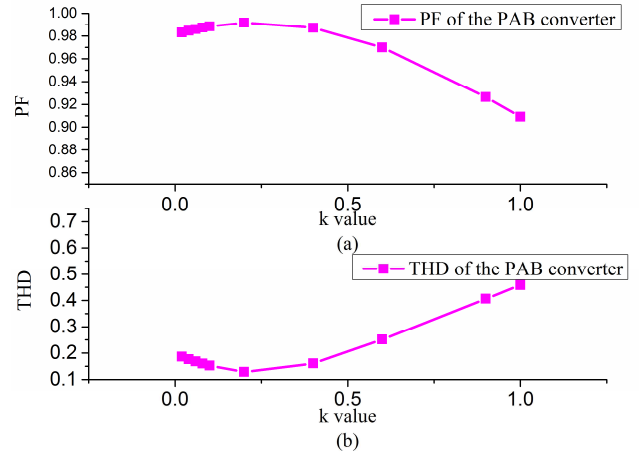


Fig. 7. (a) Trend of PF versus k . (b) Trend of THD versus k .

TABLE II
RELATIONSHIP BETWEEN k AND t_{on}

k	t_{on} (μ s)
0	5.13
0.02	5.12
0.04	5.11
0.06	5.10
0.08	5.09
0.1	5.08
0.4	4.94
0.9	4.73

The t_{on} s for different values of k are also included in Table II. t_{on} decreases gradually with the increase of k . In fact, t_{on} is nearly equal to the t_{on} of the conventional buck converter only in a case of small values of k , that is, below 0.1.

A small k (i.e., below 0.1) is a good choice to preserve the superiority of the buck converter and to consider some factors, such as PF and THD.

In this paper, t_{on} has a one-to-one correspondence with k . Thus, these two variables can be used as one constraint condition. According to the function $D_0^2 / f_s = k^* t_{on}$, D_0 and f_s are two independent parameters. Moreover, if one of them must be ensured, another must be known. For small k , we assume that the value of t_{on} is equal to that of the conventional buck converter according to the preceding analysis. For the buck converter without PAB technology, we can obtain the switching frequency function as follows:

$$f_s = \frac{1}{t_{on} + t_{off}} \quad (15)$$

$$t_{off} = \frac{i_{pk,BCM} \cdot L}{V_o} \quad (16)$$

where

$$P_o = \eta \cdot \int_{t_1}^{0.005} \frac{V_o \cdot (V_{in} \cdot \sin(100\pi \cdot t) - V_o)}{\pi \cdot L} \cdot t_{on} dt \quad (17)$$

Thus,

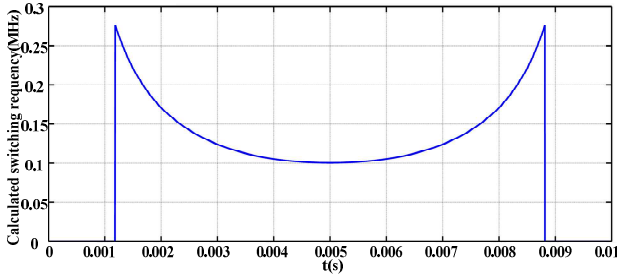


Fig. 8. Calculated switching frequency versus t of conventional buck converter.

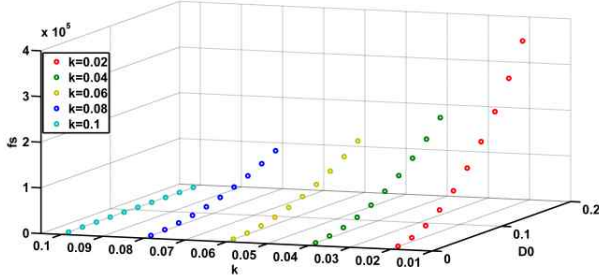


Fig. 9. Relationship between f_s and k , D_0 at 220V AC input.

$$\begin{aligned}
 f_s &= \frac{1}{t_{on} + t_{off}} \\
 &= \frac{1}{t_{on} + \frac{(V_{in} \cdot \sin(100\pi \cdot t) - V_o)}{V_o} \cdot t_{on}} \\
 &= \frac{V_o}{t_{on} \cdot V_{in} \cdot \sin(100\pi \cdot t)}.
 \end{aligned} \quad (18)$$

If the output voltage is designed at 80 V, the buck inductance is obtained as $L = 150 \mu\text{H}$. Fig.8 shows the calculated switching frequency versus the function of the phase angle in 220V and 50Hz AC input voltage process.

In this paper, k can be used to characterize the power transmission capacity of the circuit. Each value of k may correspond to a specific combination of different D_0 and f_s , as shown in Fig. 9.

The range of operating frequency illustrated in Fig.8 is approximately 0.1MHz to 0.27Mhz. Therefore, Fig.9 does not show the situation where k is greater than 0.1 because when k is greater than 0.1, f_s gradually decreases to a value smaller than the minimum value shown in Fig.8.

The selection of D_0 and f_s must not only meet requirements of the operating frequency of the circuit but also consider the output level of voltage and power. In view of these two factors, the coefficient k is set to 0.08 according to Fig.9, and f_s is set to the lowest frequency (0.1Mhz) in Fig.8. D_0 is set to 0.2 as a result of the function $D_0^2 / f_s = k \cdot t_{on}$. Then, the validation is based on these values, which proves that this solution is one of the feasible solutions.

IV. RESULTS AND DISCUSSION

The model derived from the previous section uses a 94W,

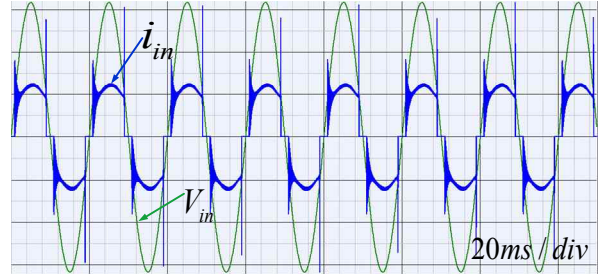


Fig. 10. Input voltage and input current waveforms of the conventional buck PFC converter.

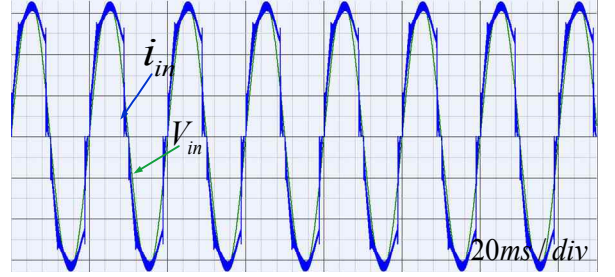


Fig. 11. Input voltage and input current waveforms of the PAB PFC converter.

TABLE III
PF AND EFFICIENCY FROM 90V INPUT TO 264V AC INPUT OF THE PAB CONVERTER

$V_{in}(V)$	PF(%)	$\eta(\%)$
90	94.19	93.16
100	97.37	93.26
115	99.02	93.65
132	98.18	94.12
180	98.46	95.79
200	98.48	96.01
230	98.31	96.12
264	98.01	96.19

220 V AC input, 80V DC output PAB PFC converter as an example. Moreover, the converter can be used as the universal input ($V_{in} = 90\text{V}$ to 264 V) front end.

Input voltage and input current waveforms of the conventional buck PFC converter are shown in Fig.10. Input voltage and input current waveforms of the PAB PFC converter are shown in Fig. 11. We can see that the strategy restores the input current during distortion time.

The PF and efficiency from 90V input to 264V input of the PAB converter are listed in Table III. The buck PFC maintains a high efficiency of approximately 96% when the input voltage is larger than 115V. The slight drop of efficiency is the result of the implementation of the control circuit with discrete ICs. Thus far, no dedicated controller IC for the buck PFC is available.

Efficiency versus load at 110 V AC input and 230 V AC input is presented in Table IV. Table IV demonstrates that the buck PFC maintains a high efficiency across the load range from 100% to 25% of the full load.

TABLE IV
EFFICIENCY VERSUS LOAD AT 110V AC INPUT AND 230V AC

INPUT		
$P_o(\%)$	$\eta(\%)@110V_{rms}$	$\eta(\%)@230V_{rms}$
100	93.24	96.12
75	95.59	95.75
50	93.39	95.16
25	91.27	94.64

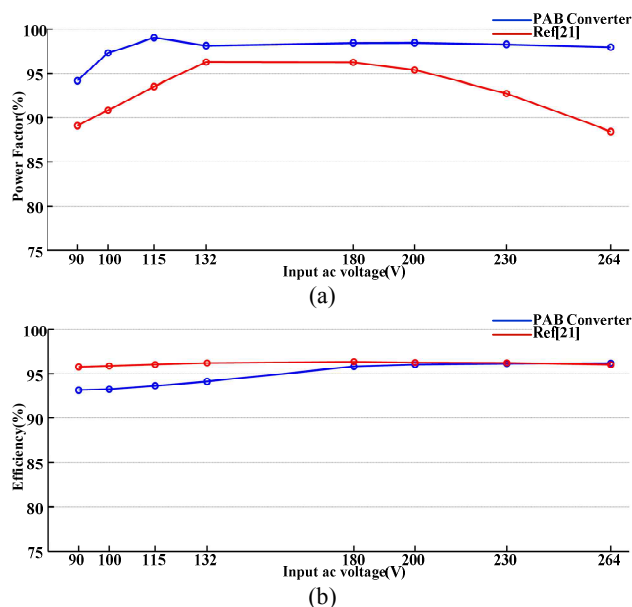


Fig. 12. (a) Measured PF of PAB converter. (b) Measured efficiency of PAB converter.

The efficiency and PF of the PAB PFC converter is compared with those of a previously proposed converter of the same type as [21] in Fig. 12. The PAB converter has a higher PF particularly under low input line voltage and high line voltage conditions. Moreover, the efficiency of the PAB converter has a good performance under high input line voltage. The efficiency of the PAB converter is slightly deteriorated compared with that of the prior converter under low input line voltage conditions. The added two diodes and a switch contribute to the total loss.

Fig. 13 shows the THD performance comparison between the PAB PFC converter and the conventional buck converter, which has the same parameters with those of the PAB converter but without pulse-assisting technique.

To compare with IEC61000-3-2 Class C limits, the vertical axis of Fig. 13 is set as the value of $I_{ac}(n)$, where $I_{ac}(n)$ is the n-order harmonic content of the input current i_{in} , and IEC(n) represents the n-order harmonic current limit of IEC61000-3-2 Class C. For example, 110V AC input voltage and 230V AC input voltage are needed to represent normal low line and normal high line, respectively. The harmonic performance of the PAB converter meets the IEC61000-3-2 Class C requirement under both voltages, whereas the conventional buck without pulse-assisting technique cannot

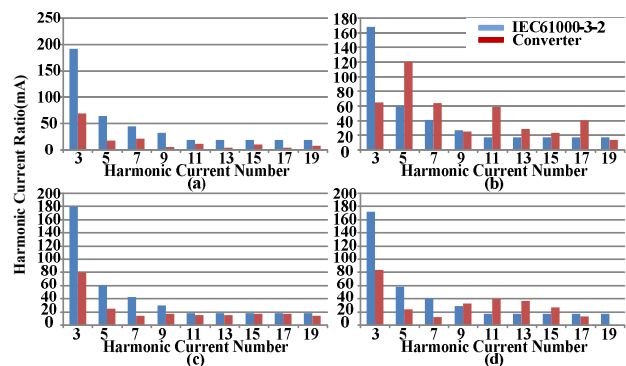


Fig. 13. THD performance comparison between the PAB PFC converter and the conventional buck converter. (a) $I_{ac}(n)$ compared with IEC(n) of PAB converter at 110V AC input. (b) $I_{ac}(n)$ compared with IEC(n) of conventional converter at 110V AC input. (c) $I_{ac}(n)$ compared with IEC(n) of PAB converter at 230V AC input. (d) $I_{ac}(n)$ compared with IEC(n) of conventional converter at 230V AC input.

meet the requirement of both voltages. In addition, the PAB converter performs effectively under normal high line.

V. CONCLUSION

According to the design considerations given in the previous sections, a 94W, 80V output, universal input ($V_{in}=90$ V to 264 V) quasi COT-controlled buck PFC prototype is produced. The IC is based on L6561 with the addition of an oscillator, a voltage subdivision structure, a comparator, and two selectors to control the PAB converter. The improved PF and THD can approach the ideal values compared with the calculated PF and THD under different selections of k factor.

The PAB PFC maintains PF of approximately 98% at nominal high line and approximately 96% at nominal low line. In addition, the PAB PFC maintains an efficiency of 98% at nominal high line and approximately 96% at nominal low line. The PAB converter achieves high efficiency across a load range from 100% to 25% of full load, and the input current harmonics can meet the IEC61000-3-2 Class C standard within the universal input voltage range. In addition, according to the preceding data, the PAB converter performs well at normal high line voltage, but it could meet the requirements at normal low line voltage.

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