Implementation of a Sliding Mode Controller for Single Ended Primary Inductor Converter

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Abstract

This paper presents the regulation of the output voltage and inductor currents in a Single Ended Primary Inductor Converter (SEPIC), operating in the continuous conduction mode (CCM) using a sliding mode controller. Owing to the time varying nature of the SEPIC converter, designing a feedback controller is a challenging task. In order to improve the dynamic performance of the SEPIC, a Sliding Mode Controller (SMC) is developed. The developed SMC is designed by using a state space average model. The performance of the developed controller with the SEPIC converter is validated at different working conditions through Matlab simulations. It is also compared with the performance while using a PI controller. The results show that the designed controller gives very good output voltage regulation under different operating conditions such as a varying input voltage, changes in the load and component variations. A 48V, 46W experimental setup for has been developed in an analog platform to validate the performance of the proposed SMC.

Key words: Converter, Dynamic, Linear, Regulation, SEPIC, SMC

I. INTRODUCTION

A DC-to-DC converter is a device that accepts a DC input voltage at one level and converts it to a DC output voltage of another level. Among the DC-DC converters, the SEPIC has unique features like a non-inverted output voltage, and its output is greater than, less than, or equal to its input voltage. Hence, the SEPIC is used for many applications such as hybrid vehicles, UPS, industrial applications, communication equipment, portable electronics, etc. [1].

The SEPIC exhibits complex dynamic behavior due to its nonlinear nature. This results from the repeated switching operation but there is still exists room for the development of a controller to improve the performance of the SEPIC [2]. In many studies, attempts have been made to implement various control methods such as PI, PID, Fuzzy, posicast controllers, etc. for the SEPIC. A PI controller is capable of providing good static and dynamic responses. A PID controller is used for SEPIC control but has poor capability in dealing with system

uncertainty and the presence of a high overshoot in the output response [3]. The posicast controller with a feedback structure has been applied to deal with the overshoot in the system step response, the sensitivity to parameters uncertainty and to eliminate the over shoot in the output response [4]. A Fuzzy logic controller for the SEPIC converter has been adopted with a SMC to reduce the chattering phenomena but it performs better only in a variable frequency [5]. SEPIC converter modeling has been discussed. However, only two sliding surfaces of the inductor current and output voltage are considered. The second inductor current and SEPIC coupling capacitor voltage are not considered for the sliding control [6].

A sliding mode controller for the SEPIC is proposed in this paper in order to ensure the stability under any operating conditions, better static and dynamic performances under input voltage disturbances, load changes and component variations. In sliding mode control, a state trajectory moves back and forth around a certain average surface in the state space. Four sliding variables are considered in this paper since the SEPIC is a fourth order system. The SMC control technique offers several advantages such as stability even for a large supply and load variations, robustness, good dynamic response and simple implementation. Its capabilities result in improved performance when compared to classical control techniques.

In this paper, a sliding mode controller for a SEPIC converter operating in the continuous conduction mode is proposed. The state space model for the control SEPIC is derived because there are several advantages to the state space model when compared to other models [7]. In this paper, the state space model is adopted. A detailed discussion of the stability condition of the SMC for the SEPIC is presented. The performance of the SMC is evaluated in terms of output voltage regulation under different operating conditions such as startup transients, line variations, load variations, steady state conditions and component variations. The performance of the SMC versus a PI controller is evaluated in a simulation in terms of robustness and stability. The proposed SMC for the SEPIC is implemented experimentally in an analog platform to validate the results.

This paper is organized as follows: In Section II, a description of the operation and a mathematical model of the SEPIC converter based on the state space technique is presented. The design of the SMC for the SEPIC is illustrated in section III. The design computation of the SEPIC circuit components and the controller gains are explained in section IV. Simulation results of the system using both the SMC and a PI controller using MATLAB SIMULINK under various conditions are discussed in section V. In section VI, the experimental results of the SEPIC using the SMC under various conditions are given. Finally conclusions are presented in Section VII.

II. SEPIC CONVERTER

A SEPIC is a type of DC-DC converter which converts input voltage to an output voltage which can be more, less, or same. The switch of the SEPIC is controlled by varying the duty cycle. This enables close and open conditions. A SEPIC is like a buck-boost converter. However, it has the unique feature of giving a non-inverted output. This means that the output is always the same polarity as the input. A series capacitor is used to couple the energy from the input to the output. The SEPIC can respond quickly to a short-circuit condition, and it works as a true shutdown mode when the switch is turned off and its output drops to 0V following a fairly hefty transient dump of charge [10].

The SEPIC is useful in applications in which the voltage can be above or below that of the regulator's intended output. The SEPIC transfers energy through the switching operation between the capacitors and the inductors. This is done in order to convert from one voltage to another. The amount of energy is controlled by switch S, which is a transistor such as a MOSFET, IGBT, etc. MOSFET offer a much higher input impedance and a lower voltage stress and do not require biasing resistors. In addition, MOSFET switching can be controlled by differences in voltage rather than a current.

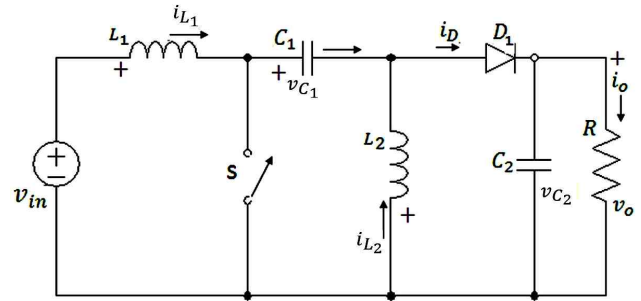There are various modeling methods available such as the
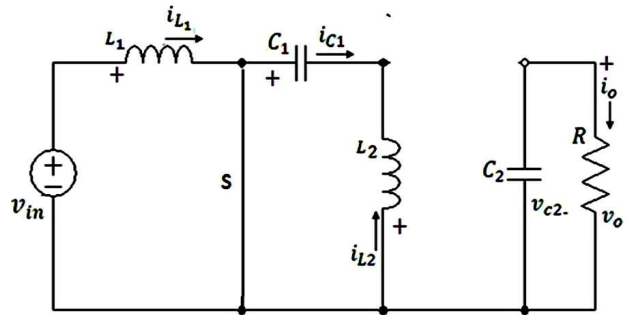

Fig. 1. Basic SEPIC converter.

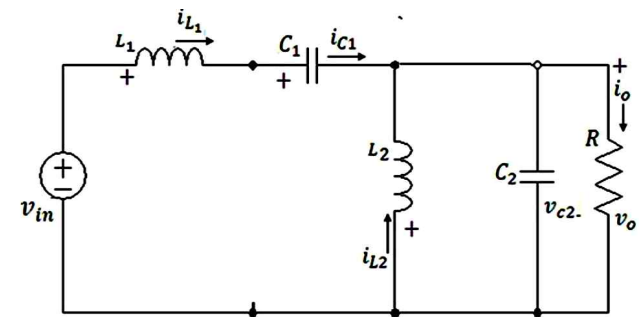Fig. 2. SEPIC converter during switch ON.

Fig. 3. SEPIC converter during switch OFF.

signal flow graph, the state space average and the small signal model. In the proposed controller, the state space averaging method is adopted. This Control method with a SMC for the SEPIC converter is to resolve the problems previously pointed. Therefore, it is proposed to design a SEPIC operated in a CCM.

A. SEPIC and its Mathematical Model

A power circuit diagram of the SEPIC is shown in Fig. 1. It includes a DC input supply voltage v_{in} , capacitors C_1 and C_2 inductors L_1 and L_2 a switch S (MOSFET), a diode $\underline{D_1}$ and a load resistance R. It is assumed that the components are ideal and that the SEPIC operates in the CCM.

Fig. 2 and Fig. 3 show the modes of operation of the SEPIC. In Fig. 2, when switch S is closed, the diode is reverse biased and open, inductor L_1 is occupied by the source voltage v_{in}, while the L_2 charges capacitor C_1, and the polarity of the inductor current and capacitor is shown in Fig.

3. The current i_{L_1} increases at a rate of:

$$\frac{di_{L_1}}{dt} = \frac{v_{in}}{L_1}, 0 \leq t \leq dT \tag{1}$$

$$v_{in} = v_{c_1} \tag{1a}$$

Where v_{c_1} is the voltage across capacitor C_1. In Fig. 3, when the switch is open, diode D_1 is forward biased and closed, inductor L_1 charges capacitor C_1, inductor L_2 discharges and C_2 is charging. At this time, the equation can be obtained as:

$$i_{in} = i_{L_1} \tag{2}$$

$$i_{L_{2a}} = i_{Da} = i_o \tag{3}$$

where i_{Da} is the average current of diode D_1, and i_o is the output current. When the SEPIC is operating in the CCM [8], [9], the voltage conversion ratio of the SEPIC can be obtained from the volt second balance of inductor L_1 in one switching period as expressed by:

$$\frac{v_o}{v_{in}} = \frac{d}{1-d} \tag{4}$$

where d is the duty cycle, and v_o is the output voltage of the SEPIC converter.

B. Mathematical Modeling of the SEPIC

In this paper the state space representation is applied. It gives several advantages when compared with other methods. These are its ability to handle the system easily with multiple inputs and outputs. The system model includes the internal state variables as well as the output variable. The model directly provides a time-domain solution, which ultimately is the thing of interest. The form of the solution is the same as that for a single 1st-order differential equation. The effect of the initial conditions can be easily incorporated into the solution and the matrix modeling is very efficient from a computational standpoint for computer implementation.

The state variables of the SEPIC (x_1, x_2, x_3, x_4) are considered as currents i_{L_1} and i_{L_2} and voltages v_{c_1} and v_{c_2} respectively when the switch is closed. The state space equation can be obtained as:

$$\begin{cases} \dot{x}_1 = -\dfrac{v_{in}}{L_1} \\[2mm] \dot{x}_2 = \dfrac{v_{c_1}}{L_2} \\[2mm] \dot{x}_3 = -\dfrac{i_{L_2}}{C_1} \\[2mm] \dot{x}_4 = -\dfrac{v_{C_2}}{RC_2} \end{cases} \tag{5}$$

$$\frac{d}{dt}\begin{bmatrix} i_{L_1} \\ i_{L_2} \\ v_{C_1} \\ v_{C_2} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{L_2} & 0 \\ 0 & \frac{-1}{C_1} & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{RC_2} \end{bmatrix}\begin{bmatrix} i_{L_1} \\ i_{L_2} \\ v_{C_1} \\ v_{C_2} \end{bmatrix} + \begin{bmatrix} \frac{-1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} v_{in} \tag{6}$$

During off as shown in Fig. 3.

$$\begin{cases} \dot{x}_1 = -\dfrac{v_{C_1}}{L_1} - \dfrac{v_{C_2}}{L_1} + \dfrac{v_{in}}{L_1} \\[2mm] \dot{x}_2 = -\dfrac{v_{C_2}}{L_2} \\[2mm] \dot{x}_3 = \dfrac{i_{L_1}}{C_1} \\[2mm] \dot{x}_4 = \dfrac{i_{L_1}}{C_2} + \dfrac{i_{L_2}}{C_2} - \dfrac{v_{C_2}}{RC_2} \end{cases} \tag{7}$$

$$\frac{d}{dt}\begin{bmatrix} i_{L_1} \\ i_{L_2} \\ v_{C_1} \\ v_{C_2} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{-1}{L_1} & \frac{-1}{L_1} \\ 0 & 0 & 0 & \frac{-1}{L_2} \\ \frac{1}{C_1} & 0 & 0 & 0 \\ \frac{1}{C_2} & \frac{1}{C_2} & 0 & \frac{-1}{RC_2} \end{bmatrix}\begin{bmatrix} i_{L_1} \\ i_{L_2} \\ v_{C_1} \\ v_{C_2} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} v_{in} \tag{7a}$$

The state space averaging technique,

$$\frac{d}{dt}\begin{bmatrix} i_{L_1} \\ i_{L_2} \\ v_{C_1} \\ v_{C_2} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{-1}{L_1} & \frac{-1}{L_1} \\ 0 & 0 & 0 & \frac{-1}{L_2} \\ \frac{1}{C_1} & 0 & 0 & 0 \\ \frac{1}{C_2} & \frac{1}{C_2} & 0 & \frac{-1}{RC_2} \end{bmatrix}\begin{bmatrix} i_{L_1} \\ i_{L_2} \\ v_{C_1} \\ v_{C_2} \end{bmatrix} + \begin{bmatrix} \frac{v_{C_1}+v_{C_2}-2v_{in}}{L_1} \\ \frac{v_{C_1}+v_{C_2}}{L_2} \\ \frac{-i_{L_1}-i_{L_2}}{C_1} \\ \frac{-i_{L_1}-i_{L_2}}{C_2} \end{bmatrix}\gamma + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} v_{in} \tag{8}$$

$$\dot{X} = AX + B\gamma + C \tag{8a}$$

where γ is the status of the switches, and $X, \dot{X}$ are the state variables of currents i_{L_1} and i_{L_2}, and voltages v_{c_1} and v_{c_2} their derivatives, respectively.

$$\gamma = \begin{cases} 1 \rightarrow S \rightarrow ON \\ 0 \rightarrow S \rightarrow OFF \end{cases} \tag{9}$$

III. DESIGN OF A SMC FOR THE SEPIC

A. Basic Requirement of a SMC

Sensing of all of the state variables and the generation of suitable references for all of them are the basic requirements of a SMC. According to the principles of SMC, the capacitor

voltages v_{c_1} and v_{c_2} are made to follow their references as dependably as possible. It is difficult to measure the inductor current reference since it usually depends on the load power demand supply voltage and the load voltage. To overcome this problem in implementation, the state variable error for the inductor current $\left(i_{L_1} - i_{L_1 ref}, i_{L_2} - i_{L_2 ref}\right)$ can be obtained from the feedback variables i_{L_1} and i_{L_2} by means of a high-pass filter under the assumption that their low-frequency component is automatically adapted to the actual operation of the converter. As such, it is found that only the high-frequency component of this variable is needed for control. The system order will be increased due to the high pass filter which can heavily alter the SEPIC converter dynamics. In order to avoid this problem, the cutoff frequency of the high-pass filter must be suitably lower than the switching frequency to pass the ripple. However, it should be more able to tolerate the quick response of the SEPIC converter.

In the design of the converter, some assumptions are made and three factors such as ideal power switches, a power supply free of DC ripple and a converter operating at a high-switching frequency are considered. To have a good response in the output voltage and current of the SEPIC, a sliding surface equation in the state space, which is expressed by a linear combination of state-variable errors ε (the respective differences between the feedback reference current/voltage and the feedback actual current/voltage) has to be chosen optimally.

$$S(i_{L_1}, i_{L_2}, v_{c_1}, v_{c_2}) = k_1 \varepsilon_1 + k_2 \varepsilon_2 + k_3 \varepsilon_3 + k_4 \varepsilon_4 \quad (9a)$$

where the coefficients, k_1, k_2, k_3 and k_4 are the proper gains; ε_1 and ε_2 are the current feedback current errors; and ε_3 and ε_4 are the feedback voltage errors as:

$$
\begin{aligned}
\varepsilon_1 &= i_{L_1} - i_{L_1 ref} \\
\varepsilon_2 &= i_{L_2} - i_{L_2 ref} \\
\varepsilon_3 &= v_{C_1} - v_{C_1 ref} \\
\varepsilon_3 &= v_{C_2} - v_{C_2 ref}
\end{aligned}
\quad (10)
$$

By substituting (10) in (9a), the following equation is obtained:

$$s(i_{L_1}, i_{L2}, v_{C_1}, v_{C_2}) = k_1(i_{L_1} - i_{L_1 ref}) + k_2(i_{L_2} - i_{L_2 ref}) + k_3(v_{C_1} - v_{C_1 ref}) + k_4(v_{C_2} - v_{C_2 1 ref}) \quad (11)$$

The signal $s(i_{L_1}, i_{L2}, v_{C_1}, v_{C_2})$ is generated using (9a) while a conventional hysteresis modulator generates the gate pulses to the MOSFET switch. The complete control
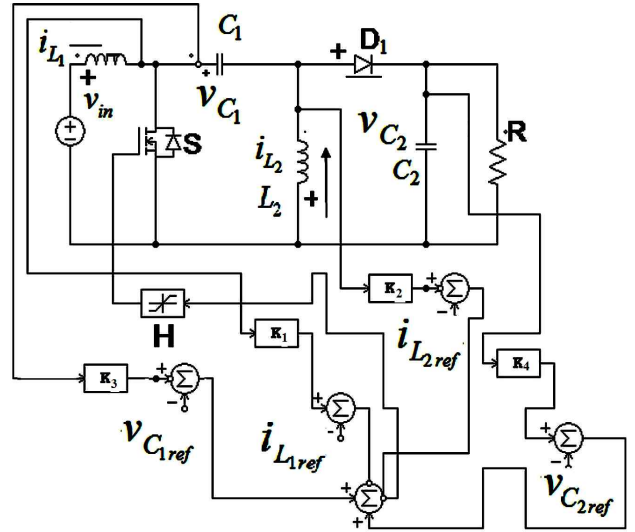

Fig. 4. Principle scheme of SMC for SEPIC converter.

arrangement of the SEPIC is shown in Fig. 4. The status of switch (γ) is controlled by hysteresis block H, which aims to minimize the error of the variables $i_{L_1}, i_{L_2}, v_{c_1}$ and v_{c_2}.

The system response is determined by the circuit parameters and coefficients k_1, k_2, k_3 and k_4. With a proper selection of these coefficients under any operating conditions, a high control strength, permanence and a quick SEPIC output response can be achieved.

B. Selection of the Control Parameters

Once the SEPIC parameters are selected, the inductances L_1 and L_2 are designed from specified input and output current ripples, capacitors C_1 and C_2 are designed so as to limit the output voltage ripple in the case of fast and large load variations, and the maximum switching frequency is selected based on the proposed converter ratings and switch type. The system behavior is completely determined by the coefficients k_1, k_2, k_3 and k_4 which must be selected so as to satisfy the existing condition and to ensure stability and a fast response, even under large supply and load variations.

According to the variable structure system, the SEPIC converter equations can best be written in the following form:

$$\dot{x} = Ax + B\gamma + D \quad (12)$$

Where, x represents the vector quantity error of the state-variable and is given by:

$$\dot{x} = x - X^* \quad (13)$$

where $X^* = \begin{bmatrix} i_{L_1 ref} & i_{L_2 ref} & v_{C_1 ref} & v_{C_2 ref} \end{bmatrix}^{\mathrm{T}}$ is the vector of the references. The substitution of (13) into (7) results in:

$$D = AX^* + C \quad (14)$$

$$D = \begin{bmatrix} 0 & 0 & \dfrac{-1}{L_1} & \dfrac{-1}{L_1} \\ 0 & 0 & 0 & \dfrac{-1}{L_2} \\ \dfrac{1}{C_1} & 0 & 0 & 0 \\ \dfrac{1}{C_2} & \dfrac{1}{C_2} & 0 & \dfrac{-1}{RC_2} \end{bmatrix} \begin{bmatrix} i_{L_{1ref}} \\ i_{L_{2ref}} \\ v_{C_1 ref} \\ v_{C_2 ref} \end{bmatrix} + \begin{bmatrix} \dfrac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} v_{in} \tag{15}$$

$$D = \begin{bmatrix} -\dfrac{v_{C_{1ref}}}{L_1} - \dfrac{v_{C_{2ref}}}{L_1} + \dfrac{v_{in}}{L_1} \\ \dfrac{-v_{C_{2ref}}}{L_2} \\ \dfrac{i_{L_{1ref}}}{C_1} \\ \dfrac{i_{L_{1ref}}}{C_2} + \dfrac{i_{L_{2ref}}}{C_2} - \dfrac{v_{C_{2ref}}}{RC_2} \end{bmatrix} \tag{15a}$$

By substituting (13) into (11), the sliding function can be rewritten in the following form:

$$S(x) = k_1 x_1 + k_2 x_2 + k_3 x_3 + k_4 x_4 = k^T x \tag{16}$$

where $k^T = \begin{bmatrix} k_1 & k_2 & k_3 & k_4 \end{bmatrix}$ and $x = \begin{bmatrix} x_1 & x_2 & x_3 & x_4 \end{bmatrix}^T$. The condition of the sliding mode requires that all of the state trajectories near the surface be directed toward the sliding surface. The SMC can implement the system conditions to remain near the sliding plane in the proper operation of the switch of the SEPIC converter. To make the system state move toward the switching surface the following conditions are essential and sufficient:

$$\begin{cases} \dot{s}(x) < 0, if \ s(x) > 0 \\ \dot{s}(x) > 0, if \ s(x) < 0 \end{cases} \tag{17}$$

The SMC is obtained by means of the following feedback control approach, which associates to the status of a switch with the value of s (x):

$$\gamma = \begin{cases} 0 \ for \ s(x) > 0 \\ 1 \ for \ s(x) < 0 \end{cases} \tag{18}$$

The condition (17) can be expressed in the form:

$$\dot{s}(x) = k^T A x + k^T D < 0, s(x) > 0 \tag{19}$$

$$\dot{s}(x) = k^T A x + k^T B + k^T D < 0, s(x) < 0 \tag{20}$$

For the simulation, by assuming that the error variable x_i suitably smaller than the references X^*, (19) and (20) can be rewritten as:
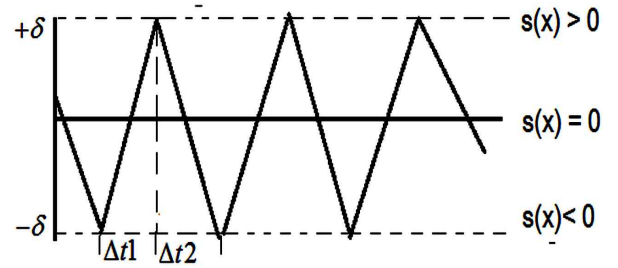

Fig. 5. Phase plane trajectory.

$$k^T D < 0, s(x) > 0 \tag{21}$$

$$k^T B + k^T D < 0, s(x) < 0 \tag{22}$$

By substituting the matrices B and D into (21) and (22), the following is obtained:

$$\frac{k_1}{L_1}[-v_{C_{1ref}} - v_{C_{2ref}} + v_{in}] + \frac{k_2}{L_2}[-v_{C_{2ref}}] + \frac{k_3}{C_1}[i_{L_{1ref}}] + \frac{k_4}{RC_2}[Ri_{L_{1ref}} + Ri_{L_{2ref}} - v_{C_{2ref}}] < 0 \tag{23}$$

$$-\frac{k_1}{L_1}[v_{in}] + \frac{k_2}{L_2}[v_{C_{1ref}}] + \frac{k_3}{C_1}[i_{L_{2ref}}] - \frac{k_4}{RC_2}[v_{C_{2ref}}] > 0 \tag{24}$$

This condition is satisfied if the inequalities (23) and (24) are true. Finally, it is necessary to guarantee that the designed sliding plane is reached for all of the initial states. If the sliding mode exists in a system defined by (14), it is sufficient that the coefficients k_1, k_2, k_3 and k_4 are non-negative.

C. Switching Frequency

A practical system cannot switch at an infinite frequency [11]. The operating range of the average switching frequency of the hysteresis relay varies from 50 kHz to 450 kHz. From this operating range, the optimum value of the chosen average switching frequency is 100 kHz and its corresponding band is 0.5. A practical relay has always exhibited the hysteresis model by:

$$\gamma = \begin{cases} 0, & \text{when } s > +\delta \text{ or} \\ & \text{when } \dot{s} < 0 \text{ and } |s| < \delta \\ 1, & \text{when } s < -\delta \text{ or} \\ & \text{when } \dot{s} > 0 \text{ and } |s| > \delta \end{cases} \tag{25}$$

where, δ is an arbitrarily small positive quantity, and 2δ is the amount of hysteresis in s(x). The hysteresis characteristic makes it impossible to switch the control on the surface s(x) = 0. As a result, switching occurs on line S = δ with a frequency depending on the slopes of i_{L_1} and i_{L_2}. This hysteresis causes phase plane trajectory oscillations with a width 2δ, near the surfaces (x) =0, as shown in Fig. 5.

Note that Fig. 5 simply confirms that in Δt_1, the function s(x) must increase from - δ to δ (s > 0), while in Δt_2 it

decreases from $+ \delta$ to δ (s < 0). The switching frequency equation is obtained by considering that the state trajectory is invariable near the sliding surface s(x) =0, and is given by:

$$fs = \frac{1}{\Delta t_1 + \Delta t_2} \qquad (26)$$

where Δt_1 is the conduction time of switch s, and Δt_2 is the off time of switch s. The conduction time Δt_1 is derived from (24) as follows:

$$\Delta t_1 = \frac{2\delta}{-\frac{k_1}{L_1}[v_{in}] + \frac{k_2}{L_2}[v_{C_{1ref}}] + \frac{k_3}{C_1}[i_{L_{2ref}}] - \frac{k_4}{RC_2}[v_{C_{2ref}}]} \qquad (27)$$

The off time Δt_2 is derived from (23) and is given by:

$$\Delta t_2 = \frac{-2\delta}{\frac{k_1}{L_1}[-v_{C_{1ref}} - v_{C_{2ref}} + v_{in}] + \frac{k_2}{L_2}[-v_{C_{2ref}}] + \frac{k_3}{C_1}[i_{L_{1ref}}] + \frac{k_4}{RC_2}[Ri_{L_{1ref}} + Ri_{L_{2ref}} - v_{C_{2ref}}]} \qquad (28)$$

The maximum value of the switching frequency is obtained by substituting (27) and (28) into (26) with the assumption that the converter is operating under no load $i_{L_{1ref(max)}} = 0$ and $1/R = 0$ and that the output voltage reference crosses its maximum value $v_{C_{2ref(max)}}$. The maximum switching frequency is obtained as:

$$f_s = \frac{k_1 v_{in}}{2\delta L_1}\left(1 - \frac{v_{in}}{v_{C_{1ref(max)}} + v_{C_{2ref(max)}}}\right) \qquad (29)$$

D. Duty Cycle

The duty cycle d is defined by the ratio between the conduction time of switch s and the switch period time, as represented by:

$$d = \frac{\Delta t_1}{\Delta t_1 + \Delta t_2} \qquad (30)$$

Considering the SMC, the instantaneous control, the ratio between the output and the input voltage must satisfy the fundamental relations under any working condition.

$$\frac{v_o}{v_{in}} = \frac{d}{1-d} \qquad (31)$$

It is essential to make a note that the switching frequency and the inductor current ripple depend on the reference voltage, the capacitor voltages v_{c_1} and v_{c_2}, and the inductor currents i_{L_1} and i_{L_2}. It is important to determine the circuit

parameters and coefficients of k_1, k_2, k_3 and k_4 that agree with the desirable values for a maximum inductor current ripple, a maximum capacitor ripple, a maximum switching frequency, stability, and a fast response under any operating conditions.

IV. CALCULATIONS OF THE COMPONENTS AND THE CONTROLLER PARAMETERS

The aim of this section is to use the previously deduced equations to calculate the component values and controller parameters for the SEPIC.

A. Calculation of v_{c_2}

From (30) and for simulation simplicity, an output voltage is chosen to produce a duty cycle close to 0.59. The output reference voltage v_o is taken as 48 V as mentioned in Table I, and a variation of the duty cycle between $d_{min} = 0.3$ and $d_{max} = 0.9$ is expected. The value of $v_{c_{2ref\,max}}$ is found to be 132V by an open loop simulation.

B. Determination of Ratio K_1/L_1 and K_2/L_2

Substituting v_{in}, $v_{c_{1ref\,max}}$, $v_{c_{2ref\,max}}$ and the duty cycle = 0.3 into (29) results in k_1/L_1 and k_2/L_2 = 5442.47 since the inductor values are equal.

C. Determination of the Ratios K_3/C_1 and K_4/C_2

From (27) and (28) and by selecting $i_{L_{1ref}} = i_{L_{1ref(max)}} = 4.41$A the obtained conditions are $1751 < k_3/C_1 < 277533$ and $1208 < k_4/C_2 < 278433$. There are some degrees of freedom in choosing the ratios of k_3/C_1 and k_4/C_2. In this controller, the ratios k_3/C_1 and k_4/C_2 are tuning parameters. It is recommended that the ratios k_3/C_1 and k_4/C_2 be chosen so that they agree with the required levels of stability and response speed. The ratios k_3/C_1 and k_4/C_2 are chosen by an iterative procedure (the ratio is modified until the transient response is satisfactory), and they are verified by a simulation. Finally, the optimum tuned adopted value for the ratios k_3/C_1 and k_4/C_2 is 7579.

D. Calculation of L_1 and L_2

A rule of thumb is to use 20% to 40 % of the inductor ripple current. 30% of the inductor ripple current was considered in this paper. The maximum inductor current ripple is chosen to be equal to 30% of the maximum average inductor current and $L_1 = 110\mu H$, which is obtained from (29). The Inductor L_1 is equal to L_2.

E. Calculation of C_1 and C_2

The maximum capacitor ripple voltages Δv_{C_1} and $\Delta v_{C_{2max}}$ are chosen to be equal to 0.5 % of the maximum capacitor voltage, $C_1 = 5\mu F$ and $C_2 = 300\mu F$.

TABLE I

PARAMETRS OF SEPIC

Parameter	Symbol	Value
Input Voltage	v_{in}	12V
Output Voltage	v_0	48V
Inductors	L_1 and L_2 .	110μH
Capacitors	C_1 and C_2	5μF,300μF
Switching frequency	fs	100kHz
Load resistance	R	50Ω
Range of duty ratio	d	0.3 to0.9

F. Coefficient Values of k_1, k_2, k_3 and k_4

Having decided on the values of the ratio k_1/L_1 and k_2/L_2 and the inductor, the value of k_1 and k_2 are obtained as 0.599. Similarly, the values $k_3 = 0.0358$ and $k_4 = 0.227$ are computed using the ratios k_3/C_1, k_4/C_2, C_1 and C_2

V.   SIMULATION RESULTS

The main purpose of this section is to discuss the simulation studies of the SEPIC with three different control methods. The simulations are performed on the SEPIC's circuits with the parameters listed in Table I, using Matlab/Simulink under the following conditions:

1. Without a feedback controller.
2. With a PI controller.
3. With a SMC controller

A. SEPIC without a Feedback Controller

The SEPIC is simulated using a pulse generator which is connected to the MOSFET gate to give a pulse input with a frequency of 100 KHz. It is found that in the absence of a feedback controller, the output voltage is not maintained at 48V. The input voltage is varied from 9 V to 15 V and the output voltage and output current are shown in Table II. The load is varied from 40 Ω to 60 Ω and the output voltage and output current are shown in Table III.

B. SEPIC with a PI Controller

The Ziegler-Nichols rules are applied for determining the values of the parameters kp and ki [12]. A PI controller with the settings of $K_p = 0.1205$ and ki = 0.00016 obtained for the given SEPIC. The validation of the system performance is done for the following five conditions:

1) Startup transients
2) Line variations
3) Load variations
4) Steady state variations
5) Component variations

1) Startup Transients: Fig. 7 shows the dynamic behavior at startup for the output voltage of SEPIC for the following input voltages v_{in}: 9V, 12V, 15V. The reference value v_o is set at 48V and the resistance is 50 Ω. It can be ascertained that

TABLE II

SIMULATED RESULTS OF THE VOLTAGE AND CURRENT OF SEPIC
WITHOUT CONTROLLER FOR VARIOUS INPUT VOLTAGES

Input Voltage(V)	v_0(V)	i_o(A)	i_{in}(A)
9V	44.14	1.471	5.994
12V	45.47	0.9094	3.673
15V	45.74	0.7623	3.092

TABLE III

SIMULATED RESULTS OF THE VOLTAGE AND CURRENT OF SEPIC
WITHOUT CONTROLLER FOR VARIOUS LOADS

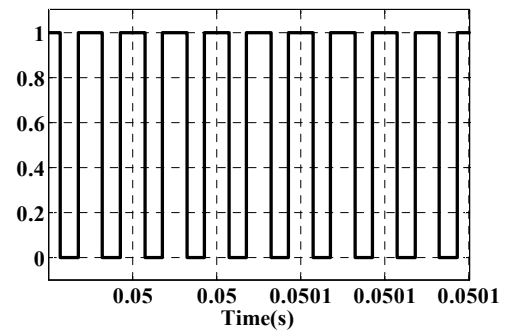| Load Ω	v_0(V)	i_o(A)	i_{in}(A)
40	44.14	1.471	5.994
50	45.47	0.9094	3.673
60	45.74	0.7623	3.092

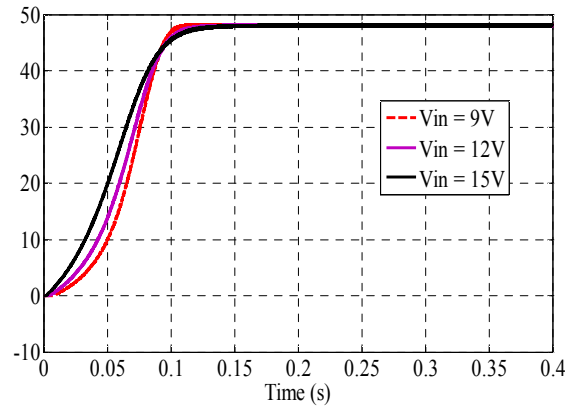Fig. 6. Response of gate pulse of SEPIC without controller for input voltage v_{in} = 12 V and d = 0.56.

Fig. 7. Dynamic behavior at startup for the average output voltage of SEPIC at R = 50Ω for PI controller.

the output voltage of the SEPIC has a little overshoot and a settling time of 0.008 s for v_{in} = 15 V, whereas for v_{in} = 12 V and v_{in} = 09 V, there are negligible overshoots and a settling time of 0.012 s and 0.015 s for the proposed SMC as shown in Fig. 8, respectively.

Fig. 9 shows the dynamic behavior of the output voltage of the SEPIC converter at startup for the following load resistances: 40 Ω, 50 Ω and 60 Ω. The input voltage is kept at 12V. It can be seen that the output voltage of the SEPIC has a negligible overshoot and a low settling time for various loads
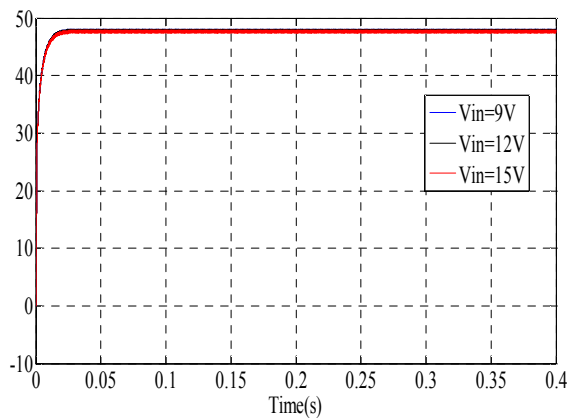
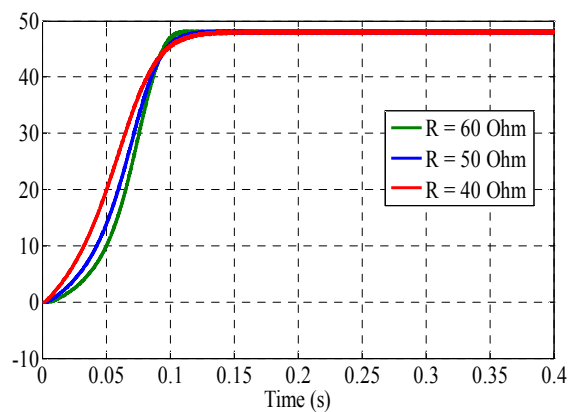Fig. 8. Dynamic behavior at startup for the average output voltage of SEPIC at R 50Ω for SMC.

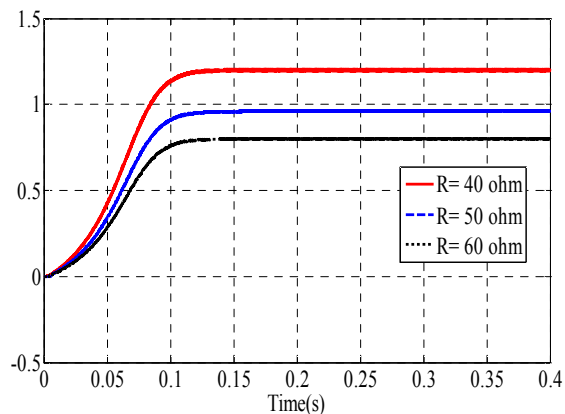Fig. 9. Dynamic behavior at startup for the average output voltage of SEPIC.

Fig. 10. Response of average output current of SEPIC in startup for various load resistances.

Fig. 10 shows the dynamic behavior at startup for the output current of the modules for the following load resistances: 40 Ω, 50 Ω and 60 Ω. It can be seen that the output current of the SEPIC for R = 40Ω, R = 50Ω, and R = 60Ω has a negligible overshoot and settling times of 0.13s, 0.125s and 0.121s, with the designed SMC. Table IV lists the simulated results of the average output current and voltage of the SEPIC with the different controllers for various input voltages and load resistances in the startup region. It can be

TABLE IV
OUTPUT VOLTAGE /CURRENT OF SEPIC FOR VARIOUS INPUT
VOLTAGES AND LOADS AT STEADY STATE

Input Voltage (V)	Voltage (steady state Values)		
	Without feedback	PI	SMC
	v_0 (V)	v_0 (V)	v_0 (V)
9V	33.92	48.08	48
12V	45.47	48.01	48
15V	57.04	48	48
Load R(Ω)	Current (steady state Values)		
	Without feedback	PI	SMC
	i_o (A)	i_o (A)	i_o (A)
40Ω	1.271	1.21	1.2
50Ω	0.9094	0.9624	0.96
60Ω	0.7623	0.81	0.8
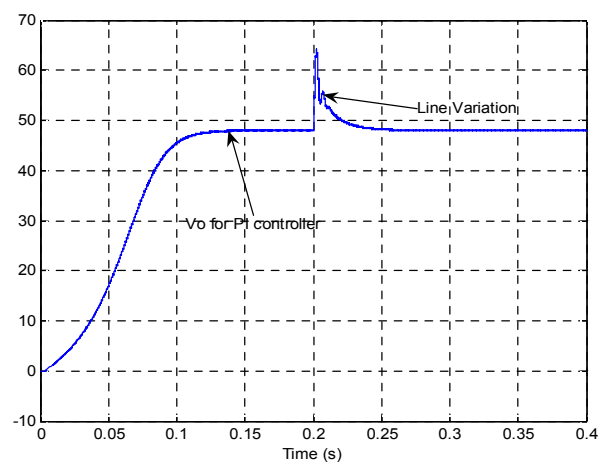
Fig. 11. Response of the average output voltage of the SEPIC converter using the PI controller for the step change in Vin (from12V-15V at t=0.2s).

determined that the potential regulation of the SEPIC using the designed SMC shows excellent performance when compared with a conventional PI controller.

2) Line Variations: Fig. 11 and Fig. 12 show the responses of the average output voltage of the SEPIC converter using a PI controller and a SMC for an input voltage step change from v_{in} = 12 V to v_{in} = 15 V (+25% line variation) at 0.2s. It can be seen that the output voltage of the SEPIC using the SMC has a maximum overshoot of 8 V (16.6%) and a settling time of 0.04 s, while the output voltage of the SEPIC using the PI controller has a severely affected overshoot of 17V (35.4%) and a longer settling time of 0.05s.

Fig. 13(a) and 13(b) show the responses of the average output voltage of the SEPIC using both a PI controller and a SMC for an input voltage step change from 12 V to 9 V (-25% line variation) at 0.2s. It can be seen that the output voltage of the SEPIC using the SMC has a maximum variation of 8 V (16.6%) and a settling time of 0.07 s, while the output voltage of the SEPIC using the PI controller has a
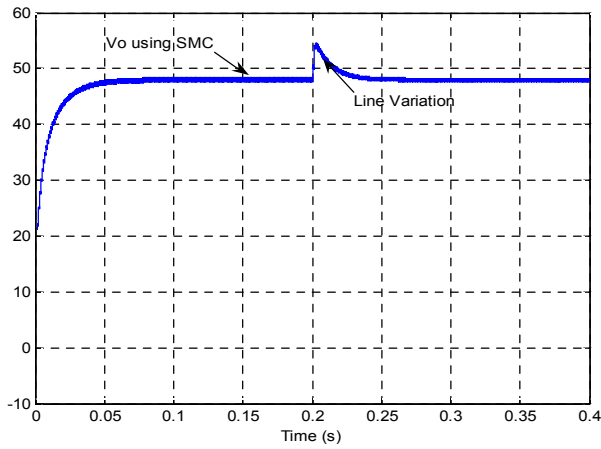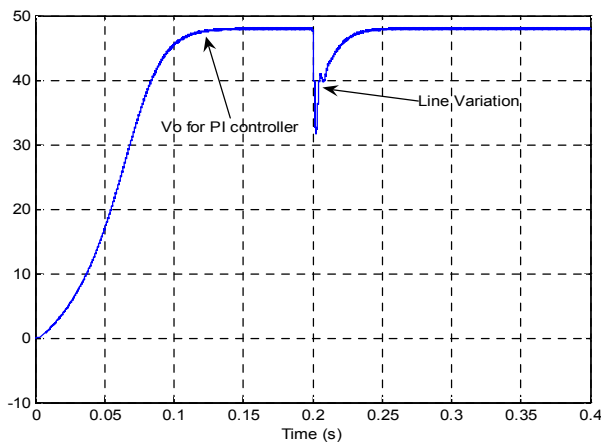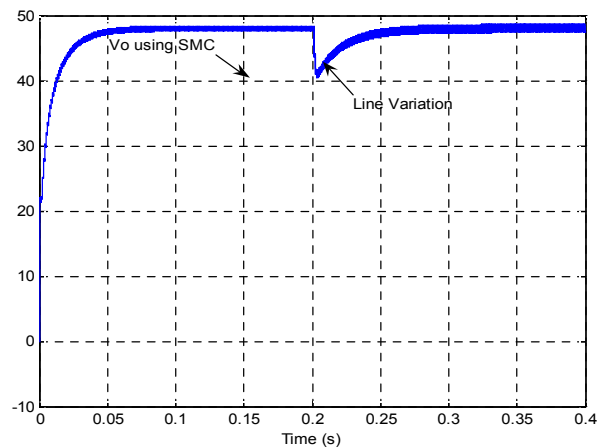
Fig. 12. Response of the average output voltage of the SEPIC converter using SMC controller for the step change in Vin (from 12V-15V at time 0.2s).
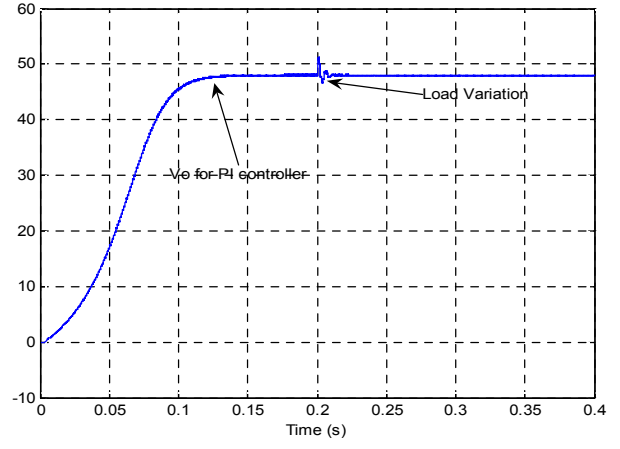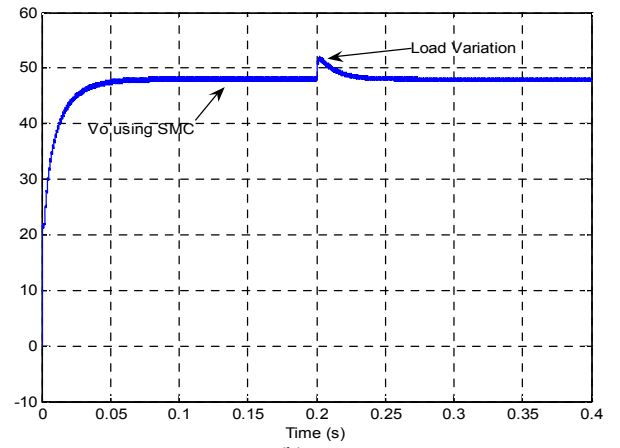

(a)

(b)

Fig. 13. (a) Response of the average output voltage of the SEPIC converter using a PI controller (12V-9V). (b) Response of the average output voltage of the SEPIC converter using SMC Controller (12V-9V) at t =0.2s.

maximum variation of 16 V (33.3%) and a longer settling time of 0.08 s.

3) Load Variations: Fig. 14(a) shows the response of the

(a)

(b)

Fig.14. (a) Response of output voltage of SEPIC when load value takes a step change from 50Ω to 60Ω at t=02s. (b) Response of output voltage when load value takes a step change from 50Ω to 60Ω in SMC in t = 0.2.

output voltage of the SEPIC when the load value takes a step change from 50 Ω to 60 Ω while using a PI controller at the time t = 0.2s. Fig 14(b) shows the response of the output voltage of the SEPIC when the load value takes a step change from 50 Ω to 60 Ω while using a SMC at time t = 0.2s. It can be seen that the output voltage of the SMC has a small overshoot of 6 V (12.5%) with a settling time of 0.06 s, while the output voltage of the SEPIC using the PI controller has a maximum overshoot of 6 V (12.5%) and a longer settling time of 0.07 s.

Fig. 15 and Fig. 16 show the response of the output voltage of the SEPIC using both a PI controller and a SMC for a load step change from 50 Ω to 40 Ω (-20% load variations) at 0.2s. It can be ascertained that the output voltage of the SEPIC using the SMC has a maximum variation of 6 V (12.5%) with a settling time of 0.07s, while the output voltage of the SEPIC using the PI controller has a variation of 8 V (16.6%) and a settling time of 0.07 s.

4) Steady State Regions: Fig. 17(a) and Fig. 17(b) show the instantaneous output voltage of the SEPIC in the steady state
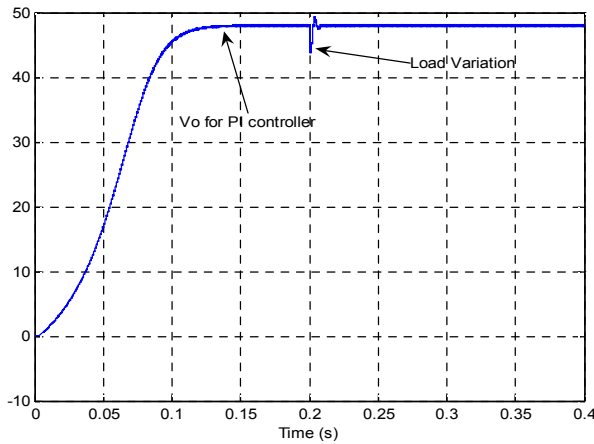
Fig. 15. Response of the output voltage of SEPIC using the PI controller for a load step change from 50Ω to 40Ω (+20% load variations) at time = 0.2s.
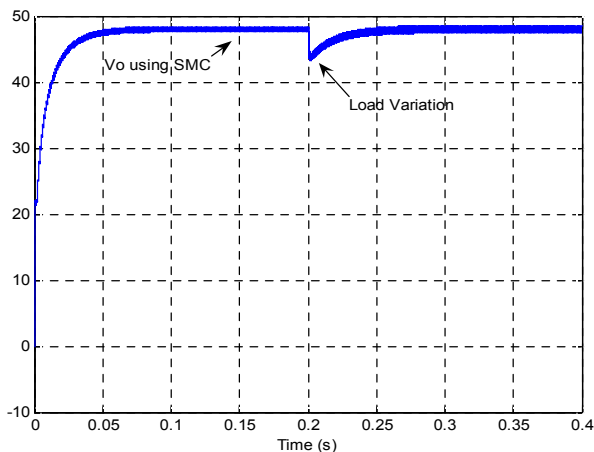

Fig. 16. Response of the output voltage of SEPIC the SMC for a load step change from 50Ω to 40Ω (+20% load variations) at time = 0.2s.

while using a PI and a SMC, respectively. It is evident that the output voltage ripple is very small, about 0.24 V.

Fig. 17(c) and Fig. 17(d) show the instantaneous current of the SEPIC in the steady state using a PI and a SMC, respectively. It is evident from the figures that ripple current is 0.005 A when using the PI.

5) Circuit Components Variations: Fig. 18(a) and Fig. 18(b) represent the response of the output voltage of the SEPIC using both a SMC and a PI controller when the inductor L_1 varies from 110μH to 150μH at time=0.2 s. It can be seen that the change does not influence the SEPIC converter's behavior due to the proficient design of the SMC in comparison with the conventional PI controller.
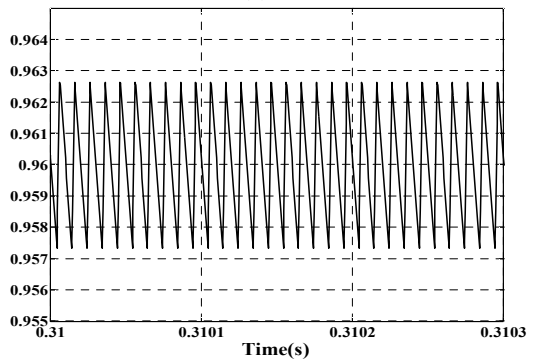
Fig. 18(c) and Fig. 18(d) represent the response of the output voltage of the SEPIC using both a PI and a SMC controller for the variation in the C_2 capacitor values from 300μF to 350μF. It can be seen that the SMC is very successful in suppressing the effect of the capacitance variation, except for a negligible output voltage ripple with a
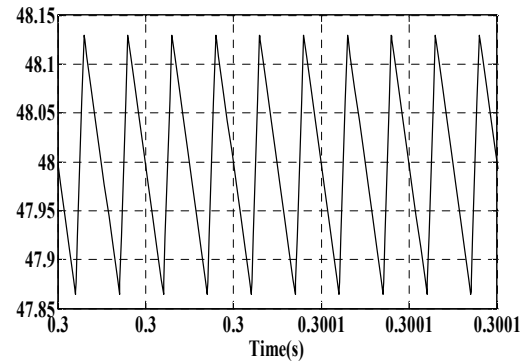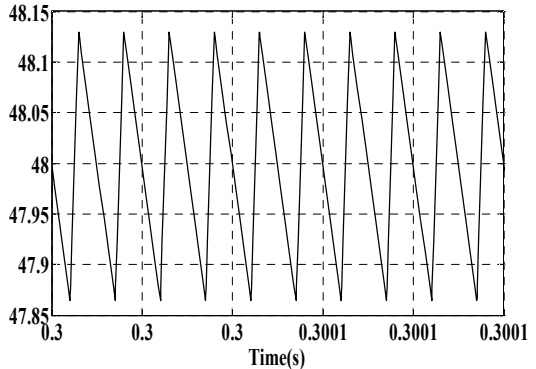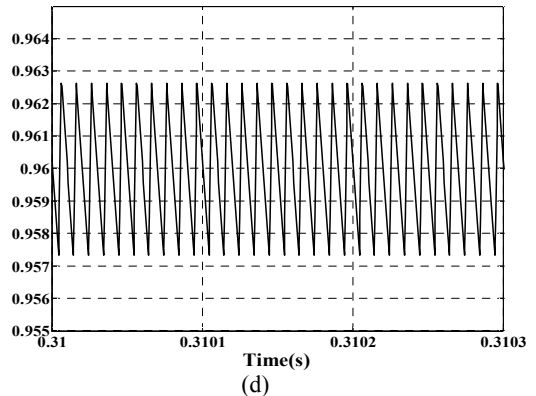

Fig. 17. (a) The instantaneous output voltage of SEPIC in the steady state using the PI controller. (b) Instantaneous output voltage of SEPIC in the steady state using the SMC. (c) Instantaneous output current of SEPIC in the steady state using the PI controller. (d) Instantaneous output inductor current of SEPIC in the steady state using the SMC controller.
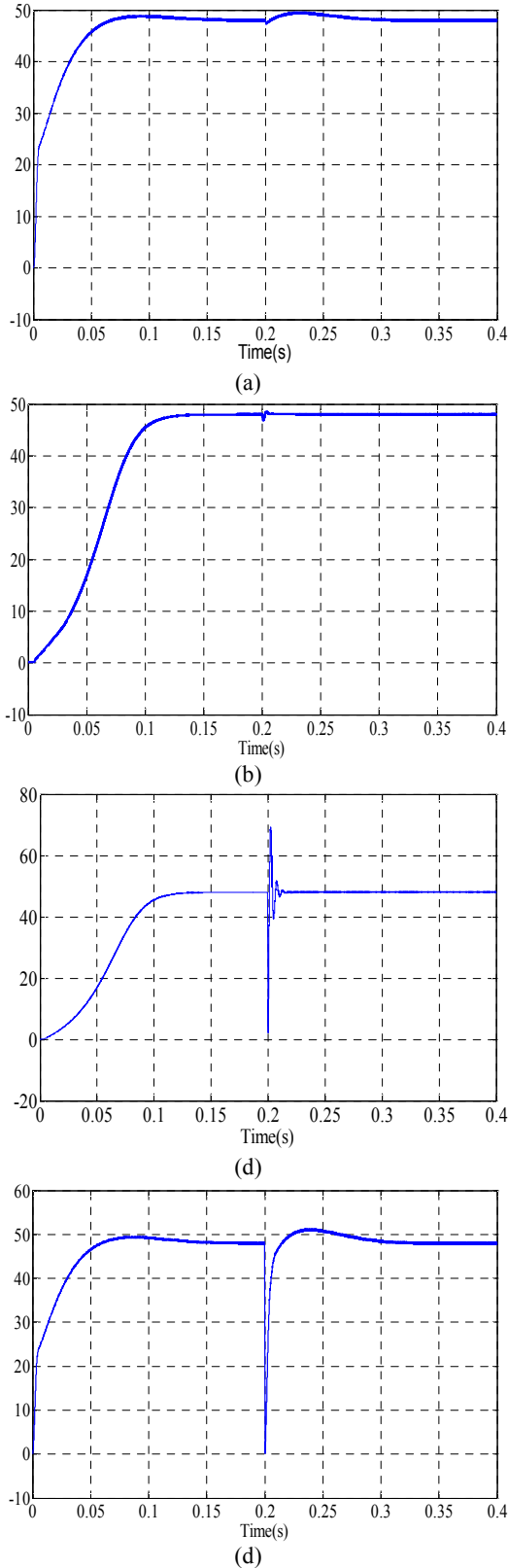
(a)

(b)

(d)

(d)

Fig. 18. (a) Response SMC on Inductor L_1 Variations from 110μH TO 150 μH at t = 0.2s. (b) Response PI on Inductor L_1 Variations from 110μH TO 150 μH at t = 0.2s. (c) Response PI on Capacitor C_2 Variations from 300μF TO 350 μF. (d) Response SMC on Capacitor C_2 Variations from 300 μF TO 350 μF.
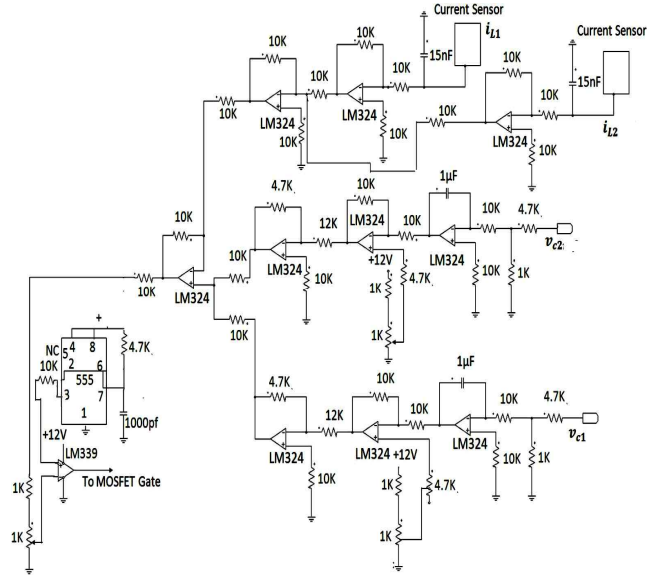

Fig. 19. SEPIC Control circuit using SMC at analog platform.

quick settling time and a proper current distribution, in comparison with the conventional PI controller.

VI. EXPERIMENTAL SETUP

A prototype SEPIC converter is built whose specifications are given in Table V. The system performance is verified for different conditions.

Fig. 19 shows a photograph of the designed laboratory type SMC controlled SEPIC. The SEPIC is designed using the proposed SMC controller and tested in the laboratory. It gives good performance during transient conditions such as line, load and parameter variations. This is similar to the simulated results obtained from MATLAB-Simulink.

   1)   Line variations
   2)   Load variations
   3)   Steady state region variations
   4)   Circuit component variations

The prototype SEPIC using the SMC circuits is shown in Fig. 19. The SMC controller is built using analog ICs LM324, LM339 and a 555 Timer. The parameters of the controller are the same as those calculated in section 4 and they are given below:

$k_1 = k_2 = 0.599$, $k_3 = 0.378$, $k_4 = 0.227$ and d = 0.3

The designed SMC is implemented in an analog platform as shown in Fig. 19. The capacitor voltages v_{c_1} and v_{c_2}, and inductor currents i_{L_1} and i_{L_2} of the SEPIC are measured and then compared with reference signals by using an LM324 that gives error signals. The inductor current error signal is further processed through a high pass filter for the purpose of

TABLE V
LIST OF COMPONENTS

S.L No	Components	Specification/ Part Value
1	MOSFET	IRF832
2	Diode	30DF4L
3	L_1 and L_2	110µH
4	C_1 and C_2	5µF and 300µF
5	IC	LM324
6	IC	555, LM339
7	Current Sensor	WCS1600

filtering out the low frequency component of the current as the controller allows only high frequency signals. Then, the output of all of the SMC signals are summed up and compared using an LM339 to generate a pulse width modulated (PWM) gate drive control signal for the MOSFET. Using the SMC, the switching frequency of the gate pulse is varied to regulate both the output current and the voltage, and to improve the dynamic performance of the SEPIC.

1) Line Variations: Initially an input voltage of 12V is given to the SEPIC and the output voltage reference value is set at 48V in the SMC controller. Fig. 20 shows the experimental response of the output voltage of the SEPIC using the SMC for an input voltage step change from 12V to 15V (+25% line variation) at time 0.2s. It is found from the experimental response that the output voltage of the SEPIC using the SMC has a maximum overshoot of 7.5V (15.6%) and settling time of 0.04 s.

Fig. 21 shows the experimental response of the output voltage of the SEPIC using the SMC for an input voltage step changes from 12V to 9V (-25% line variation) at time t = 0.2s. It can be seen that from the experimental response of the output voltage of the SEPIC using the SMC has a maximum variation of 6 V (12.5%) and settling time of 0.07s.

2) Load Variations: Fig. 22 shows the experimental response of the output voltage of the SEPIC using the SMC for a load step change from 50 Ω to 60 Ω (+20% load variation) at time t = 0.2s. It can be seen from the experimental results that the output voltage of the SEPIC using the SMC has and overshoot of 6V (12.5%) with a quick settling time of 0.06s.

Fig. 23 shows the experimental response of the output voltage of the SEPIC using the SMC for a load step change from 50Ω to 40Ω (-20% load variations) at time 0.2s. It can be seen that from the experimental results that the output voltage of the SEPIC using the SMC has a small overshoot of 6V (12.5%) and a quick settling time of 0.07s.

Table VI shows the experimental and simulation results of the output voltage and current of the SEPIC with the developed sliding mode controller for various input voltages and load resistances. From Table VI, it can be clearly seen
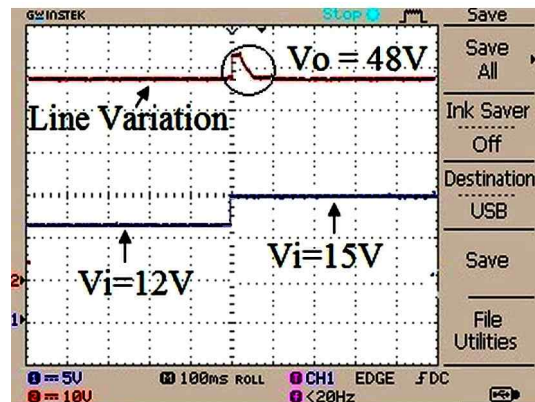

Fig. 20. Response of the SEPIC using the SMC for an input voltage changes from 12 to 15V.
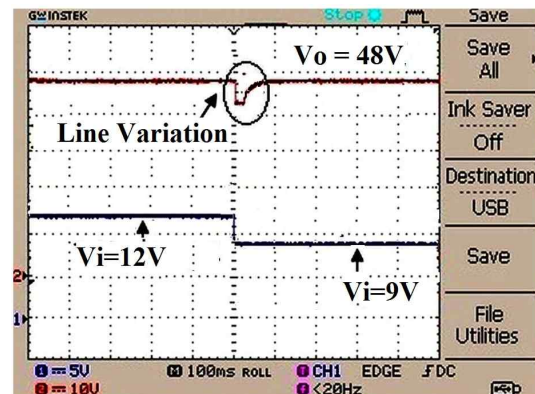

Fig. 21. Response of the SEPIC using the SMC for an input voltage changes from 12V to 9V.
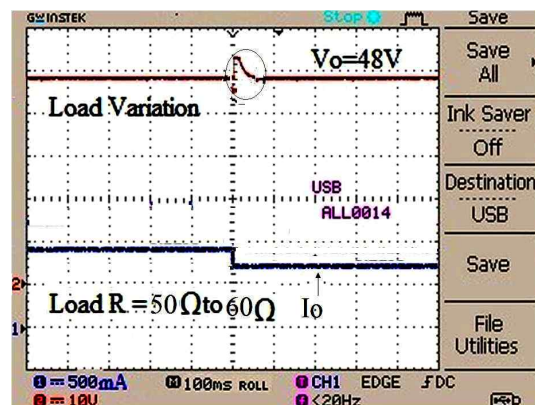

Fig. 22. Response of the SEPIC using the SMC for load changes from50 Ω to 60Ω.

that the voltage regulation and current of the SEPIC using the designed SMC show excellent performance with a tolerance of 0.01V (0.02%) or 0.01A (0.008%).

3) Steady State Region: Fig. 24 shows the experimental instantaneous output current of the SEPIC in the steady state region using the SMC. It is evident from this figure that the peak to peak current ripple is 0.03A.
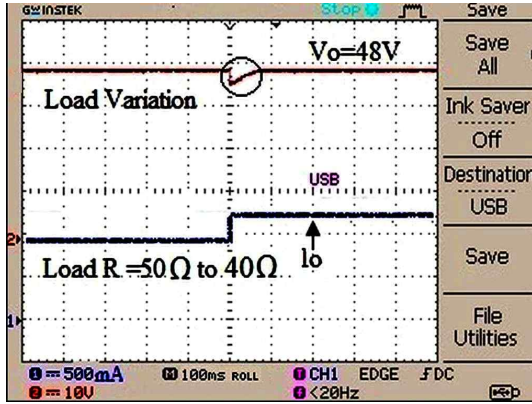
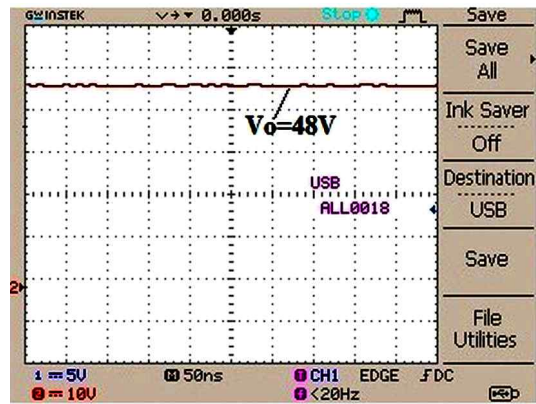Fig. 23. Response of the SEPIC using the SMC for load changes from 50 Ω to 40Ω.

TABLE VI
EXPERIMENTAL AND SIMULATED OUTPUT VOLTAGE /CURRENT OF
SEPIC FOR VARIOUS INPUT VOLTAGES AND LOADS

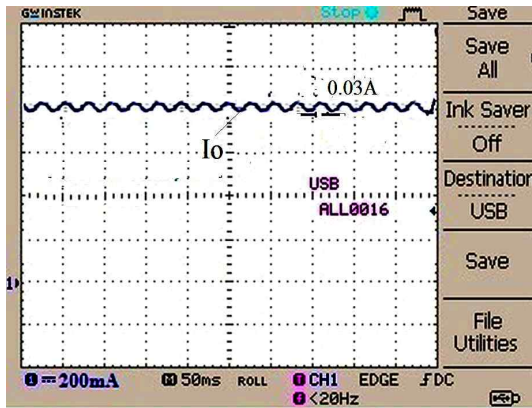| Input Voltage (V)	Voltage (Steady state) (R=50Ω)	
	Simulation (SMC)	Experimental (SMC)
	v_0 (V)	v_0 (V)
9V	48	48.01
12V	48	48.01
15V	48	48.01
Load R(Ω)	Current(steady state) (v_{in}=12V)	
	Simulation (SMC)	Experimental (SMC)
	i_o (A)	i_o (A)
40Ω	1.2	1.21
50Ω	0.96	0.96
60Ω	0.8	0.81

Fig. 24. Response of the SEPIC using the SMC for load current steady state condition for load R = 60Ω, v_{in}=12V.

Fig. 25 shows the experimental instantaneous output voltage of the SEPIC in the steady state region using the SMC. It is evident from the figure that the peak to peak current ripple is 0.35V.

4) Circuit Components Variations: Fig. 26 and Fig. 27 show the experimental responses of the output voltage of the
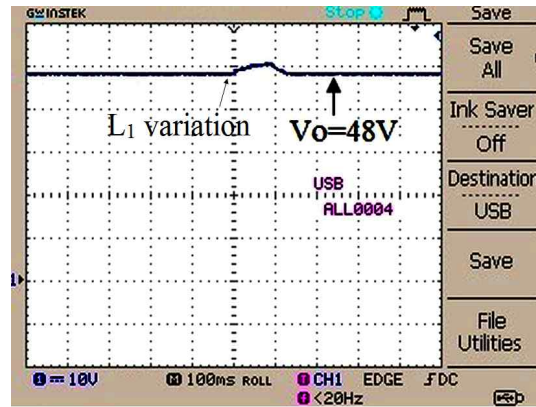

Fig. 25. Response of the SEPIC using the SMC for load Output voltage at steady state condition for load R = 60Ω, v_i=12V.

Fig. 26. Response of the output voltage variation for an inductor L_1 variation in load from110µH to150µH.
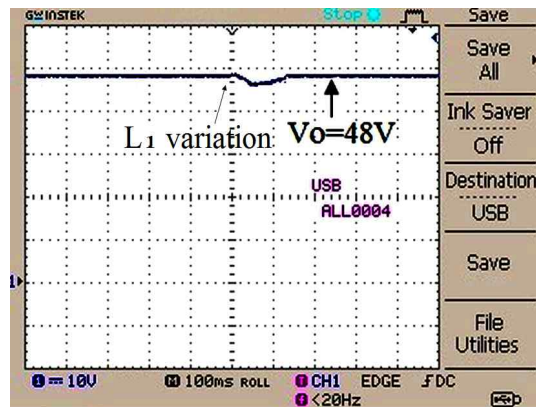

Fig. 27. Response of output voltage of SEPIC using SMC due to inductor variation from 110 µH to 90 µH.

SEPIC for an inductor L_1 variation from 110µH to 150 µH and an inductor L_1 variation from 110µH to 90 µH. It can be seen that the change in the inductor value does not influence the experimental SEPIC's behavior due to the quick control action of the SMC. The proposed SMC is very successful in suppressing the effect of inductance variations except for a negligible output voltage ripple and a quick settling time. Fig. 28 and Fig. 29 show the capacitor C_2 variation from
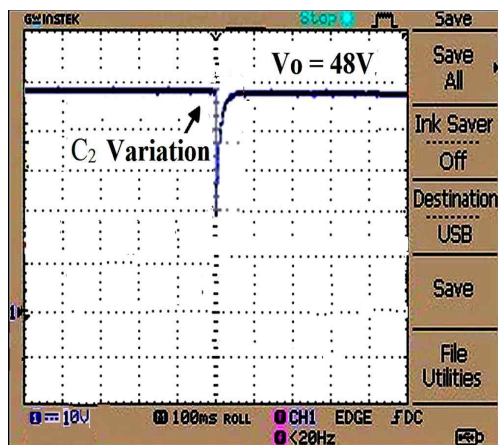
Fig. 28. Response of the output voltage of the SEPIC using the SMC for an capacitor C_2 variation from 300μF to 350μF.

300μF to 350μF and from 300μF to 250μF, respectively. It can be seen that the change in the capacitor value does not influence the SEPIC's behavior due to the quick control action of the SMC. It can be seen that the proposed SMC is very successful in suppressing the effects of capacitance variations except for a negligible output voltage ripple and a quick settling time.
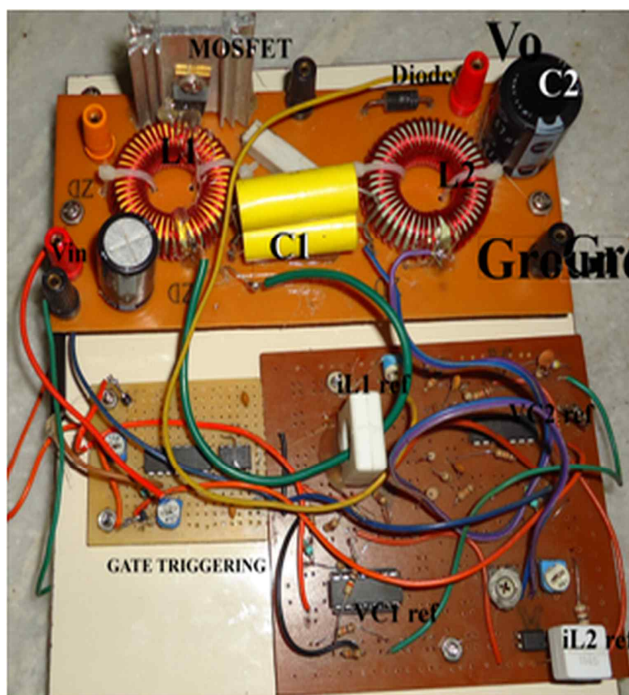

Fig. 29. Photograph of Designed Laboratory type SMC controlled SEPIC.

TABLE VII
COMPARISON OF SIMULATION AND EXPERIMENTAL RESPONSE FOR LINE VARIATION

	Step change in input voltage from 12V to 15V			Step change in input voltage from 12V to 9V		
Controller	Settling time(s)	Overshoot v_o(V)	% Overshoot	Settling time(s)	Variation of v_o(V)	% Variation
PI	0.05	17	35%	0.08	16	33.3%
Simulation-SMC	0.04	8	16.6%	0.07	8	16.6%
Experimental-SMC	0.04	7.5	15.6%	0.07	6	12.5%

TABLE VIII
COMPARISON OF SIMULATION AND EXPERIMENTAL RESPONSE FOR LOAD VARIATION

	Step change in load from 50Ω to 60Ω			Step change in load from 50Ω to 40Ω		
Controller	Settling time (s)	Overshoot of v_o(V)	% Overshoot	Settling time(s)	Variation of v_o(V)	% Variation
PI	0.07	6	12.5%	0.07	8	16.6%
Simulation-SMC	0.06	6	12.5%	0.07	6	12.5%
Experimental-SMC	0.06	7	14.5%	0.07	6	12.5%

TABLE IX
COMPARISON OF SIMULATION AND EXPERIMENTAL RESPONSE FOR COMPONENT VARIATION

	Step change in inductor L_1 from 110μH to 150μH			Step change in Capacitor C_2 from 300μF to 350μF		
Controller	Settling time(s)	Overshoot of v_o (V)	% Overshoot	Settling time(s)	Variation of v_o(V)	% Variation
PI	0.09	3	6.25%	0.02	42	87.6%
Simulation-SMC	0.09	2	4.1%	0.02	39	81.2%
Experimental-SMC	0.09	2	4.1%	0.01	30	62.08%

Tables VII, VIII and IX show a comparison of the PI controller, the SMC simulation and the SMC experimental in terms of line variation and load variation, and component variation. The performances are compared and listed in the Tables for transient conditions during the operation of the SEPIC converters with the controllers.

In summary, from the Fig. 20 to 28, it is clearly indicated that the experimental results of the SEPIC using the designed SMC agree with the simulated results with a tolerance of ±2%. Finally, the developed SMC performed well under all of the operational circumstances of the SEPIC.

VII. CONCLUSIONS

The closed loop control of a SEPIC is successfully designed using the SMC theory and CCM. The proposed SMC controller function has been demonstrated technically in an analog platform. A major advantage over linear PI controllers lies in the fact that the sliding mode controller is robust to large variations in line, load and parameter variations without changing the sliding coefficients. A number of simulations and experiments are carried out in order to demonstrate the good performance of the SMC controller. The proposed system is suitable for real-world commercial applications, like the power supplies for medical equipment, computer power supplies, uninterrupted power supplies, etc. Simulation and experimental results show that the proposed SMC maintains a regulated output voltage in the SEPIC in various regions.

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