

# Dead Angle Reduction of Single-Stage PFC Using Controllable Coupled Inductors

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## Abstract

This paper presents a new structure of single-stage flyback power factor correction (PFC) converter with a controllable coupled negative magnetic feedback (NMF) winding. NMF winding is used to reduce the bulk capacitor voltage at high line voltages and light loads. However, it would cause line current distortion at zero crossing condition. In the proposed circuit, a series winding is used with NMF inductor to eliminate the NMF inductor at low line voltages. As a result, the dead angle of the input current, near zero voltage crossing, is eliminated and the power factor is increased. The presented experimental results of the proposed PFC converter confirm the integrity of the new idea and the theoretical analysis.

**Key words:** Controlled coupling, Dead angle, inductors, Power factor correction (PFC), Single stage

## I. INTRODUCTION

Active power factor correction (PFC) methods have been widely used since harmonic regulations, such as IEC61000-3-2, have been approved. Conventional two-stage PFC converters can provide desirable characteristics, such as high-power factor and low-voltage stress. The disadvantages of this type of PFC converter are complexity and high number of elements. Therefore, this type is usually applied for high-power applications. Single-stage PFC ( $S^2$ PFC) converters are introduced for cost-effective conditions. In these converters, output voltage regulation and current shaping are achieved by using only one control circuit. An internal bulk capacitor ( $C_b$ ) is used to compensate the instantaneous difference between the varying input power and a constant output power. Therefore, the voltage across the bulk capacitor is not controlled. This condition occurs particularly when the input current shaping part operates under discontinuous conduction mode (DCM), whereas the DC/DC part operates under continuous conduction mode (CCM). At light load condition, the voltage across the bulk capacitor increases. At light load conditions, with 220 V<sub>ac</sub> to 240 V<sub>ac</sub> input voltage, the capacitor voltage can be above the desirable voltage, 450 V<sub>DC</sub>, which makes the single-stage

design impractical for applications with a universal input voltage range. Different methods are presented to reduce high bulk capacitor voltage stress [1]-[4]. Variable frequency control (VFC) reduces the bulk capacitor voltage stress [5]. However, VFC cannot effectively reduce the bulk capacitor voltage below 450 V<sub>DC</sub>, even with wide frequency variation range, which is not desirable for the magnetic component and EMI filter design. Another solution is to operate both the input current shaping and the DC/DC stage in DCM, in which the independence of the bulk capacitor voltage from the load is achieved [6]. However, compared with the efficiency in CCM operation of the DC/DC stage, the efficiency in DCM is reduced because of high conduction losses. When operating the DC/DC stage in the CCM/DCM boundary mode, the switching losses is reduced but the switching frequency increases at light load condition [7], [8]. Fig. 1 shows a conventional single-stage boost-flyback PFC converter with the addition of a second primary winding  $N_{NMF}$  in series with diode  $D_2$  [9].

By using  $N_{NMF}$  winding, when the switch is turned on, the induced voltage across  $N_{NMF}$  would reduce the effective voltage across  $L_b$ . Thus, a large duty cycle is necessary to keep the same volt-second product across  $L_b$ . Since the output voltage is constant, the voltage  $V_b$  is reduced with a large duty cycle. In addition, part of the input energy is directly transferred to the output through the coupled windings  $N_{NMF}$  and  $N_s$ . Since the extra primary winding voltage has opposite polarity with respect to the rectified input voltage during the switch-on interval, this winding is called negative magnetic

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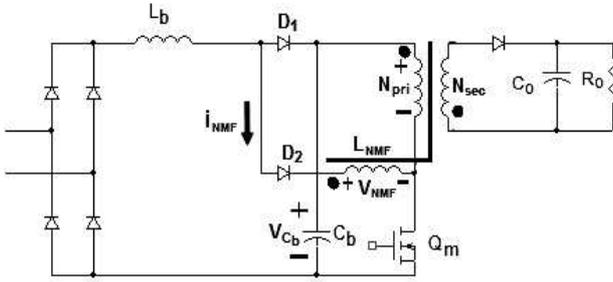


Fig. 1. Conventional single-stage flyback PFC with NMF inductor.

feedback (NMF). Because the input voltage is a sinusoid waveform, a dead angle exists in the input current when the input voltage becomes lower than the feedback voltage on  $L_{NMF}$ , which decreases the power factor. An auxiliary switch can be used to eliminate the dead angle problem. This solution improves the power factor, but increases the cost of the components at the same time [10], [11]. In such a circuit, the auxiliary switch current is high and equal to the main switch. However, in the proposed PFC presented in the current paper, an auxiliary switch is in series with the control winding circuit. Thus, the peak current and average current of the auxiliary switch are very low because of the turn ratio between the control and NMF winding and the low-duty cycle of the auxiliary switch.

A new structure based on NMF winding without dead angle of input current is proposed in this paper. As explained, using NMF inductor results in line current distortion near the zero crossing voltage because the line current cannot flow when the instantaneous line voltage is lower than the voltage induced across  $L_{NMF}$ . If NMF is eliminated at low line voltages, line current can flow even at very low line voltages. Although it should be noted that at high line voltages, NMF inductor is necessary to limit  $V_b$  particularly at light load condition [10]-[12].

In the proposed PFC, a series winding is used with NMF winding to eliminate NMF winding effect at low line voltages. The series winding is coupled in the opposite direction with NMF winding. Thus, the effect of NMF winding induced voltage during zero crossing distortion is eliminated. At high line voltages, the coupling between series winding and NMF winding is eliminated by disconnecting the control winding, which is the interface of the coupling. Therefore, NMF winding would reduce the boost inductor charging current when the main switch is on, and series winding acts as a series inductor with NMF winding. Using this method reduces the dead angle of input current near zero voltage crossing caused by the NMF winding and increases the power factor.

## II. CONTROLLABLE COUPLED INDUCTORS

In this paper, a new structure of controllable coupled inductors is proposed, as shown in Fig. 2. The coupled

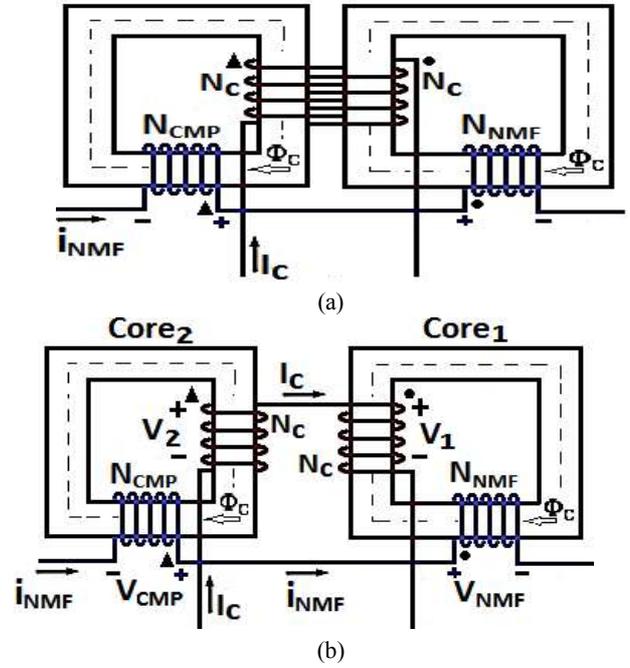


Fig. 2. Controllable coupled windings, NMF, and CMP with the control winding on the center leg (a) with cross winding and (b) with separate winding.

inductors are implemented by using two U cores and three windings, namely, NMF winding ( $N_{NMF}$ ), control winding ( $N_C$ ), and compensation winding ( $N_{CMP}$ ).  $N_C$  is wound commonly on both legs of the inner part of the cores in the opposite direction. According to the fact that total ampere-turn products for each core is 0,

$$\sum N.I_{(Core1)} = N_C \cdot I_C + N_{NMF} \cdot I_{NMF} = 0. \quad (1)$$

$$\text{Thus, } I_C = - (N_{NMF} / N_C) \cdot I_{NMF} \quad (2)$$

$$\text{and } \sum N.I_{(Core2)} = -N_{CMP} \cdot I_{NMF} - N_C \cdot I_C = -N_{CMP} \cdot I_{NMF} - N_C \cdot (-N_{NMF} / N_C) \cdot I_{NMF}. \quad (3)$$

$$\text{If } N_{CMP} = N_{NMF}, \quad (4)$$

$$\text{then } \sum N.I_{(Core2)} = 0. \quad (5)$$

The following relation is obtained because of the coupling between windings,  $N_{NMF}$  and  $N_C$  (right leg):

$$V_1 = V_{NMF} \cdot N_C / N_{NMF}. \quad (6)$$

Short circuiting the control winding obtains 0 as the voltage across the  $N_C$  (left leg);

$$-V_2 + V_1 = 0. \quad (7)$$

$$\text{Thus, } V_2 = V_1 = V_{NMF} \cdot N_C / N_{NMF}. \quad (8)$$

Moreover, given that the coupling between windings,  $N_{CMP}$ , and  $N_C$  (left leg),

$$V_{CMP} = N_{NMF} \cdot V_2 = V_{NMF}. \quad (9)$$

According to (9), opposite voltages are produced in both legs of control winding because of the short circuit condition of control winding. Thus, the polarity of the voltage induced in CMP winding is opposite the voltage of NMF winding. As a result, the total voltage across both windings,  $N_{NMF}$  and  $N_{CMP}$ , is 0, and these two series windings act as short circuit.

The block diagram of the proposed single-stage PFC with controllable coupled inductors is shown in Fig. 3. The

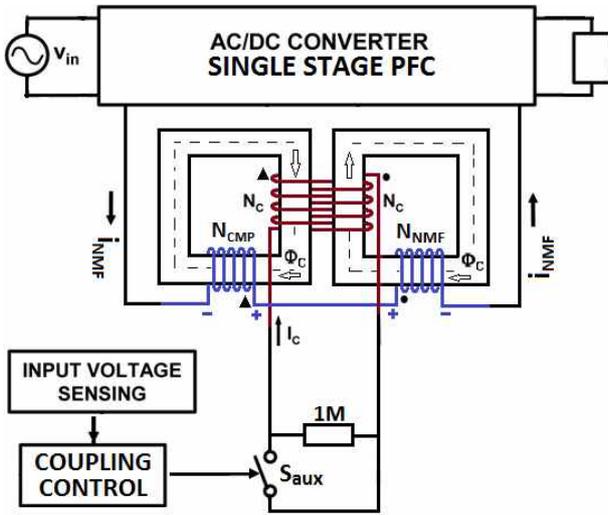


Fig. 3. Block diagram of the proposed single-stage PFC with controllable coupled inductors,  $L_{NMF}$ , and  $L_{CMP}$ .

coupling of the two windings,  $N_{NMF}$  and  $N_{CMP}$ , is controlled by the control winding connection. The control circuit includes the switch  $S_{aux}$ , the input voltage sensing circuit, and  $N_C$  winding connection control circuit.

At high line voltages, switch  $S_{aux}$  is turned off, thereby opening the control winding,  $N_C$ . Therefore, no current exists through winding  $N_C$ . Thus, the windings  $N_{NMF}$  and  $N_{CMP}$  do not have any coupling with each other, and  $N_{CMP}$  acts as a series inductor with  $N_{NMF}$  winding as shown in Fig. 4(a). Consequently, NMF winding compensates the variation of bulk capacitor voltage caused by load variation.

At low line voltages, switch  $S_{aux}$  is turned on, and the NMF winding flux flows through the control winding  $N_C$ , thereby inducing a magnetic flux  $\phi_c$  in two U cores in the same direction. According to the winding structure of  $N_{NMF}$  and  $N_{CMP}$ , the control winding  $N_C$  is coupled with them, and the voltage induced on the windings  $N_{NMF}$  and  $N_{CMP}$  is the same in amplitude but with opposite polarity. Consequently,  $V_{CMP} = -V_{NMF}$ , as shown in Fig. 4(b). Thus, the combination of these two series inductors acts as a short circuit. Therefore, NMF inductor is eliminated by series combination with  $N_{CMP}$ . Consequently, the charge current branch of the boost inductor does not include NMF inductor. Thus, the dead angle of input current is reduced to 0, which is the same as the state where no NMF winding exists in the charging path of the boost inductor. With the dead angle elimination, the input peak current reduces and decreased THD is achieved.

The turn-on signal for switch  $S_{aux}$  is generated with a comparator, which compares the scaled rectified line voltage  $K \cdot V_{in(rect)}$  with the reference voltage  $V_{ref}$ . Voltage  $V_{ref}$  is equal to the induced voltage on the NMF winding, when the main switch is closed.  $S_{aux}$  is turned on to bypass NMF winding when the instantaneous scaled rectified line voltage is lower than the reference voltage, which occurs near the 0 crossing of the line voltage.

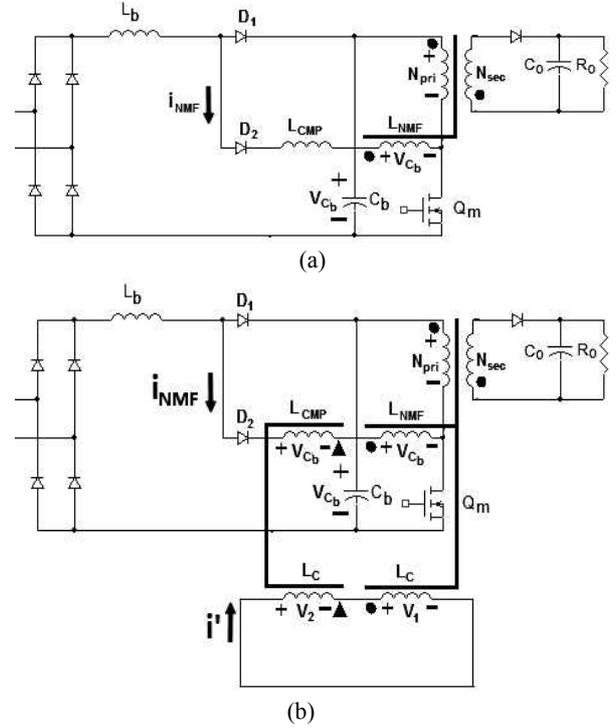


Fig. 4. Equivalent circuit of the proposed single stage PFC. (a) At high line,  $L_{CMP}$  acts as series inductor with  $L_{NMF}$ . (b) At low line,  $L_{CMP}$  acts as oppositely coupled inductor with  $L_{NMF}$ .

This technique has no significant effect on the main switch voltage stress, because the maximum voltage stress of the switch is affected from output voltage in both cases. This is due to the fact that the main switch voltage stress bases on the flyback part of the converter, not on the boost part of the converter. However, the main switch current waveform is affected only at low line voltages, because the current of the auxiliary circuit passes through the main switch. Thus, the main switch current increases at low line voltages, wherein the current is not high. At any rate, the peak of switch current is not affected. The switch peak current is equal to  $I_{sw(peak)} = (V_{in} - V_{Cb} \cdot N_{NMF}/N_{pri}) \cdot d \cdot T_S \cdot (1 + N_{NMF}/N_{pri}) / (L_b + L_{CMP})$  (10) where  $d$  is the converter duty cycle,  $T_S$  is the switching cycle time, and  $V_{Cb}$  is the bulk capacitor voltage.

### III. DESIGN CONSIDERATIONS

#### A. NMF Inductance ( $N_{NMF}$ ) Design

The single-stage flyback PFC converter operates like a conventional flyback converter when  $N_{NMF}/N_{Primary}$  is greater than or equal to 1, because according to Fig. 1, diode  $D_2$  is off when the switch is on in this condition.

However, in the single-stage flyback PFC converter, diode  $D_2$  should conduct and diode  $D_1$  should be reverse biased when the main switch  $Q_m$  is on. Thus,

$$N_{NMF}/N_{Primary} < 1. \quad (11)$$

Therefore, for proper operation of single-stage flyback PFC

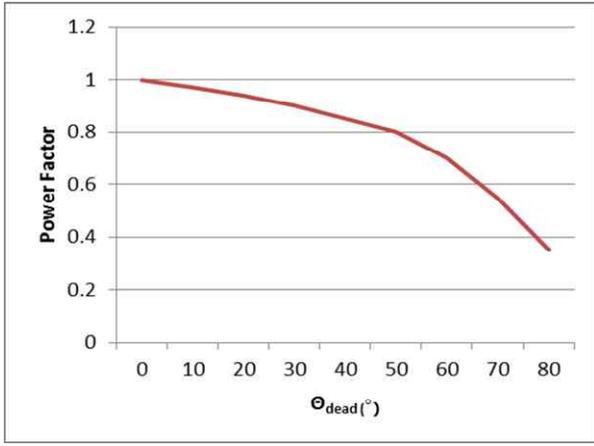


Fig. 5. Plot of power factor, versus the dead angle ( $\Theta_{dead}$ ).

converter, the turn ratio of  $N_{NMF}/N_{Primary}$  must be chosen less than 1. Changing the  $N_{NMF}/N_{Primary}$  turn ratio changes the dead angle of the input current. A smaller  $N_{NMF}/N_{Primary}$  would provide better power factor and smaller input current dead angle. However, the bulk capacitor voltage and switch voltage stress increase. Thus,  $N_{NMF}/N_{Primary}$  turn ratio should not be chosen too small. In general, an  $N_{NMF}/N_{Primary}$  turn ratio of approximately 0.5 is sufficient. With this value, a good trade-off among the bulk capacitor voltage, switch voltage stress, input current dead angle, and current harmonic distortion can be achieved. The proposed converter is in Class D harmonic current limit category. With turn ratio  $N_{NMF}/N_{Primary}$  of 14/29, the converter not only complies with EN61000-3-2 Class D harmonic current limits but also controls the bulk capacitor voltage, such that the capacitor voltage would be below the desirable voltage, 450 V<sub>DC</sub>. According to (4),  $N_{CMP}$  is equal to  $N_{NMF}$ .

The dead angle of the input current should be calculated near 0 voltage crossing. The auxiliary switch ( $S_{aux}$ ) is closed at zero crossing. Thus, according to Fig. 4(b), the input current flows if

$$V_{in(peak)} > V_{CMP} - V_{NMF} = V_{CMP} - V_{Cb} \cdot N_{NMF} / N_{pri} \quad (12)$$

Thus, the input current dead angle is equal to

$$\Theta_{dead} = \sin^{-1}((V_{CMP} - V_{Cb} \cdot N_{NMF} / N_{pri}) / V_{in(peak)}). \quad (13)$$

Thus, with increasing the NMF inductance, the ratio of  $L_{NMF}/L_{pri} = N_{NMF}/N_{pri}$  is increased, and the input current dead angle would increase. Fig. 5 shows the plot of power factor versus the dead angle ( $\Theta_{dead}$ ).

### B. Magnetizing Inductance ( $L_M$ ) Design

The average output power of a flyback DCM converter is derived by using the following [10]:

$$P_i = P_o / \eta = V_{Cb}^2 \cdot d^2 \cdot / (2L_M \cdot f_S) \quad (14)$$

where  $L_M$  is the magnetizing inductance of the flyback transformer,  $f_S$  is the switching frequency,  $d$  is the converter duty cycle, and  $V_{Cb}$  is the bulk capacitor voltage.

According to the PFC parameters in Table I,  $P_{out} = 120$  W,  $\eta = 90\%$ ,  $f_S = 50$  KHZ,  $V_{Cb} = 120$  V, and  $d = 60\%$ . The

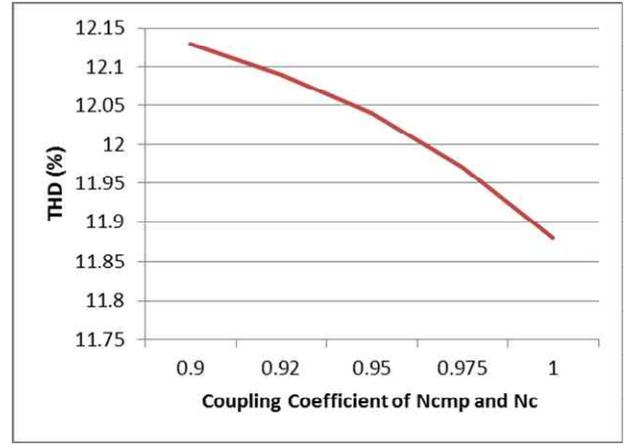


Fig. 6. Plot of THD versus coupling coefficient of  $N_{CMP}$  and  $N_C$ .

magnetizing inductance of the flyback transformer ( $L_M$ ) is obtained from (14) 388  $\mu$ H and is chosen to be 400  $\mu$ H.

According to the power of the converter, the power of flyback transformer is approximately 120 W.  $N_C$  winding operates for a short period (approximately 10% of whole period). Thus,  $N_C$  winding does not considerably affect the flyback transformer power, and EE2525 ferrite core (with 0.5 mm air gap to achieve increased saturation point) is used for this power [13]. All transformer windings are wound in four layers to reduce leakage inductances.

### C. Controllable Inductance ( $N_C$ ) Design

One of the advantages of this technique is the controll of the current of the auxiliary switches. The turn ratio of  $N_C/N_{NMF}$  should be reduced to reduce current stress of auxiliary switches. The turn ratio of  $N_C/N_{NMF}$  of approximately 0.5 provides a good trade-off between the auxiliary switch current and voltage stress.

According to Equation (9),  $V_{NMF}$  and  $V_{CMP}$  would not become exactly equal by decreasing the coupling coefficient of  $N_{CMP}$  and  $N_C$ . Thus, the total harmonic distortion increases. The simulation demonstrates that the total harmonic distortion increases by decreasing the coupling coefficient of  $N_{CMP}$  and  $N_C$ . However, this increase is not high and is approximately 5% of the full range of practical coupling coefficient variation (0.90 to 0.99). Fig. 6 shows the plot of THD versus coupling coefficient of  $N_{CMP}$  and  $N_C$ .

The power processed with auxiliary transformer ( $P_{aux}$ ) is equal to

$$I_{CMP(ave)} = (V_{in}/L_b) \cdot d^2 \cdot T_S / 2; \quad (15)$$

$$V_{CMP} = V_{Cb} \cdot (N_{CMP} / N_{Primary}) \cdot (N_{C1} / N_{C2}); \quad (16)$$

$$I_{C2(ave)} = I_{CMP} \cdot (N_{CMP} / N_{C2}) = (V_{in}/L_b) \cdot d^2 \cdot T_S / 2 \cdot (N_{CMP} / N_{C2}); \quad (17)$$

$$V_{C2} = V_{Cb} \cdot (N_{C1} / N_{Primary}); \quad (18)$$

$$P_{aux(ave)} = V_{CMP} \cdot I_{CMP} + V_{C2} \cdot I_{C2} = 2V_{Cb} \cdot (N_{CMP} / N_{Primary}) \cdot (N_{C1} / N_{C2}) \cdot (V_{in}/L_b) \cdot d^2 / 2; \quad (19)$$

where  $N_{C1}$  is the right leg of control winding, which is coupled by NMF winding, whereas  $N_{C2}$  is the left leg of control winding, which is coupled by CMP winding.

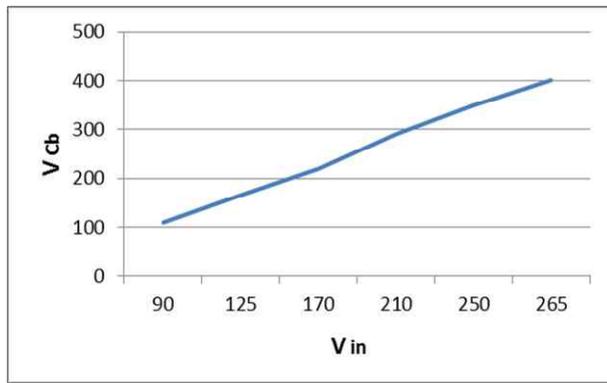


Fig. 7. Plot of DC bus voltage ( $V_{Cb}$ ) versus input voltage ( $V_{in}$ ).

According to PFC parameters in Table I, the power processed with auxiliary transformer ( $P_{aux}$ ) is approximately 20 W, and EE1515 ferrite core is used for this power given that the auxiliary transformer acts in a short period (approximately 10% of the entire period) [13].

#### D. Bulk capacitor design

The bulk capacitor is used to compensate the instantaneous difference between the varying input power and the constant output power. Thus, its capacity should be large enough to compensate this large power difference. With smaller capacitor, the voltage of bulk capacitor changes rapidly and would increase to balance the difference between the input and the output power. Decreasing the bulk capacitor capacity to 470  $\mu$ F would double the bulk capacitor ripple. Thus, the harmonic distortion of input current would increase.

The bulk capacitor voltage (DC bus voltage) is a function of the input voltage, the ratio of inductances  $L_b/L_M$ , the turn ratio of  $N_{NMF}/N_{pri}$ , and the output voltage [14]. DC bus voltage increases with increasing input voltage from low line to high line voltage. However, the NMF inductance controls its voltage, such that the DC bus voltage is kept below the desired voltage, 450 V<sub>DC</sub>, at the full range of the input voltage from low line to high line voltage. This finding can be observed from the simulation results, which are presented in Fig. 7.

## IV. CONTROL CIRCUIT

Fig. 8 shows the schematic of the single-stage PFC flyback converter by using controlled coupled inductors. The rectified input voltage is sensed by a circuit, including diodes  $D_4$ ,  $D_5$ , zener diode  $Z_1$ , capacitor  $C_1$ , and transistor  $Q_1$ . MOSFETs  $S_a$  and  $S_b$  are connected in series with the control winding  $N_C$ . When the input voltage increases above the value that is determined by  $V_{NMF}$ , the voltage across the capacitor  $C_1$  turns the zener diode  $Z_1$  on only at high line voltages where rectified input voltage is higher than  $V_{NMF}$ . When  $Z_1$  is turned on, switch  $Q_1$  is turned on. Thus, the gate voltage of MOSFETs  $S_a$  and  $S_b$  are 0, and they are turned off. Thus, the control winding current reduces to 0, and the coupling

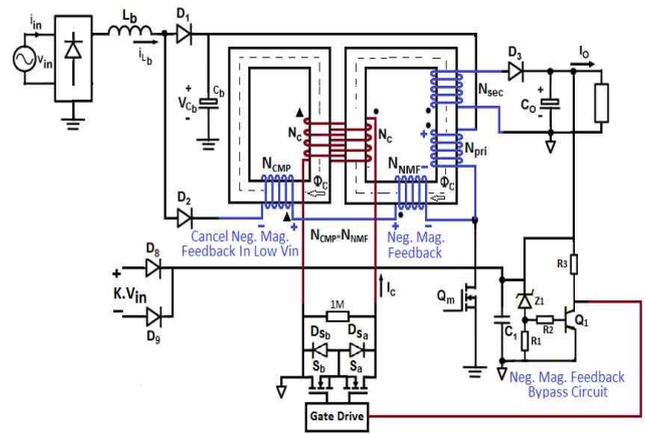


Fig. 8. Schematic of the proposed single stage PFC with conjugated controllable inductors,  $L_{NMF}$  and  $L_{CMP}$ .

between  $N_{NMF}$  and  $N_{CMP}$  is eliminated.

At low line, where the rectified input voltage is lower than  $V_{NMF}$ , the voltage across capacitor  $C_1$  is lower than the breakdown voltage of  $Z_1$ , and  $Q_1$  is turned off and MOSFETs  $S_a$  and  $S_b$  are turned on. Therefore, the coupling between the three windings,  $N_C$ ,  $N_{NMF}$  and  $N_{CMP}$ , is established. Series combination of MOSFETs  $S_a$  and  $S_b$  makes both directions of current in the auxiliary circuit possible. The direction of control winding flux causes the voltages across  $L_{NMF}$  and  $L_{CMP}$  to be in opposite directions. Thus, the series combination of  $L_{NMF}$  and  $L_{CMP}$  acts as short circuit.

Fig. 9 shows the detailed schematic of the control and gate drive circuits for main and auxiliary switches.

Two series-connected MOSFETs are used because the current of the auxiliary circuit is in both directions. This condition occurs because of the coupling between one of the auxiliary circuit windings with flyback transformer. The series-connected MOSFETs are actually source connected. However, the gate drives are opto-isolated to have a stable control loop. Thus, the gate drives could have been used even for drain-connected MOSFETs.

Controller IC is SG3525. Moreover, any feedback is unnecessary from the input voltage or current waveforms because of inherent PFC of flyback-boost PFCs.

According to Fig. 8, the reference voltage (the break down voltage of  $Z_1$ ), which is compared with  $K \cdot V_{in}$ , is constant. Increasing the amplitude of the input voltage ( $V_{in}$ ) changes the auxiliary switches the turn-on angle. Thus, the total harmonic distortion increases. The simulation demonstrates that the total harmonic distortion increases by increasing the input voltage from low line to high line voltage. However, this increase is not high and is approximately 8% for the full range of input voltage variation. Fig. 10 shows the plot of THD versus input voltage ( $V_{in}$ ).

## V. EXPERIMENTAL RESULTS

The proposed single-stage PFC flyback using conjugated

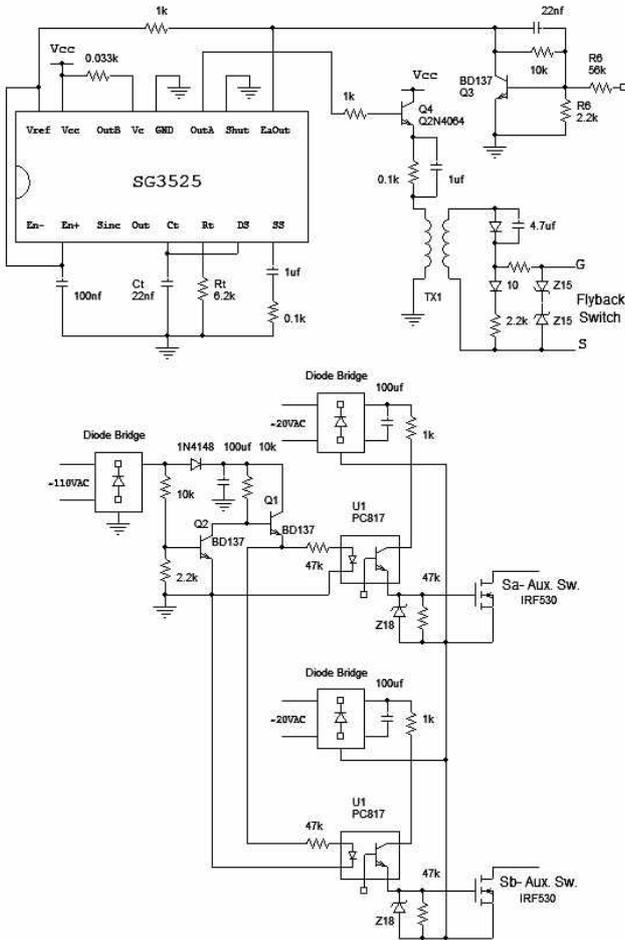


Fig. 9. Schematic of control and gate drive circuits for main and auxiliary switches.

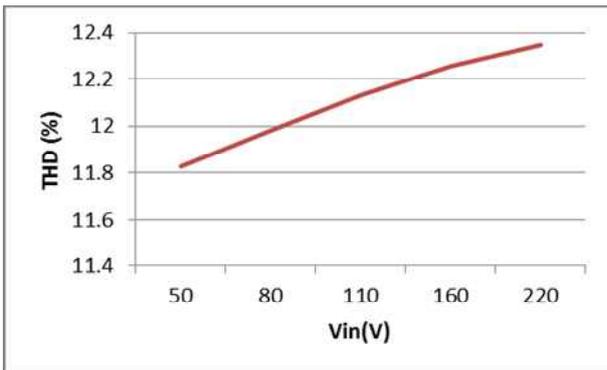


Fig. 10. Plot of THD versus input voltage ( $V_{in}$ ).

controllable inductors is simulated by using computer and then implemented to verify the operation, analytical analysis, and performance of the proposed circuit. The PFC is designed to operate at 120 W and 100 V<sub>DC</sub> output. The circuit parameters are listed in Table I, and the components used for implementation of the circuit are listed in Table II and shown in Fig. 11.

Fig. 12 shows the input current waveform. A complete period of  $I_{L_b}$  current without and with compensated series

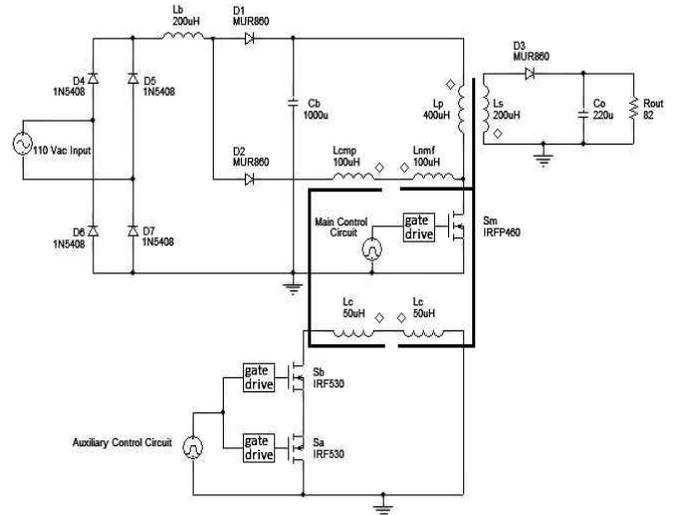


Fig. 11. Implemented schematic of the proposed single-stage PFC with controllable coupled inductor  $L_{CMP}$ .

TABLE I  
PFC PARAMETERS

$V_{in}$	110 V <sub>rms</sub>	$V_{out}$	100 V <sub>DC</sub>
$P_{out}$	120 W	$f_{sw}$	50 KHz
$L_{Primary}$	400 $\mu$ H	$N_{Primary}$	29 turns, $\varnothing 0.5 \times 4$
$L_{Secondary}$	200 $\mu$ H	$N_{Secondary}$	20 turns, $\varnothing 0.5 \times 4$
$L_{NMF}$	100 $\mu$ H	$N_{NMF}$	14 turns, $\varnothing 0.5 \times 4$
$L_{CMP}$	100 $\mu$ H	$N_{CMP}$	14 turns, $\varnothing 0.5 \times 4$
$L_C$	50 $\mu$ H	$N_C$	10 turns, $\varnothing 0.5 \times 4$
$L_b$	30 $\mu$ H		

TABLE II  
LIST OF KEY COMPONENTS

Main switch ( $S_m$ )	IRFP460	$R_{out}$	82 $\Omega$
Auxiliary switches ( $S_a, S_b$ )	IRFP350	Output Cap. ( $C_{out}$ )	220 $\mu$ f
Main transformer core	EE2525	Rectifier diodes ( $D_4, D_5, D_6, D_7$ )	1N5408
Auxiliary transformer core	EE1515	Flyback diodes ( $D_1, D_2, D_3$ )	MUR860
Bulk cap. ( $C_b$ )	1000 $\mu$ f	Controller IC	SG3525

inductor is shown in Figs. 12(a) and 12(b), respectively. The dead time of input current in the proposed single-stage PFC with NMF and without compensated series inductor is approximately 1 ms, which is approximately 10% of  $I_{L_b}$  period [Fig. 12(c)]. Applying series CMP winding with NMF winding reduces the dead angle to 0.01 ms (0.1% of  $I_{L_b}$  period), as shown in Fig. 12(d). Fig. 12(e) illustrates that the voltage of CMP winding is opposite that of NMF winding voltage, and they can eliminate each other. The THD of the PFC is approximately 12%.

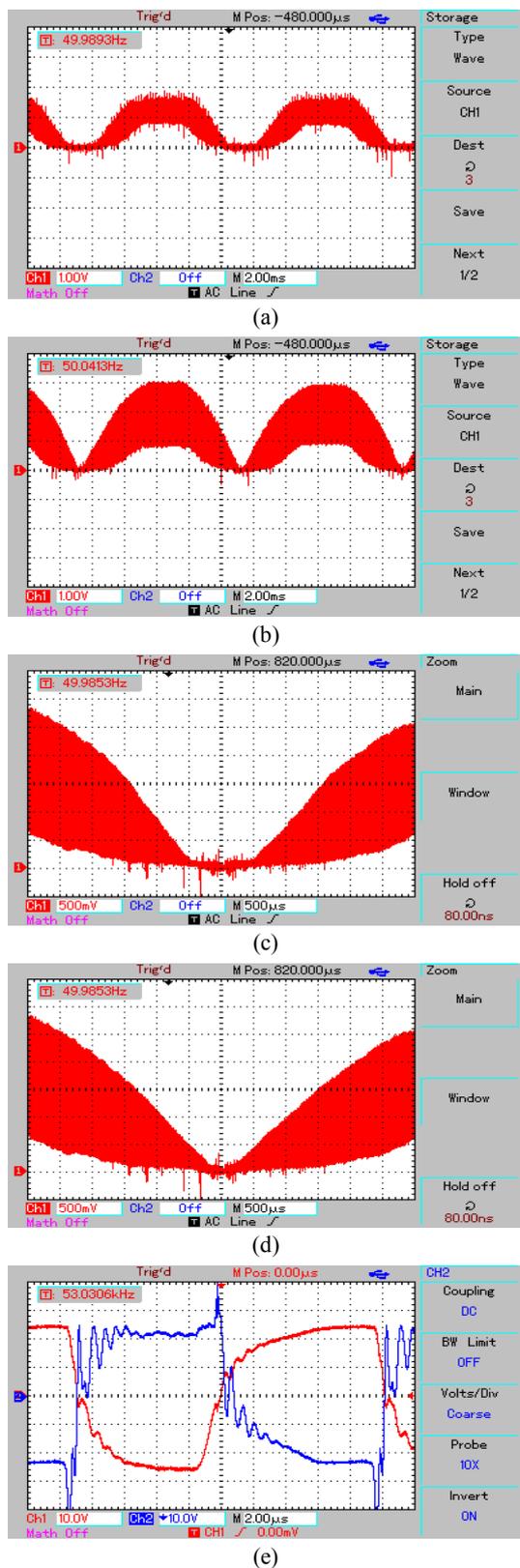


Fig. 12. Experimental results of the proposed single-stage PFC. (a)  $I_{Lb}$  without controllable coupled inductors; (b)  $I_{Lb}$  with controllable coupled inductors; (c) scaled  $I_{Lb}$  without controllable coupled inductors; (d) scaled  $I_{Lb}$  with controllable coupled inductors; (e) blue color line:  $V_{CMP}$ ; red color line:  $V_{NMF}$ .

## VI. CONCLUSION

A single-stage flyback PFC with a controllable coupled NMF winding is presented in this paper. NMF inductor is used in series with the boost inductor to reduce the bulk capacitor voltage at light load condition. A new structure of coupling between the NMF and compensation (CMP) windings is used with a common control winding to overcome the problem of input current dead angle. CMP and NMF windings are coupled in opposite directions at low line voltages. Thus, no NMF winding exists in the boost inductor charge current branch, and zero crossing distortion is eliminated at low line. At high line voltage, the coupling between CMP and NMF is eliminated. Thus, NMF winding reduces the bulk capacitor voltage. Experimental results obtained from a 100 V/100 W circuit shows that the proposed PFC converter achieves the dead time of 0.01 ms for universal input voltage.

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