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Control of Parallel Connected Three-Phase PWM Converters without Inter-Module Reactors

Bassim M. H. Jassim*, Bashar Zahawi†, and David J. Atkinson**

*College of Engineering, Baghdad University, Baghdad, Iraq
†Department of Electrical and Computer Engineering, Khalifa University, Abu Dhabi, UAE
**School of Electrical and Electronic Engineering, Newcastle University, Newcastle upon Tyne, UK

Abstract

This paper presents a new current sharing control strategy for parallel-connected, synchronised three-phase DC-AC converters employing space vector pulse width modulation (SVPWM) without current sharing reactors. Unlike conventional control methods, the proposed method breaks the paths of the circulating current by dividing the switching cycle evenly between parallel connected equally rated converters. Accordingly, any inter-module reactors or circulating current control will be redundant, leading to reductions in system costs, size, and control algorithm complexity. Each converter in the new scheme employs a synchronous dq current regulator that uses only local information to attain a desired converter current. A stability analysis of the current controller is included together with a simulation of the converter and load current waveforms. Experimental results from a 2.5kVA test rig are included to verify the proposed control method.

Key words: Control of power electronic converters, Current control, DC-AC power conversion, Parallel operation, PWM converters

I. INTRODUCTION

The parallel operation of voltage fed converters is commonly used in high power applications to increase the current handling capability of power electronic circuits. The technique is also widely employed to increase system efficiency, flexibility, and reliability [1], [2] in aerospace and wind turbine applications, through providing essential redundancy. However, along with the obvious benefits offered by the parallel connection of converter circuits, such an arrangement gives rise to a number of concerns. Key amongst these is the problem of the circulating currents that flow in such systems. The term circulating current describes the uneven current sharing between various equally rated converter units. This leads to current distortion and unbalanced operation, which can damage the converters, as well as a general decline in overall system performance. Circulating currents are generated between parallel inverters unless they have uniform modulation [3]. Therefore, the reference modulating waveforms and carrier waveforms should have exactly the same amplitude, phase and frequency to avoid this problem. The physical parameters of the converters and the dead-time between the upper and lower switching signals in each converter leg should also be the same. However, this is not possible in practice. For this reason, current sharing control methods are necessary to limit the circulating current in parallel-connected converter systems.

In order to prevent or reduce the flow of circulating currents, a separate dc or ac power supply [4]-[6] or isolated ac sides via a transformer [7]-[9] can be used. These approaches will lead to increased system size and cost, and reduced efficiency (due to the extra core and copper losses when an isolation transformer is employed). An alternative approach is to utilize inter-module current sharing reactors on the output terminals of each inverter in order to provide a high impedance in the circulating current loop [10], [11]. However, this option will not provide a solution to the flow of low frequency circulating currents and it adds considerably to the cost and size of the system.

Recent improvements in digital signal processing (DSP)

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†Corresponding Author: bashar.zahawi@kustar.ac.ae
Tel: +971-2-4018219, Khalifa University
*College of Engineering, Baghdad University, Iraq
**School of Electrical and Electronic Eng., Newcastle University, UK

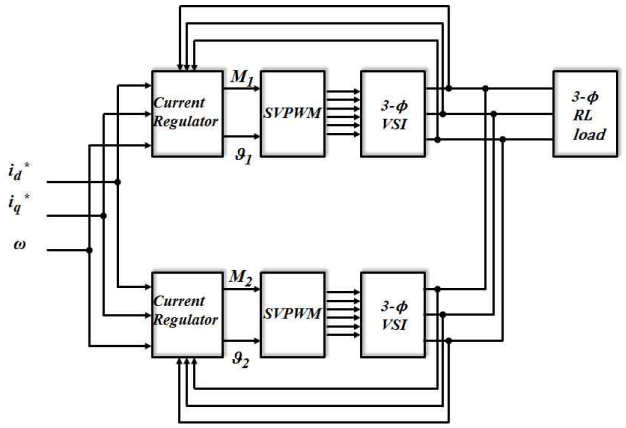

Fig. 1. Control block diagram.

controllers and advanced pulse width modulation (PWM) techniques have made it possible to directly connect the dc and ac sides of a converter with small passive components to reduce the circulating currents. A method for controlling the zero sequence circulating current (ZSCC) in a parallel-connected three-phase rectifier [12] has been proposed, where the ZSCC is calculated from the three-phase currents, and a PI controller is used to determine the interval time of the zero vectors so that the ZSCCs will be zero. However, the effectiveness of this technique diminishes when the zero vectors interval time becomes small [13]. An open loop compensation master/slave dual-modulator has also been proposed to mitigate the ZSCCs [14] in parallel connected converters. In this scheme, the zero sequence modulating waveform of the master converter is adopted by all of the slave converters, leading to a considerable reduction in the ZSCC. However, like all master/slave schemes, this approach has a low reliability and is susceptible to failure.

Coordinate control has also been suggested for parallel-connected three-phase boost rectifiers [15] to control the flow of ZSCCs. In this strategy, the line current symmetrical components are calculated for all of the converters. The zero and negative sequence currents are then eliminated by using simple PI controllers, while the positive sequence line current components are controlled for even load sharing. This approach is highly effective in terms of circulating current mitigation. However, a very heavy computational capability is required for its implementation.

This paper presents a new control method for parallel-connected, synchronised three-phase DC-AC converters based on time sharing of the converter switching cycle that minimises the paths of the converter circulating currents. The switching cycle is divided equally between the parallel connected converters to break the path of the converter circulating current. This eliminates the need for current sharing reactors and circulating current control algorithms. Although the proposed current sharing control method is applicable to ac drive applications, in this study it was decided for the sake

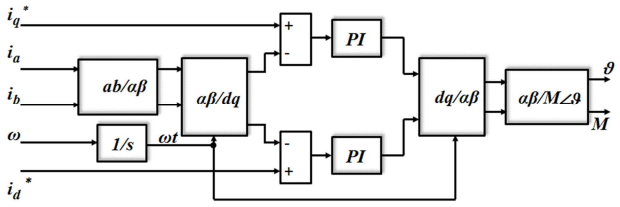

Fig. 2. Synchronous frame dq current regulator.

of simplicity to examine the performance of the current controller with an RL load since the main objective is the removal of the current sharing reactors. Simulation results showing the basic operation of the scheme have already been published [16]. In this paper, the concept is extended to provide decoupled d-axis and q-axis current regulation (needed for vector controlled machine drives and grid connected applications). The performance of the proposed control strategy is experimentally verified using a 2.5kVA test rig.

For commercial implementation of the proposed scheme, each converter should have independent but synchronised control hardware. However, for the sake of convenience, the test rig described in this paper executes both controllers in one TMS320F28335 DSP microcontroller.

II. PROPOSED CURRENT CONTROL METHOD

Fig. 1 shows a block diagram of the proposed current controller. Space Vector PWM (SVPWM) is commonly employed in power electronic conversion circuits because it offers a number of advantages in terms of dc link voltage utilization, total harmonic distortion (THD) levels and simple duty cycle calculations. However, SVPWM naturally excites the flow of ZSCCs when converters are connected in parallel [17]. When employing SVPWM, the duty cycles, d_1, d_2 and d_0, of the vectors, $\mathbf{V}_1$, $\mathbf{V}_2$ and $\mathbf{V}_0$, are obtained from (1), where M is the modulation index and ϑ is the angle of the desired output voltage vector. Full control of the switch duty cycles can be obtained by adjusting these two parameters (M and ϑ).

$$\begin{aligned} d_1 &= M.\sin\left(\pi/3 - \vartheta\right) \\ d_2 &= M.\sin\left(\vartheta\right) \\ d_0 &= 1 - d_1 - d_2 \end{aligned} \tag{1}$$

To minimize the circulating current paths, the switching cycle in the proposed control strategy is divided evenly between the equally rated converters, i.e. for n parallel connected converters, each converter is active for only 1/n of a switching cycle. In this case, most of the circulating current paths are broken, thus eliminating the need for current sharing reactors which are normally employed on the output of each converter. This reduction in the circulating current paths also removes the need for a separate current sharing controller within the converter control loop.

The three-phase converter currents are measured during the part of the switching cycle in which the converter is active.

These current measurements are supplied to a synchronous dq frame current regulator, as shown in Fig. 2. Two PI controllers are employed to control the direct (i_d) and quadrature axis (i_q) currents separately. The difference between the demanded and measured current values is supplied to the PI controllers, whose outputs are then transformed back to the stationary $\alpha\beta$ frame. Polar representation is then used to produce a desired modulation index (M) and angle (ϑ) for each converter.

The nature of the proposed control method means that the stray inductance in the current transfer paths from one converter to another must be minimised in order to minimise the current overlap periods and to avoid large dv/dt values since the current is shared between the two converters. In practice this means that the two converters must be closely matched in terms of their physical arrangements and care must be taken to reduce cable lengths and other sources of inductance in the circuit.

III. Stability Analysis and Determination of the PI Controller Gains

To optimize the PI controller gains of a sampled data system in the continuous time domain, it is necessary to determine an equivalent continuous time model that considers the delay time (T_d) produced by the sampling process and the algorithm computation time [18], [19]. The design objective in such an exercise is to maximizes the controller gains (K_p and K_i) with the desired phase margin (ϕ_m) while the forward path open loop gain tracks through unity [20].

It has been proven [21] that the exact same gain settings can be used regardless of whether a synchronous dq frame current regulator, a stationary frame proportional resonant (PR) regulator or a classical stationary frame PI controller is used. Performing an analysis for a stationary reference PI current regulator (for the sake of simplicity), the average value model, including the effects of the delay time, is shown in Fig. 3. The PWM converter is modelled as a linear gain (k_b=V_{dc}/√3, the magnitude of the fundamental phase voltage when SVPWM is used), and the delay is represented by an exponential function (e^{-sT_d}) in the forward path. For ac drive applications, the performance of the PI current regulator can be enhanced if the back emf is estimated and added to the command modulation depth reference signal after the PI compensator output as a feedforward compensation, as detailed in [21]. For the sake of simplicity, only an RL load is considered in this paper. The PI compensator transfer function $\mathbf{G}_c(s)$ can then be expressed as:

$$\boldsymbol{G}_c(s) = K_p + {k_i}/{s} \tag{2}$$

In addition, the open loop transfer function $\mathbf{G}(s)$ can be expressed as:

$$\mathbf{G}(s) = {[K_b(K_p s + K_i)e^{-sT_d}]}/{[s(R + sL)]} \tag{3}$$

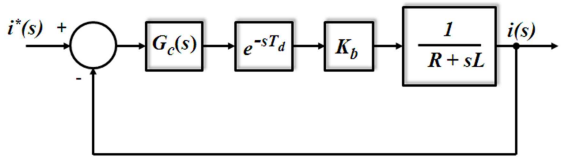

Fig. 3. Control diagram of converter with delay effect.

where R and L are the load resistance and inductance, respectively. The phase angle of $G(s)$ at the cross over frequency ω_c (i.e. the frequency at which a unity gain occurs at the desired phase margin ϕ_m) is given by:

$$\angle G(s) = \tan^{-1}\left({\omega_c K_p}/{K_i}\right) - \omega_c T_d - ({\pi}/{2}) - \tan^{-1}\left({\omega_c L}/{R}\right) = -\pi + \phi_m \tag{4}$$

The term $\tan^{-1}\left({\omega_c L}/{R}\right)$ can be approximated by $\pi/2$ since $(\omega_c L/R) \gg 1$. Thus, from the last equation:

$$\phi_m \approx \tan^{-1}\left({\omega_c K_p}/{K_i}\right) - \omega_c T_d \tag{5}$$

This yields:

$$\omega_c = \left[\tan^{-1}\left({\omega_c K_p}/{K_i}\right) - \phi_m\right]/{T_d} \tag{6}$$

From (6), the maximum value of ω_c that can be obtained for a given ϕ_m is:

$$\omega_{c(max)} = [(\pi/2) - \phi_m]/T_d \tag{7}$$

By setting the open loop gain to unity at $\omega_{c(max)}$, the maximum possible magnitude of K_p can be calculated as:

$$K_p \approx {\omega_{c(max)} L}/{K_b} \tag{8}$$

since $(\omega_{c(max)} K_p) \gg K_i$ and $(\omega_{c(max)} L / r) \gg 1$ for typical AC current regulated systems [20]. The integral gain can now be obtained so that the assumption $\tan^{-1}(\omega_c K_p/K_i) \approx \pi/2$ is validated by using a suitable value for the integral gain such as:

$$K_i = {\omega_{c(max)} K_p}/{10} \tag{9}$$

By using the system parameters L=10mH, R=10Ω, K_b=115.47V, and T_d=250μs (corresponding to a delay in the forward control path of the three PWM switching periods introduced by the sampling and updating process), with a suitable phase margin of ϕ_m=40° for satisfactory control performance, the controller gains are calculated as K_p=0.3 and K_i=105. To verify the design of the controller, a bode plot of the open loop transfer function is shown in Fig. 4. The design is further confirmed with the closed loop step response shown in Fig. 5. The maximum gains settings can be applied

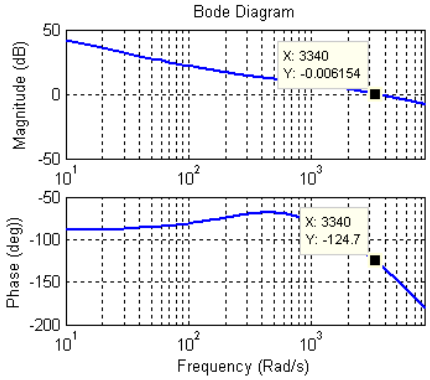

Fig. 4. Bode plots of open loop forward path considering delay effect; L=10mH, R=10Ω, K_p=0.3, K_i=105.

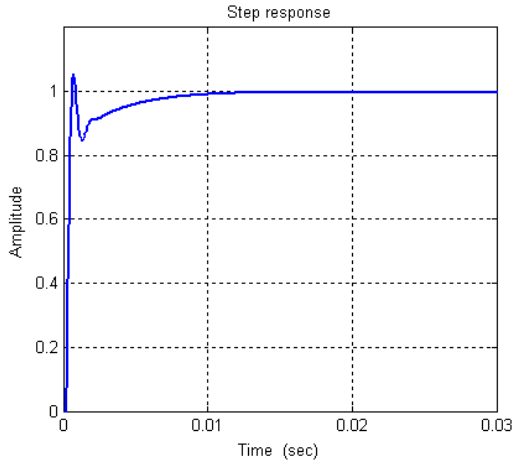

Fig. 5. Closed loop step response; L=10mH, R=10Ω, K_p=0.3, K_i=105.

to a stationary PR current regulator and by association to a synchronous dq frame regulator as detailed in [20].

IV. Simulation Results

The performance of the proposed control strategy was examined using a MATLAB/SIMULINK model. The fundamental and switching frequencies were set to 50Hz and 6kHz, respectively. A dc link voltage of 200V was assumed to give an *ac* line voltage of 110V with a modulation index of 0.8. To simulate the cable impedance, a 5mΩ resistance in series with a 1μH inductance were employed on the output lines of each converter. A schematic diagram of the circuit under consideration is shown in Fig. 6.

The switching cycle is divided equally between two equally rated converters with the first converter being activated during the first half and the second converter during the second half of the switching cycle. Fig. 7 shows the gate signals for all twelve switches of the two inverters for operation in the first sector of the SVPWM scheme, with the switching periods, T_1, T_2, and T_0, calculated using equation (10). The converter switches are supplied with zero logic states for the periods during which the

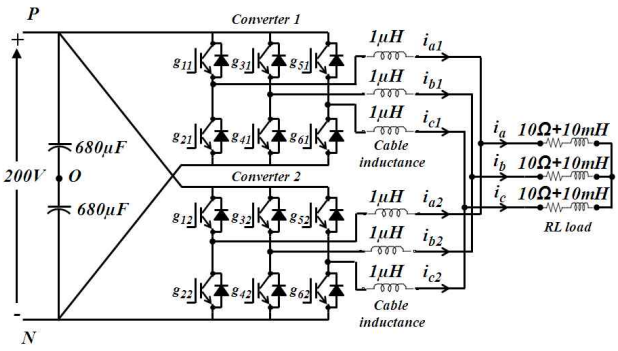

Fig. 6. Schematic diagram of parallel converter circuit.

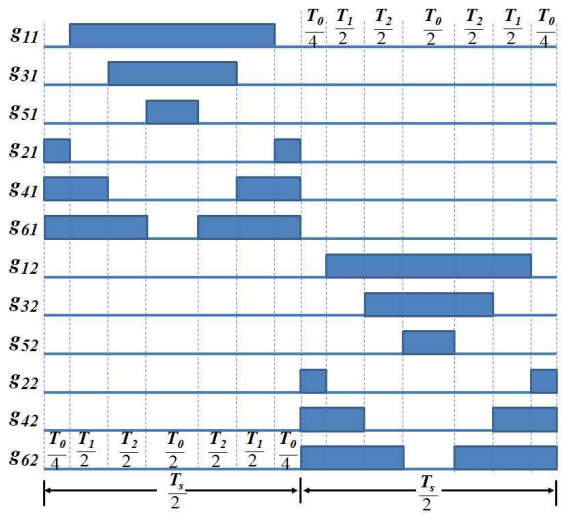

Fig. 7. Converters gate signals.

converter is deactivated.

$$T_1 = M(T_s/2)\sin(\pi/3 - \vartheta)$$
$$T_2 = M(T_s/2)\sin(\vartheta) \quad (10)$$
$$T_0 = (T_s/2) - T_1 - T_2$$

To confirm the redundancy of the current sharing reactors and circulating current control, two operating conditions were simulated. In the first test, two converters with different parameters were employed. The first converter had the physical parameters listed in Table I, while the parameters of the second converter were reduced by 30%. In addition, the dead time for the second converter was decreased by 20% to introduce an additional significant imbalance to the system.

Fig. 8 shows the converter and load current waveforms when the conventional SVPWM control strategy is adopted for the two converters with no inter-module reactors. It can be seen very clearly that the converter current waveforms are significantly distorted with very high uncontrollable current spikes reaching values of up to 80A. Clearly such an arrangement would not be possible in practice since the current spikes would almost certainly cause serious damage to the converters. In the second test, the proposed control method

TABLE I
CONVERTER PARAMETERS

Cable resistance and inductance	0.5mΩ+1μH
IGBT on resistance	1mΩ
IGBT forward voltage	1.9V
Freewheeling diode on resistance	1mΩ
Freewheeling diode forward voltage drop	1.15V
Rectifier diode on resistance	5.2mΩ
Rectifier diode voltage drop	1.13V

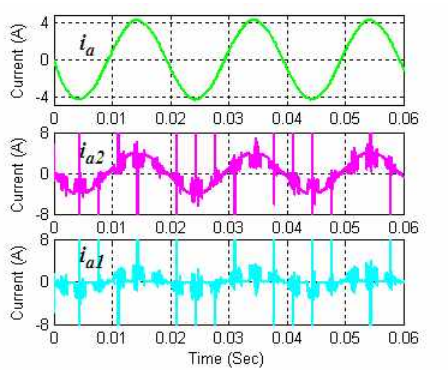

Fig. 8. Load and converter current waveforms; conventional SVPWM control.

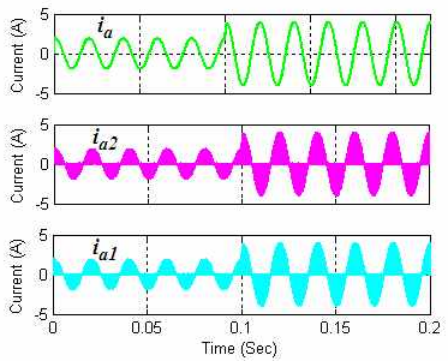

Fig. 9. Load and converter current waveforms with the proposed control method.

is activated with the exact same parameter and dead time settings as the first test and again with no inter-module reactors. Using the PI gains calculated above (K_p=0.3 and K_i=105), the system waveforms are presented for both the steady state and transient operating conditions. A step change in the desired q-axis current from 2A to 4A is applied at t = 0.1sec, while the d-axis current is controlled to zero. Fig. 9 shows how the two converters share the current evenly during both the transient and steady states conditions. The q-axis load current is successfully controlled to the desired values, as shown in Fig. 10.

V. EXPERIMENTAL VALIDATION

An experimental test rig comprised of two parallel DC-AC converters was designed and constructed to validate the operation of the proposed control strategy. Six discrete IGBTs

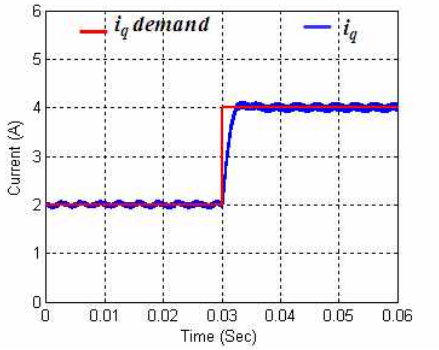

Fig. 10. q-axis load current transient response.

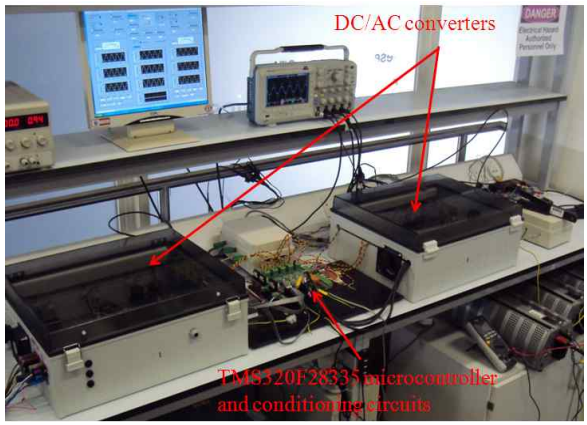

Fig. 11. Photograph of the experimental setup.

(IRG7PH35UD1PbF) were employed in each 1.25kVA inverter implementation. A three-phase inductive load was constructed using three single-phase resistors and inductors connected in series (10Ω+10mH). The control algorithm was implemented using one TMS320F28335DSP microcontroller. Fig. 11 shows a photograph of the experimental test rig, including the two converters and the DSP microcontroller board.

The DSP timers were configured to create a triangular output with a frequency of 12kHz. This triangular output is used for PWM generation and ADC converter synchronization. The ADCs for each converter are activated once every two carrier cycles. After reading all of the demanded and measured current values, the desired duty cycle is calculated and then updated. The sampling and calculation process introduce a delay of 3 carrier periods (i.e. 250μs) in the forward control path.

The calculated optimum PI gains (K_p=0.3 and K_i=105) were used again to obtain the system waveforms shown in Fig. 12. A step change in the desired q-axis current from 2A to 4A was applied, while the d-axis current was controlled to zero. The figure shows the converter and load current waveforms when the proposed control method was adopted. It is clear that the two converters share the load current evenly during both the steady state and transient conditions. The rms values of the two experimental converter currents were measured at 1.52A and

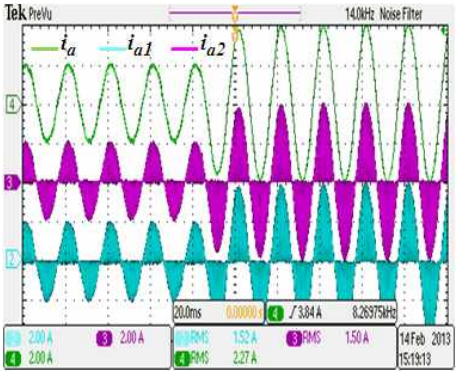

Fig. 12. Experimental load and converter current waveforms with the proposed control method (20ms/div; 2A/div).

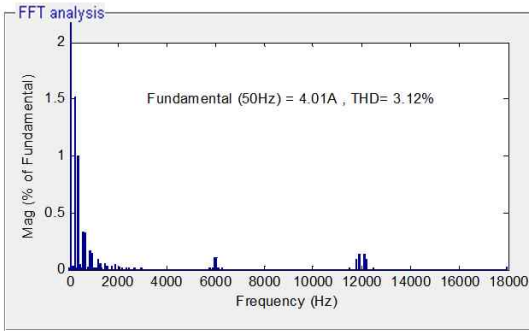

Fig. 13. Harmonic spectrum of experiment load current.

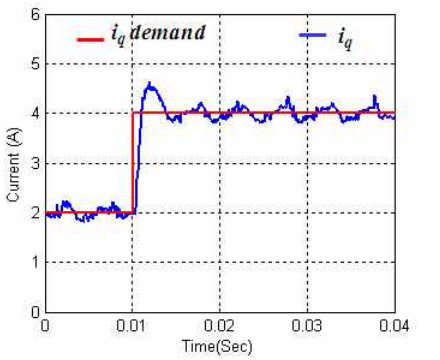

Fig. 14. Experimental q-axis load current transient response.

1.50A (Fig. 12). Load current data was collected from an oscilloscope using a sampling frequency of 625 kHz. It was then transferred to the Simulink environment were a FFT analysis was implemented. The harmonic spectrum of the load current is shown in Fig. 13. The figure includes a THD value of 3.12% calculated from the measured harmonic data. The q-axis load current transient response is depicted in Fig. 14.

VI. Conclusions

A new computationally efficient, current sharing controller for directly paralleled, synchronised three-phase DC/AC converters has been proposed in this paper. This controller eliminates the need for inter-module reactors and/or a separate circulating current controller. A stability analysis of the new controller is also presented. The proposed method divides the operating time equally between the parallel connected converters. As a result, the circulating current paths are eliminated and the connection of inter-module reactors becomes unnecessary, leading to big advantages in terms of the size and cost of the system. Based on local information, each converter uses only one dq synchronous frame current regulator to attain a desired current. The proposed current sharing strategy can lead to high values of the converter d*v*/d*t* if care is not taken to ensure that the stray inductance paths are minimised. The performance of the proposed controller is simulated and experimentally evaluated using a test rig comprised of two parallel connected 1.25kVA three-phase voltage fed converters.

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Bassim M. H. Jassim received his B.S. and M.S. degrees in Electrical Engineering from University of Baghdad, Baghdad, Iraq, in 1989 and 1996, respectively, and his Ph.D. degree in Electrical Engineering from Newcastle University, Newcastle upon Tyne, UK, in 2014. From 1989 to 1991, he was a Research Engineer with the commission of research and development at the Ministry of Industry, Baghdad, Iraq. From 1996 to 2001, he was a Researcher with the State Company for Electronic Systems, Baghdad, Iraq. In 2001, he joined the faculty of the Department of Electrical Engineering at the University of Baghdad, where he presently holds the position of Lecturer. His current research interests lie in the area of power electronics, including three-phase converter design and control, parallel converter operation and power factor regulation.

Bashar Zahawi received his B.S. and Ph.D. degrees in Electrical and Electronic Engineering from Newcastle University, Newcastle upon Tyne, UK, in 1983 and 1988, respectively. From 1988 to 1993, he was a Design Engineer with a UK manufacturer of large variable speed drives and other power conversion equipment. In 1994, he was appointed as a Lecturer in Electrical Engineering at the University of Manchester, Manchester, UK. From 2003 to 2014, he was a Senior Lecturer in the School of Electrical and Electronic Engineering, Newcastle University. In 2014, he joined the faculty of the Department of Electrical and Computer Engineering, Khalifa University, Abu Dhabi, UAE, where he presently holds the position of Professor of Electrical Power Engineering. His current research interests include power conversion and the application of nonlinear dynamical methods to electrical circuits and systems. Dr Zahawi is a recipient of the Crompton Premium award from the Institution of Electrical Engineers (IEE) and the Denny Medal from the Institute of Marine Engineering, Science and Technology (IMarEST). He is a chartered electrical engineer.

David J. Atkinson received his B.S. degree in Electrical and Electronic Engineering from Sunderland Polytechnic, Sunderland, UK, in 1978, and his Ph.D. degree from Newcastle University, Newcastle upon Tyne, UK, in 1991. He is currently a Senior Lecturer in the School of Electrical and Electronic Engineering, Newcastle University. He joined the university in 1987, after 17 years in the industry with NEI Reyrolle Ltd, Hebburn, UK, and British Gas Corporation, Cramlington, UK. His current research interests include the control of power electronics systems such as electric drives and converters. Dr. Atkinson is a chartered electrical engineer and a recipient of the Power Premium award from the Institution of Electrical Engineers (IEE).