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FPGA Based Robust Open Transistor Fault Diagnosis and Fault Tolerant Sliding Mode Control of Five-Phase PM Motor Drives

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Abstract

The voltage-source inverters (VSI) supplying a motor drive are prone to open transistor faults. To address this issue in fault-tolerant drives applicable to electric vehicles, a new open transistor fault diagnosis (FD) method is presented in this paper. According to the proposed method, in order to define the FD index, the phase angle of the converter output current is estimated by a simple trigonometric function. The proposed FD method is adaptable, simple, capable of detecting multiple open switch faults and robust to load operational variations. Keeping the FD in mind as a mandatory part of the fault tolerant control algorithm, the FD block is applied to a five-phase converter supplying a multiphase fault-tolerant PM motor drive with non-sinusoidal unbalanced current waveforms. To investigate the performance of the FD technique, the fault-tolerant sliding mode control (SMC) of a five-phase brushless direct current (BLDC) motor is developed in this paper with the embedded FD block. Once the theory is explained, experimental waveforms are obtained from a five-phase BLDC motor to show the effectiveness of the proposed FD method. The FD algorithm is implemented on a field programmable gate array (FPGA).

Key words: Fault detection, Fault-tolerant converters, FPGA, Multiphase power converters, Open switch fault, PM motor drive

I. INTRODUCTION

The motor drives used in electric vehicles, hybrid electric vehicles, space craft, the chemical industry, electric aircraft and transportation should meet a high level of safety and reliability. The fault-tolerant concept (e.g. multiphase permanent magnet motor drives) is an effective solution to address these criteria [1]. In order to operate a fault-tolerant system, fast FD and isolation of faulty components are of paramount importance [2]. The VSIs supplying motor drives are prone to various faults. Therefore, they should be equipped with a FD section.

A comprehensive review of the fault types and detection methods for a VSI has been presented in [3]. The fault types in power converters can be divided into open switch and short circuit faults. Short circuit faults are often destructive.

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In the case of this type of fault, a system should be shut down immediately after FD. If it is detected quickly enough, typically less than10 μs in case of an IGBT, it is possible to avoid system shutdown. Such fast detection is necessary to operate fault-tolerant converters with an extra leg [3]. It should be noted that nowadays, short circuit FD and protection methods have been successfully implemented in high performance custom designed commercial drivers.

On the other hand, open circuit faults are less destructive. The primary effect of such faults is a reduction in system performance. However, if they are not detected, secondary faults may occur [3]. Three different research lines have been developed in the literature to detect open switch faults: signal (i.e. the current or voltage of a power converter) based methods, model based methods and reference based methods [4].

In terms of the model based method, a simple and fast open switch FD method was presented in [5]. A model reference adaptive system for permanent magnet synchronous motor (PMSM) drives was used to predict the motor current. The FD index was defined as the difference between the real and estimated current. This method is cheap since it does not

require extra sensors. However, it is well-known that the prediction of the load response is sensitive to load parameter uncertainties.

A simple, fast, efficient and robust detection method can be achieved if the difference between the load current and the reference value is defined as the FD index. This technique is known as the reference based FD method. To make the diagnostic variable independent from the load parameters, the residue value has been normalized with respect to the average absolute value of the load current [6]. However, the application of this method is limited to systems with a closed loop control.

The signal based FD method is another simple detection method. The inputs of this method are the output voltage or current of the power converter. Both methods have been investigated in the literature. The voltage based methods are fast, simple and efficient [7]-[10]. Detection times of less than 10 μs have been presented in the literature [7], [8]. However, the presented methods are not cost effective, since it is necessary to use extra sensors in the power converters.

The signal based FD method can also be implemented with the converter output current. Since measurements of the converter output current are usually necessary for control purposes, it is not mandatory to utilize additional sensors to detect faults. Different FD methods based on the output current of power converters have been presented in the literature. Tools such as Park's vector modulus, the normalized dc current method, the slope method, the frequency method, and wavelet transformation [3] are used in these methods to define the FD index. However, all of these methods have some drawbacks such as slow FD, single switch FD, low robustness to load transients and complexity. In this category, several high performance FD methods have recently been presented in the literature. The methods proposed in [4], [11], and [12]-[16] are among the best of these. The diagnostic variables in [4] and [12] are based on the normalized average current with respect to the absolute average current value. In [13], the diagnostic variable is based on Park's vector phase angle. In all of these studies, the input current is a three-phase sinusoidal balanced current. However, in case of multiphase fault-tolerant converters, the input current can be a non-sinusoidal unbalanced current. Due to these characteristics, the presented methods show poor performance in some fault scenarios in multiphase converters. In order to improve the robustness of the FD method in case of load transients, the phase currents have been normalized with respect to Park's vector modulus in [12]. However, this method is less effective in multiphase converters with an unbalanced non-sinusoidal current. Moreover, in multiphase converters, there is more than one equivalent perpendicular page after applying Park's transformation. As a result, the calculation of Park's vector modulus is more complicated.

Nuno et al. presented a high performance FD method to diagnose faults in permanent magnet synchronous generators [13]. According to this method, it is possible to calculate the phase angle in the stationary reference frame in three-phase converters. After applying Park's transformation to multiphase currents, there is more than one equivalent perpendicular page in the stationary reference frame. To develop this method in a multi-phase converter, several phase angles should be considered at the same time to define the FD index. A FD method based on multiple fault indexes (i.e. the estimated phase angle and the normalized phase currents) has been presented in [15]. This method is computationally demanding. The application of this method in multiphase drives is more challenging, since there are multiple harmonics in the phase current.

These concerns are taken into account and an effective FD method is proposed in this paper. The current signals in the *abcde* frame are directly used to define the FD index.

To realize the continuous operation of a fault tolerant drive, the FD block should be combined with a fault tolerant control algorithm. Although the fault tolerant control of multiphase machines in the steady state has been well studied in [17]; there is a lack of knowledge on online FD and fault tolerant control. This case is considered as another concern of the research in this paper.

Two contributions are shown in this paper. Firstly, a new open transistor FD method in VSIs is proposed. Secondly, in order to evaluate the performance of the FD method in a closed loop system, a SMC is developed to implement the inner controller of a five-phase PM motor drive. The proposed FD block is included in the control algorithm. This paper is an improved version of the FD method presented in [18]. The proposed FD algorithm is implemented on an FPGA due to its high processing power and its large number of input-outputs.

The rest of this paper is presented as follows. In section II, a case study, fault scenarios and the proposed FD method are explained. The proposed FD method is included in the fault-tolerant SMC algorithm of a five-phase BLDC motor in section III. In order to validate theory and to investigate the performance of the presented FD method, experimental results are shown in section IV. In section V, some conclusions and remarkable points are presented.

II. Proposed FD Method

Due to their fault tolerant capabilities, five-phase permanent magnet (PM) motors can maintain a high level of safety and reliability [19]. To implement a fault-tolerant algorithm, such systems should detect and isolate faults and continue operation with a minimal derating. To achieve these goals, a multiphase fault-tolerant converter with FD and isolation ability is considered here, as shown in Fig. 1. It

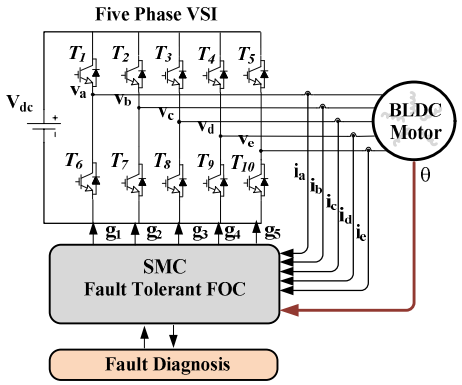


Fig. 1. Configuration of the fault-tolerant power converter.

should be noted that the converter output current in this specific application can be non-sinusoidal and unbalanced under different operational modes.

In terms of a multiphase converter, the following faulty modes can occur: single switch open circuit, single phase open circuit, multiple open switch and open phase faults. It should be noted that the number of faulty modes in a multiphase converter can be much more than that of a three-phase converter.

Considering practical cases, a five-phase BLDC motor drive can tolerate up to two faulty phases.

To evaluate a FD method, some performance criteria should be considered. Firstly, it should be fast, which means that the FD method should detect faults with a minimum time after a fault. After FD, to realize fault-tolerant operation, it is necessary to localize and isolate the faulty switch. Therefore, fault localization is another performance criterion. Thirdly, the FD method should be robust to transients, which means that the FD method should avoid false alarms during load transients. It should be noted that the transient type in a motor drive may occur due to speed or torque reference variations. Fourthly, the FD method should be adaptable, which means that the FD strategy can be used in any converter configuration such as three-phase, four-phase, five-phase or any multiphase converter. Finally, simple implementation is an important advantage for a FD strategy. Regarding all of the aforementioned criteria, a novel FD method is proposed as follows.

To detect a fault, it is important to define a FD index. In practical applications, the converter output current is usually a noisy signal. Prior to signal processing, it is necessary to apply a low pass filter to eliminate the non-desirable components in the current spectrum. It is recommended to set the cut off frequency of the filter at least 10 times the fundamental frequency. If the cut off frequency is chosen too high, it cannot eliminate distorting components effectively. On the other hand, if a low value is selected, filter imposes a long delay on the filtered signal. This delay can slow down the detection speed which is a critical criterion in a FD method.

To define the FD index, the phase angle of the converter output current is estimated in this paper. Being independent from the load operational conditions makes the phase angle a unique variable to define the FD index. Its value varies between $-\pi$ and π under normal operational conditions.

After filtering the signal, the current signal and its delayed current sample during a quarter of one fundamental cycle T are divided. The FD index is calculated from inverse tangent of the calculated signal as:

$$D = \tan^{-1}\left(\frac{i(t)}{i(t-T/4)}\right). \tag{1}$$

where i is the current signal of the power converter, and D is the FD index. Under healthy conditions, the D value varies between $-\pi$ and π. Under the faulty mode, the phase current is zero during half of a period in case of a single switch fault. Under an open phase fault, the phase current is zero. Regarding single switch fault and from (1), the D value is:

$$D = \begin{cases} -\pi, -\frac{\pi}{2}, 0, \frac{\pi}{2}, \pi & \text{single switch fault} \\ 0 & \text{open phase fault} \end{cases} \tag{2}$$

Once the D value is equal to the faulty mode, the FD is done after a delay. To realize this purpose, a new function is defined as:

$$y = \begin{cases} 1 & |D| = 0, \frac{\pi}{2}, \pi \\ 0 & otherwise \end{cases} \tag{3}$$

After that, the average value of y is calculated during one cycle as:

$$x = \frac{1}{T}\int_0^T y dt. \tag{4}$$

The x value is zero under healthy conditions. Its value increases to one in case of a fault. This value is compared with a threshold value to detect faults. If the x value is higher than the threshold value, then a fault is detected. It should be noted that the theoretical value of the threshold value is zero. However, in practice due to noise and calculation accuracy, a higher value is chosen.

In order to maintain the fault-tolerant concept in multiphase power converters, it is necessary to localize the faulty switch. After that, the faulty component can be replaced with an extra leg or isolated completely from the converter. Here a simple approach based on the current polarity is applied to localize the faulty component. According to this method, the input phase current is passed through a weight function. This function estimates the input current i to values between -1 and 1 as follows:

$$S(i(t)) = \begin{cases} 1 & i(t) \geq 0.1 \\ 0 & -0.1 < i(t) < 0.1 \\ -1 & i(t) \leq -0.1 \end{cases} \tag{5}$$

where current values less than 0.1 A (i.e. a typical threshold

value) are considered equal to zero. However, in practice a different value can be chosen for this threshold. The fault localization block samples and calculates the average value of the converter output current simplified by equation (5) during one fundamental cycle as follows:

$$\bar{I} = \frac{1}{T}\int_o^T S(t)dt. \quad (6)$$

where $\bar{I}$ is the average value of the phase current in one fundamental period. The $\bar{I}$ value is compared with a positive and a negative threshold value. If the average value is higher than the positive threshold, then the lower switch is the faulty component at the corresponding phase. Similarly, if the average value is lower than the negative threshold, then the upper switch is the faulty component. The absolute threshold value chosen in this paper is 0.5. Under an open phase fault, the D value approaches zero. This advantage is utilized to localize open phase faults in this paper. The average value of D is calculated during one fundamental cycle. If this value is equal to zero, the fault type will be open phase.

For clarification, each faulty mode in one leg of the power converter is shown by a numerical code. Codes -1, 1, and 2 correspond to an upper switch fault, a lower switch fault and an open phase fault, respectively.

The FD block, the fault localization block and the diagnostic variable waveforms under different faulty modes are shown in Fig. 2. In terms of the proposed FD method, its main advantage is its simple implementation. Since the FD index is calculated from the phase angle, it is robust to high load transients. On the other hand, this method is adaptable, since no special transformations related to the converter topology are used. This method can be used in a two-level converter with any number of phases. Moreover, this method only requires the measurement of the converter output current. Therefore, it can be used in a system with an open loop or a closed loop control. Finally, unlike the methods presented in the literature, it is possible to detect an open phase fault without using an auxiliary variable.

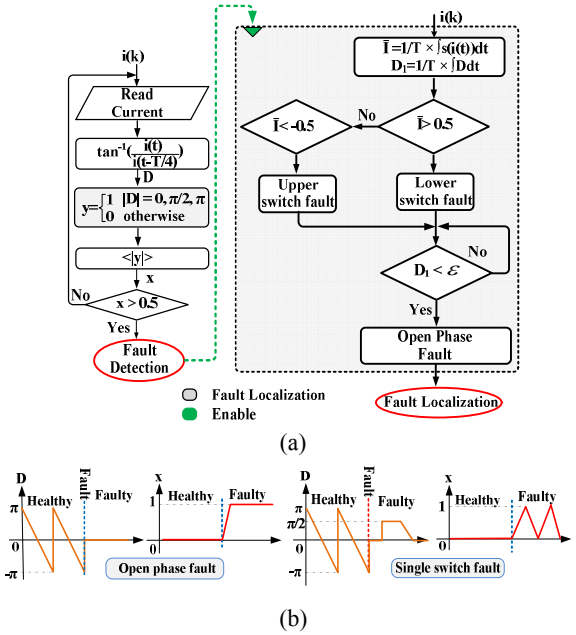


Fig. 2. Proposed FD method. (a) FD block diagram. (b) FD index.

TABLE I
OPTIMIZED PHASE CURRENTS WITH ISOLATED NEUTRAL

Current	A	B	C	D	E
one faulty phase					
I_1(PU)	0	0.99	0.99	1	0.98
θ_1	-	51	137	232	-41
I_3(PU)	0	0.17	0.08	0.09	0.19
θ_3	-	23	52	186	-19
two adjacent faulty phases					
I_1(PU)	0	0	0.59	0.95	0.67
θ_1	-	-	82	218	0
I_3(PU)	0	0	0.12	0.29	0.16
θ_3	-	-	44	102	41
two nonadjacent faulty phases					
I_1(PU)	0	0.99	0	0.98	0.99
θ_1	-	77	-	2	-42
I_3(PU)	0	0.16	0	0.19	0.17
θ_3	-	15	-	55	-21

III. THE FAULT-TOLERANT SMC OF A FIVE-PHASE BLDC MOTOR USING THE PROPOSED FD METHOD

In this part, the presented FD method is used to maintain the fault-tolerant concept in a five-phase BLDC motor with a closed loop control.

A five-phase PM motor drive can be operational with up to two faulty phases [19]. To achieve the desired torque and speed control, it is necessary to calculate the reference currents of the motor under healthy and faulty modes. Recently, a considerable amount of research has been conducted on this subject. Salehi et al. presented an optimization algorithm to calculate the reference currents under healthy and faulty modes [20]. According to this method [20], a fault-tolerant control with a ripple free torque is achieved. Here, the final results of the optimized reference currents are summarized in Table I.

In order to set the reference torque and speed in a five-phase PM motor drive, a closed loop control can be used. Field oriented control (FOC) is used to control the drive. To implement the FOC, an inner controller is used to track the reference currents. According to the analysis presented in [20], a ripple free torque using the optimized reference currents in table I can be achieved. SMC is used in this paper to set the current references. A block diagram of the fault-tolerant control method is shown in Fig. 3. As can be seen, the SMC provides the reference voltage for the space vector

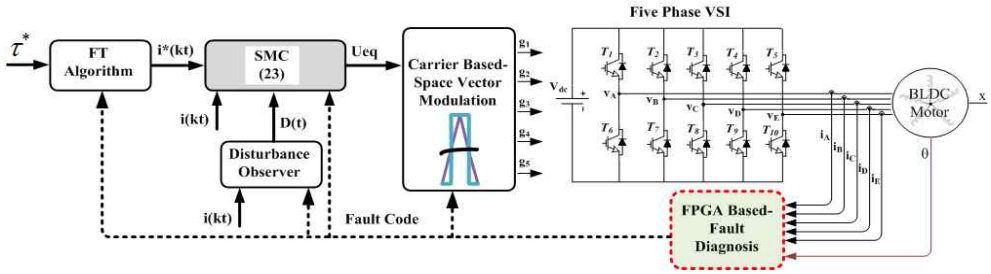


Fig. 3. FD and the fault-tolerant control.

modulator. Therefore, the switching frequency is constant.

The theory of the SMC method is presented in the following. It should be noted that the focus of this paper is on the inner controller of the motor. Its effect on the performance of the FD method is evaluated in the rest of this paper.

In the following section, the basic equations of a five-phase BLDC motor are reviewed.

A. Dynamics Modelling of Five-Phase BLDC Motors

Several methods have been presented in the literature to model multiphase motors under healthy and faulty conditions [21]-[23]. The models can be implemented either in the stationary frame [21], in the synchronous reference frame [22] or in the abcde reference frame [23]. In this paper, the modelling method presented in [23] is used due to its simplicity under healthy and faulty conditions.

The model of a five-phase BLDC motor with a trapezoidal back EMF under the healthy mode is:

$$\begin{bmatrix} v_{ax}-e_a \\ v_{bx}-e_b \\ v_{cx}-e_c \\ v_{dx}-e_d \\ v_{ex}-e_e \end{bmatrix} = \begin{bmatrix} r_a & 0 & 0 & 0 & 0 \\ 0 & r_b & 0 & 0 & 0 \\ 0 & 0 & r_c & 0 & 0 \\ 0 & 0 & 0 & r_d & 0 \\ 0 & 0 & 0 & 0 & r_e \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \\ i_d \\ i_e \end{bmatrix} + \begin{bmatrix} l_a & m_1 & m_2 & m_2 & m_1 \\ m_1 & l_b & m_1 & m_2 & m_2 \\ m_2 & m_1 & l_c & m_1 & m_2 \\ m_2 & m_2 & m_1 & l_d & m_1 \\ m_1 & m_2 & m_2 & m_1 & l_e \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_a \\ i_b \\ i_c \\ i_d \\ i_e \end{bmatrix}. \tag{7}$$

where i_j is the phase current, v_{jx} is the phase to neutral voltage of each phase, r_j is the phase equivalent resistance, l_j is the phase equivalent inductance, m_1 is mutual inductance between two-adjacent phases, m_2 is mutual inductance between two-nonadjacent phases, and e_j is the back EMF in each phase of the motor where j = {a, b, c, d, e}. The back EMF will be estimated as follows:

$$\begin{aligned} e &= \lambda_{m1}\omega_e \cos(\theta - \frac{2\pi n}{5}) \\ &+ \lambda_{m3} 3\omega_e \cos(3(\theta - \frac{2\pi n}{5})),\ n = 0,1,2,3,4. \end{aligned} \tag{8}$$

where λ_{m1} and λ_{m3} are the first and third harmonic amplitudes of the rotor flux linkage, ω_e is the electrical rotational velocity, Θ is the rotor electrical angle, and *n=0, 1, 2, 3, 4* represent the phases *a*, *b*, *c*, *d*, *e*, respectively.

B. Model of the Motor under Faulty Mode

Under an open phase fault, the neutral voltage of a motor floats due to the back electromotive force in the faulty phase [21], [23]. Therefore, the same healthy model of the machine in (7) can be used in the faulty mode. It is necessary to consider the induced voltage in the faulty phases. This voltage is shown by v_n in this paper. Its value is calculated similarly to [23].

Under faulty conditions, the row and column related to the faulty phase can be removed from (7). Therefore, the machine model under one faulty phase *A* is modified as:

$$\begin{bmatrix} v_{bx}-e_b \\ v_{cx}-e_c \\ v_{dx}-e_d \\ v_{ex}-e_e \end{bmatrix} = \begin{bmatrix} r_b & 0 & 0 & 0 \\ 0 & r_c & 0 & 0 \\ 0 & 0 & r_d & 0 \\ 0 & 0 & 0 & r_e \end{bmatrix} \begin{bmatrix} i_b \\ i_c \\ i_d \\ i_e \end{bmatrix} + \begin{bmatrix} l_b & m_1 & m_2 & m_2 \\ m_1 & l_c & m_1 & m_2 \\ m_2 & m_1 & l_d & m_1 \\ m_2 & m_2 & m_1 & l_e \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_b \\ i_c \\ i_d \\ i_e \end{bmatrix} - v_n \begin{bmatrix} 1 \\ 1 \\ 1 \\ 1 \end{bmatrix}. \tag{9}$$

$$v_n = \frac{m_1}{4}(\frac{di_b}{dt} + \frac{di_e}{dt}) + \frac{m_2}{4}(\frac{di_c}{dt} + \frac{di_d}{dt}).$$

Similarly, the model can be modified in the case of two open phase faults. In the case of an open phase fault in phases *A* and *B*, the model is recalculated as:

$$\begin{bmatrix} v_{cx}-e_c \\ v_{dx}-e_d \\ v_{ex}-e_e \end{bmatrix} = \begin{bmatrix} r_c & 0 & 0 \\ 0 & r_d & 0 \\ 0 & 0 & r_e \end{bmatrix} \begin{bmatrix} i_c \\ i_d \\ i_e \end{bmatrix} + \begin{bmatrix} l_c & m_1 & m_2 \\ m_1 & l_d & m_1 \\ m_2 & m_1 & l_e \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_c \\ i_d \\ i_e \end{bmatrix} - v_n \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix}. \tag{10}$$

$$v_n = \frac{(m_1+m_2)}{3}\frac{di_c}{dt} + \frac{2}{3}m_2\frac{di_d}{dt} + \frac{(m_1+m_2)}{3}\frac{di_e}{dt}.$$

The nominal model of a motor without considering disturbances and parameter uncertainties can be rewritten from (7) under healthy and faulty modes as:

$$\begin{aligned} &\dot{x} = Ax + Bu. \\ &x = [i_a\ i_b\ i_c\ i_d\ i_e]^T, \\ &u = [v_{ax}-e_a, v_{bx}-e_b, v_{cx}-e_c, v_{dx}-e_d, v_{ex}-e_e]^T \end{aligned} \tag{11}$$

where A=-R/L and B=1/L, where R and L are the resistance and inductance matrixes of the machine, respectively.

C. Sliding Mode Control

The SMC of a five-phase BLDC motor is explained in this section. The purpose for this is to calculate the control law. The control law is designed to enforce the system states on

the sliding surface and to remain on the surface.

Due to its robustness to parameter uncertainties and external disturbances, simple implementation, and fast convergence rate [24], [25], [26], the nonlinear SMC is used here to implement the inner controller of the fault-tolerant FOC algorithm.

In industrial applications, a PM motor is considered as a system with mismatched uncertainties [27]. Therefore, it is important to reduce or eliminate the effects of the uncertainties on controller performance.

The SMC algorithms presented in the literature can deal with these problems with three different methods [27]. The first solution is to focus on system stability using classical control tools such as the adaptive approach. The main drawback of this approach is that the uncertainties should vanish, which is not possible in practical applications. The second approach is using an integral SMC based on a high frequency switching gain and integral term. Although this method is more practical, the controller performance is reduced due to the integrator term. A large overshoot and a long settling time are the main drawbacks among others. At the expense of higher chattering levels and reduced nominal controller performance, both of these methods can be robust to uncertainties. The third approach is using a disturbance observer integrated into the SMC. The main advantages of this method in comparison to other two are its reduced chattering problem and better nominal performance [27]-[29].

In case of an inverter fault, a disturbance appears in the system. In this paper, a SMC with an integrated disturbance observer is used to set the reference currents of the five-phase BLDC motor. The observer can deal with both uncertainties and disturbances due to faults in the inverter.

The SMC can be achieved in two steps. In the first step, the sliding surface is chosen.

To design the controller, the error function and the sliding surface are defined as follows:

$$\delta = [i_a^* - i_a \;\; i_b^* - i_b \;\; i_c^* - i_c \;\; i_d^* - i_d \;\; i_e^* - i_e]^T. \tag{12}$$

$$s = \delta. \tag{13}$$

where s is the sliding surface, δ is the error function, and i^* is the reference current.

In the second step, a control law is calculated so that the sliding surface is achieved.

To achieve the sliding surface, the exponential approach law is used as:

$$\dot{s}(t) = -\varepsilon \times Sat(s(t)) - Ks(t). \tag{14}$$

where K>0, 0<ε<1 and Sat is a saturation function defined as:

$$Sat(x) = \begin{cases} 1 & x \geq 1 \\ x & -1 < x < 1 \\ -1 & x \leq -1 \end{cases} \tag{15}$$

The dynamic of the control law is affected by K and ε [30]. For higher K values, the control law will be less sensitive to uncertainties. On the other hand, by increasing the ε value, the controller will be faster. However, the chattering level on the controller output will be higher. To design these parameters, a trade-off should be made to ensure desirable dynamics and a low chattering level on the control signal.

By solving the differential equation in (14), the time to reach the sliding surface is:

$$t = 1/\varepsilon \times (s(0) + K/2 \times s^2(0)). \tag{16}$$

From (16), it can be concluded that by increasing ε and decreasing K, the reaching time is reduced. At the same time, the robustness is increased. However, the chattering level on the control state increases.

The SMC law in (14) can be rewritten in discrete form as:

$$s(k+1) - s(k) = -\varepsilon T_e Sat(s(k)) - KT_e s(k). \tag{17}$$

where T_e is the sampling period.

When the control state is driven on the sliding surface, *s(k)* is a small positive or a small negative value. Therefore, (17) can be rewritten as:

$$s(k+1) = \pm \varepsilon T_e. \tag{18}$$

According to (18), the sliding band (i.e. chattering level) is a fixed value equal to εT_e. The chattering level can be decreased by decreasing ε and T_e.

D. Inner Current Controller Design Based SMC

To achieve this goal, the ideal model of the machine in (11) is rewritten considering parameter variations and external disturbances as follows:

$$\dot{x} = Ax + Bu + D(t). \tag{19}$$

where all of the uncertainties are lumped as *D(t)*.

In this section, the equivalent control law is calculated. The derivative of the sliding surface in (13) is obtained as:

$$\dot{s} = \dot{\delta}. \tag{20}$$

The derivative of the current error in (12) and the reaching law in (14) are substituted in (20) as:

$$-\varepsilon \times Sat(s(t)) - Ks(t) = (\dot{i} - \dot{i}^*). \tag{21}$$

By substituting the machine ideal model from (19), (21) can be rewritten as:

$$-\varepsilon \times Sat(s(t)) - Ks(t) = Ax + Bu - \dot{i}^* + D. \tag{22}$$

From (22), the equivalent control law is calculated as:

$$U_{eq} = -B^{-1}(Ax - \dot{i}^* + D + \varepsilon Sat(s(t)) + Ks(k)). \tag{23}$$

where U_{eq} is the reference voltage. This voltage should be produced by the inverter. The calculated reference voltage is used as the input of the space vector modulator in order to produce the desired reference voltages of the inverter.

As can be seen from (23), a disturbance is included in the reference voltage. Therefore, the controller should be robust to disturbances. To achieve this goal, a disturbance observer is designed in this paper in the following section.

It should be noted that the calculation of U_{eq} is the same under both healthy and faulty conditions. The only difference is that matrixes A and B of the machine model need to be

replaced depending on each operational mode of the motor (i.e. healthy, single phase faulty or two-phase faulty).

E. Sliding Mode Disturbance Observer

According to the proposed approaches in [26] and [28], an observer is designed in this paper to estimate disturbances. In order to reduce the effect of uncertainties, a sliding mode observer is designed to estimate the uncertainties in (23). The sliding surface is designed as:

$$s = \delta + \lambda \int \delta. \tag{24}$$

where λ is a positive constant, and δ is the difference between the estimated and real current.

Due to the integrator term in (24), a zero steady state error can be achieved. The reaching law is designed similar to (14). The observer is designed as:

$$\dot{\hat{x}} = A\hat{x} + Bu - \varepsilon \times Sat(s(t)) - Ks(t). \tag{25}$$

where upper letter ^ is used to show the estimated states.

In order to evaluate the stability of the designed observer, the Lyapunov function is defined as:

$$V = \frac{1}{2}s^2. \tag{26}$$

The derivative of (26) is calculated as:

$$\dot{V} = s\dot{s}. \tag{27}$$

According to the Lyapunov stability criterion, the necessary condition to reach the sliding surface is [26]:

$$s(t).\dot{s}(t) < 0. \tag{28}$$

The derivative of the sliding surface in (28) can be rewritten from (19) and (25) as:

$$\dot{\delta} + \lambda\delta = A(\hat{x} - x) + \varepsilon Sat(s(t)) + Ks(t) - D. \tag{29}$$

From (29), (28) can be rewritten as:

$$((\delta + \lambda \int \delta)(A\delta + \lambda\delta + \varepsilon Sat(s(t)) + Ks(t) - D) < 0. \tag{30}$$

Under steady sate conditions, the sliding surface and its dynamics will reach zero. Therefore, the estimated disturbance can be obtained from (29) as:

$$\hat{D} = Sat(s(t)) + Ks(t). \tag{31}$$

F. Stability Analysis of the Controller

In order to evaluate the stability of the designed controller, the Lyapunov function and its derivative are defined to be the same as (26) and (27). In addition, the sliding surface is same as (12).

According to the Lyapunov stability criterion, the necessary condition to reach the sliding surface is [26]:

$$s(t).\dot{s}(t) < 0. \tag{32}$$

From (19), (32) can be rewritten as:

$$\delta(A\delta - \varepsilon Sat(s(t)) - Ks(t)) < 0. \tag{33}$$

From (33), it can be seen that by choosing positive values for *K* and *ε,* the controller will be robust.

It should be noted that under healthy conditions, the sliding surface approaches a small value. This value depends on the controller design. Under faulty conditions, its value is increased significantly since an inverter is non-controllable. This means that the controller performance in the presence of a fault in the inverter may be reduced remarkably.

This can affect the performance of the FD block. Once the motor phase currents are equal to the reference currents, the FD index in (1) can be calculated accurately. In the case of SMC, it can still maintain a good tracking performance even under the faulty mode. Therefore, this control method was used in conjunction with the proposed FD block in this paper.

IV. Experimental Results

In order to validate the proposed theory, experimental results are obtained. The FD method is included in the fault-tolerant SMC algorithm of a five-phase BLDC motor. The experimental setup is shown in Fig. 4(a). The motor parameters are shown in table II.

The test motor has an outer rotor in-wheel structure. This configuration is applicable to electric vehicles. The control algorithm is implemented in a dSPACE model ds1005, and the FD algorithm is implemented on an FPGA. As can be seen, the multiphase motor is connected to a three-phase PMSM motor operating as a load. This motor is controlled by a National Instrument control board known as a compactRio (i.e. cRio). The dc-link voltage of the five-phase inverter is 24 V. The sampling frequency is 4 kHz, and the switching frequency is 4 kHz. The motor speed is set at 50 rpm by the load motor.

The results are presented in four parts. In the first step, the implementation of the FD algorithm on a FPGA is discussed. In the second step, the performance of the FD method is evaluated under different faulty conditions. In the third step, a comparison is made between the proposed FD method and the other methods in the literature. In the last step, the FD method is used to implement the fault-tolerant control algorithm in real time. In the first step a fault is detected. After that, depending on the faulty mode, appropriate remedial strategies are taken to maintain continuous operation of the motor.

A. Implementation of the FD Algorithm on a FPGA

Nowadays, FPGAs are finding more industrial applications due to their decreasing cost and increasing logic resources [31], [32]. Due to their high processing power and large number of digital I/Os, a FPGA is chosen to implement the FD algorithm in this paper.

It should be noted that the FPGA is a powerful candidate for FD in power electronics and motor drives. Due to its high processing power, the algorithms of the FD in power converters and motors can be implemented on a PGA. On the other hand, it can sample a signal with a very high frequency. This is very important for the detection of and protection from short circuit faults in power converters. Moreover, due

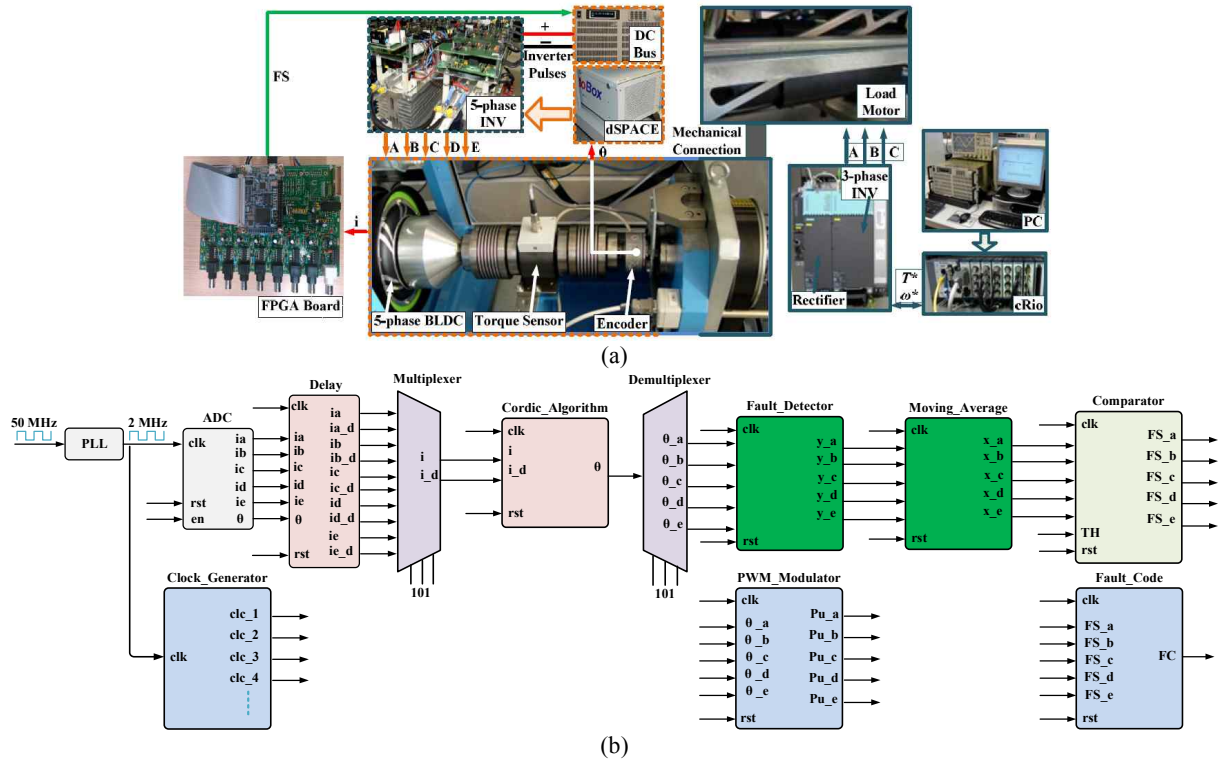
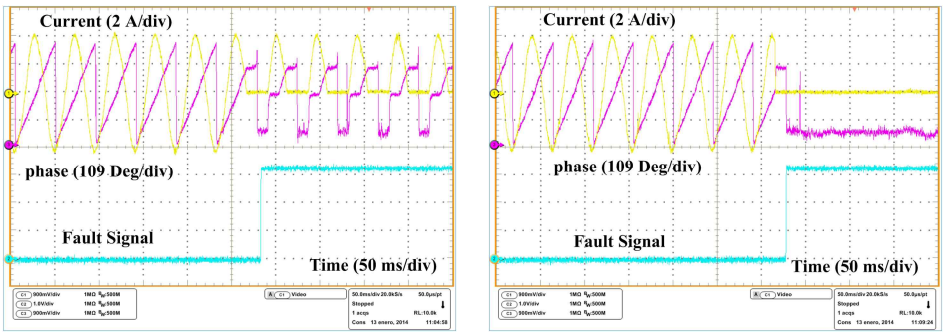


Fig. 4. (a) Experimental setup. (b) Hardware implementation of the FD block on FPGA.



(a) (b)

Fig. 5. Experimental results of FD with FPGA. (a) Results of the FD under lower open switch fault. (b) Results of the FD under open phase fault.

TABLE II
MOTOR PARAMETERS

Number of Pole Pairs		26
Stator Resistance (Ω)		0.1
Stator Inductance (μH)	l	408
	m_1	8
	m_2	8
Nominal Torque (Nm)		8
Nominal Power (Watt)		350
Nominal Phase Current (A-rms)		5
Nominal Phase Voltage (V-rms)		16
Nominal Speed (rpm)		400
Permanent Magnet Flux (Wb)		0.48
Moment of Inertia (μkgm^2)		235

to its high number of input-outputs, a lot of signals can be measured to implement the FD algorithm. In terms of highly reliable motor drives (e.g. the fault tolerant motor drives applicable to electric vehicles), there are a lot of feedbacks from the fault detectors already embedded in the hardware (e.g. the over current sensor, the short circuit signal from the switch gate driver, the over voltage sensor, temperature sensors, etc.). In a fault tolerant system, a very fast and powerful processor is necessary to manage and protect from these faults. A low cost FPGA is a high performance candidate to implement the FD algorithm. Therefore, there was a strong motivation to use a FPGA for implementing the FD algorithm in this paper.

The FD algorithm was implemented on an EP4CE22F17C5N FPGA Cyclone IV from Altera Company,

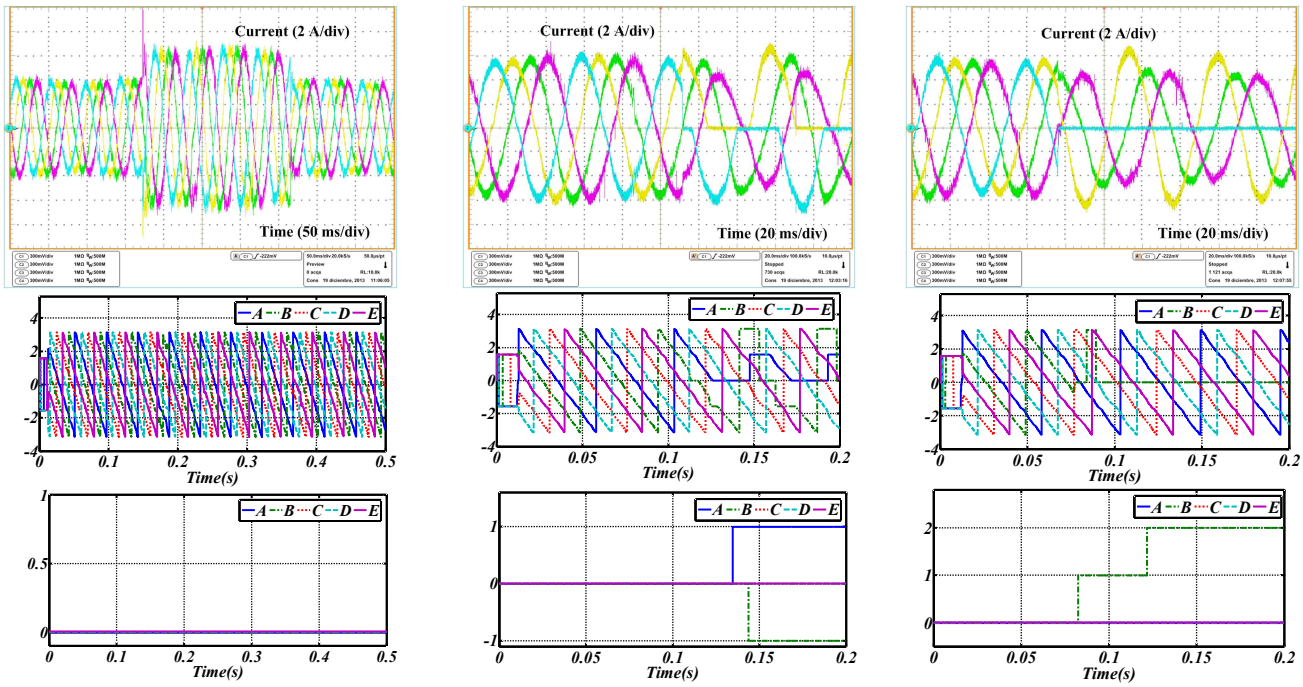


Fig. 6. Experimental results of FD. (a) Performance evaluation of FD method under load transients. (b) Single switch FD under healthy mode. (c) Open phase FD under healthy mode.

which is available on a DE0_Nano board. The hardware implementation of the FD algorithm on a FPGA is shown in Fig. 4(b). The motor phase currents are sampled at 15 kHz. The sampled signals are stored in a 12 bit register. According to the FD index in (1), the phase currents are delayed during one-quarter of the fundamental cycle. This block is denoted by the Delay in Fig. 4(b).

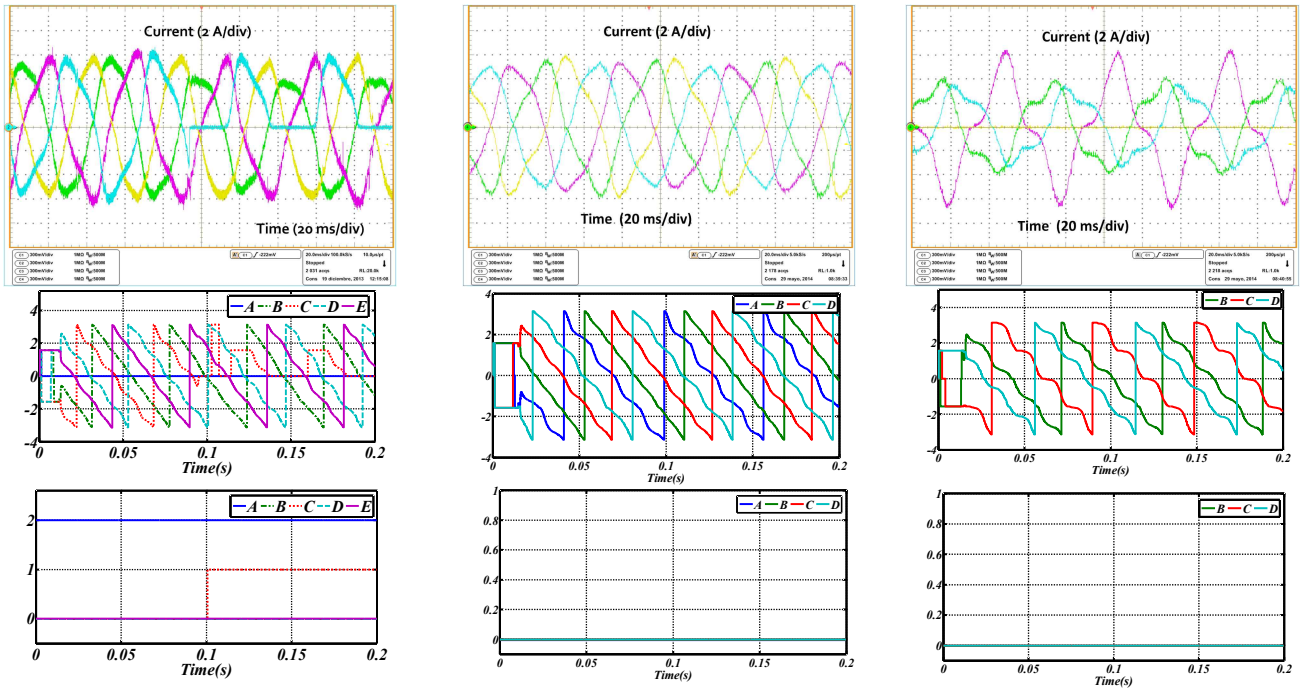
After that, the phase angle of the current signal is estimated by the Inverse Tangent function. This function was implemented on a FPGA based on the Cordic algorithm. The inputs to the FD method are the real and delayed current in each phase of the motor. All of the codes were written in Verilog HDL. In order to optimize the resources, only one block was used to implement the Cordic algorithm. The phase currents are sent to this block by a multiplexer. After estimation of the phase angle, the phase angle of each phase is extracted by a demultiplexer.

After the phase angle estimation, the Fault_Detector block described in (3) is used to determine if there is a faulty sample. The average value of the fault signal is calculated during one fundamental cycle by a Moving_Average block. The output of this block was described in (4). Finally to generate the fault signal (FS), the x value is compared with a threshold value. The threshold value can be set by a 12 bit register TH.

In order to simplify the evaluation of the developed algorithm, a simple pulse width modulation (PWM) block shown by the PWM_Modulator in Fig. 4(b) was developed in the FPGA. Here, any signal can be modulated by this block. The digital outputs are filtered by a simple LC filter on the developed FPGA board. This method is quite suitable for evaluating the efficiency of the developed algorithm step by step.

To further improve the hardware implementation of the FD algorithm, a simple counter shown by the Clock_Generator block in Fig. 4(b) was used to generate the custom clocks for each block of the algorithm. Moreover, the fault signals in all of the phases were sent to the Fault_Code block. This block produces a simple numerical code for each operational mode of the motor drive. By using this code, reconfiguration of the whole system can be done quickly.

To validate the performance of the implemented algorithm, two case studies are considered. In the first case, the healthy mode control of the motor is implemented. After five cycles, a lower switch fault is forced into phase a. To show the effectiveness of the developed algorithm on a FPGA, the FD index and fault signal are converted to analog signals. A summary of the resource utilization is shown in table III. The experimental results of this case are shown in Fig. 5(a). As can be seen, a fault is detected during a quarter of one cycle. The estimated phase angle value is constant after the fault. In the second case study, an open phase fault is forced into the inverter, and the resultant waveforms are shown in Fig. 5(b). As can be seen, a fault is detected during less than a quarter of one fundamental cycle. The phase angle value after the fault is equal to 45 degrees. According to the presented experimental results, both open switch and open phase faults were effectively detected. In addition, the phase angle of the motor current was successfully estimated.



(a) (b) (c)

Fig. 7. Experimental results of FD (a) under faulty mode (b) under one faulty phase mode (c) under two-adjacent faulty phase mode.

TABLE III
UTILIZATION OF RESOURCES IN FPGA

Logic utilization	Used	Available	Utilization(%)
Combinational functions	1673	22320	7
Total registers	1139	22320	5
Pins	19	154	12
Memory bits	4896	608256	1
PLL	1	4	25

As discussed in section II, the estimated phase angle under the faulty mode is a constant value equal to 0, π/2, and π. However, in the experimental results, it approached to π/4. This is mainly due to the specific implementation of the Cordic algorithm. As can be seen from Fig. 4, the FD is separately implemented on the FPGA. The FS in each phase is sent to dSPACE.

B. Experimental Results of the FD

To evaluate the performance of the FD method, experiments are conducted under different operational modes. In the first step, the robustness to the load transients is evaluated. Two 50% step changes are imposed on the phase current. The experimental waveforms are shown in Fig. 6(a). According to these results, the FD block is robust to load transients.

In the second step, a single lower switch fault and an upper switch fault are forced into phases *a* and *b*, respectively. This case study is a common fault type in VSIs. The experimental results of this case are shown in Fig. 6(b). As can be seen from the fault signal waveform, the fault code in phase *a* is equal to 1 which corresponds to a lower switch fault. At the same time, the fault code in phase *b* is -1. From these results, it can be seen that the FD time is less than a quarter of one period.

In the third step, an open phase fault is forced into the inverter. This case was implemented in phase *a*. The experimental waveforms are shown in Fig. 6(c). According to these results, the fault is detected during less than a quarter of one fundamental cycle. However, the fault is localized during one fundamental cycle.

In the last step, the FD under the faulty mode is considered. To emulate this mode, phase *a* of the motor is disconnected. The control method is updated for one faulty phase mode. A new open switch fault is forced into phase *b*. The results are shown in Fig. 7(a). As can be seen, the fault is effectively detected under the faulty mode.

In order to evaluate the performance of the FD method in the case of non-sinusoidal currents, the motor is operated under one and two-adjacent faulty phases, respectively. The results are shown in Figs. 7(b) and 7(c), respectively. As can been seen, the FD method is robust under both operational modes. It is worth noting that the FD index (i.e. D) shown in Fig. 7 is distorted under the faulty mode control. This is mainly due to the third harmonic component in the motor phase current.

As shown by the experimental results, the proposed FD method is robust to load transients. In addition, it can detect multiple open switch and open phase faults. The FS sent by the FPGA block is included in the fault-tolerant SMC algorithm to maintain the continuous operation of the motor. Details are discussed in the next section.

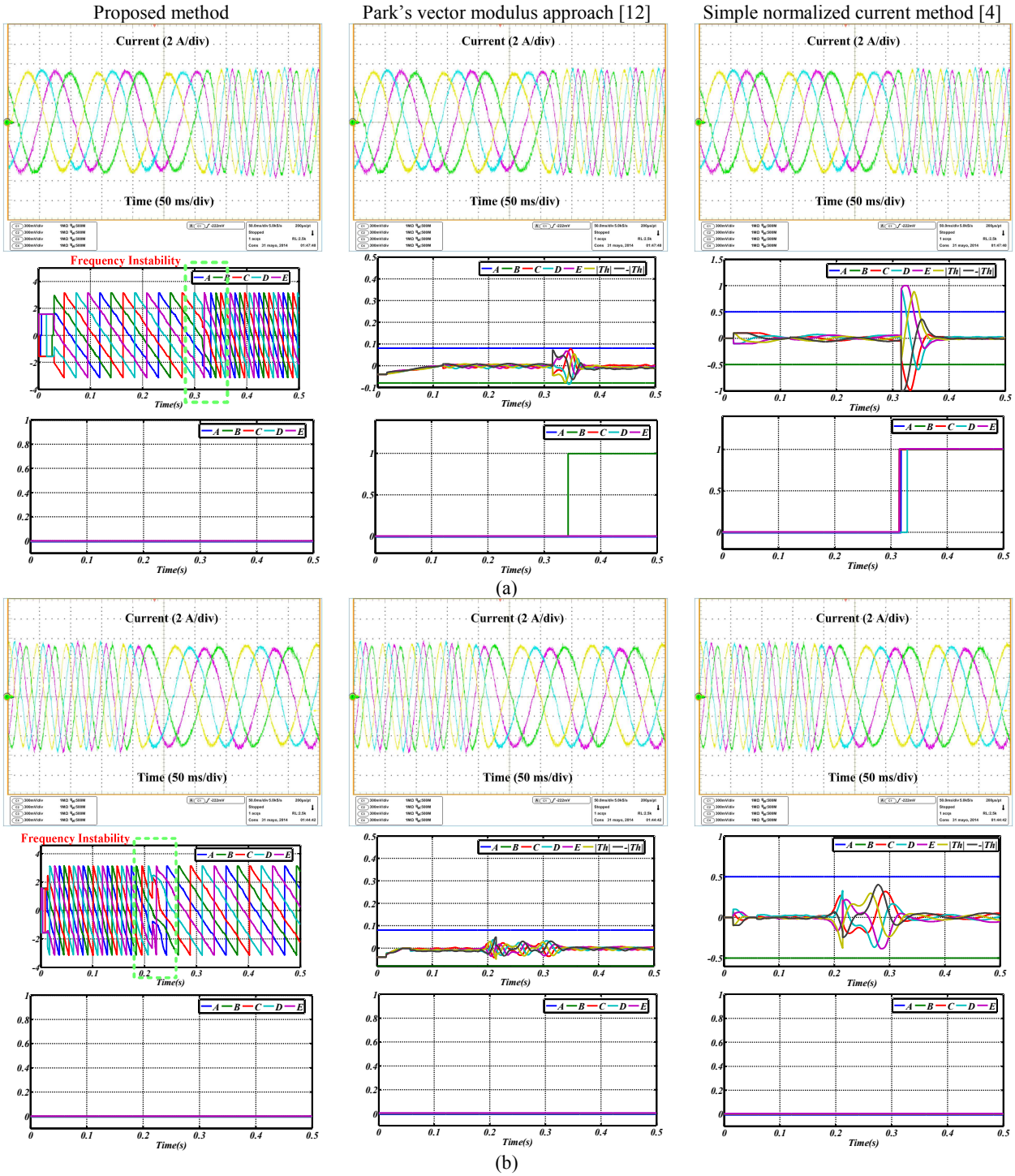


Fig. 8. Comparison of FD methods under (a) acceleration mode. (b) deceleration mode. (TH: the threshold to detect the fault).

C. Comparison between Proposed FD Method and the Other Methods in the Literature

In order to further validate the characteristics of the proposed FD method, a comparison is made between two high performance FD methods already presented in the literature (i.e. the methods in [4] and [12]) and the proposed method. It should be noted that only the simple FD index in [4] is used for comparison. However, the authors have proposed additional signals to improve the FD performance.

The performance of each method is evaluated under four operational modes including the acceleration, deceleration, braking, and reverse modes. The results under the acceleration and deceleration modes are shown in Figs. 8(a) and 8(b), respectively. The motor speed is increased from 20 rpm to 50 rpm and vice versa. As can be seen in Fig. 8(a), in

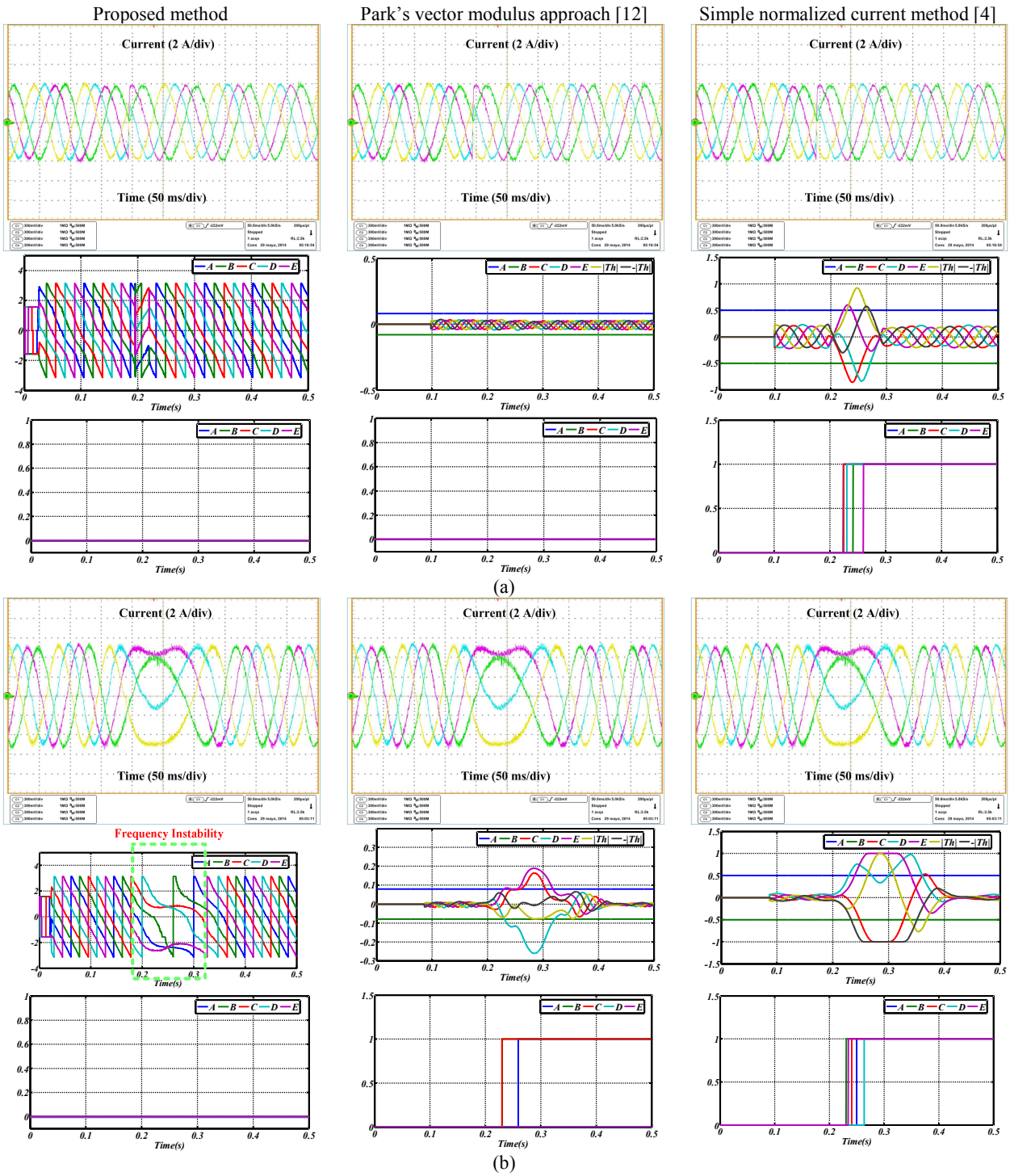
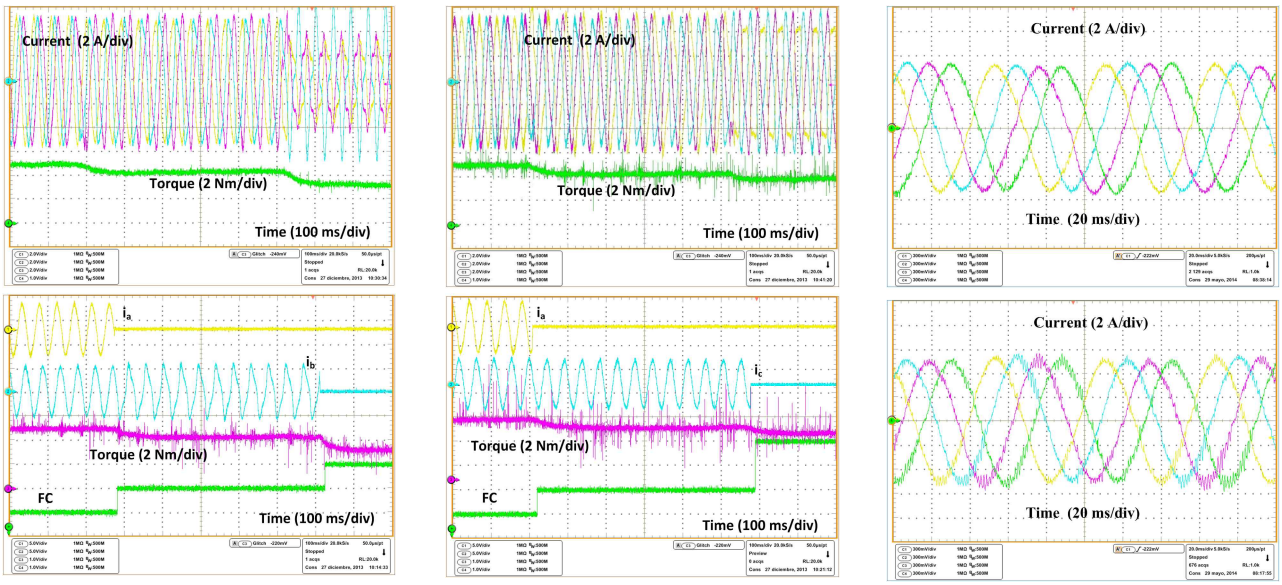


Fig. 9. Comparison of FD methods under (a) braking mode. (b) reverse operational mode.

contrast to the methods in [4] and [12], the proposed method is robust to acceleration conditions. Moreover, all of the methods are robust to the deceleration test as shown in Fig. 8(b).

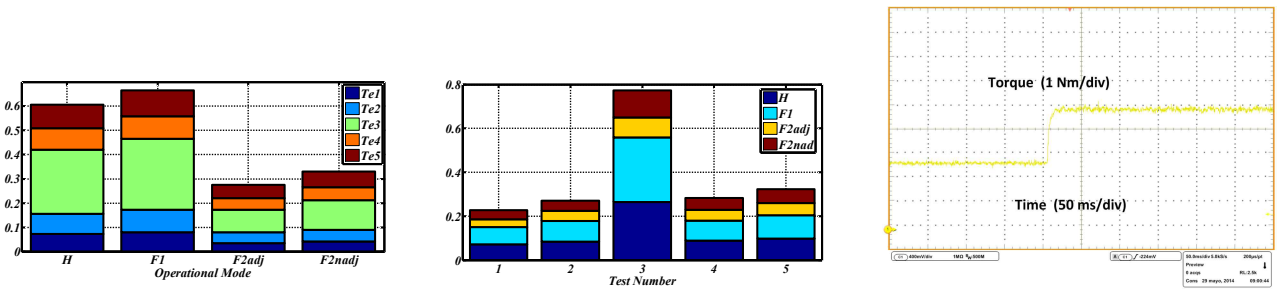
In the second step, the comparison is done under the braking and reverse operational modes. The results are shown in Fig. 9. Under the braking mode, the torque reference value is changed from -5 to 5 Nm. The motor speed is fixed at 23.8 rpm. According to Fig. 9(a), the method in [4] is not robust to the braking test.

In the case of the reverse test shown in Fig. 9(b), the motor speed is changed from -23.8 rpm to 23.8 rpm instantaneously. The torque reference value is fixed at 5 Nm. Under this mode, all of the methods produce a false alarm except for the proposed method.



(a) (b) (c)

Fig. 10. Experimental results of the fault-tolerant control. (a) two-adjacent faulty phase mode. (b) two-nonadjacent faulty phase mode. (c) robustness of controller to parameter variation (upper: SMC with nominal parameters, lower: SMC with parameter uncertainty)



(a) (b) (c)

Fig. 11. Experimental results SMC performance. (a) Energy of error under each mode. (b) Energy of error under each test. (c) Torque waveform.

D. Experimental Results of Fault-Tolerant Control

In order to implement fault-tolerant control of a five-phase PM motor, the generated FS is included in the SMC algorithm. Under each operational mode, a simple code is produced by the FD block implemented on a FPGA.

The operational code of the healthy mode, the one faulty phase mode, the two-adjacent faulty phase mode and the two-nonadjacent faulty phase mode are 1, 2, 3, and 4, respectively. The algorithm of the space vector modulation, the reference currents and the SMC are updated according to this code.

In the first case study, the motor was operated under the healthy mode. Then, a fault was forced into phase *a*. After that, another fault was started in phase *b* which is adjacent to phase *a*. The experimental waveforms of this case are shown in Fig. 10(a).

As can be seen, the fault-tolerant algorithm is done effectively. The healthy phase currents are shown with torque waveforms. The faulty phase currents are also shown with torque waveforms and the operational code of the motor drive.

In the second case study, the first fault is forced in phase *a*, and the second fault is forced in phase *c*. It should be noted that phase *c* is nonadjacent to phase *a*. The final results of this case are shown in Fig. 10(b). According to these results, the proposed FD method can be effectively applied in a system with fault-tolerant capability.

In order to show the effectiveness of the SMC, three case studies are considered. In the first case, the effect of parameter uncertainties on controller performance is studied. The motor is operated once with the nominal parameters used in the control method. After that, the self-inductance of the machine is increased by about 50%. The results for both cases are shown in Fig. 10(c). As can be seen, the controller can still track the reference currents. However, small high frequency disturbances appears in the current waveform.

To analytically validate the robustness of the controller under the different operational modes of the machine, five case studies are considered. In each case, the average energy of the current error function given in (12) is calculated during one fundamental period as:

$$E = \frac{1}{T}\int_0^T (\delta_a^2 + \delta_b^2 + \delta_c^2 + \delta_d^2 + \delta_e^2)dt. \tag{32}$$

Test one is implemented under the nominal parameters of the motor. In case of test two, the phase resistance in all of the phases is reduced by 50%. In case of test three, the self-inductance in all of the phases is reduced by 50%. In case of test four, the phase resistance is decreased by 50% while the inductance matrix is increased by 50%. Finally, in case of test five, the back EMF amplitude is reduced by 50%. The experimental waveforms are shown in Fig. 11. As can been seen in Fig. 11(a), the highest error of energy is achieved under the one faulty phase mode. According to Fig. 11(b), the highest error is achieved in case of test three under all of the operational modes of the machine. It is worth noting that in practical applications, the self-inductance of the machine is almost constant under all of the operational modes.

It should be noted that although the error value in the case of test three is high, the SMC performance is still high. Moreover, by choosing controller gains that are high enough, error values can be reduced in this test.

Since, the SMC is known as a fast control method, a step change was implemented on the motor reference torque. The final torque waveform is shown in Fig. 11(c). The result validates the fast response of the control method.

V. CONCLUSION

A new open transistor FD method is proposed in this paper. The phase angle of the motor phase current is estimated by a trigonometric function. The estimated value is used to define a FD index. The experimental waveforms were presented for a five-phase VSI supplying a PM motor under different operational modes. The FD algorithm was executed on a FPGA. Details of the hardware implementation were explained. According to the obtained results, the proposed method is fast, robust and reliable. Furthermore, it is an adaptable, simple and efficient method. It is possible to detect and localize multiple open switch faults. A detection speed of less than a quarter of one fundamental cycle may be achieved. However, this depends on the load current at the fault initiation point. To evaluate the effectiveness of the FD method, a SMC was developed to set the current references in a five-phase PM motor with an embedded FD block. The SMC has the advantage of tracking the reference currents quickly and accurately. These features are important for the FD strategy. The FD block was included in the fault-tolerant control algorithm of a five-phase BLDC motor drive. It was shown that remedial strategies can be effectively taken after FD in order to maintain the continuous operation of the motor. A real time fault-tolerant continuous control was achieved.

ACKNOWLEDGMENT

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