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Classification of Grid Connected Transformerless PV Inverters with a Focus on the Leakage Current Characteristics and Extension of Topology Families

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Abstract

Grid-connected transformerless photovoltaic (PV) inverters (TPVIs) are increasingly dominating the market due to their higher efficiency, lower cost, lighter weight, and reduced size when compared to their transformer based counterparts. However, due to the lack of galvanic isolation in the low voltage grid interconnections of these inverters, the PV systems become vulnerable to leakage currents flowing through the grounded star point of the distribution transformer, the earth, and the distributed parasitic capacitance of the PV modules. These leakage currents are prohibitive, since they constitute an issue for safety, reliability, protection coordination, electromagnetic compatibility, and module lifetime. This paper investigates a wide range of multi-kW range power rating TPVI topologies and classifies them in terms of their leakage current attributes. This systematic classification places most topologies under a small number of classes with basic leakage current attributes. Thus, understanding and evaluating these topologies becomes an easy task. In addition, based on these observations, new topologies with reduced leakage current characteristics are proposed in this paper. Furthermore, the important efficiency and cost determining characteristics of converters are studied to allow design engineers to include cost and efficiency as deciding factors in selecting a converter topology for PV applications.

Key words: Classification, Common-mode, Efficiency, Grid, Inverter, Leakage Current, PV Inverter, PWM, Topology, Transformerless

I. INTRODUCTION

Since fossil fuel based energy sources have been decreasing and interest in renewable energy sources has been rapidly growing over the last two decades, wind and solar power conversion technologies have experienced rapid development, growth, and maturation. In particular, photovoltaic (PV) energy conversion system products have flooded the global market over the last five years [1]. A wide range of new technology products and a large number of research papers have appeared in the PV field (with a strong correlation between the two). In particular, low-voltage grid-connected residential and commercial systems have dominated the PV field due to the fact that the generated power can be used most beneficially and the electric utility authorities give high energy buying price incentives to PV system owners. Power electronic converters, as interface devices between the grid and PV modules, constitute an important part of PV systems, and different types of converters are used for different applications.

In practical applications, based on the power electronic converter type utilized, grid connected PV systems generally consist of three types: Module Integrated Converter (MIC) based sub-kW single-phase units [2], large-scale solar farm type 100kW-1MW (and higher typically by paralleling) rated units (as central/multi-string inverters), and finally the kW range single/three-phase units (as string/multi-string/central inverters). Of these three types, the MIC based units and the large-scale units currently correspond to a smaller portion of applications, while kW range units have largely dominated the field, due to the strong demand, especially in Europe both in residential and commercial applications. The power electronic conversion technologies involved in these

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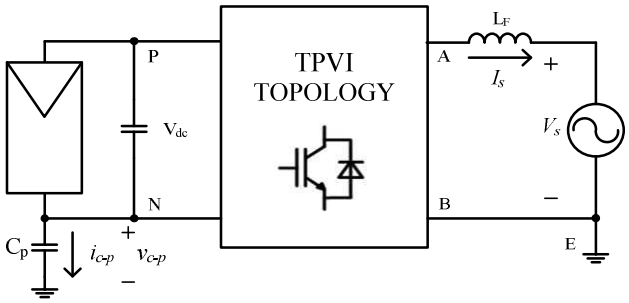

Fig. 1. PV system with grid-connected transformerless PV inverter (TPVI). Regarding the parasitic leakage currents, the PV module equivalent stray capacitance, C_p, represents the most critical parasitic element in the system.

structures determine the overall PV system performance interms of efficiency, reliability, and human and system safety. Since most of them are related to power quality and human safety, the power electronic conversion system characteristics must meet strict grid codes and regulations established by energy system authorities (such as IEEE 1547, EN 61000-3-2, EN 50160, IEC 61727, DIN VDE 0126-1-1, etc.). As a result, technological challenges arise. Because of these challenges, significant R&D efforts from all around the world have focused on grid connected power electronic converters for PV applications.

Of the three main groups summarized above, the dominant kW range type converters are widely investigated. Of the kW range converters, the transformerless technology is developed to provide higher efficiency, lower cost, lighter weight, and reduced size when compared to transformer based systems [3], [4]. Therefore, transformerless systems are increasingly dominating the market. However, due to the lack of galvanic isolation, the leakage current flowing through the parasitic capacitor of the PV modules in such systems (Fig. 1) has become an issue in terms of safety, reliability, protection coordination, electromagnetic compatibility, and lifetime (especially for some thin film module types) [5]-[8]. Thus, leakage current has become a major figure of merit for evaluating such systems (the lower the better) [9]-[12]. Since the leakage current characteristic is mostly determined by the converter topology (through the structure and switching patterns, as shown later in this paper), it becomes possible to classify and evaluate high efficiency grid-connected transformerless PV inverter (TPVI) topologies based on their leakage current characteristics. From here on, instead of the generic name "converter," the name "inverter" will be utilized since the power electronic energy conversion stage of a PV system involves dc to ac conversion.

In the literature, there are numerous surveys [2], [4], [11]-[14] and topology invention studies on TPVIs [15]-[28]. However, there is no systematic classification of topologies, and the relationships between the invented topologies and possibility for extending these topology classes have not been covered. In particular, for high efficiency TPVIs, the leakage current, which is a major performance characteristic, has not been used as a prime characteristic for classification and surveying. In this paper, a classification of TPVIs based on leakage current attributes yields an improved understanding of converter behaviour to help future development of new TPVI topologies, and reduces the complexity. Instead of learning the operating principles and performance attributes of each topology individually (among many topologies), learning the common properties and emphasizing the basic differences is presented. Based on this approach, the topology families are extended with newly proposed topologies [28]. Since this approach yields benefits in terms of new topology inventions and aids in the understanding of operating principles and behaviours of a large number of topologies, it is expected to be highly beneficial to engineers in analysis, design, topology selection, and performance evaluation.

In this paper, first PV inverters are surveyed and classified according to their leakage current attributes. Then, TPVIs (extended with proposed topologies) are classified with their structures, operating principles, and switching patterns provided in detail. Once the families are grouped, the leakage current attributes are demonstrated and emphasized as the defining property. In addition, the topologies and topology families are evaluated with respect to their efficiency and semiconductor power utilization characteristics, to guide design engineers in the selection of a topology with a consideration of economic constraints.

The topology classification and extension study provided in the paper is performed for single phase systems. However, in application, single phase units are put together to establish three-phase systems (by numerous leading manufacturers). Thus, the classification and extension covers three-phase applications as well. The power rating is also increased by up-scaling converters or paralleling. Thus, the application range of such topologies extends to nearly 100kW. A significant percentage of rooftop and commercial PV installations with several tens of kW ratings are established from single-phase TPVI modules. Thus, single-phase topologies have a wide range of practical application. In this paper, single stage topologies are covered unless otherwise stated. However, pre-regulator boost stages can be easily added. Therefore, a wide range of applications is covered in the topology classification/survey/extension of this paper.

II. CLASSIFICATION

Most dc/ac power conversion applications (including PV systems), voltage source inverters (VSIs) are favourable due to their efficiency, size, and cost advantages over current source inverters and other types of inverters. However, the common-mode voltage (CMV) variations in conventional VSIs introduce a prohibitive amount of leakage currents in PV systems. Therefore, many VSI type TPVI topologies

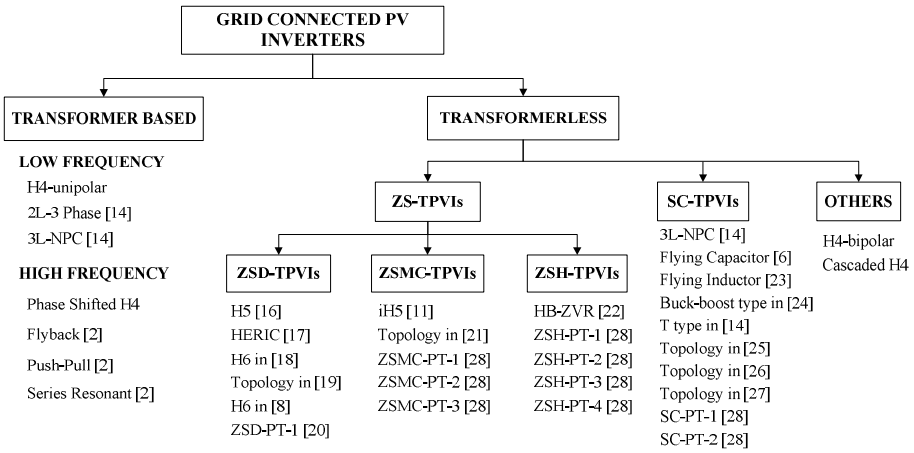

Fig. 2. Leakage current characteristics based classification of PV inverter topologies with major family representatives.

with reduced leakage current characteristics are developed to overcome this weakness [15]-[25]. In addition, topologies with different structures from VSIs but with similar low leakage current attributes are developed [23], [24]. Therefore, a large number of topologies exists. Nevertheless, based on the leakage current reduction method used, PV inverters can be divided to two groups as transformer based and transformerless inverters (shown in Fig. 2).

Topologies with direct galvanic isolation by means of transformers yield a low leakage current due to the naturally confined parasitic current path. In such topologies, the leakage current is only dependent on the transformer parasitic capacitances, which are usually very low. The leakage current is negligible and generally not an issue in such topologies. A transformer is often provided for the purpose of voltage level adjustments, while a reduced leakage current is an additional benefit. In some cases, it is used mainly to confine the leakage current and for the grounding requirements of some module types [12]. Otherwise, a direct connection of the converter to the grid may lead to grid code violations or the aforementioned drawbacks due to the large leakage current. The transformer-based topologies can be classified into two groups as low (grid) frequency and high frequency transformer based topologies. Both MIC (high frequency transformers) and above 100kW (low frequency transformers) applications use transformers. In the kW range transformer based systems, typically high frequency transformer based topologies are used (such as phase shifted full bridge converters). A brief summary of transformer-based topologies, shown in Fig. 2, is provided in [2], [28]. Although transformer based PV systems provide low leakage current characteristics, their demand is decreasing due to their efficiency, size, weight, and cost drawbacks, especially in the kW and above range.

The second class, TPVIs, have the advantages of higher efficiency, lower cost, lighter weight, and smaller size. Therefore, they are continually replacing their transformer-based counterparts. However, due to a lack of galvanic isolation, TPVIs are vulnerable to the capacitive leakage currents flowing through the grounded distribution transformer and the earth (due to large PV module capacitances). Therefore, it is strongly desirable to unite the aforementioned advantages of TPVIs with reduced leakage current characteristics without excessively increasing the converter size, complexity, and cost. Some of the existing power converter topologies with favourable leakage current attributes have been adopted. However, a larger number of new topologies have been invented for the purpose of TPVI applications for PV systems [16]-[27]. In spite of the abundance of TPVI topologies, the main topological (non-filtered) leakage current reduction techniques can be subdivided into two main groups and most of the TPVIs can be grouped under these two as illustrated in Fig. 2. These two groups are the zero state TPVI (ZS-TPVI) topology group and the solidly clamped TPVI (SC-TPVI) topology group. Although numerous TPVI topologies with reduced leakage current characteristics belong to the aforementioned groups of topologies, there are a few "other TPVI topologies" such as H4 [15] and the cascaded H-bridge topology [6], which do not fit into the above classifications and they are not studied here. The following sections focus on the aforementioned two TPVI groups. Among all of the discussed topologies in the following sections, numerous topologies have been invented through the research of authors and reported in [28]. These TPVIs are termed as proposed topologies according to the classes they belong to (for example, ZSD-PT-1 is a proposed topology-1 belonging to the ZSD-TPVI topology class).

III. ZERO STATE TPVI TOPOLOGIES

As shown in Fig. 3, the conventional full-bridge VSI (H4) topology has many favourable features for single-phase TPVI applications. These features include a simple modular structure with a small component count (low cost) and a low dc-bus voltage requirement (1.1 to 1.3 times the peak value of the grid voltage). The latter attribute results in lower voltage

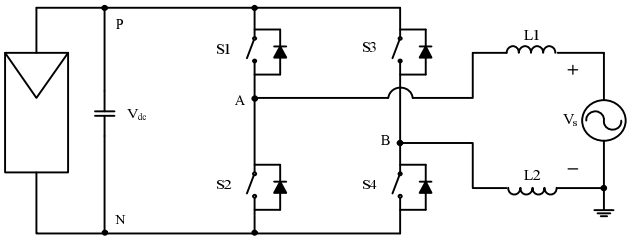

Fig. 3. The classical H4 inverter topology.

rating switches (low cost), reduced converter losses (high efficiency), and a smaller number of PV modules connected in series (lower voltage, and better at meeting the safety and reliability requirements). Operating the H4 with unipolar pulse-width modulation (PWM) yields a low current ripple and a small filter inductor. However, it causes a large CMV and its associated leakage current depending on the equivalent PV source parasitic capacitance, which could be prohibitive. Operating the H4 with bipolar PWM yields a reduced CMV and less leakage current. However, it causes a large current ripple and requires a large filter inductor. Thus, the H4 topology exhibits major weaknesses for both PWM methods. In unipolar PWM, the top (S1/S3) or bottom (S2/S4) two switches are in the on-state for a portion of the PWM cycle, yielding zero output voltage (V_{AB}=0, called zero-state) and a high CMV during this interval. The remaining time is spent on the active states creating a nonzero output voltage, but zero CMV. Since a change occurs between the active and zero states in every PWM cycle, a varying CMV with a high magnitude results. Thus, the zero-state of the H4 is problematic in terms of leakage current.

As their name suggests, the ZS-TPVI topologies overcome the leakage current problem due to the zero states of the H4 by means of topological modifications. The Zero State Decoupled (ZSD) TPVIs decouple the dc side (PV source) and ac side (output, ac grid) during the zero states in order to block the leakage current. The Zero State Midpoint Clamped (ZSMC) TPVIs use two mechanisms, the decoupling mechanism of the ZSD-TPVI topologies and the midpoint clamping mechanism. The midpoint clamping mechanism connects the short-circuited output terminals (V_{AB}=0) at the zero output voltage intervals to the dc-bus midpoint so that the CMV is stabilized (kept constant). The Zero State Hybrid (ZSH) TPVIs exhibit a combination of the leakage current characteristics of the first two interchangeably with respect to time. These three approaches define the three topology subclasses that are discussed in the next section. To achieve a higher energy conversion efficiency and a smaller sizing of the components, TPVIs are generally operated at unity power factor (PF=1). For this condition, the switch gate signals for the three discussed groups of topologies are common, and they will be discussed in the following sections and depicted in Fig. 4.

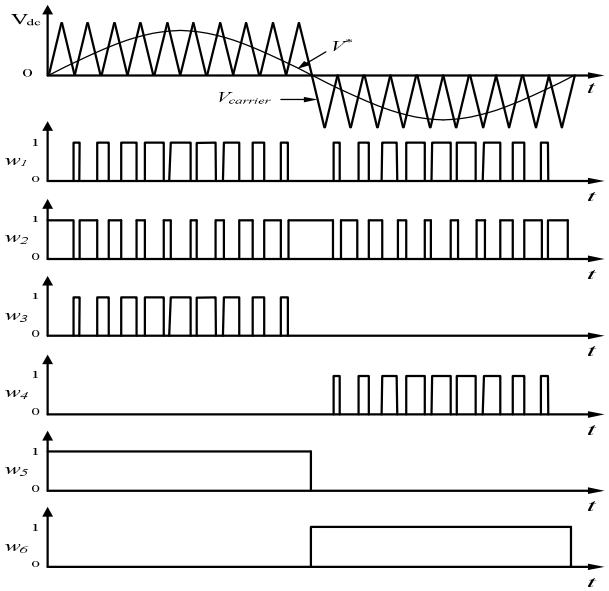

Fig. 4. Generic gate logic signals of controlled switches of ZS-TPVI topologies (PF=1).

TABLE I
ACTIVE SWITCHES OF ZSD-TPVI TOPOLOGIES (PF=1)

	POSITIVE CYCLE VOLTAGE (V_{AB})		NEGATIVE CYCLE VOLTAGE (V_{AB})	
TOPOLOGY	V_{dc}	Zero	$-V_{dc}$	Zero
H5 [16]	S1,S4,S5	S1,D3	S2,S3,S5	S3,D1
HERIC [17]	S1,S4	S6,D5	S2,S3	S5,D6
H6 in [18]	S1,S4,S5,S6	S1,S4,D7	S2,S3,S5,S6	S2,S3,D7
Topology in [19]	S1,S2,S6	S2,D7	S3,S4,S5	S3,D8
H6 in [8]	S1,S4,S6	S4,D7	S2,S3,S5	S3,D8
ZSD-PT-1 [20]	S1,S4	S6,D3	S2,S3,S5	S3,D6

A. Zero State Decoupled TPVI Topologies

The first subgroup of ZS-TPVI topology group is the ZSD-TPVI topology subgroup. As the name suggests, these inverters provide reduced leakage current by means of decoupling (or isolating) the ac and dc sides during zero states via establishing proper switch configurations. The recently invented and commercialized H5 [16] (Fig. 5(a)), Heric [17] (Fig. 5(b)), H6 [18] (Fig. 5(c)), and the topologies in Fig. 5(d)-(f) belong to the ZSD-TPVI topology group. The active semiconductors on the line current path of these topologies under PF=1 operation are provided in Table I. The gate logic signals provided in Fig. 4 are assigned near the associated switches as depicted in Fig. 5 (a)-(f). In this topology subgroup, zero state decoupling is obtained at the expense of an increase in the switch count when compared to H4. A thorough investigation of the leakage current attributes of this subgroup of topologies is provided in [20], [28].

B. Zero State Midpoint Clamped TPVI Topologies

The second subgroup of ZS-TPVI topologies, the zero state midpoint clamped (ZSMC) TPVI subgroup, is a relative of

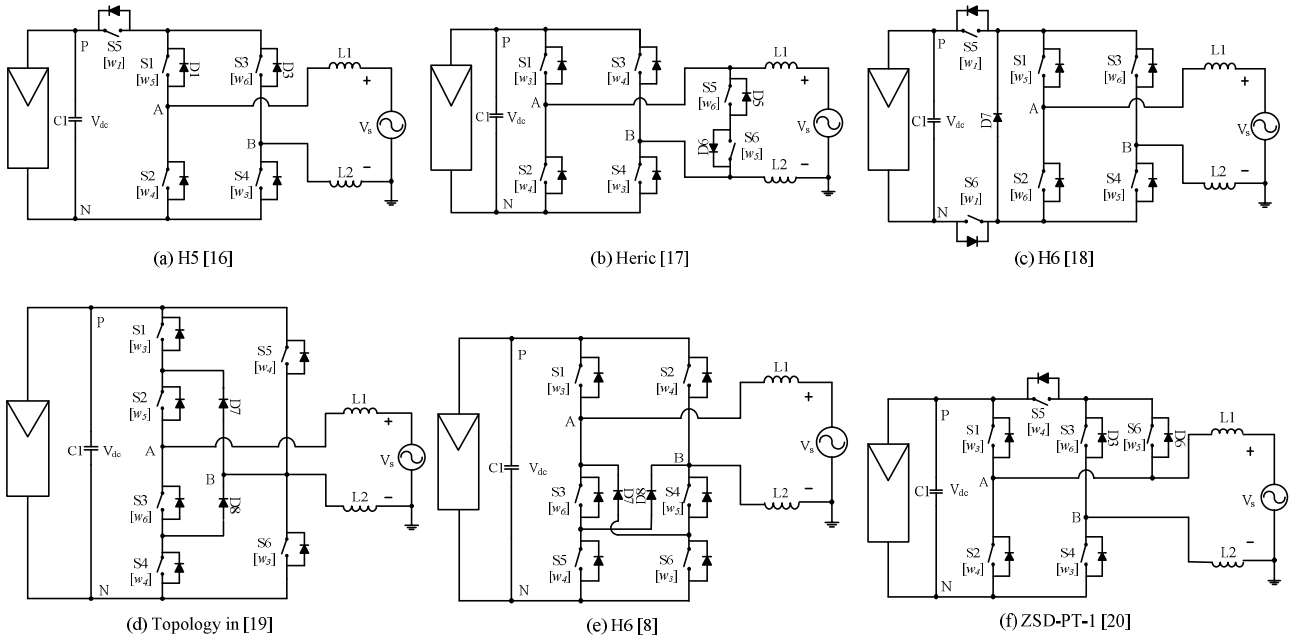

Fig. 5. ZSD-TPVI topologies.

the ZSD-TPVI topology subgroup and most of them can be derived from these topologies to obtain better leakage current characteristics. For this purpose, the ZSMC-TPVI topologies not only decouple the ac and dc circuits at zero states, but also connect the short-circuited inverter output terminals (V_{AB}=0) to the midpoint of the dc-bus. Thus, the CMV is stabilized (ideally fixed). For example, the iH5 topology (Fig. 6(a), [11]) is derived from the H5 topology by inserting additional switches (S6, D6) to achieve midpoint connections at the zero states. As in this case, the connection to the midpoint of the dc-bus usually requires additional active switches, or splitting diodes as in the case of the topology illustrated in Fig. 6(b). In the case of active switch utilization in the midpoint of the dc-bus connection, the current through the switch is negligible. As a result, the rating of the switch is significantly smaller than that of the other switches. Since the midpoint current is low in these topologies, splitting of the dc-bus can be achieved by small capacitors, without affecting the total dc-bus capacitor size and its rating. In Fig. 6(a)-(e), the topologies belonging to the ZSMC-TPVI subgroup are depicted with their corresponding switch gate logic signals assigned near the controlled switch of each topology for PF=1 operation as shown in Fig. 4. In Table II, the switches that are conducting during the active and zero states, and the midpoint connecting (MC) switches at the zero output voltage durations are listed to further clarify the operation at PF=1.

C. Zero State Hybrid TPVI Topologies

The third subgroup of ZS-TPVI topologies is the zero state hybrid (ZSH) TPVI topology subgroup. The decoupling of the ac and dc circuits of the ZSD-TPVI topologies and the

TABLE II
ACTIVE SWITCHES OF ZSMC-TPVI TOPOLOGIES (PF=1)

	POSITIVE CYCLE VOLTAGE (V_{AB})		NEGATIVE CYCLE VOLTAGE (V_{AB})		MC SWITCH
TOPOLOGY	V_{dc}	Zero	$-V_{dc}$	Zero	
iH5 [11]	S1,S4,S5	S1,D3	S2,S3,S5	S3,D1	S6,D6
Topology in [21]	S1,S4,S5,S6	S1,S4,D7, D8	S2,S3,S5,S6	S2,S3,D7,D8	Naturally
ZSMC-PT-1 [28]	S1,S4	S6,D5	S2,S3	S5,D6	S7,D7
ZSMC-PT-2 [28]	S1,S2,S6	S2,D8	S3,S4,S5	S3,D9	S7,D7
ZSMC-PT-3 [28]	S1,S4	S6,D3	S2,S3,S5	S3,D6	S7,D7

midpoint connection of the ZSMC-TPVI topologies are realized interchangeably (in every half grid cycle) in the ZSH-TPVI topologies, constituting a hybrid characteristic with respect to time. The members of this subgroup are demonstrated in Fig. 7, where HB-ZVR (H-Bridge/H4 Zero Vector Rectifier) is reported in [22], and the rest are reported in [28]. The midpoint connection switches of the ZSMC-TPVIs are replaced by a midpoint connection diode (MC diode) to obtain most of the ZSH-TPVI topologies. For instance, the ZSH-PT-2 is obtained by replacing the S6-D6 pair of iH5 by diode D6 only. The gate logic signals provided in Fig. 4 are assigned near the corresponding switches of these topologies. Moreover, the switches on the line current path and the MC diodes are listed in Table III to help understand the operations of the topologies.

IV. SOLIDLY CLAMPED TPVI TOPOLOGIES

The second group of the TPVI topologies, the SC-TPVI topology group, realizes a solid connection between the ac side and the dc side circuits, so that the equivalent parasitic capacitor voltage is kept constant. Depending on the parasitic

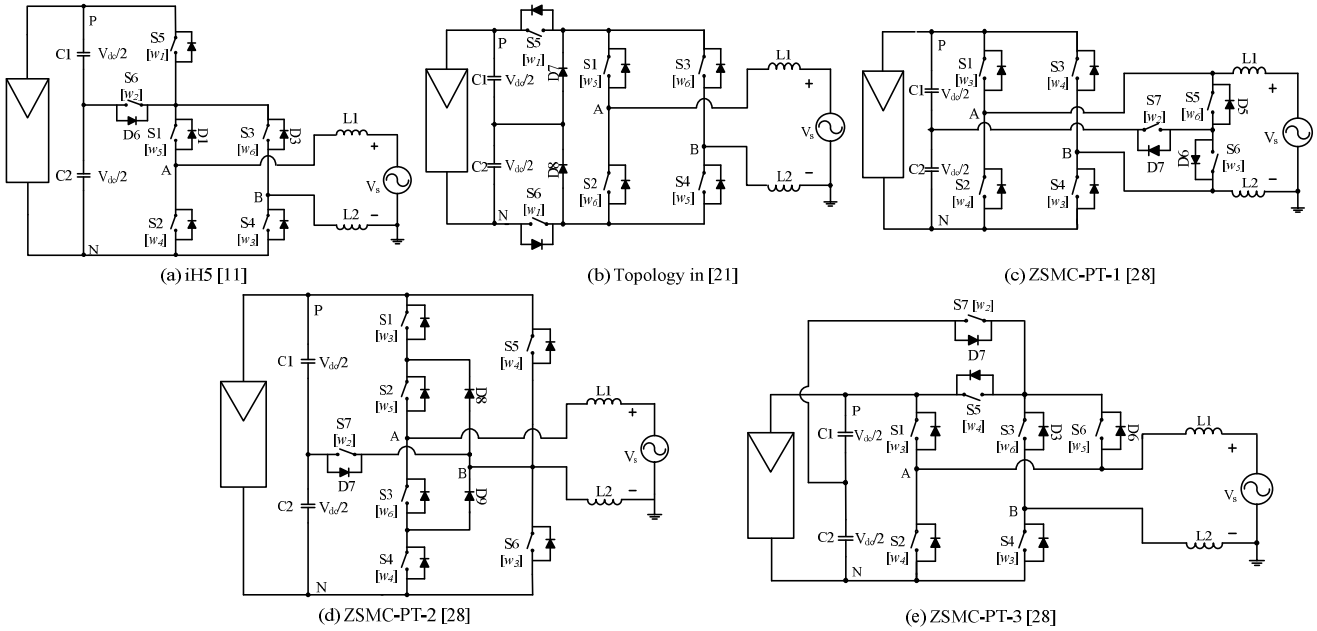

Fig. 6. ZSMC-TPVI topologies.

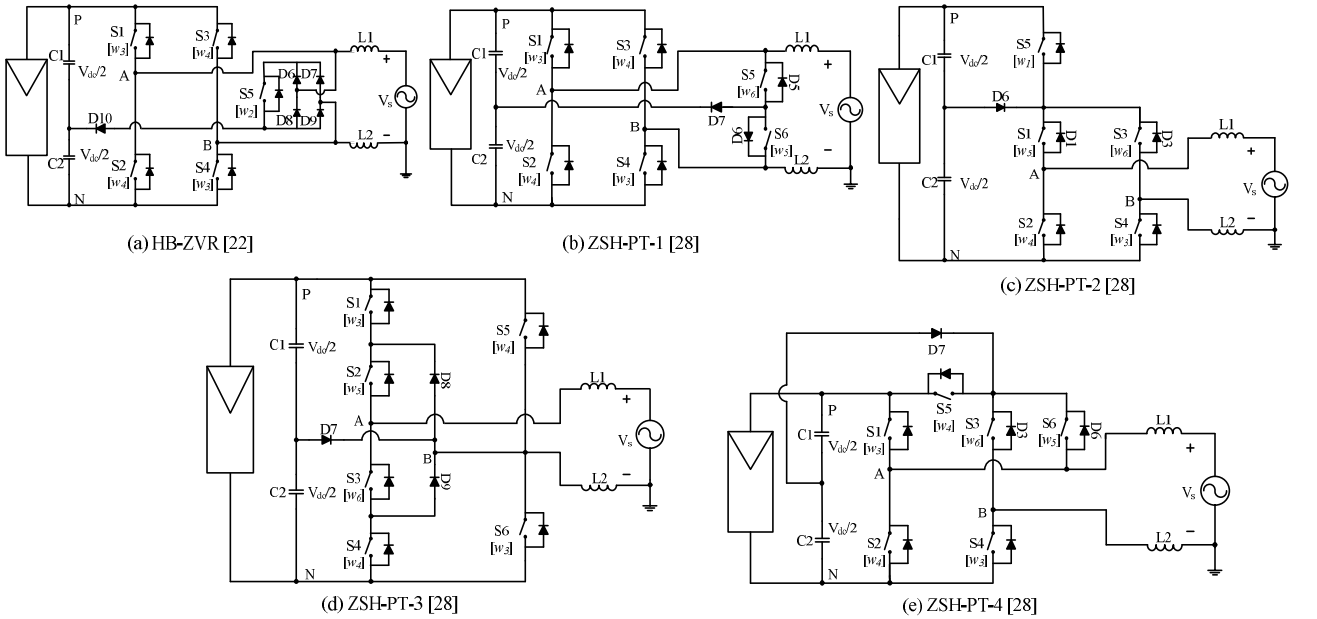

Fig. 7. ZSH-TPVI topologies.

TABLE III
ACTIVE SWITCHES OF ZSH-TPVI TOPOLOGIES (PF=1)

	POSITIVE CYCLE VOLTAGE (V_{AB})		NEGATIVE CYCLE VOLTAGE (V_{AB})		MC DIODE
TOPOLOGY	V_{dc}	Zero	$-V_{dc}$	Zero	
HB-ZVR [22]	S1,S4	S5,D8,D7	S2,S3	S5,D6,D9	D10
ZSH-PT-1 [28]	S1,S4	S6,D5	S2,S3	S5,D6	D7
ZSH-PT-2 [28]	S1,S4,S5	S1,D3	S2,S3,S5	S3,D1	D6
ZSH-PT-3 [28]	S1,S2,S6	S2,D8	S3,S4,S5	S3,D9	D7
ZSH-PT-4 [28]	S1,S4	S6,D3	S2,S3,S5	S3,D6	D7

capacitance value, because of slow or no voltage variations, the parasitic capacitor current becomes negligible. Most of the SC-TPVI topologies are successfully adapted from existing applications, such as motor drives and uninterruptible power supplies, to grid-connected PV systems. However, unlike the relation between the ZS-TPVI topology classes, the derivation of new topologies in this topology class is not algorithmic.

The neutral point clamped (NPC) three-level VSI in Fig. 8(a) [14], the T-type topology in Fig. 8(b) [14], and the flying capacitor topology in Fig. 8(c) [6] with midpoint clamping to the neutral wire of the utility grid, belong to the SC-TPVI

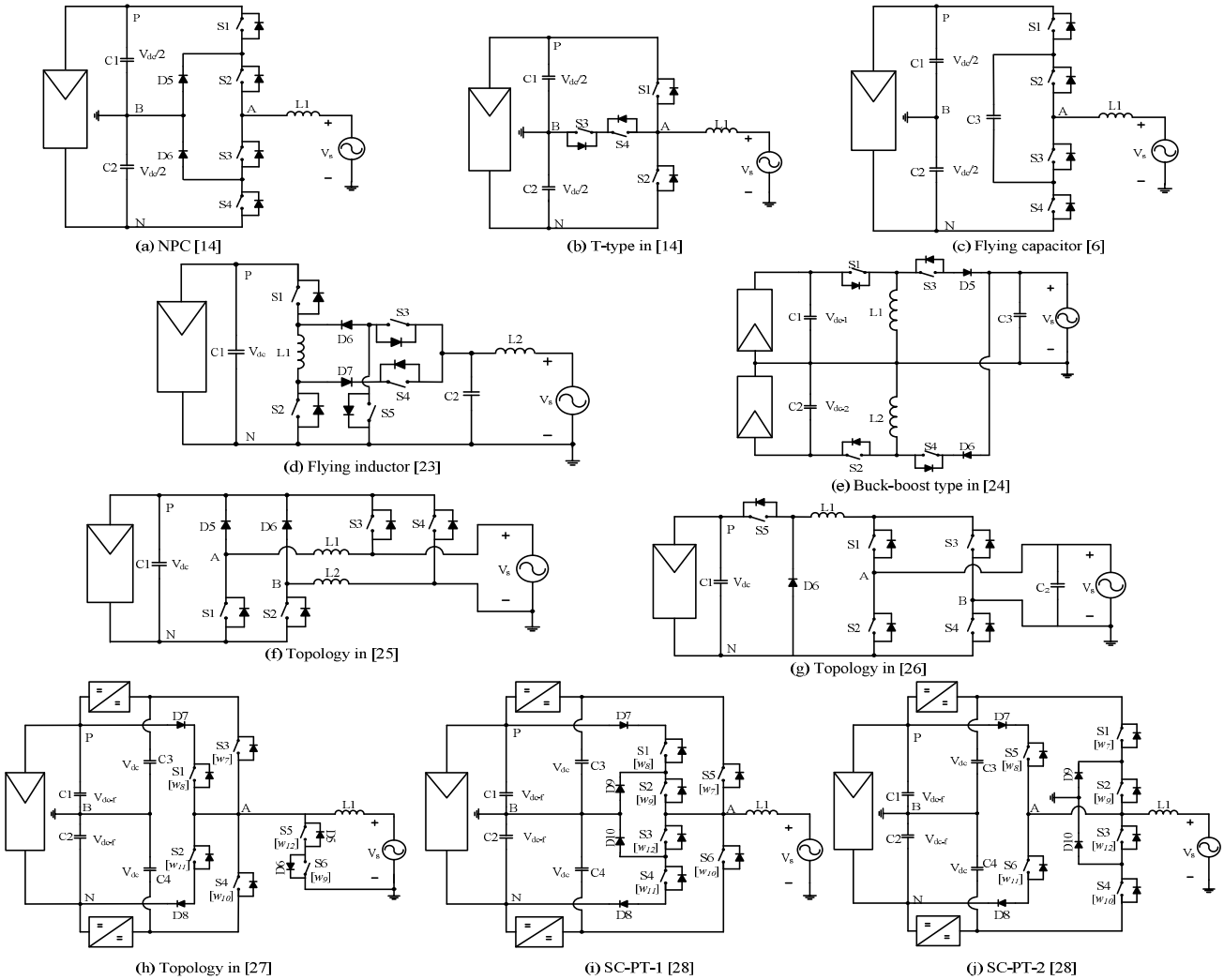

Fig. 8. SC-TPVI topologies.

topology group. These topologies generally require a higher dc-bus voltage (2.2 to 2.6 times the peak value of the grid voltage) with respect to the first group (ZS-TPVIs), which decreases the conversion efficiency (~%1-2 reduction as a boost stage is required) [14]. However, like the ZS-TPVIs, these topologies provide a low filter inductor current ripple due to the three-level output voltage. The topologies in Fig. 8(d) and (e) also belong to the SC-TPVI topology family since they have a solid connection from the neutral wire to the dc-bus (therefore the PV source) side. In Fig. 8(f) [25] and Fig. 8(g) [26], the two topologies belonging to this class are illustrated, where the solid connection is provided by making use of controlled switches at a low frequency. In particular, the commutation of the solidly connecting switches is provided near the zero crossings of the grid voltage at PF=1. For example, the equivalent parasitic capacitance (C_p, as shown in Fig. 1) of the topology shown in Fig. 8(g) has an ideally constant (zero) voltage for the positive half cycle of the grid since the solid connection is provided by S4 during this period. Similarly, due to the solid connection provided by S2 during the negative half cycle, the low frequency grid voltage is imposed on C_p. Thus, the voltage on C_p varies slowly and yields a negligible leakage current. In TPVI applications, multilevel topologies are favourable, since their input and output current characteristics are well suited for higher efficiency and component size reduction. A commercial five-level topology belonging to the SC-TPVI topology group is depicted in Fig. 8(h) [27]. The partial boosting strategy of this topology increases the overall conversion efficiency and decreases the boost-stage size. With the feed-forward voltage ($V_{dc\text{-}f}$) the output voltage of this topology becomes a five-level and a smaller output filter inductor and a reduced filter inductor loss is obtained. Two topologies, SC-PT-1 and SC-PT-2, with the same boosting and output voltage characteristics are given in [28] and they are depicted in Fig. 8(i) and (j), respectively. The gate logic signals of the three five-level commercial SC-TPVI topologies in Fig. 8(h), (i), and (j) are depicted in Fig. 9 for PF=1. Furthermore, these signals are assigned near the corresponding controlled switches in Fig. 8(h), (i), and (j) to

TABLE IV
ACTIVE SWITCHES OF SC-TPVI TOPOLOGIES(PF=1)

	POSITIVE CYCLE VOLTAGE (V_{AB})			NEGATIVE CYCLE VOLTAGE (V_{AB})		
TOPOLOGY	V_{dc}	V_{dc-f}	Zero	$-V_{dc}$	$-V_{dc-f}$	Zero
Topology in [27]	S3	S1,D7	S6,D5	S4	S2,D8	S5,D6
SC-PT-1 [28]	S5	S1,S2,D7	S2,D9	S6	S3,S4,D8	S3,D10
SC-PT-2 [28]	S1,S2	S5,D7	S2,D9	S3,S4	S6,D8	S3,D10

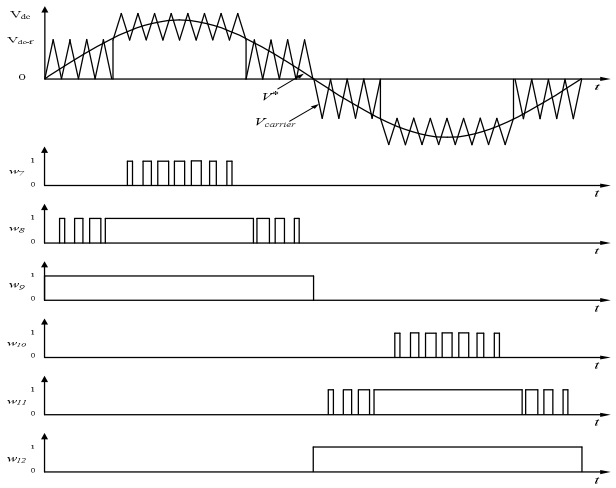

Fig. 9. Generic gate logic signals of controlled switches of the five-level SC-TPVI topologies [in Fig. 8(h) the topology in [27], Fig. 8(i) SC-PT-1, and Fig. 8(j) SC-PT-2] at PF=1.

simplify the understanding of these topologies. In order to aid in understanding the operating principles of these topologies, the switches on the line current path are listed in Table IV with respect to the output voltage (V_{AB}) applied.

V. LEAKAGE CURRENT CHARACTERISTICS OF THE TPVIS

Since the prevention of leakage currents is crucial in the transformerless grid interconnection of PV energy sources, the existing and proposed TPVI topologies were classified in the previous sections based on their leakage current attributes. Having provided the structural details and switching patterns, which relate to the leakage current attributes of the TPVI topologies, it becomes possible to evaluate the leakage current as a distinguishing characteristic of each TPVI group/subgroup. For this purpose, simulations of all of the voltage source topologies are performed and the simulation waveforms of representatives of the topology classes are presented in this paper (H5 for the ZSD-TPVI, the topology in [21] for the ZSMC-TPVI, ZSH-PT-1 for the ZSH-TPVI, and SC-PT-1 for the SC-TPVI) for the parameters in Table V. The simulation models of the TPVI topology classes are depicted in Fig. 10. For the ZS-TPVI topologies, the filter inductor is split in two, and distributed to the phase and neutral wires equally (Fig. 10(a)) such that the common-mode immunity and reliability are enhanced. The representative ZS-

TABLE V
PV SYSTEM SIMULATION PARAMETERS

P_{rated}	Rated Power	3 kW, PF=1
V_s	Grid Voltage	220 V_{rms}, 50 Hz
V_{dc}	Dc-bus Voltage	400 V
V_{dc-f}	Feed-forward Dc-bus Voltage	200 V
f_s	Switching Frequency	20 kHz
L_F	Total Filter Inductance	2 mH
C_p	Parasitic Capacitance	500 nF
L_{line}	Line Inductance/phase	10 µH
R_{line}	Line Resistance/phase	10 mΩ

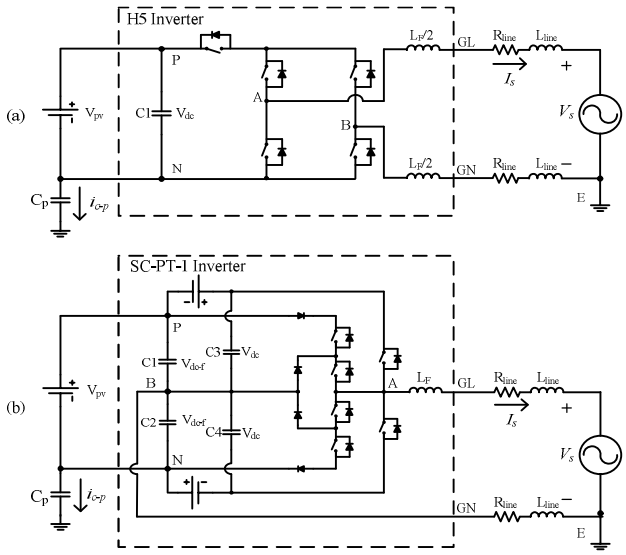

Fig. 10. Simulation models of the H5 (a) and SC-PT-1 (b) topologies.

TPVI topologies have the same leakage current simulation model. Thus, each system model is obtained by replacing H5 of Fig. 10(a) with the associated circuit topology. In the case of the simulated SC-TPVI topology (Fig. 10(b)), filter inductor is only inserted to the phase wire, and the neutral wire is solidly connected to the dc-bus midpoint. The leakage current characteristics gathered from the simulations of the representative topologies are shown in Fig. 11 for a complete grid period.

Decoupling the ac and dc sides during the zero state intervals, the ZSD-TPVI topologies share common leakage current characteristics as depicted in the waveform of Fig. 11(a) for the H5 topology (Fig. 5(a)) as the representative of the ZSD-TPVI topologies. As a prime characteristic of these topologies, after every decoupling event of each PWM period, a needle shaped leakage current pulse occurs due to the mismatch of voltages on the ac and dc sides (peaking especially near the zero crossings of the grid voltage, where the mismatch is largest [20]).

As shown in Fig. 11(b), the leakage current characteristics of the representative topology of the ZSMC-TPVI subgroup in [21] (Fig. 6(b)) is seen to have a dominant grid frequency component rather than a high frequency content, which is due to a nearly constant CMV appearing on the equivalent

parasitic capacitor of the PV modules. Although these topologies are mostly derived from the ZSD-TPVIs, they exhibit better leakage current attributes (improvement in the order of magnitude) because of the midpoint connections during the zero states.

The leakage current characteristics of the representative topology of the ZSH-TPVI subgroup, ZSH-PT-2, is depicted in Fig. 11(c), which is common for the other members of the subgroup in Fig. 7 also. The characteristics of the current consist of the characteristics of the half grid period portions of the leakage current characteristics of the ZSD-TPVI and ZSMC-TPVI topologies (shown in Fig. 11(a), (b)) interchangeably, depending on the polarity of the derivative of the grid voltage (shown in Fig. 11(c)) [28].

The leakage current characteristics of SC-PT-1 are depicted in Fig. 11(d) as the representative of the SC-TPVIs. In these topologies, the voltage on the neutral wire [between the grid neutral point (GN) and the earth (E)] carries the PWM ripple current. Thus, the PWM ripple voltage is induced on the neutral wire. In the PWM frequency range C1=C2 pose a low impedance when compared to C_p. Thus, the ripple voltage appears on C_p. As a result, a leakage current (carrying the PWM ripple characteristics) flows through C_p. In order to observe the relationship between the line current and the leakage current, the line current is also illustrated in Fig. 11(d). Note that in the figure, the small phase current ripple regions yield a small leakage current. From this discussion, it should be also noted that in actual application any voltage on the neutral wire appears in parallel with the equivalent parasitic capacitor of a PV system with grounded frames. Thus, the higher the frequency and amplitude of the voltage induced on the neutral wire due to either by the inverter or other sources, the larger the leakage current.

In Table VI, the peak and rms values of the leakage currents of the simulated TPVI topologies of each group/subgroup are compared. As can also be inferred from the simulation waveforms in Fig. 11, the ZSMC-TPVI topologies exhibit the lowest leakage current characteristics in terms of both the peak and the rms values. Nevertheless, the members of other TPVI classes have low leakage current levels (less than an ampere), in the order of standard restrictions (for example, the standard DIN VDE 0126-1-1 requires peak leakage currents of less than 300mA). With small common-mode filters included, the leakage current attributes of these TPVI topologies can be further improved. Therefore, the discussed TPVI topology families are feasible in terms of leakage current characteristics.

The above-obtained simulation based leakage current performance results can also be verified by means of analytical/mathematical models of the TPVIs. Such work, which involves common-mode and differential-mode equivalent circuits has been published by the authors in [20], [28], and [29]. Analytical models for the leakage current

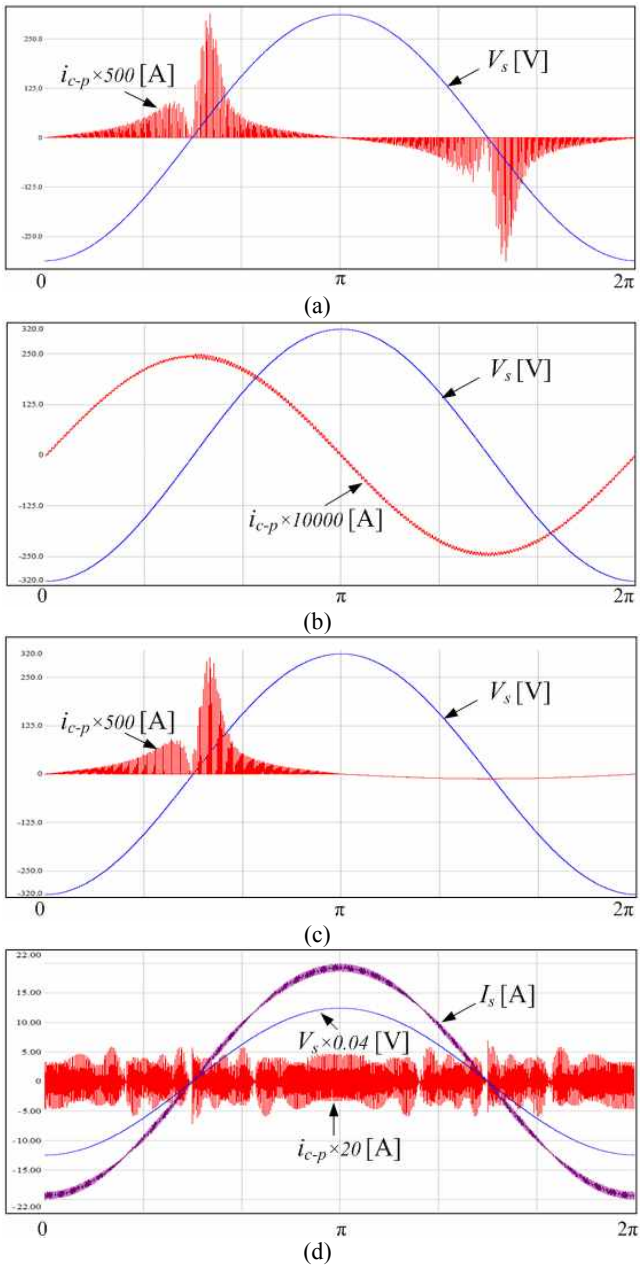

Fig. 11. Illustration of grid voltage (blue), grid current (purple), and parasitic capacitor current (red) of the representatives of TPVItopology classes; (a) H5, (b) topology in [21], (c) ZSH-PT-2, (d) SC-PT-1.

TABLE VI
LEAKAGE CURRENT ATTRIBUTES OF TPVIS

TOPOLOGY	ZSD-TPVI	ZSMC-TPVI	ZSH-TPVI	SC-TPVI
$i_{c\text{-}p}$ (peak)	597 mA	25 mA	596 mA	373 mA
$i_{c\text{-}p}$ (rms)	46 mA	17 mA	33 mA	91 mA

evaluation of several TPVIs are also investigated in [9], [10]. In the analyses and simulations of the leakage currents, the equivalent PV module parasitic capacitance is considerably larger (on the order of tens, hundreds of nF) than the other parasitic capacitances such as case to the heatsink or

semiconductor switch output capacitances. Such small parasitic capacitances (other than the PV module equivalent parasitic capacitance) are taken into consideration neither in the simulations nor in the analyses (for the aforementioned reason and for the sake of simplicity in the analyses and illustration of the effect of the PV module equivalent parasitic capacitor only is considered). Thus, the simulation models as those shown in Fig. 10 are simple and sufficient for the study of basic leakage current, as demonstrated in [30].

VI. Additional Performance Characteristics of the TPVIs

While the leakage current characteristics of the TPVIs are useful in classification and aid in determining topologies with a smaller common/differential mode filter size, the final decision in selecting a topology involves additional features such as the total converter cost, size, efficiency, etc. Thus, it is beneficial to evaluate the discussed topologies according to such characteristics to complement the main approach. For this reason, important additional features will be considered in this section.

TPVIs can be distinguished according to their cost and energy conversion efficiency indicators such as the total number of active switches, the number of switches on the current path, and the number of output voltage levels to determine the most feasible topology for an application. These performance indicators are listed in Table VII for each topology. Among these, the number of active switches emphasizes the cost and complexity of a topology and is directly understood.

The average number of switches on the current path of a topology is proportional to the conduction losses. As a result, it is inversely proportional to the energy conversion efficiency. This indicator for voltage source converters can be calculated by a summation of the averages of all the output voltage states' duty cycle functions $d_{v-j}(\theta)$ weighted by the number of semiconductors on the current path at the associated states $\#s_{v-j}(\theta)$ as formulated in (1), where j denotes the output voltage state index. The duty cycle function is dependent on the modulation index M, which is defined as the ratio of the voltage reference peak value to the dc-bus voltage ($M=V^*_p/V_{dc}$). In Table VII, the average number of switches on the current paths of the topologies are listed for M=0.9 and PF=1 as in [31].

$$\langle \#s \rangle = \sum\nolimits_j \frac{1}{2\pi} \int_0^{2\pi} d_{v-j}(\theta) \#s_{v-j}(\theta)\, d\theta \qquad (1)$$

To obtain information of how the semiconductor ratings are utilized effectively in a topology, a device utilization factor is defined as in (2). This factor is the ratio of the inverter rated power to the total volt-ampere ratings of the switches and it directly relates to the total power semiconductor cost of the converter. In Table VII, the associated normalized C_{DU} values of each topology are listed according to a grid voltage of 230 V. Semiconductors with 600 V and 300 V blocking voltage ratings are assumed depending on the maximum blocking voltage of the associated switch. Normalization is carried out with respect to the conventional full-bridge topology C_{DU} value. It should be noted that the midpoint connecting switches in the related topologies have negligible current ratings. As a result, their contribution to the total switch volt-ampere summation is taken as zero (assuming their cost will be minor).

$$C_{DU} = \frac{P_{rated}}{\sum_k I_{k-peak} V_{k-peak}} \qquad (2)$$

The output voltage level number of a TPVI is another indicator of the cost and the energy conversion efficiency since the output filter inductor losses and size are tightly related to this number. In Table VII, the output voltage level number of each topology is also listed. As the number increases, the peak to peak current ripple can be decreased. As a result, either the switching frequency can be decreased or the filter size and losses can be reduced for the same current total harmonic distortion. In the study in [31], the term ripple factor for the output filter inductor is defined and it is observed that the peak value of this factor is halved when the output voltage level number is increased from 3 to 5. From the performance indicators formed in Table-VII for the voltage source type TPVI topologies, it is clear that the three-level NPC, the T-type and the topology in [25] have superior performance in terms of the number of active switches (4 for single-phase systems). In terms of the number of switches on the current path, the T-type topology and the topology in [27] have a small numerical value. Therefore, these topologies are expected to exhibit superior energy conversion efficiency performance. In the output voltage level number, which is another indicator of energy conversion efficiency, the topology in [27], the SC-PT1 topology, and the SC-PT2 topology have the best characteristics since they have a 5-level output voltage. Although there is a superior size reduction and an efficiency increase in 5-level topologies, it should be noted that the device utilization factor greatly decreases in 5-level topologies as the number semiconductors utilized is increased.

It should be noted that the specific efficiency and cost values of a TPVI for a PV application are subject to the available power semiconductors in the market and the design criteria. Numerical efficiency evaluations and comparisons are provided by the authors in [28], [32] and other publications such as [33]. These studies confirm the basic conclusions arrived in this discussion. Therefore, it is the design engineers' task to set the converter specifications, select the device ratings and complete the design to obtain a final efficiency characteristic and final converter cost.

TABLE VII
PERFORMANCE ATTRIBUTES OF TPVIS

	TOPOLOGY	Total active switches	Switches on current path	C_{DU} (normalized)	Output voltage level
ZSD-TPVI	H5	5	2.57	0.88	3
	HERIC [17]	6	2	0.67	3
	H6 in [18]	6	3	0.67	3
	Topology in [19]	6	2.57	1	3
	H6 in [8]	6	3	1	3
	ZSD-PT-1 [20]	6	2.28	0.88	3
ZSMC-TPVI	iH5 [11]	6	2.57	0.88	3
	Topology in [21]	6	4	0.67	3
	ZSMC-PT-1 [28]	7	2	0.67	3
	ZSMC-PT-2 [28]	7	2.57	1	3
	ZSMC-PT-3 [28]	7	3	0.88	3
ZSH-TPVI	HB-ZVR [22]	5	2.43	0.8	3
	ZSH-PT-1 [28]	6	2	0.67	3
	ZSH-PT-2 [28]	5	2.57	0.88	3
	ZSH-PT-3 [28]	6	2.57	1	3
	ZSH-PT-4 [28]	6	2.28	0.88	3
SC-TPVI	NPC	4	2	1	3
	T-type	4	1.43	0.67	3
	Flying Capacitor	4	2	1	3
	Topology in [25]	4	2	1	3
	Topology in [26]	5	3	0.8	3
	Topology in [27]	8	1.67	0.4	5
	SC-PT-1 [28]	8	2.02	0.5	5
	SC-PT-2 [28]	8	2	0.5	5

This discussion mainly provides help in making a favourable topology choice.

VII. CONCLUSION

Grid-connected transformerless PV inverters (TPVIs) are favourable when compared to transformer based structures in the applications due to their positive attributes of high efficiency, low cost, small size, and improved lifespan. However, one main concern involves the leakage current, safety, and reliability issues due to the lack of galvanic isolation. Thus, many inverter topologies have been invented. This paper surveyed these topologies, and evaluated and classified them in terms of leakage current behaviour as a prime characteristic involving their feasibility in the application field. In addition, TPVI topologies are investigated with respect to several performance attributes such as the total number of active switches, the number of switches on the current path, and the device utilization factor. All of these are directive in the topology selection in applications.

With the aid of the leakage current based classification approach, a large number of topologies can be placed in a small number of basic groups. Thus, this classification yields a simplified overview of the topologies. Not only the topologies could be placed under a simplified tree, but also the switching patterns exhibit commonalities, aiding the design and implementation engineers. Furthermore, this approach has an additional benefit of extending the families with new topology members based on the classification method. Thus, a family tree of topologies with basic switching patterns becomes available to engineers for topology selection, design, development, and implementation.

Having defined the topology family tree and the switching patterns, the leakage current characteristics could be demonstrated by means of system simulations of selected family members. It is shown that in the zero state decoupling methods the mismatch between the line voltage and the parasitic capacitor voltage is the cause of leakage current, while in the solidly clamped methods the neutral wire voltage variation plays the major role. In the zero state midpoint connected methods, the leakage current is the lowest since the grid voltage is followed by the parasitic capacitance. It has been shown that the leakage current peak and rms values are less than an ampere. These values are within the level of standard requirements that could be easily reduced to meet the restrictions by small common-mode filters. Therefore, the TPVI family is feasible in terms of the leakage current characteristics. These findings are in accordance with the wide spread use of TPVI technology based products in the application field.

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