

# Dual-Output Single-Stage Bridgeless SEPIC with Power Factor Correction

Chih-Lung Shen<sup>†</sup> and Shih-Hsueh Yang<sup>\*</sup>

<sup>†\*</sup>Dept. of Electronic Eng., National Kaohsiung First University of Science and Technology, Kaohsiung, Taiwan

## Abstract

This study proposes a dual-output single-stage bridgeless single-ended primary-inductor converter (DOSSBS) that can completely remove the front-end full-bridge alternating current–direct current rectifier to accomplish power factor correction for universal line input. Without the need for bridge diodes, the proposed converter has the advantages of low component count and simple structure, and can thus significantly reduce power loss. DOSSBS has two uncommon output ports to provide different voltage levels to loads, instead of using two separate power factor correctors or multi-stage configurations in a single stage. Therefore, this proposed converter is cost-effective and compact. A magnetically coupled inductor is introduced in DOSSBS to replace two separate inductors to decrease volume and cost. Energy stored in the leakage inductance of the coupled inductor can be completely recycled. In each line cycle, the two active switches in DOSSBS are operated in either high-frequency pulse-width modulation pattern or low-frequency rectifying mode for switching loss reduction. A prototype for dealing with an 85–265 V<sub>rms</sub> universal line is designed, analyzed, and built. Practical measurements demonstrate the feasibility and functionality of the proposed converter.

**Key words:** Bridgeless PFC, Coupled inductor, Dual-output converter, Single stage, Universal line input

## I. INTRODUCTION

The topologies of power factor corrector (PFC) generally contain buck, boost, buck–boost, Zeta, ‘Cuk, single-ended primary-inductor converter (SEPIC), and flyback. Buck PFC can decrease the input voltage to obtain an output voltage less than the peak value of the line voltage [1]. However, zero-crossing distortion degrades power factor. On the contrary, boost PFC can achieve a unity power factor, but its output voltage is higher than its input. Boost PFC cannot deal with the applications of low output voltage, unless it embeds a step-down direct current (dc)/dc stage. Another disadvantage of boost PFC is that power components withstand high-voltage stresses [2], [3]. Buck–boost can obtain an output voltage whose magnitude is either larger or smaller than the input. Nevertheless, the polarity reversal on output and isolated driving requirement will become potential problems [4]. Similar to buck–boost, ‘Cuk and Zeta have the feature of stepping up or down input voltage. However, pulsating input

current and high-side driving are required for Zeta, while ‘Cuk still has the polarity reversal problem [5]–[7]. Flyback PFC can resolve the polarity reversal problem and possesses the characteristic of galvanic isolation, but it has the significant drawback of low efficiency [8]–[13]. Compared with the aforementioned step-up/step-down PFCs, the SEPIC type performs better in total harmonic distortion (THD), efficiency, and power factor [14]–[16].

To reduce component count and improve efficiency, a bridgeless structure attracts a great deal of interest in fulfilling power factor correction. Although high efficiency can be achieved in typical bridgeless PFC topologies derived from boost, buck, or buck–boost [17]–[20], the aforementioned drawbacks still exist. Some researchers have proposed a bridgeless PFC with respect to SEPIC configuration [21]–[23]; however, two diodes are needed to accomplish rectification. Given that the two diodes have to block a voltage higher than the mains, the problems of large cut-in voltage and reverse recovery losses remain. In literature [24], the front-end alternating current–dc bridge rectifier is completely done away with, but the step-down property is lost.

To overcome all the mentioned drawbacks, a novel dual-output single-stage bridgeless SEPIC (DOSSBS) with power factor correction is proposed (Fig. 1). Unlike the

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<sup>†</sup>Corresponding Author: clshen@ncku.edu.tw

Tel: +84908337518, Nat'l Kaohsiung First Univ. of Science and Tech.

<sup>\*</sup>Dept. of Electronic Eng., National Kaohsiung First University of Science and Technology, Taiwan

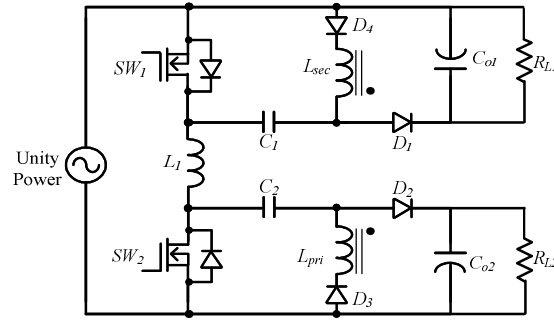


Fig. 1. Main power circuit of the proposed DOSSBS.

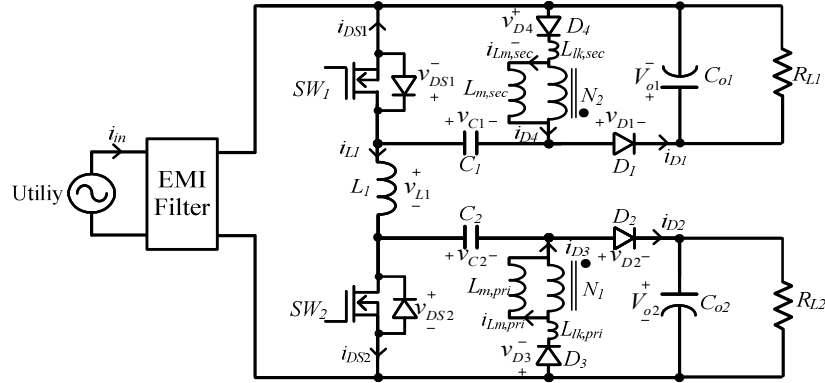


Fig. 2. Representation of voltage polarity and current direction of the proposed converter.

conventional PFC, the proposed DOSSBS can complete power factor correction without the need for a front-end bridge rectifier, which therefore simplifies converter structure, avoids the problem of power loss on rectifier diode, and decreases component count. DOSSBS is distinguished by the features of single stage, bridgeless, and high efficiency. It can also provide dual individual outputs in a single stage. A 100 W universal line input prototype is built and examined for verification. Experimental results validate the proposed DOSSBS.

With respect to practical applications, the proposed DOSSBS can serve as a power supply with power factor correction to drive electric appliances, which need two different levels of source voltage. DOSSBS can power appliances in a single converter, instead of two separate converters, thereby yielding high energy conversion efficiency and low cost. For example, in an intelligent lighting system application, DOSSBS can simultaneously drive light-emitting diodes and provide power for the dimming circuits of the communication interface.

The remainder of this paper is organized as follows. Section II describes the operation principle of the proposed DOSSBS. Section III deals with the design considerations of the converter. Section IV provides practical measurements and a performance comparison with other PFCs. Finally, Section V concludes.

## II. OPERATION PRINCIPLE

For the operation description of the proposed DOSSBS, the

definitions of current direction and voltage polarity are given in Fig. 2. The two active switches alternately operate at a high frequency within an interval of line cycle. During the positive half-line cycle,  $SW_1$  is always closed, and  $SW_2$  operates at a high frequency. During the negative half-line cycle,  $SW_1$  switches in a high frequency, while  $SW_2$  is kept in on-state. As the high-frequency switching pattern is not in constant use, the switching loss of the proposed converter can be significantly reduced.

The operation of the converter can be divided into four main modes over one switching period. Figs. 3 and 4 show the corresponding equivalents and conceptual key waveforms when the converter is operated in the positive half cycle respectively. The corresponding mode-equivalents and conceptual key waveforms in the negative cycle are illustrated in Figs. 5 and 6. The converter operation in the positive half cycle is discussed mode by mode below.

**Mode 1 [Fig. 3(a),  $t_0$ - $t_1$ ]:** Over the entire positive half-line cycle,  $SW_1$  is always in on-state, while  $SW_2$  is operated in a high switching frequency to control input current.  $SW_2$  is turned on at the beginning of mode 1. In mode 1, input voltage is directly connected to the input inductor  $L_1$ . The current  $i_{L1}$  is linearly built, and the capacitor  $C_2$  dumps energy to the primary of the coupled inductor through  $SW_2$  and  $D_3$ . Meanwhile, the capacitor  $C_{o2}$  supplies energy for the load  $R_{L2}$ , and the capacitor  $C_{o1}$  for the load  $R_{L1}$ . The voltage across the inductor  $L_1$  is given by

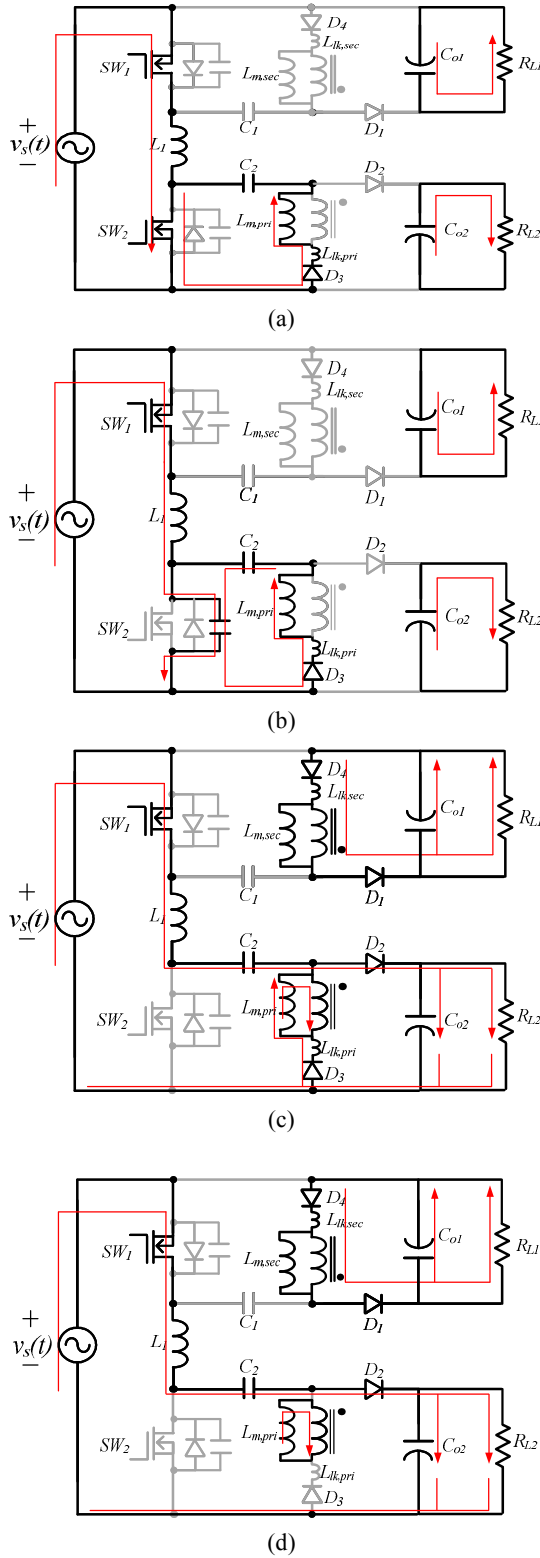


Fig. 3. Equivalents during one switching period in the positive half-line cycle. (a) Mode 1, (b) Mode 2, (c) Mode 3, and (d) Mode 4.

$$v_{L1} = v_s(t) + V_{DS1,on} - V_{DS2,on}, \quad (1)$$

where  $v_s(t)$  represents the line voltage, and  $V_{DS1,on}$  and  $V_{DS2,on}$  stand for the voltage drop on  $SW_1$  and  $SW_2$  respectively.

Supposing that the line voltage is purely sinusoidal and equal to  $V_m \sin(2\pi f_{line} t)$ , the above equation becomes

$$v_{L1} = V_m \sin(2\pi f_{line} t) + V_{DS1,on} - V_{DS2,on}, \quad (2)$$

where  $V_m$  is the amplitude of line voltage, and  $f_{line}$  denotes the line frequency. The on-state voltage  $V_{DS1,on}$  in Eq. (2) is less than the forward voltage of a rectifier diode. Compared with traditional full-bridge PFCs, the proposed DOSSBS replaces an active switch with two low-frequency rectifier diodes, such that it can significantly decrease conduction loss. The inductor current  $i_{L1}$  can be determined as follows:

$$i_{L1}(t) = i_{L1}(0) + \int_0^t \frac{V_m \sin(2\pi f_{line} t') + V_{DS1,on} - V_{DS2,on}}{L_1} dt', \quad (3)$$

Under the boundary mode operation, given that the initial value of the inductor current  $i_{L1}(0)$  is zero, the converter can achieve zero current switching feature at  $SW_2$ .

In mode 1, the capacitor  $C_2$  discharges to the primary magnetizing inductance  $L_{m,pri}$  and the primary leakage inductance  $L_{lk,pri}$  of the coupled inductor. The current  $i_{D3}$  can be calculated by

$$i_{D3}(t) = i_{D3}(0) + \int_0^t \frac{v_{C2}(t') - V_{DS1,on} - V_{D3,f}}{L_{pri}} dt', \quad (4)$$

where  $v_{C2}(t)$  stands for the voltage across the capacitor  $C_2$ ,  $V_{D3,f}$  means the forward voltage of the diode  $D_3$ , and  $L_{pri}$  denotes the measured inductance with respect to the input terminals of the coupled inductor while the secondary is open.  $L_{pri}$  is the sum of  $L_{m,pri}$  and  $L_{lk,pri}$ .

**Mode 2 [Fig. 3(b),  $t_1$ - $t_2$ ]:** This mode begins as soon as  $SW_2$  is turned off. In mode 2, the energy stored in the inductors  $L_1$ ,  $L_{m,pri}$ , and  $L_{lk,pri}$  continues to increase. The voltage across the parasitic capacitor of  $SW_2$  also increases, but the capacitors  $C_{o1}$  and  $C_{o2}$  still dump energy to the loads  $R_{L1}$  and  $R_{L2}$  respectively. The voltage across  $SW_2$  can be expressed as

$$v_{DS2} = v_s(t) + V_{DS1,on} - v_{L1} = v_{C2}(t) - V_{D3,f} - L_{pri} \frac{di_{D3}}{dt}. \quad (5)$$

The voltage  $v_{DS2}$  continuously increases during mode 2. At the moment that  $v_{DS2}$  reaches the magnitude of input voltage, this mode ends, and the polarities of the inductors  $L_1$ ,  $L_{m,pri}$ , and  $L_{lk,pri}$  reverse. All the inductors start discharging.

**Mode 3 [Fig. 3(c),  $t_2$ - $t_3$ ]:** During this mode, the inductor  $L_1$  releases energy to the capacitors  $C_2$  and  $C_{o2}$ , and the energy stored in the leakage inductance  $L_{lk,pri}$  will be recycled to the output through  $L_{m,pri}$ ,  $D_2$ , and  $D_3$ .  $L_{m,pri}$  dumps energy to  $C_{o2}$  and  $C_{o1}$ .

From the equivalent circuit of mode 3, the voltage across the parasitic capacitor of  $SW_2$  is clamped at  $v_{c2} + V_{o2}$ . Thus, the voltage stress of  $SW_2$ ,  $V_{stress}$ , and  $SW_2$ , can be determined as follows:

$$V_{stress,SW2} = v_s(t)|_{\max} + V_{o2} = V_m + V_{o2}. \quad (6)$$

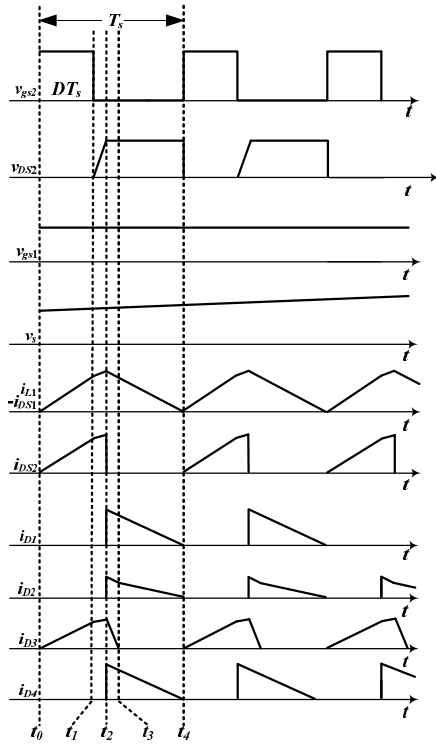


Fig. 4. Conceptual waveforms corresponding to the operation modes in the positive half-line cycle.

The inductor current  $i_{L1}$  can be obtained by

$$i_{L1}(t) = i_{L1}(t_2) - \int_{t_2}^t \frac{V_m |\sin(2\pi f_s t')| + V_{DS1} - V_{C2} - V_{D2,f} - V_{o2}}{L_1} dt' \quad (7)$$

where  $i_{L1}(t_2)$  is the initial value of  $i_{L1}$  at  $t = t_2$ , and  $V_{D2,f}$  is the voltage drop on the diode  $D_2$ . This mode ends when the current of the leakage inductance  $L_{lk,pri}$  drops to zero.

**Mode 4 [Fig. 3(d),  $t_3$ - $t_4$ ]:** In mode 4, the inductor  $L_1$  continues supplying energy to the capacitors  $C_2$  and  $C_{o2}$ , while the coupled inductor transmits energy to  $C_{o1}$ . The current flowing through  $L_{m,pri}$  linearly decreases, which can be estimated by

$$i_{Lm,pri}(t) = i_{Lm,pri}(t_3) - \frac{k}{n} \int_{t_3}^t \frac{(V_{o1} + V_{D1,f} + V_{D4,f})}{L_{m,pri}} dt' \quad (8)$$

In the negative half-line cycle, the roles of  $SW_1$  and  $SW_2$  exchange.  $SW_1$  is operated in high frequency to control input current, while  $SW_2$  is kept in on-state over the entire half cycle. The operation of the proposed converter is symmetrical in two half-line cycles of input voltage. The description of operation in the negative half-line cycle is similar to that in the positive which also has four modes. The equivalent circuits and conceptual waveforms are illustrated in Figs. 5 and 6, respectively.

### III. DESIGN CONSIDERATIONS

#### A. Equivalent Iron Loss Resistance

1)  $V_{o1} = V_{o2}$ : Minimum switching frequency  $f_{sw,min}$  is a key parameter for the design of the input inductor  $L_1$ . Switching

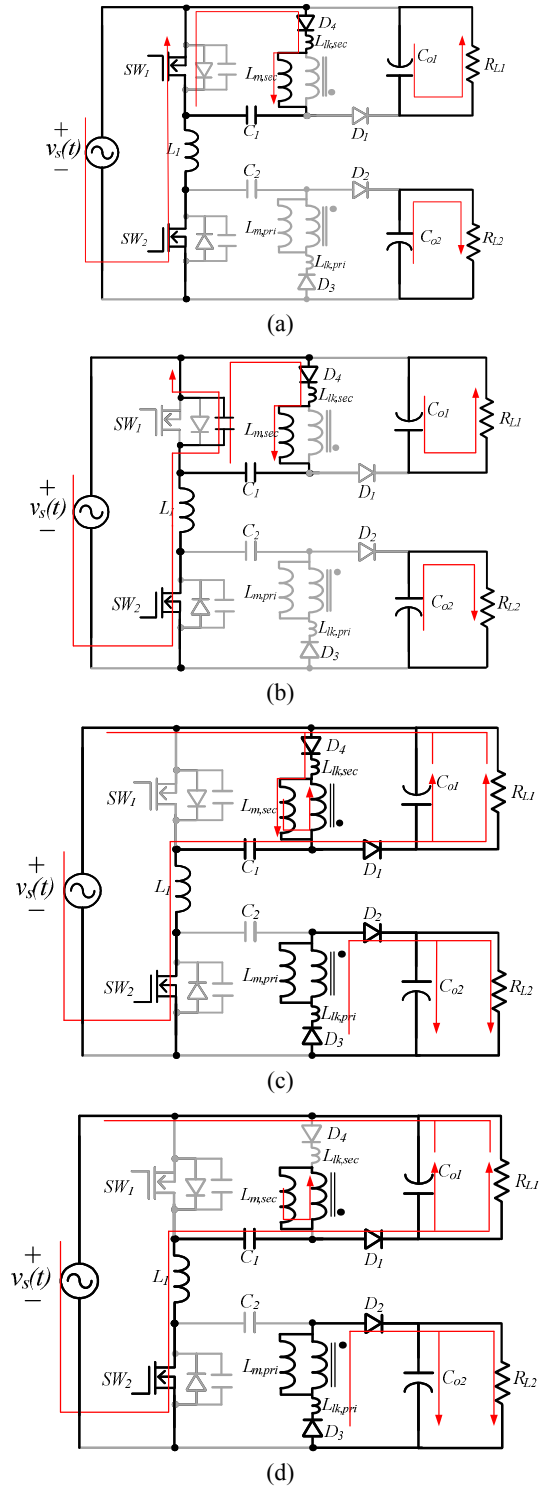


Fig. 5. Equivalent circuits during one switching period in the negative half-line cycle. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4.

frequency can be estimated by determining the on-time and off-time periods of the active switch. As power factor correction is performed under a constant on-time switching pattern,  $f_{sw,min}$  can be obtained after determining the maximum off time. However, a low line input voltage indicates a high on-time interval. Thus, maximum on time  $T_{on,max}$  and maximum off

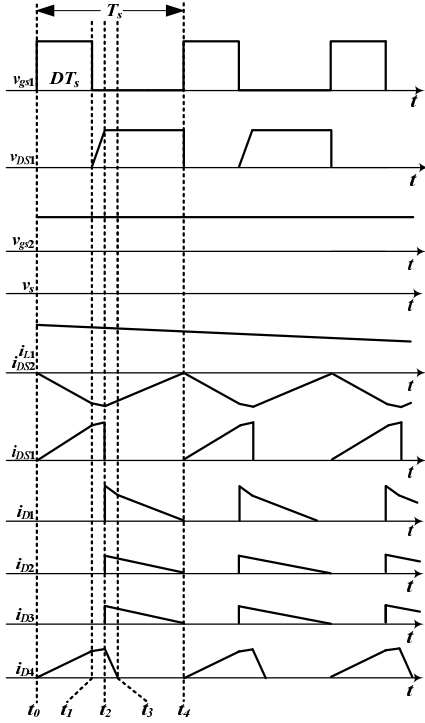


Fig. 6. Conceptual waveforms corresponding to the operation modes in the negative half cycle.

time  $T_{off,max}$  over the range of universal line input should be determined in advance for  $f_{sw,min}$  calculation.

Supposing that the range of universal line input is from  $V_{rms,min}$  to  $V_{rms,max}$ ,  $T_{on,max}$  then occurs when the line voltage is  $V_{rms,min}$ . Given that output power is equal to the multiplication of input power and converter efficiency, the following equation holds:

$$\frac{2 \cdot P_o}{\eta \cdot \sqrt{2} \cdot V_{rms,min}} = \int_0^{T_{on,max}} \frac{\sqrt{2} \cdot V_{rms,min}}{L_1} dt', \quad (9)$$

where  $\eta$  denotes the converter efficiency, and  $P_o$  is the output power. Over a half-line cycle, the maximum off time  $T_{off,max}$  appears at the peak of the sinusoidal line voltage. Accordingly, if the two output voltages of the converter are equal,  $V_{o1} = V_{o2} = V_o$ , then

$$\int_0^{T_{on,max}} \frac{\sqrt{2} \cdot V_{rms,min}}{L_1} dt' - \int_{T_{on,max}}^{T_{on,max} + T_{off,max}} \frac{V_o}{L_1} dt' = 0. \quad (10)$$

From Eqs. (9) and (10), solving  $T_{on,max}$  and  $T_{off,max}$  obtains

$$T_{on,max} = \frac{P_o \cdot L_1}{\eta \cdot V_{rms,min}^2}, \quad (11)$$

and

$$T_{off,max} = \frac{2 \cdot P_o \cdot L_1}{V_o \cdot \eta \cdot \sqrt{2} \cdot V_{rms,min}}. \quad (12)$$

The minimum switching frequency is calculated by

$$f_{sw,min} = \frac{1}{T_s} = \frac{1}{T_{on,max} + T_{off,max}}. \quad (13)$$

Substituting Eqs. (11) and (12) into Eq. (13), we obtain

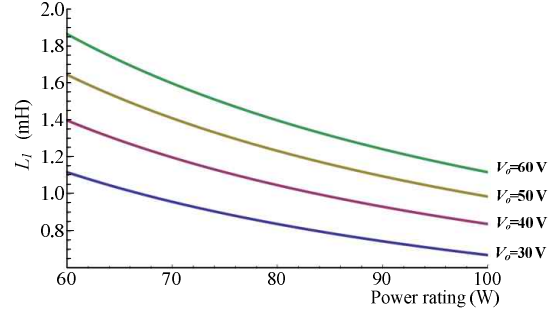


Fig. 7. Relationship between input inductance and output power under different output voltages.

$$f_{sw,min} = \frac{1}{T_s} = \frac{1}{T_{on,max} + T_{off,max}}. \quad (14)$$

To determine the value of the input inductor  $L_1$ , Eq. (14) can be rewritten as

$$L_1 = \frac{\eta \cdot V_{rms,min}^2 \cdot V_o}{P_o \cdot f_{sw,min} \cdot (V_o + \sqrt{2} V_{rms,min})}. \quad (15)$$

Supposing that  $\eta = 0.93$ , then two output voltages are equal, and the minimum line input voltage is  $85 V_{rms}$ . Fig. 7 shows the relationship among input inductance, power rating, and output voltage. High power rating requires low input inductance; under a certain power rating, a high output voltage needs large input inductance. Considering that a small input inductance will result in a high switching frequency, the minimum switching frequency should be larger than 20 kHz to avoid audio frequency.

2)  $V_{o1} \neq V_{o2}$ : The determination of input inductance in Eq. (15) is only suitable for the condition  $V_{o1} = V_{o2}$ . If  $V_{o1} \neq V_{o2}$ , then the minimum switch frequencies of  $SW_1$  and  $SW_2$  will differ. Therefore, two values will be elected as input inductance and are expressed as

$$L_\alpha = \frac{\eta \cdot V_{rms,min}^2 \cdot V_{o2}}{P_o \cdot f_{sw2,min} \cdot (V_{o2} + \sqrt{2} V_{rms,min})}, \quad (16)$$

and

$$L_\beta = \frac{\eta \cdot V_{rms,min}^2 \cdot V_{o1}}{P_o \cdot f_{sw1,min} \cdot (V_{o1} + \sqrt{2} V_{rms,min})}. \quad (17)$$

$f_{sw1,min}$  and  $f_{sw2,min}$  denote the minimum switching frequencies of  $SW_1$  and  $SW_2$  respectively. The smaller one between  $L_\alpha$  and  $L_\beta$  is chosen as the input inductance, that is,

$$L_1 = \min[L_\alpha, L_\beta]. \quad (18)$$

The converter power rating is 100 W, and the minimum line voltage is  $85 V_{rms}$ . Fig. 8 illustrates the relationship among two output voltages and the minimum switching frequencies of  $SW_1$  and  $SW_2$ .  $f_{sw1,min}$  will be larger than  $f_{sw2,min}$  when  $V_{o1} > V_{o2}$ . On the contrary,  $f_{sw1,min}$  is less than  $f_{sw2,min}$  when  $V_{o1} < V_{o2}$ . If  $V_{o1} = V_{o2}$ , both switching frequencies are identical.

$f_{sw1,min}$  and  $f_{sw2,min}$  vary with input line voltage and output power. For example,  $\eta = 0.93$ ,  $V_{o1} = 30 V$ ,  $V_{o2} = 60 V$ , and input inductance  $L_1 = 670 \mu H$ . Fig. 9 shows the relationship

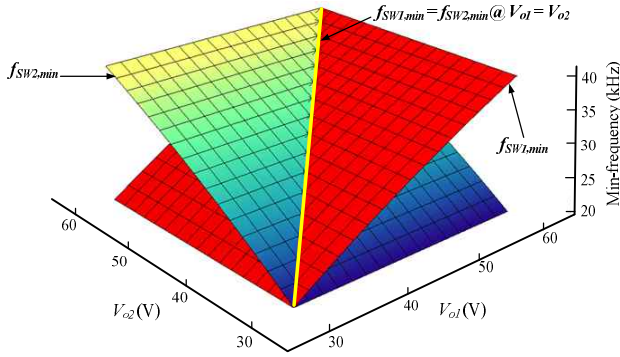


Fig. 8. Relationship among the minimum switching frequencies of  $SW_1$  and  $SW_2$  and dual output voltages.

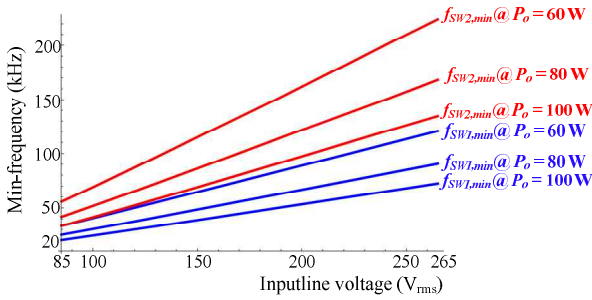


Fig. 9. Relationship between minimum switching frequency and input voltage under different output powers.

among the minimum switching frequencies of the two active switches, input voltage, and output power.

### B. Design of the Coupled Inductance

The coupling coefficient of a coupled inductor can be evaluated as follows:

$$k = \sqrt{1 - \frac{L_{lk,pri}}{L_{pri}}} \quad (19)$$

Rearranging Eq. (19) yields

$$L_{pri} = \frac{L_{lk,pri}}{1 - k^2} \quad (20)$$

When the inductance  $L_{sec}$  is in the output terminals while the primary is open,

$$L_{sec} = \frac{L_{lk,sec}}{1 - k^2} \quad (21)$$

where  $L_{lk,sec}$  is the leakage inductance of the secondary. The relationship between  $L_{lk,pri}$  and  $L_{lk,sec}$  is given by

$$L_{lk,sec} = n^2 L_{lk,pri} \quad (22)$$

The magnetizing inductance in the secondary  $L_{m,sec}$  also equals the primary magnetizing inductance  $L_{m,pri}$  times the square of turn ratio. The following relationship is then derived:

$$L_{sec} = n^2 L_{pri} \quad (23)$$

The terminal voltage of the secondary,  $V_{Lsec}$ , can be computed by

$$V_{Lsec} = n \cdot V_{Lm,pri} = n \cdot k \cdot V_{o2} \quad (24)$$

where  $V_{Lm,pri}$  is the voltage across the magnetizing inductance of the primary. Given that  $k$  is less than unity, the following inequality holds:

$$n^2 > \left( \frac{V_{Lsec}}{V_{o2}} \right)^2 \quad (25)$$

Thus, the design for the coupled inductor should meet the following inequality:

$$L_{sec} > L_{pri} \left( \frac{V_{Lsec}}{V_{o2}} \right)^2 \quad (26)$$

### C. Coupled Capacitance

The energy-transferred capacitors  $C_1$  and  $C_2$  are also key components because their values significantly influence input line current. Both capacitors must be in a proper design for their steady-state voltage waveforms to be consistent with the rectified input line voltage, and the low-frequency oscillating with input inductor or coupled inductor can be avoided. In practical consideration, resonant frequency should be larger than line frequency but less than minimum switching frequency, that is,

$$f_{line} < f_{r1} < f_{sw1,min} \quad (27)$$

and

$$f_{line} < f_{r2} < f_{sw2,min} \quad (28)$$

where  $f_{r1}$  and  $f_{r2}$  are the resonant frequencies of  $L_1$ - $C_2$ - $L_{pri}$  and  $L_1$ - $C_1$ - $L_{sec}$  respectively. They are calculated as

$$f_{r1} = \frac{1}{2\pi\sqrt{C_1(L_1 + L_{sec})}} \quad (29)$$

and

$$f_{r2} = \frac{1}{2\pi\sqrt{C_2(L_1 + L_{pri})}} \quad (30)$$

According to Eqs. (29) and (30), the capacitances of  $C_1$  and  $C_2$  can be calculated by

$$C_1 = \frac{1}{(2\pi f_{r1})^2 (L_1 + L_{sec})} \quad (31)$$

and

$$C_2 = \frac{1}{(2\pi f_{r2})^2 (L_1 + L_{pri})} \quad (32)$$

respectively.

### D. Output Capacitance

The frequency of output ripple is twice the line frequency. A low output voltage ripple is accompanied by a large output capacitance. Once the output voltage ripple  $\Delta V_o$  is specified, the corresponding output capacitance  $C_o$  can be estimated by

$$C_o = \frac{P_o}{4 \cdot f_{line} \cdot V_o \cdot \Delta V_o} \quad (33)$$

### E. Switch Stress

In this converter, the voltage stress across active switch can



TABLE I

KEY COMPONENTS AND VALUES OF THE PROTOTYPE

Component	Value
power MOSFET ( $SW_1$ and $SW_2$ )	IXFH26N50Q
diode ( $D_1$ and $D_4$ )	BYV34
diode ( $D_2$ )	30US30DN
diode ( $D_3$ )	MBR854
coupled capacitance ( $C_1$ )	680 nF
coupled capacitance ( $C_2$ )	2 $\mu$ F
coupled inductance ( $L_{pri}$ )	850 $\mu$ H
inductance ( $L_{sec}$ )	3.4 mH
input inductor ( $L_I$ )	670 $\mu$ H
output capacitor of port 1 ( $C_{o1}$ )	1000 $\mu$ F
output capacitor of port 2 ( $C_{o2}$ )	470 $\mu$ F

be estimated by the peak value of the uppermost universal line voltage  $V_{pk,max}$  plus output voltage. Therefore,

$$V_{stress,SW1} = V_{pk,max} + V_{o1}, \quad (34)$$

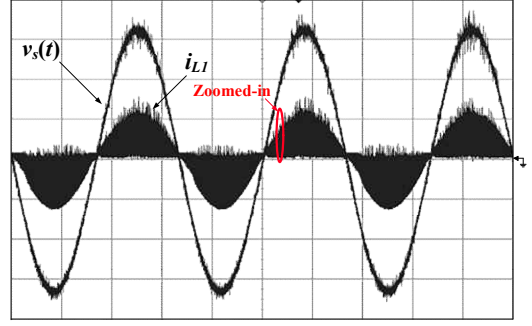
and

$$V_{stress,SW2} = V_{pk,max} + V_{o2}. \quad (35)$$

#### IV. EXPERIMENTAL RESULTS

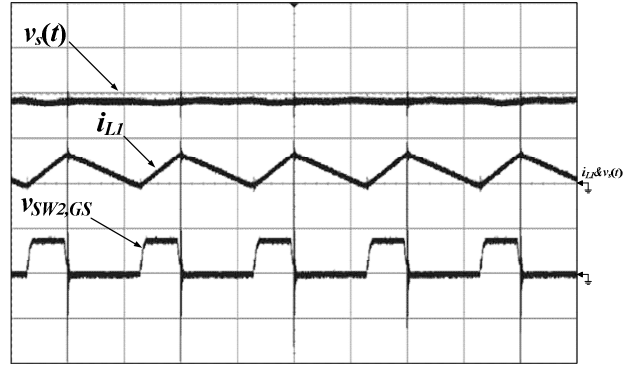
A prototype is built, simulated, and examined to verify the feasibility of the proposed DOSSBS. In the prototype, the universal line input voltage is over the range of 85-265 V<sub>rms</sub>, the line frequency is 60 Hz, the output voltage of ports 1 and 2 are 30 and 60 V respectively, that of port 2 is 60 V, and the converter power rating is 100 W. The key component values are summarized in Table I.

Fig. 10 shows the measured waveforms of the line voltage  $v_s$  and the input inductor current  $i_{LI}$  at full load when the line voltage is 110 V<sub>rms</sub>. The envelope of  $i_{LI}$  in Fig. 10 is sinusoidal and can be in phase with the line voltage. In the positive half-line cycle,  $SW_2$  is operated at a high frequency, but  $SW_1$  is always in on-state. Fig. 11 shows the zoomed-in waveforms in the positive half-line cycle. The control signal of  $SW_2$  is in a high frequency, and the input inductor current is controlled at a boundary conduction manner. The filtered source current  $i_{in}$  is shown in Fig. 12, which illustrates that  $i_{in}$  is sinusoidal and in phase with the line voltage. Fig. 13 shows the two output voltages at ports 1 and 2 to demonstrate that both ports can be kept constant at 30 and 60 V under full load. Figs. 14 and 15 present the corresponding waveforms of the step-change transient response of DOSSBS, while the output power at port 1 changes from light to heavy load and from heavy to light load respectively. Both figures indicate that even under step-change loading, DOSSBS still can still feature rapid transient response and sustain stable output voltages. The waveforms of  $v_{C1}$  and  $v_{C2}$  are presented in Fig. 16, which depicts that the positive voltages of  $v_{C1}$  and  $v_{C2}$  are sinusoidal, and the maximum negative voltages equal the output voltages of ports 1 and 2.



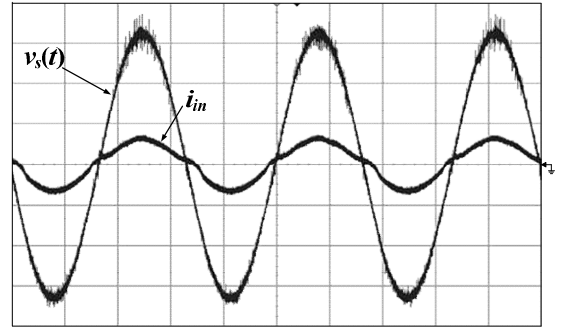
( $v_s$ : 50 V/div,  $i_{LI}$ : 1 A/div, time: 5 ms/div)

Fig. 10. Measured waveforms of the line voltage  $v_s$  and the input inductor current  $i_{LI}$  at full load.



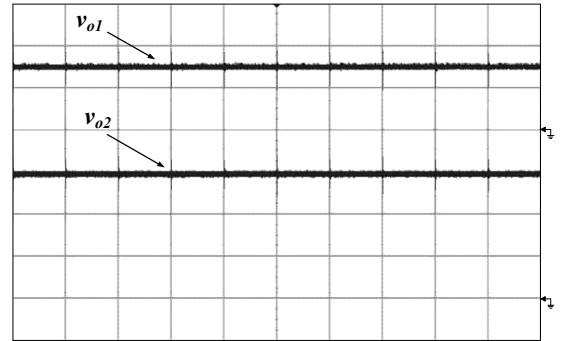
( $v_s$ : 50 V/div,  $i_{LI}$ : 1 A/div,  $v_{SW2,GS}$ : 20 V/div, time: 20  $\mu$ s/div)

Fig. 11. Zoomed-in waveforms of input inductor current and associated control signal in the positive half-line cycle.



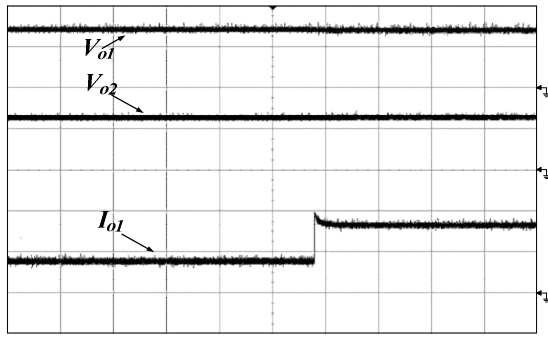
( $v_s$ : 50 V/div,  $i_{in}$ : 2 A/div, time: 5 ms/div)

Fig. 12. Measured waveforms of line voltage and filtered source current.



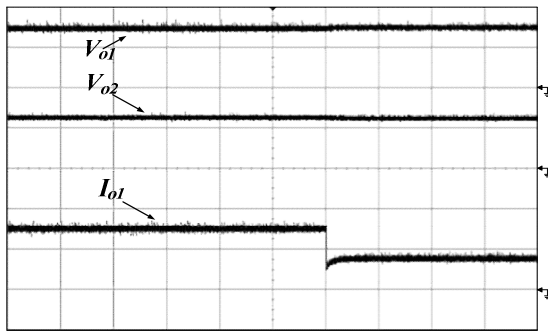
( $V_{o1}$ : 20 V/div,  $V_{o2}$ : 20 V/div, time: 5 ms/div)

Fig. 13. Measured waveforms of output voltages at ports 1 and 2.



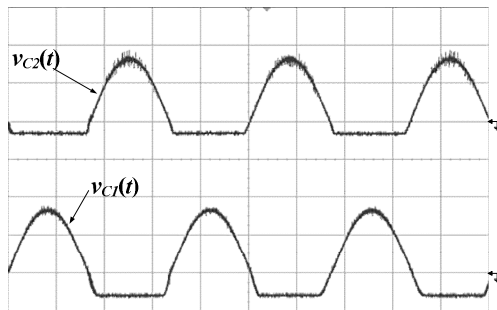
( $V_{o1}$ : 20 V/div,  $V_{o2}$ : 50 V/div,  $I_{o1}$ : 1 A/div, time: 50 ms/div)

Fig. 14. Related waveforms while the output power of port 1 changes from light to heavy load.



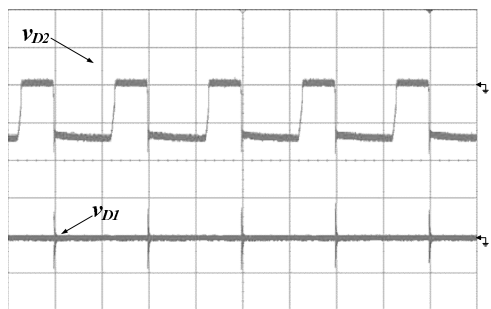
( $V_{o1}$ : 20 V/div,  $V_{o2}$ : 50 V/div,  $I_{o1}$ : 1 A/div, time: 50 ms/div)

Fig. 15. Related waveforms while the output power of port 1 changes from heavy to light load.



( $v_{C2}$ : 100 V/div,  $v_{C1}$ : 100 V/div, time: 5 ms/div)

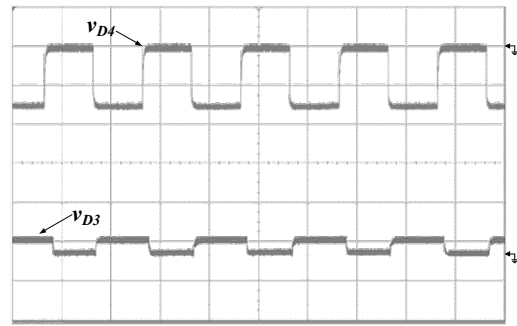
Fig. 16. Measured waveforms of  $v_{C1}$  and  $v_{C2}$ .



( $v_{D2}$ : 100 V/div,  $v_{D1}$ : 10 V/div, time: 20  $\mu$ s/div)

Fig. 17. Measured waveforms of  $v_{D1}$  and  $v_{D2}$ .

Fig. 17 presents the voltages across the diodes  $D_1$  and  $D_2$  when the line voltage  $v_s$  increases to 90 V. The blocking voltage of  $D_2$  is equal to  $v_{C2}$  plus output voltage at port 2, at approximately



( $v_{D4}$ : 50 V/div,  $v_{D3}$ : 10 V/div, time: 20  $\mu$ s/div)

Fig. 18. Measured waveforms of  $v_{D3}$  and  $v_{D4}$ .

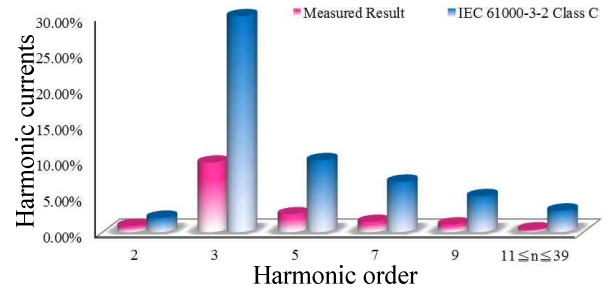


Fig. 19. Measured result of current harmonics.

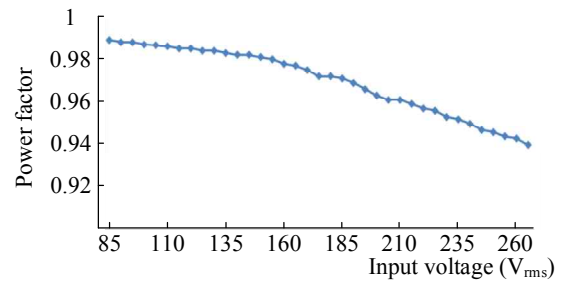


Fig. 20. Measured power factor over the range of universal line input at full load.

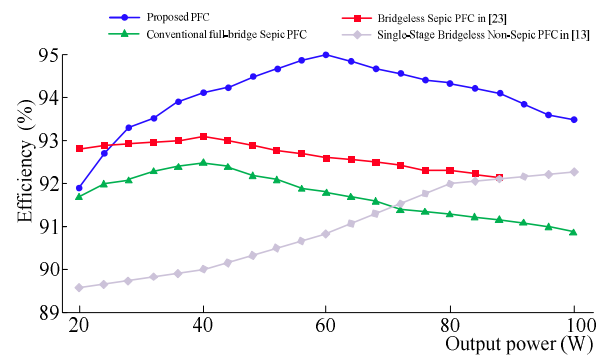


Fig. 21. Efficiency measurement from light to full load while line voltage is 110  $V_{rms}$ .

150 V. Under the same input voltage of 90 V, the measured waveforms of  $v_{D3}$  and  $v_{D4}$  are shown in Fig. 18. The reversed voltage across  $D_4$  is approximately 75 V. The result of harmonic measurement is shown in Fig. 19, which expresses that DOSSBS can meet the standard of IEC 61000-3-2 Class C.



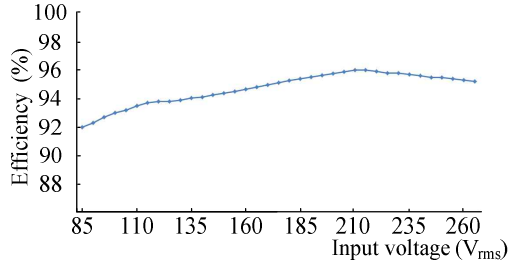


Fig. 22. Efficiency measurement over the range of universal line input from 85 V<sub>rms</sub> to 265 V<sub>rms</sub>.

TABLE II  
COMPARISON AMONG THE PROPOSED CONVERTER AND OTHER  
TYPES OF SINGLE-STAGE PFC

	[13]	[16]	[20]	[23]	[24]	proposed
<b>MOSFETs</b>	2	1	1	2	2	2
<b>fast diodes</b>	1	4	3	1	2	4
<b>slow diodes</b>	2	4	4	2	0	0
<b>capacitors</b>	3	3	2	3	4	4
<b>coupled inductor</b>	1	0	0	0	0	1
<b>inductors</b>	0	2	2	3	3	1
<b>output ports</b>	1	1	1	1	1	2

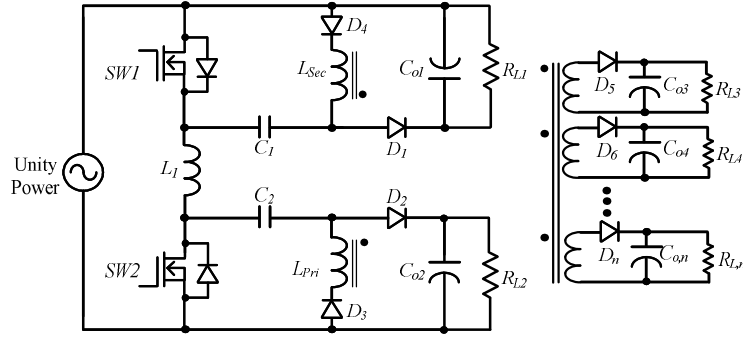


Fig. 23. Main circuit schematic of the expanded configuration of the proposed converter.

The measured THD is 14.8%. Fig. 20 shows the measured power factor over the range of universal line input at full load, in which the maximum power factor approaches unity. Figs. 21 and 22 illustrate the prototype efficiency. Fig. 21 shows the efficiency curve from 4 W to 100 W, while line voltage is 110 V<sub>rms</sub>. The figure also demonstrates that DOSSBS can achieve the highest efficiency among the converters of conventional full-bridge SEPIC PFC, bridgeless SEPIC PFC, and bridgeless non-SEPIC PFC. The maximum efficiency of the prototype is up to 95% at approximately 60 W. Efficiency measurement over the entire range of universal line input under full load is presented in Fig. 22, in which the efficiencies at 110 and 220 V<sub>rms</sub> are 93.5% and 95.7% respectively. A comparison with other types of single-stage PFC is summarized in Table II. The proposed converter does not require low-speed diode and dual-output topology.

## V. CONCLUSION

This study proposes DOSSBS PFC, which can deal with a wide range of input of 85-265 V<sub>rms</sub> of universal line and provide dual outputs. In the proposed converter, the front-end rectifier is completely removed, thereby simplifying configuration, decreasing component count, and reducing conduction losses. A coupled inductor is incorporated to

replace two separate inductors and thus reduce converter volume, as well as recycle the energy stored in leakage inductance. Practical measurements validate the proposed DOSSBS, whose configuration can be expanded for multiple-output applications. Fig. 23 shows the main power schematics, in which the inductors of all the additional output ports can be coupled with  $L_{pri}$  and  $L_{sec}$ .

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**Chih-Lung Shen** was born in Tainan, Taiwan, R.O.C. in 1962. He received his B.S. degree from National Taiwan University of Science and Technology, Taipei, Taiwan in 1988; his M.S. degree from National Tsing-Hua University, Hsinchu, Taiwan in 1991; and his Ph.D. degree from National Chung Cheng University, Chia-Yi, Taiwan, R.O.C. in 2003, all in electrical engineering. He is currently with the Department of Electronic Engineering, National Kaohsiung First University of Science and Technology (NKFUST), Kaohsiung, Taiwan, where he is a full professor, the department director of Electronic Engineering, and the director of the Photovoltaics Technology Research Center. His research interests include electric ignition system, photovoltaic-powered systems, active power filters, and power converter design.



**Shih-Hsueh Yang** was born in Kaohsiung, Taiwan in February 1989. He received his B.S. degree in Undergraduate Honors Program of Engineering in 2011 and his M.S. degree in Industrial Technology Master Program on Green Energy and IC Design in 2013 from NKFUST. His research interests include power conversion dc/dc, ac/dc PFC converters, dc/ac inverters, and analog IC design.