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Design of Parallel-Operated SEPIC Converters Using Coupled Inductor for Load-Sharing

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Abstract

This study discusses the design of a parallel-operated DC-DC single-ended primary-inductor converter (SEPIC) for low-voltage application and current sharing with a constant output voltage. A coupled inductor is used for parallel-connected SEPIC topology. Generally, two separate inductors require different ripple currents, but a coupled inductor has the advantage of using the same ripple current. Furthermore, tightly coupled inductors require only half of the ripple current that separate inductors use. In this proposed work, tightly coupled inductors are used. These produce an output that is more efficient than that from separate inductors. Two SEPICs are also connected in parallel using the coupled inductors with a single common controller. An analog control circuit is designed to generate pulse width modulation (PWM) signals and to fulfill the closed-loop control function. A stable output current-sharing strategy is proposed in this system. An experimental setup is developed for a 18.5 V, 60 W parallel SEPIC (PSEPIC) converter, and the results are verified. Results indicate that the PSEPIC provides good response for the variation of input voltage and sudden change in load.

Key words: Converter, Coupled, Parallel, Pulse Width modulation , Ripple, Single-ended Primary-inductor Converter

I. INTRODUCTION

The DC-DC converters that operate in parallel have several advantages, such as low component stress, good thermal management, more reliability, and less maintenance than single DC-DC converters. The single-ended primary-inductor Converter (SEPIC) is a DC-DC converter that possesses reduced output ripple, high efficiency, and high-voltage transfer gain. The minimum values of the equivalent inductance and capacitance are calculated. The Minimum Value of the Output Voltage Ripple and the switch peak current are calculated in Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode. The stress of the switching current and the design method were discussed to determine the equivalent inductance and capacitance of the SEPIC in [1].

A stability property of the closed- loop control procedure was developed to design a globally asymptotical stabilizing linear proportional plus integral controllers for SEPIC in [2]. The optimization technique for a Proportional -Integral-Derivative (PID) controller to achieve Maximum-Power-Point Tracking of SEPIC was discussed. A weight function based on gradient descent method was developed to optimize the PID parameters by adding a low-pass filter term [3]. The operational analysis of an isolated time-sharing dual-input, single-ended primary-inductor was analyzed. A study demonstrated that active-clamping technique and zero-voltage switching can be achieved on the first-turned-on input leg, and the active-clamping leg with a proper driving strategy reduces component stress [4].

The investigation of coupled-inductor SEPIC design issues focused on the correlation that exists among the sizes of the coupling capacitor and the magnetic coupling factor of coupled inductors. The voltage conversion ratio and amplitude of the peak-to-peak ripple current in the input and output ports of the coupled inductors were demonstrated [5].Voltage multiplier and active-clamp techniques were applied to the conventional SEPIC converter to increase the voltage gain and reduce the voltage stresses of the power switches and diode [7]. The proposed converter utilizes a single controlled power switch and two inductors; it can provide high-voltage gain without an

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extreme switch duty cycle. The two inductors can be coupled into one core to reduce the input current ripple without affecting the basic DC characteristic of the converter. Moreover, voltage stresses across all the semiconductors are less than half of the output voltage [8].

A Proportional Integral (PI) controller was designed to reduce the output current ripple for SEPIC, which demonstrates the possibility of eliminating the Electro Magnetic Interference (EMI) filter [9]. Non-isolated bidirectional soft-switching SEPIC/ZETA converter with reduced ripple currents was discussed. The SEPIC/ZETA explains that can be operated in the forward SEPIC and reverse ZETA modes with reduced ripple currents, and have increased voltage gains that are attributed to the optimized selection of duty ratios [10].

The tightly coupled inductor structure only requires a single core for mutual inductance to force the ripple current into splitting equally between two coupled inductors [11].

A high step-up DC-DC converter with a coupled-inductor and voltage-doubler circuits was discussed, and the converter achieved high step-up voltage gain with an appropriate duty ratio and low-voltage stress on the power switches. The energy stored in the leakage inductor of the coupled inductor can also be recycled to the output with the operating principles and the steady-state analyses of the converter in [12]

Considering all these facts, a coupled inductor is used in the present study, and a parallel operation of SEPIC with current sharing method is proposed. The PSEPIC is operating with CCM using a PI controller. First, a state-space model for a PSEPIC is derived, and then a PI controller is designed for control. The performance of the PI controller and the coupled inductor topology are assessed in terms of load-current sharing and stability, which are implemented in analog platform. This parallel-operated SEPIC with the coupled inductor design has numerous advantages, such as improved stability, robustness, and good dynamic response.

This paper is organized as follows: The basic operation of a SEPIC converter is presented in Section II. The design of the proposed PSEPIC converter is given in Section III. The simulation results of the proposed PSEPIC converter using a PI controller under a step-load change and step-input voltage-change conditions are discussed in Section IV. The experimental results of PSEPIC with the coupled inductor are revealed in Section V. The conclusion is discussed in Section VI.

II. SEPIC CONVERTER

SEPIC is a type of DC-DC converter that allows its output to be greater than, less than, or equal to the input voltage. The duty cycle of the control transistor controls the SEPIC output. The SEPIC circuit is presented in Fig. 1. It consists of input supply, inductors L_{1a}, L_{1b}, switch S_1, diode D_1, capacitor C_1, output capacitors C_2, and resistor R. The SEPIC exchanges

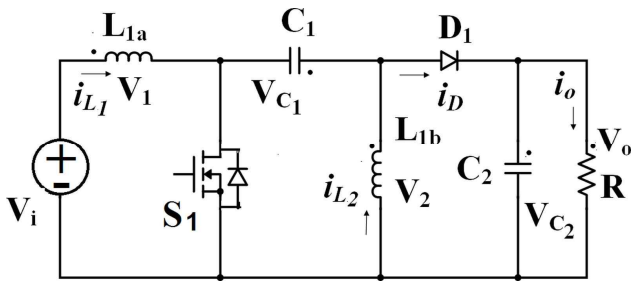
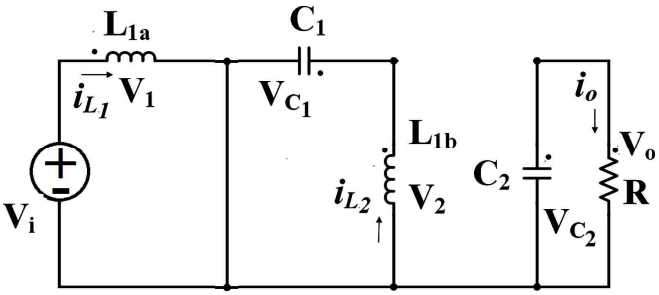
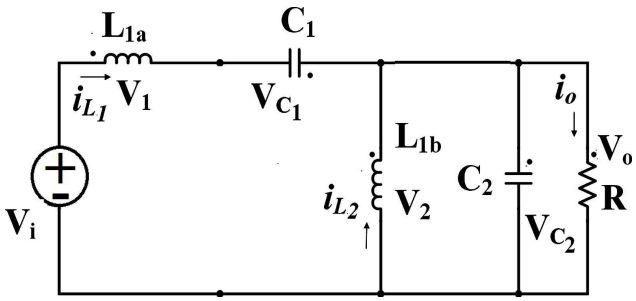


Fig. 1. Schematic of a SEPIC Converter.



(a)



(b)

Fig. 2. (a) SEPIC during Switch-On Mode. (b) SEPIC during Switch-Off Mode.

energy between the capacitors and inductors to convert from one voltage to another. Switch S_1 controls the amount of energy exchanged.

Figs. 2(a) and 2(b) show the operational modes of the SEPIC. In Fig. 2(a), the diode D_1 is reverse-biased and open, and the source voltage v_i occupies the Inductor L_{1a} when the switch S_1 is closed. When switch S_1 is off, the current that passes through capacitor C_1 becomes the same as the current i_{L1a}. Furthermore, we can conclude that power is delivered to the load from both L_{2a} and L_{1a} while S_1 is off. L_1 changes C_1 during this off mode, and will, in turn, recharge L_2 during the on mode, as shown in Fig. 2(b).

Fig. 3. shows the circuit diagram of a SEPIC with a coupled inductor.

III. DESIGNING OF PROPOSED PSEPIC CONVERTER

A parallel connection of a SEPIC converter is a reliable and efficient way to increase the power rating of the SEPIC

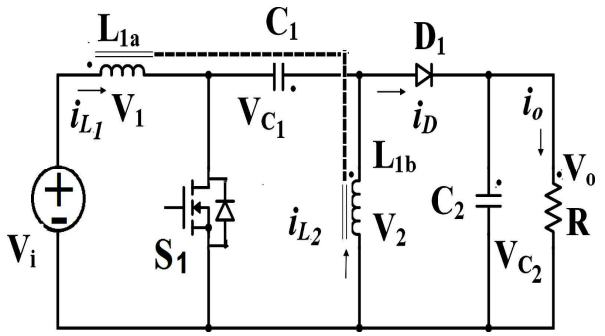


Fig. 3. SEPIC with a coupled inductor.

module, which removes the limit of the current ceiling of power semiconductor switches. PSEPIC is a viable alternative method to satisfy the power requirement, which can be more than the capacity of the large single SEPIC module.

PSEPIC requires a current-sharing mechanism to ensure proper operation. Various methods can be used to obtain load-current sharing, such as average current sharing, master–slave scheme, democratic current sharing, and autonomous master–slave scheme. In this study, a simple PI controller is used to force the output voltage of the PSEPIC into following the voltage reference. The main benefits of this PSEPIC are robustness, stability of output voltage, lower component count, and lower inductor value compared with operating two SEPIC converters with separate inductors.

Conventional SEPIC possesses two inductors, L_{1a} and L_{2a}. Therefore, this tool requires a large space in the printed circuit board. The tightly coupled inductors are inside a single package when used in the proposed PSEPIC, which provides not only compactness, but also uses the same ripple current. Half of the inductor value that the separate inductors have can be used because the proposed PSEPIC is a coupled inductor. Fig. 4. shows the block diagram of the proposed PSEPIC.

The designed PSEPIC works in a cycle with a small off-mode to avoid EMI. Only one SEPIC operates for a low load. If the load exceeds more than 50% of the load current, then the other SEPIC shares the load current. Hence, less circuit losses occur and the components experience no stress. Identical components are used for both SEPIC converters. A switch control circuit drives PSEPIC. Initially, SEPIC-I is switched on to receive the load current when the load is exceeded. SEPIC-II is then switched on to share the load, with a 10% delay of the switching period to avoid EMI and overloading.

A. Selection of Component Ratings

The design of various components in the circuit is shown in Fig. 1 and is explained in this section. A coupled inductor involves a simultaneous parallel energy pathway and works as an energy storage element for ripple-current steering. Fig. 5. shows the coupled inductor. The voltage across the inductor L_1 is considered as V_1, and the voltage across L_2 is considered as V_2. The current that passes through the inductors L_1 and L_2 are

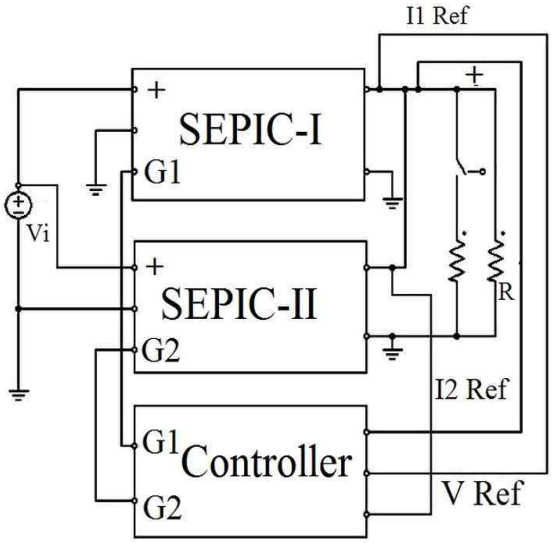


Fig. 4. Block diagram of the proposed PSEPIC.

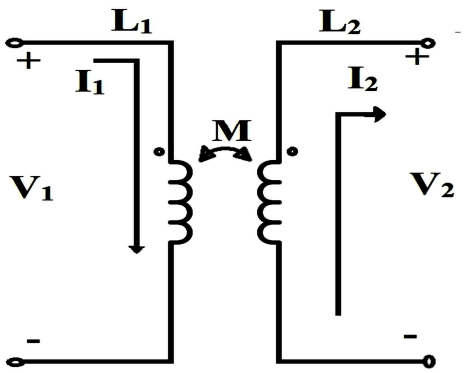


Fig. 5. Coupled inductor.

considered as i_1 and i_2 respectively. Mutual inductance also has a relationship with the coupling coefficient, which is between 1 and 0, as given in Eq. (1).

$$M = k\sqrt{L_1 L_2} \tag{1}$$

where M is the mutual inductance, k is the coupling coefficient, and L_1 and L_2 are self-inductance.

$$V_1 = L_1 \frac{di_1}{dt} + M \frac{di_2}{dt} \tag{2}$$

$$V_2 = L_2 \frac{di_2}{dt} + M \frac{di_1}{dt} \tag{3}$$

The proposed PSEPIC works similarly with separate inductors and coupled inductors. For the circuit to operate properly, a volt-microsecond balance must be maintained across each magnetic core. In other words, the products of each inductor voltage and time must be equal in magnitude and opposite in polarity during the MOSFET ON and OFF times for the two separate inductors. However, the coupled inductor can manage without such problems. The capacitor voltage for separate inductors is also charged to the input voltage, which can be algebraically shown. A coupled inductor is preferred for the proposed PSEPIC because of its reduced component count,

TABLE I
COMPARISON OF COUPLED AND SINGLE INDUCTOR-BASED PSEPIC

Parameters	Conventional	Proposed
Foot print	More	Less
Inductor value	Full	Half
Ripple current	Separate	Sharing
Voltage stress	High	Low

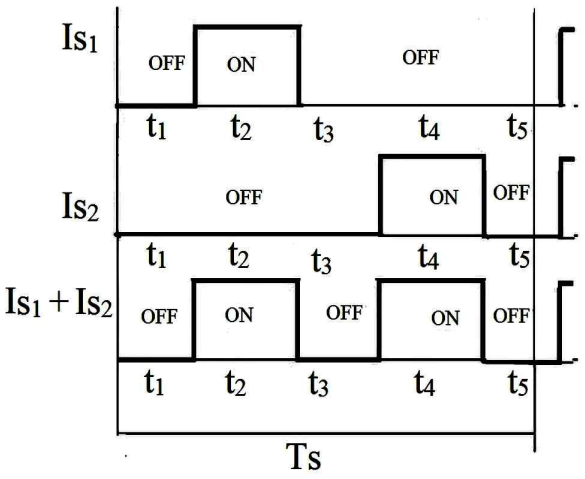


Fig. 6. Duty cycle.

better integration, and less inductance requirement compared with using two single inductors. A coupled inductor PSEPIC can benefit from leakage inductance, which reduces current losses. The selected coupled inductors have a 1:1 turn ratio for volt-microsecond balance.

The developed PSEPIC converter with a coupled inductor has many advantages compared with a separate single inductor, as seen in Table I.

B. Duty Cycle Consideration

The duty cycle of the proposed PSEPIC is shown in Fig. 6. In the figure, Is_1 and Is_2 represent the current that passes through the switches SEPIC-I and SEPIC-II respectively. The efficiency of the SEPIC should be maximized. The proposed PSEPIC operates on CCM, and the duty cycle of switch D is given in Eq. (4).

$$D = \frac{V_o + V_D}{V_i + V_o + V_D} \tag{4}$$

$$\frac{D}{1-D} = \frac{\dfrac{V_o + V_D}{V_i + V_o + V_D}}{1 - \dfrac{V_o + V_D}{V_i + V_o + V_D}} \tag{5}$$

where V_D is the forward voltage drop of the Schottky diode. In PSEPIC, the ratio between input current i_i and output current i_o is given in Eq. (6):

$$\frac{D}{1-D} = \frac{V_o + V_D}{V_i} = \frac{i_i}{i_o} \tag{6}$$

C. Inductor Ripple Current

One of the first steps in designing any PWM-switching regulator is to determine the inductor ripple current Δi_L, which can be obtained using Eq. (7). Normally, 20% to 40% of the input current is accepted as the ripple current. In this study, the ripple current is 30%.

$$\Delta i_L = 30\% \times \frac{i_1'}{\eta} \tag{7}$$

where η is the efficiency of the PSEPIC, which is 90%, and i_1' is the accurate estimate of the input current. In ideal cases, a tightly coupled inductor that has single cores with the same number of windings for each conductor, and the mutual inductance forces the ripple current to split equally between two coupled inductors. The design of the inductor value is determined to be half of what will be required for two separate inductors, and is given as Eq. (8):

$$L_{1a} = L_{1b} = \frac{1}{2} \times \frac{V_{i(\min)} \times D_{(\max)}}{\Delta i_L \times f_{s(\min)}} \tag{8}$$

where L_{1a} and L_{1b} are the inductance of the coupled inductors, $V_{i(\min)}$ is the minimum input voltage, $D_{(\max)}$ is the maximum duty cycle, and f_s is the switching frequency. When load changes are considered, the saturation current rating of the tightly coupled inductor must be 20% higher than the steady-state peak current in the input of inductor $i_{L1a(peak)}$ and is calculated as in Eq. (9):

$$i_{L_{1a(peak)}} = i_1' + \frac{\Delta i_L}{2} = i_1 \times \left\{1 + \frac{30\%}{2}\right\} \tag{9}$$

The capacitor C_2 must be able to provide the load current and have sufficient capacitance with a low Equivalent Series Resistance (ESR). C_2 is selected based on Eq. (10):

$$\Delta V_{(c)ripple} \le \frac{i_o \times D_{(\max)}}{C_2 \times f_{s(\min)}} + ESR \times \left[i_{L1a(peak)} + i_{L2a(peak)}\right] \tag{10}$$

where $\Delta V_{(c)ripple}$ is the ripple voltage of the capacitor C_2. Furthermore, ESR can be ignored. Low ESR capacitors are used, and the value of capacitor C_2 can be calculated using Eq. (11).

$$C_2 \ge \frac{i_o \times D_{(\max)}}{\Delta V_{(C)ripple} \times f_{s(\min)}} \tag{11}$$

The output capacitor must have a Root Mean Square (RMS) current rating that is more than the output RMS current, which is given in Eq. (12).

$$i_{C_{2(RMS)}} = i_o \times \sqrt{\frac{D_{(\max)}}{1 - D_{(\max)}}} \tag{12}$$

The coupling capacitor C_1 obtains a large RMS current that is related to the output power and is given in Eq. (13).

$$i_{C_{1(RMS)}} = i_i \times \sqrt{\frac{1 - D_{(\max)}}{D_{(\max)}}} \tag{13}$$

The maximum voltage across coupling capacitor C_1 is given

TABLE II
PARAMETERS OF PSEPIC

Parameter	Symbol	Specification
Input voltage	V_i	15–24 V DC
Output Voltage	V_o	18.5 V
Inductor	L_{1a},L_{1b}	44 μH
Capacitor	C_1	47 μF
Capacitor	C_2	630 μF
Switching Frequency	f_s	100 KHz
Load	R	6 Ω
Duty cycle	D	0.3 to 0.9

in Eq. (14):

$$V_{S_{1(\max)}} - V_{L_{1b(\max)}} = V_i + V_o - V_o = V_i \tag{14}$$

The ripple voltage across C_1 can be calculated using Eq. (15):

$$\Delta V_{C_1} = \frac{i_o \times D_{(\max)}}{C_1 \times f_s} \tag{15}$$

D. MOSFET Selection

MOSFET (S_1) is the main active component and must be selected in such a way that it can handle the peak voltage and the current with low loss in the circuit. The peak current rating of switch S_1 is given in Eq. (16):

$$i_{S_{1(peak)}} = i_{L1a(peak)} + i_{L1b(peak)} = i_1' + i_o + \Delta i_L \tag{16}$$

Table II shows the parameters of the designed PSEPIC.

IV. SIMULATION

The purpose of this section is to discuss the simulation of the PSEPIC with a PI controller. A PI controller with a Kp setting of 0.1205 and a Ti of 0.00016 s is obtained using the Ziegler–Nichols tuning technique. These results are used for the design of the PSEPIC feedback controller. The developed circuit performance is verified with different conditions, such as startup, line variation, load variation, and steady-state condition.

Simulations are performed using the listed parameters, as shown in Table II. The simulated results of the output voltage and the current without a PI controller for each module are listed in Tables III and IV respectively. The voltage regulation and current distribution have some equalities. Fig. 7. shows the simulink diagram of PSEPIC with separate inductors, and Fig. 8 shows the coupled inductor-based PSEPIC.

The performance of the proposed PSEPIC with a PI controller that was obtained through simulation is analyzed and verified as follows.

A. Startup Transient

Fig. 9 shows the startup behavior of the PSEPIC output voltage for different input voltages viz 15, 18.5, and 24 V, in which the reference value of the input voltage is set to 18.5 V and the load resistance is 6 Ω. The output voltage has no overshoot, and the settling time is 0.25 s. Fig. 10. shows the output current of PSEPIC for the same set of reference output voltages and load resistance values.

TABLE III
SIMULATED RESULT OF OUTPUT VOLTAGE OF PSEPIC WITHOUT CONTROLLER

Change on Vi (V) for Load R = 6 Ω	Vi (V)	Vo_1 (V)	Vo_2 (V)	Vo (V)	I_1 (A)	I_2 (A)	Io (A)
	15	16.5	16.5	16.5	1.38	1.36	2.75
	18	18.9	18.9	18.9	1.78	1.38	3.16
	24	25.4	25.4	25.4	2.21	2.08	4.29

TABLE IV
SIMULATED RESULT OF OUTPUT CURRENT OF PSEPIC WITHOUT CONTROLLER

Change on R for Vi (15V)	R	Vo_1 (V)	Vo_2 (V)	Vo (V)	I_1 (A)	I_2 (A)	Io (A)
	4	17.4	17.2	17.4	2.37	1.97	4.3
	6	18.9	18.9	18.9	1.78	1.38	3.16
	8	23.4	23.4	23.4	3.05	2.82	5.85

Fig. 11 shows the startup response of the PSEPIC output voltage for the different load resistances of 4, 6, and 8 Ω, and the reference output voltage of 18.5 V. Irrespective of the variation of load resistance, the output voltages remain constant at 18.5 V. The input voltage is kept at 15 V during the above simulation. Fig. 12 shows the PSEPIC output current for the different load resistances of 4, 6, and 8 Ω using a PI controller. The output voltage is constant at 18.5 V for all three loads, and the currents are 4.625, 3.08, and 2.312 A, respectively.

B. Step Change in Load

Fig. 13 shows the response of the PSEPIC output voltage when the load is forced to step change from 6 Ω to 4 Ω (-33% load variation) at time t = 0.4 s. The output voltage of PSEPIC has a small overshoot of 1.2 V with a settling time of 0.05 s. Fig. 14 shows that the response of the PSEPIC output voltage for a load step changes from 6 Ω to 8 Ω (+33% load variation) at time t = 0.4 s. The output voltage of the PSEPIC also has the maximum over shoot of 1.5 V with the settling time of 0.05 s. Figs. 13 and 14 show that the simulated output of the designed PSEPIC exhibits good performance on load disturbances.

C. Steady-State Condition

Figs. 15 and 16 show the steady-state output voltage and output current of the PSEPIC when Vi = 15 V and load resistance R = 6 Ω. Steady-state variation of the voltage is 0.015 V, which is a good constant voltage requirement. The output voltage ripple is low at approximately 0.015 V (0.083%), and the peak-to-peak ripple current is 0.002 A.

In summary, Figs. 9–16 show that the PSEPIC results have good performance.

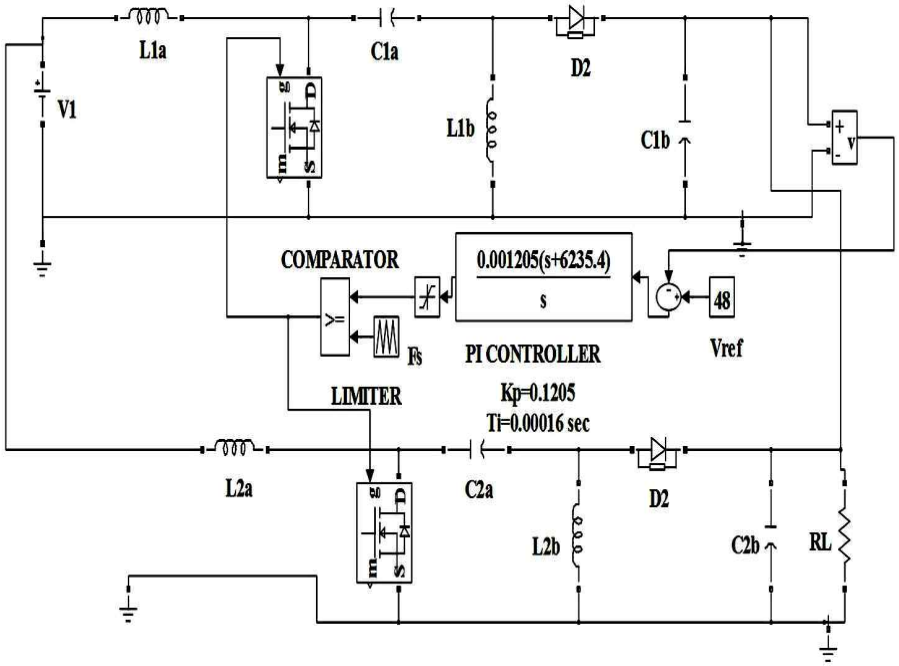


Fig. 7. Simulink diagram with separate inductor PSEPIC.

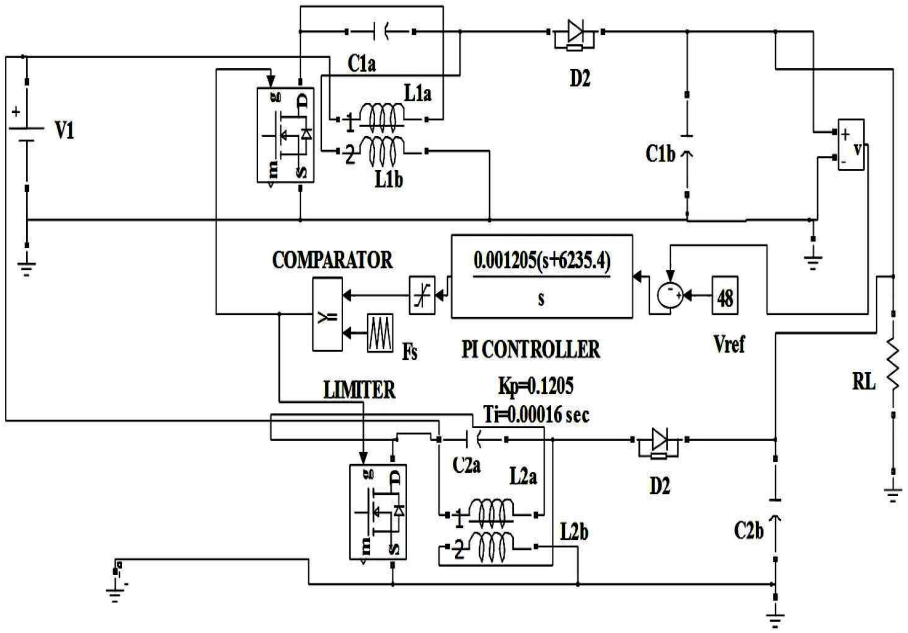


Fig. 8. Simulink diagram of the Proposed PSEPIC.

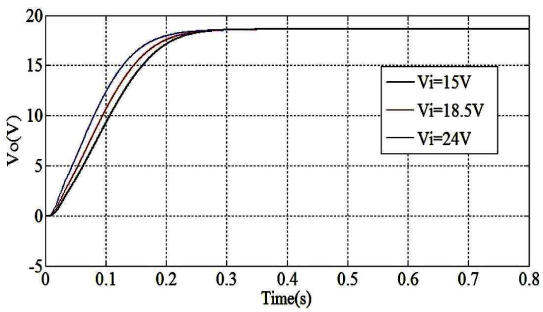


Fig. 9. Response of the PSEPIC output voltage at various input voltages at startup.

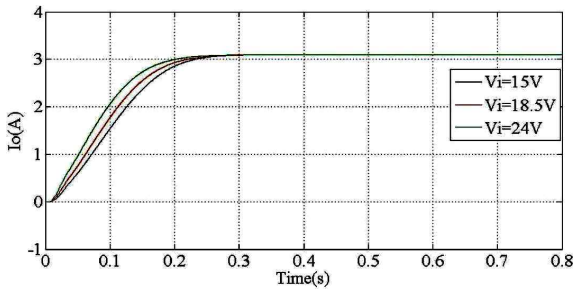


Fig. 10. Response of the PSEPIC output current at various input voltages at startup.

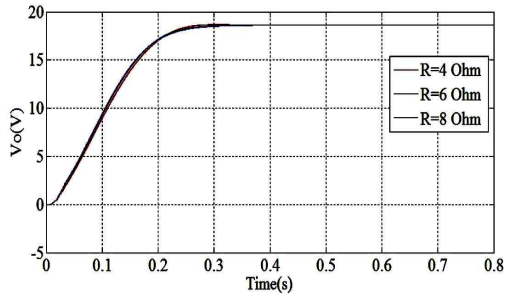


Fig. 11. Response of the PSEPIC output voltage during startup for various load resistances.

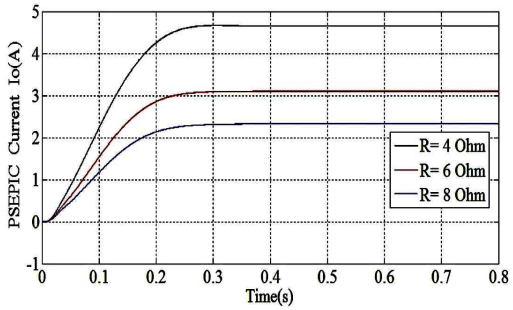


Fig. 12. Response of the PSEPIC output voltage during startup for various load resistances.

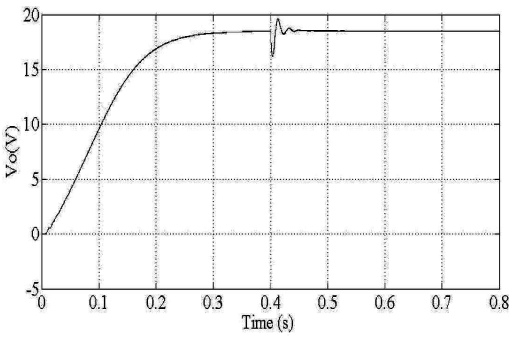


Fig. 13. Response of output voltage when the load changes from 6 Ω to 4 Ω.

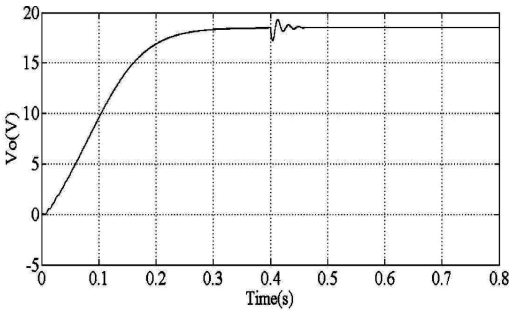


Fig. 14. Response of output voltage when load changes from 6 Ω to 8 Ω.

V. Experimental Results

The purpose of this section is to discuss the experimental results of the proposed PSEPIC with a PI controller. The validation is done with different conditions viz line variation, load variation, and steady-state operation.

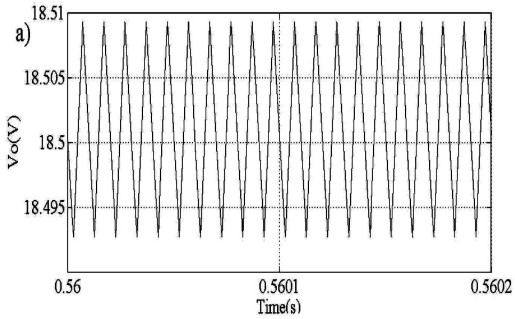


Fig. 15. Response of PSEPIC output voltage at the steady-state condition.

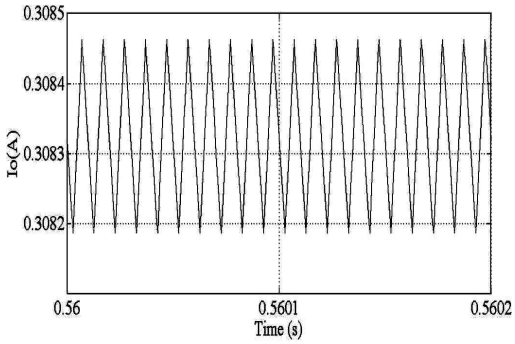


Fig. 16. Response of PSEPIC output voltage at the steady-state condition.

The experimental setup of the PSEPIC with coupled inductors is developed with the same specifications as the simulation. This setup is shown in Fig. 17. The parameters of the main circuit and components of the control circuits are given in Tables V and VI. A photograph of the PSEPIC experimental setup is shown in Fig. 18.

A. Operation of the Circuit

The purpose of PSEPIC is to share the load and consider the maximum duty cycle. Generally, duty cycle D with time Ts is accepted as t_1 and t_2, as shown Fig. 6. The proposed PSEPIC shares the 30% ON in SEPIC-I and 30% ON in SEPIC-II. Hence, the maximum tapping of energy from the supply is derived.

Only a simple PI controller is used in this work. The PSEPIC gate is given separate pulses with a small time delay using IC KA3525, which operates and controls the PSEPIC with the individual gate voltage from pin numbers 11 and 14. A reference voltage of 18.5 V is given to pin 1, and a fraction of the PSEPIC output voltage is given to KA3525. According to the error between the above two voltages, the gate pulse width will be adjusted to maintain the output voltage at a constant value. When the output voltage of PSEPIC either exceeds 24 V or goes below 15 V, the comparator LM324 sends a shutdown signal to pin 10 of KA3525. Thus, the gate pulses are cut off.

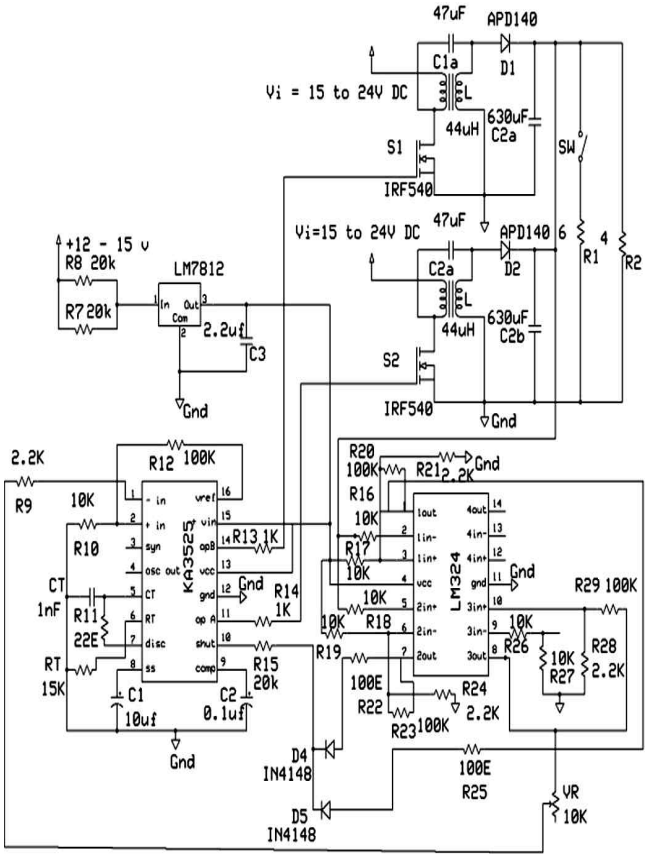


Fig. 17. Experimental circuit of PSEPIC.

TABLE V
PARAMETERS OF MAIN CIRCUIT

Symbol	Component	Specification
C1a,C2a	Capacitor	47 µF
C1b,C2b	Capacitor	630 µF
L	Inductors	44 µH
S1 & S2	MOSFET	IRF540
D1,D2	Schottky	APD140

TABLE VI
LIST OF CONTROL CIRCUIT COMPONENTS

Symbol	Components	Specification
C1	Capacitor	10 µF/40 V
CT	Capacitor	1 nF/40 V
C2	Capacitor	0.1 uF/63 V
VR	Variable Resistor	10 K
IC1	IC KA3525	12 V
D4,D5	Diode	IN4148
R7,R8,	Resistor	20 K
R9,R21,R24,R28	Resistor	2.2 K
R11	Resistor	22 Ω
RT	Resistor	15 K
R12,R20,R22, R23,R25,R29	Resistor	100 K
R10,R16, R17,R18, R19,R26,R27,	Resistor	10 K
R13,R14	Resistor	1 K

Fig. 18. Experimental setup of PSEPIC.

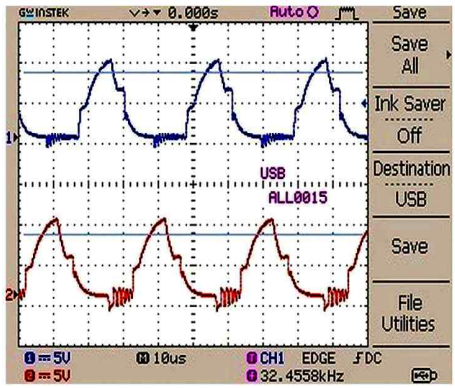


Fig. 19. Response of PSEPIC pulse.

Using this simple controller, the duty cycle of the gate pulse is varied to regulate the output voltages, which improves the dynamic performance of PSEPIC. The performance of the PSEPIC obtained from the experiment is analyzed in the following section.

B. Line Variation

Fig. 20 shows the experimental response of the output voltage of the PSEPIC when there is an input voltage change from 15 V to 18.5 V at time t = 0.4 s. The reference value of the output voltage is set to 18.5 V. The load resistance value is kept at 6 Ω. The experimental response demonstrates that the average output voltage of the PSEPIC has a maximum undershoot of 1.96 V and a settling time of 0.05 s.

Fig. 21 shows the experimental response of the average PSEPIC output voltage when an input voltage step changes from 24 V to 18.5 V at time 0.4 s. The experimental response demonstrates that the output voltage of the PSEPIC has a maximum undershoot of 1.96 V and a settling time of 0.05 s.

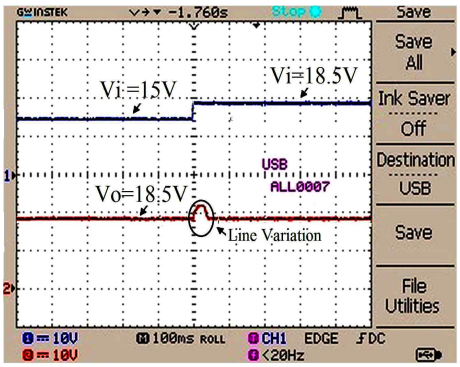


Fig. 20. Response of output voltage on line variation when the input voltage suddenly changes from 15 V to 18.5 V.

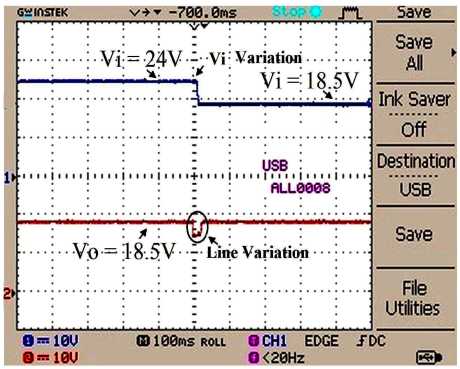


Fig. 21. Response of output voltage on line variation when input voltage suddenly changes from 24 V to 18.5 V.

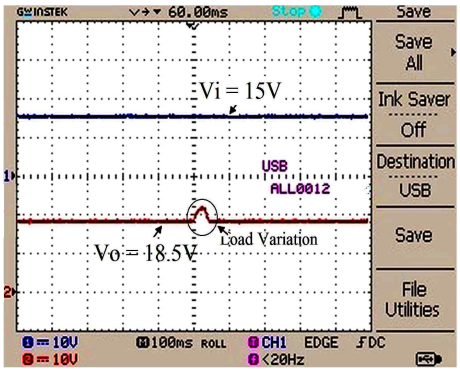


Fig. 22. Response of output voltage on load variation when the load suddenly changes from 6 Ω to 4 Ω.

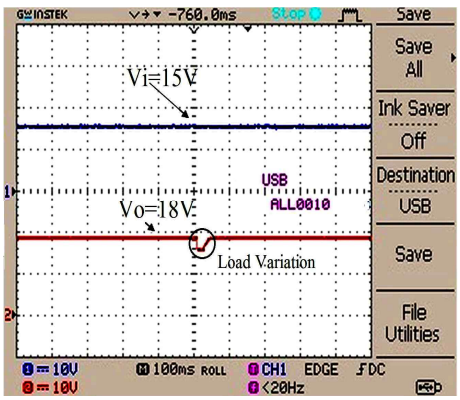


Fig. 23. Response of output voltage on load variation when the load suddenly changes from 6 Ω to 8 Ω.

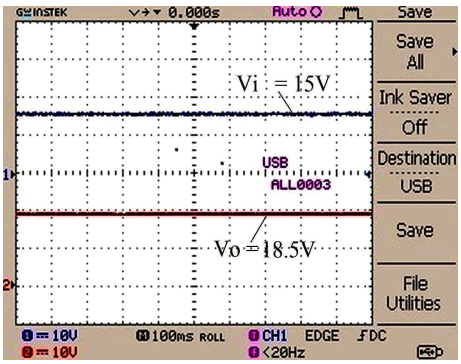


Fig. 24. Response of PSEPIC on output voltage for the input voltage of 15 V.

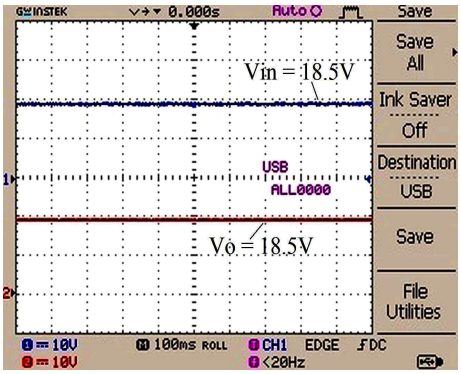


Fig. 25. Response of PSEPIC on output voltage for the input voltage of 18.5 V.

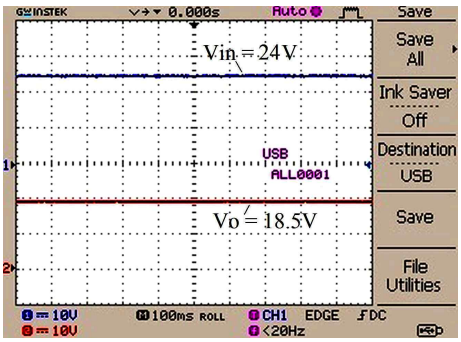


Fig. 26. Response of PSEPIC on output voltage for the input voltage of 24 V.

C. Load Variation

Fig. 22 shows the response of PSEPIC output voltage when the load is forced to step change from 6 Ω to 4 Ω (-33% load variation) at time t = 0.4 s. The output voltage of PSEPIC has a small overshoot of 2 V with a settling time of 0.06 s. Fig. 23 shows the response of the PSEPIC output voltage for a load that step changes from 6 Ω to 8 Ω (+33% load variation) at time t = 0.4 s. Furthermore, the output voltage of the PSEPIC has a maximum overshoot of 3 V with a settling time of 0.06 s. Figs. 22 and 23 show that the experimental output of the designed PSEPIC exhibits good performance on load disturbances.

D. Steady-State Region

TABLE VII
EXPERIMENTAL AND SIMULATED VALUES OF CHANGE IN INPUT VOLTAGE AND CURRENT

Change in line Voltage from 15 V to 24V	Voltage (V)					
	Experimental			Simulation		
	Vo_1	Vo_2	Vo	Vo_1	Vo_2	Vo
	18.5	18.5	18.5	18.5	18.51	18.51
Change in load	Current (A)					
	Experimental			Simulation		
	I1	I2	Io	I1	I2	Io
4 Ω	2.31	2.35	4.66	2.3	2.3	4.6
6 Ω	1.49	1.49	2.98	1.5	1.5	3
8 Ω	1.12	1.12	2.24	1.15	1.15	2.3

Figs. 24, 25, and 26 show the experimental output voltage of the PSEPIC in the steady-state region for Vi = 15 V, 18.5 V, and 24 V, respectively. The reference value of Vo is kept at 18.5 V. The output voltage is kept constant for all three inputs.

Table VI shows the comparison of simulation and experimental results when the input voltage is at 15, 18.5, and 24 V. The PSEPIC circuit is stable and produces 18.5 V. In the simulation and the experimental setup, the output voltage is kept constant at 18.5 V. Thus, the results are close to the experimental and simulated values.

In cases of various loads, the PSEPIC response is to maintain its output voltage and share the load current. In Table VII, the output currents and voltages of the simulation and experimental setup have the nearest values.

In summary, Figs. 19-26 indicate that the experimental results of the PSEPIC agree with the simulated results with a tolerance of ±2%. The proposed coupled inductor with simple PI controller also performs well in all operational situations of the PSEPIC. The novelty of the circuit is its use of a coupled inductor with a simple PI controller. The PI controller provides the gate pulse for both the switches in PSEPIC with time delay. Another advantage is the ON and OFF time. Therefore, the proposed PSEPIC is considered to share only when the load is exceeded by more than half; otherwise, one SEPIC will operate. This characteristic is the uniqueness of this novel technique.

VI. CONCLUSION

Considering its advantages of load sharing, maintaining constant voltage, reducing the footprint of components, component counts, and stress on components, the parallel-connected SEPIC converter for low-voltage applications is developed. A coupled inductor is used for this PSEPIC because single and separate inductors utilize considerable ripple currents. As a result, this coupled inductor utilizes only half of the ripple current that two separate inductors use. PSEPIC is verified under various conditions, such as startup transient, load variation, line variation, and steady-state condition to maintain a constant voltage and load sharing. An analog control circuit is designed to generate PWM signals to fulfill the closed-loop control function. A stable output voltage is kept constant at 18.5 V with a common input voltage. The proposed PSEPIC shares the load current according to the load conditions. The experimental setup is developed for an 18.5 V 60 W PSEPIC, and the results are verified. The results show evidence that the proposed PSEPIC provides good response for line variation and shares the load current. This PSEPIC also withstands sudden changes in load.

REFERENCES

[1] E. Babaei and M. E. Seyed Mahmoodieh, "Calculation of output voltage ripple and design considerations of SEPIC converter," *IEEE Trans. Ind. Electron.,* Vol. 61, No.3, pp. 1213-1222, Mar. 2014.

[2] A. Jaafar, A. Alawieh, R. Ortega, E. Godoy, and P. Lefranc, "PI stabilization of power converters with partial state measurements," *IEEE Trans.Contr. Syst. Technol.,* Vol. 21, No. 2, pp. 560-568, Mar. 2013.

[3] A. El Khateb, N. A Rahim, J. Selvaraj, and M. N. Uddin, "Maximum power point tracking of single-ended primary-inductor converter employing a novel optimisation technique for proportional-integral-derivative controller," *IET Power Electron.*, Vol. 6, No. 6, pp. 1111-1121, Jul. 2013.

[4] S. Y. Yu and A. Kwasinski, "Analysis of soft-switching isolated time-sharing multiple-input converters for DC distribution systems," *IEEE Trans. Power Electron.*, Vol. 28, No. 4, pp. 1783-1794, Apr. 2013.

[5] G. Di Capua and N. Femia, "A critical investigation of coupled inductors SEPIC design issues," *IEEE Trans. Power Electron.*, Vol. 61, No.6, pp. 2724-2734, Jun. 2014.

[6] K. M. Kazimierczuk, *Pulse-Width MODULATED DC-DC Power Converters*, John Wiley & Sons, Chap. 1, 2008.

[7] H.-L. Do, "Soft-switching SEPIC converter with ripple-free input current," *IEEE Trans. Power Electron.,* Vol. 27, No. 6, pp 2879-2887, Jun. 2012.

[8] H.-Y. Lee, T.-J. Liang, J.-F. Chen, and K.-H. Chen, "Design and implementation of a bidirectional SEPIC-Zeta DC-DC Converter," in *Proc. IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 101-104, 2014.

[9] M. R. Cosetin, P. C. V. Luz, E. A. Bitencourt, M. F. da Silva, F. Bisogno, J. M. Alonso, and R. N. do Prado, "Off-line single-stage SEPIC-Buck converter for dimmable LED lighting with reduced storage capacitor," in *Proc. 15th European Conference on Power Electronics and Applications (EPE)*, pp. 1-10, 2013.

[10] M.-S. Song, Y.-D. Son, and K.-H. Lee, "A non-isolated bidirectional soft-switching SEPIC/ZETA converter with reduced ripple currents," *Journal of Power Electronics*, Vol. 14, No. 4. pp. 649-660, Jul. 2014.

[11] T.-F. Wu, Y.-S. Lai, J.-C. Hung, and Y.-M. Chen, "Boost converter with coupled inductors and buck boost type of active clamp," *IEEE Trans. Ind. Electron.*, Vol. 55, No. 1, pp. 154-162, Jan. 2008.

[12] L.-S. Yang, T.-J. Liang, H.-C. Lee, and J.-F. Chen, "Novel high step-up DC-DC converter with coupled-inductor and voltage-doubler circuits," *IEEE Trans. Ind. Electron.,* Vol. 58, No. 9, pp. 4196-4206, Aug. 2011.

[13] J. Falin, "Designing DC/DC converters based on SEPIC topology," *Texas Instruments Analog Application Journal* pp. 18-23, 2008.

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