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An FPGA-Based Modified Adaptive PID Controller for DC/DC Buck Converters

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Abstract

On the basis of the conventional PID control algorithm, a modified adaptive PID (MA-PID) control algorithm is presented to improve the steady-state and dynamic performance of closed-loop systems. The proposed method has a straightforward structure without excessively increasing the complexity and cost. It can adaptively adjust the values of the control parameters (K_p, K_i and K_d) by following a new control law. Simulation results show that the line transient response of the MA-PID is better than that of the adaptive digital PID because the differential coefficient K_d is introduced to changes. In addition, experimental results based on a FPGA indicate that the MA-PID control algorithm reduces the recovery time by 62.5% in response to a 1V line transient, 50% in response to a 500mA load transient, and 23.6% in response to a steady-state deviation, when compared with the conventional PID control algorithm.

Key words: Dynamic performance, FPGA, MA-PID, Steady-state deviation

I. INTRODUCTION

Digital control for switch-mode power converters (SMPCs) has gained more popularity in a wide range of applications due to its many advantages when compared to analog control, including design flexibility, lower sensitivity, elimination of passive tuning components, programmability, etc.[1]-[3]. For digital SMPCs, the two most important types of performance are the dynamic performance and the static performance. With the rapid development of electronic devices and large-scale digital integrated circuits, power converters are required to have a smaller area and a faster dynamic response.

Many of the classical control schemes for SMPCs have some inherent limitations in the design of the controller that can limit the stability margins, robustness and dynamic performance of a system. However, conventional PID controllers are commonly used in SMPCs due to their simplicity, intuition, and ease of implementation. Recent research trends in the PID control area have been well summarized in many studies. In [4], a Genetic algorithm is applied to discover the supreme values for the PID controller's parameters within a short time period. This algorithm has stability robustness, efficiency and optimum dynamic response in a very short time period. An online compensator auto-tuning method which tunes the parameters of the compensator has been proposed to achieve optimized dynamic performance in [5]-[6]. In addition, a fast PID method has been presented in [7]-[9]. In this method, the PID control is divided into two parts, the P control and the I-D control. An 8 bit A-D Converter is used for the P control and an 11 bit A-D Converter is used for the I-D control. However, these methods require relatively complex algorithmic steps to tune the control parameters, or extra software and hardware conditions [10]-[15]. In addition, they may introduce undesirable oscillations in the output. In [11], a novel trajectory prediction control algorithm has been presented. It uses current detection and voltage detection, requiring more than two A/D converters.

In order to overcome the aforementioned limitations, an adaptive digital PID (AD-PID) controller is presented in [15]. This controller reduces the output voltage deviation and settling time by changing the values of the parameters (K_p and K_i). One of the advantages of this method is that it is easy to implement. Nevertheless, this algorithm still has some risks in terms of dynamic performance and static performance. Based on this method, this paper presents a modified adaptive PID (MA-PID) control algorithm. This algorithm tunes the parameters (K_p, K_i and K_d) using predetermined rules, such as

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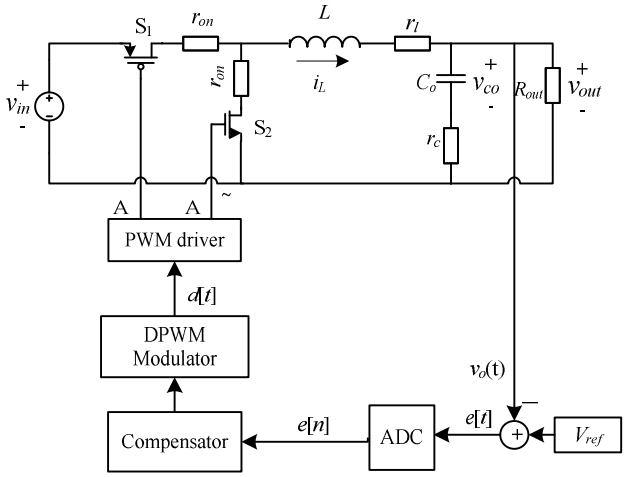


Fig. 1. Block diagram of a power converter with digital controller.

phase margin and gain requirements. The modified algorithm can further improve the dynamic performance (e.g. line transient response). However, it can also effectively eliminate the unstable facts that exit in the literature [15].

The following section introduces the modified adaptive PID control method and algorithm. In addition, it gives a description of the difference between the conventional and MA-PID controls. Section III describes the simulation process of a DC-DC buck converter using MATLAB software, and it presents simulation results. Section IV presents the process of FPGA implementation and an experimental comparison between the conventional PID and MA-PID controllers. Finally, some conclusion are given in section V.

II. MA-PID CONTROL TECHNIQUE

A. Conventional PID Control Law

An A/D converter, a compensator and a DPWM constitute a feedback loop, with which the power stage forms a closed-loop feedback system, as shown in Fig. 1. The purpose of the closed-loop system is primarily to adjust the output voltage V_{out} to match a precise and stable voltage reference V_{ref} over a range of load currents, input voltage values and temperature variations [1].

Based on [16] and [17], a precise mathematical model of the converter can be established under non-ideal conditions. Using a small signal approximation, the open-loop gain function of the original ring without a compensating network can be written as equation (1).

Where r_{on}, r_l and r_C are the switch-tube on-resistance, the equivalent series resistance of the inductance, and the equivalent series resistance of the capacitance, respectively. $G_m(s) = 1/U_m$, and U_m is the amplitude of the saw-tooth wave.

In [18], the essence of the compensation is to join the calibration device with a suitable frequency characteristic, and to make the shape of the frequency characteristic of the open-loop system into a desire shape, as follows:

- The low-frequency gain is sufficiently large to enhance the steady-state accuracy of the system.
- The slope of the logarithmic amplitude-frequency characteristic in the middle-frequency stage is always -20dB/dec and it occupies a sufficiently wide frequency band, to guarantee that the system has a proper phase margin.
- The higher the cross frequency of the loop gain, the faster the transient response of system will be.

According to the above principles, the transfer function of a digital PID compensator via the s-z transformation can be calculated as:

$$G_{PID}(z) = \frac{U(z)}{E(z)} = K_P + K_I/(1-Z^{-1}) + K_D(1-Z^{-1}) \quad (2)$$

Where K_p, K_i and K_d are the constant coefficients of the proportional gain, integral term, and derivative term, respectively.

B. Modified Adaptive PID (MA-PID) Control Law

In general, the higher the loop bandwidths which can still guarantee the stability of the system, the better the dynamic performance of the closed-loop system. The theoretical bandwidth have to be under half of the switching frequency. However, the bandwidth of the loop is not more than one-tenth of the switching frequency in practical designs [20]. In the steady state, it may lead to unsteadiness if the bandwidth of a system is more than that limitation. Nevertheless, the dynamic performance can be improved by increasing the proper bandwidth in the transient state, which can be obtained by altering the values of K_p, K_i and K_d.

Fig. 2 shows the variation tendencies of the bode-plots for different values of K_p, K_i and K_d. From Fig. 2(a), it can be seen that as K_p increases, the bandwidth of the closed-loop system becomes higher and the phase margin decreases. From Fig. 2(b), it can be observed that the gain increases and the phase margin decreases when K_i increases. From Fig. 2(c), it can be seen that the cross-frequency of the system becomes higher and the phase margin increases as K_d increases. By comparing Fig. 2(a) and Fig. 2(c), it can be observed that these two parameters (K_p and K_d) are complementary and act as a mutual restraint. Hence, the three parameters should be properly adjusted in order to achieve the desired gain, bandwidth and phase margin requirements. Fig. 2(d) shows the variation tendencies of the bode-plots when K_p, K_i and K_d increase simultaneously. It can

$$G_O(s) = G_m(s)G_d(s) = \frac{1}{U_m}\frac{V_{out}}{D} * \frac{1+sCr_C}{1+s[\frac{L}{R_{out}+r_{on}+r_l} + \frac{CR_{out}(r_{on}+r_l)}{R_{out}+r_{on}+r_l} + Cr_C] + s^2LC\frac{R_{out}+r_C}{R_{out}+r_{on}+r_l}} \quad (1)$$

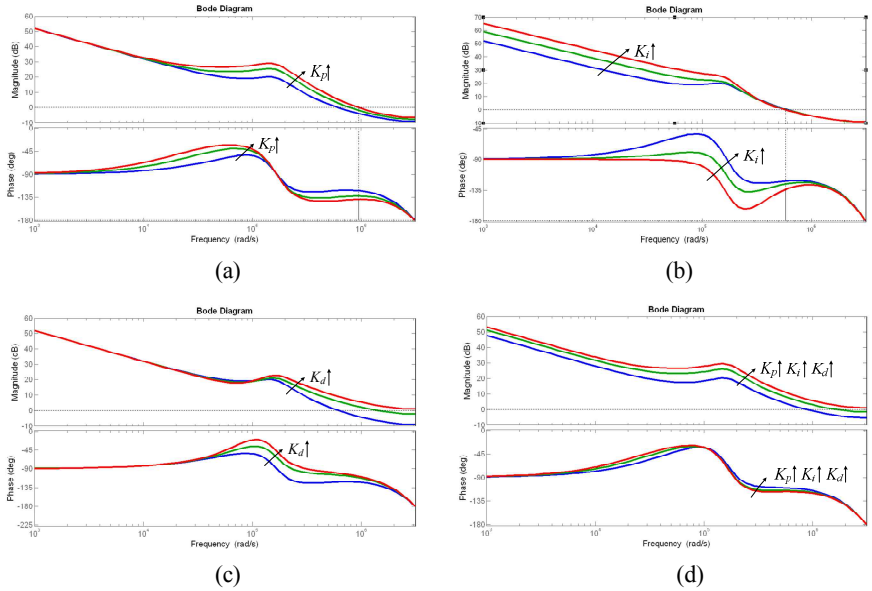


Fig. 2. The variation tendency of bode-plots for different values of K_p, K_i and K_d.(a) K_p increases. (b) K_i increases. (c) K_d increases. (d) K_p, K_i and K_d increase.

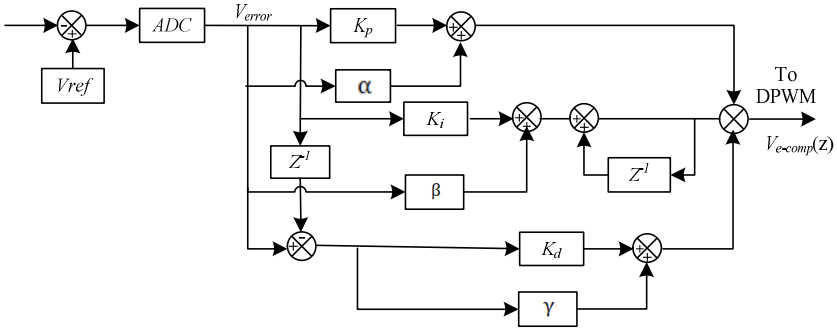


Fig. 3. Adaptively digital PID compensator realization diagram.

be seen from Fig. 2(d) that the compensated system has a proper phase margin, a sufficiently wide frequency band and a sufficiently large low-frequency gain to enhance the steady-state accuracy of the system and improve the transient response.

Therefore, a modified adaptive PID (MA-PID) compensator is proposed. It maintains a lower bandwidth in the steady state to make the system stable and has a higher bandwidth in the transient state, which can make the voltage deviation lower and the recovery time shorter. The transfer function of the MA-PID controller, as shown in Fig. 3, is given by:

$$G_{MA-PID}(z) = (K_p + \alpha) + (K_I + \beta)/(1 - Z^{-1}) + (K_D + \gamma) * (1 - Z^{-1}) \tag{3}$$

Where α, β and γ are adaptively varied following the error signal during the transient state and remain zero in the steady state.

It can be observed from Fig. 4 that the error signal (v_{error}) is divided into four states. These states are the rising transient state, falling transient state, transition state and steady state. Once the error signal (v_{error}) surpasses the threshold voltage V_{thr} as a result of a transient, the values of α, β and γ, whose values are zero during steady state, are changed abruptly to different values in order to increase the bandwidth and gain of the loop. The MA-PID control algorithm tracks v_{error} to detect its peak value ($V_{error\text{-}peak}$). Once the absolute value of the error signal changes, the values of α, β and γ are adjusted as given by (4), (5) and (6).

$$\alpha = \left\{ \begin{array}{ll} 0, & |v_{error}(k)| < |V_{thr}| \\ \left. \begin{array}{ll} \Delta K_p, & |v_{error}(k-1)| \le |v_{error}(k)| \\ \dfrac{|v_{error}(k)|}{|V_{error-peak}|} * \Delta K_p, & |v_{error}(k-1)| > |v_{error}(k)| \end{array} \right\} & v_{error}(k) * v_{error}(k-1) > 0 \\ \Delta K_{p2}, & v_{error}(k) * v_{error}(k-1) \le 0 \end{array} \right\} |v_{error}(k)| \ge |V_{thr}| \tag{4}$$

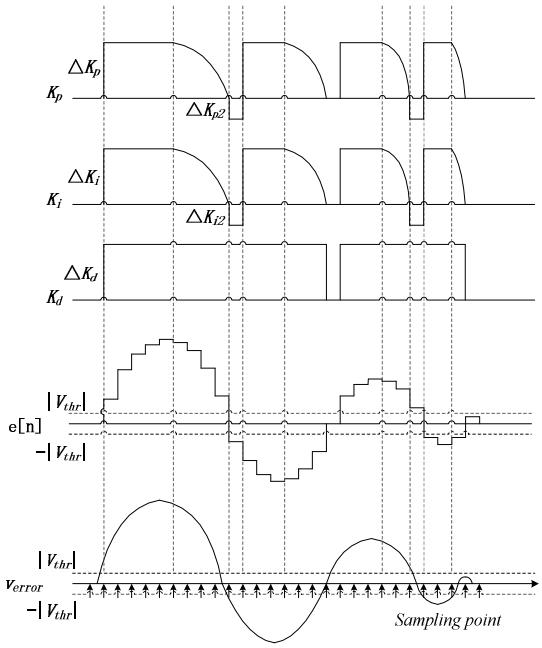


Fig. 4. Waveforms of MA-PID controller operation.

TABLE I

DESIGN SPECIFICATION FOR THE BUCK CONVERTER

Parameter	Value	Unit
Input voltage (V_{in})	5	V
Output voltage (V_{out})	1.8	V
Inductor (L)	4.7	μH
Inductor DCR (r_l)	200	mΩ
Output capacitor (C_o)	10	μF
Capacitor ESR (r_c)	100	mΩ
Switching frequency (f_s)	1	MHz

Fig. 5 shows a flowchart of the MA-PID algorithm. It can be seen that the value of $V_{error\text{-}peak}$ is different for different dynamic variations. As in [15], $V_{error\text{-}peak}$ is a variable but not fixed because the ratio of v_{error} and $V_{error\text{-}peak}$ is not equivalent to one for all transient conditions. In addition, the error signal is handled specially during the transition state to avoid the number of overshoot/undershoot. Thus, the MA-PID control strategy has the ability to adapt and work well under different dynamic types.

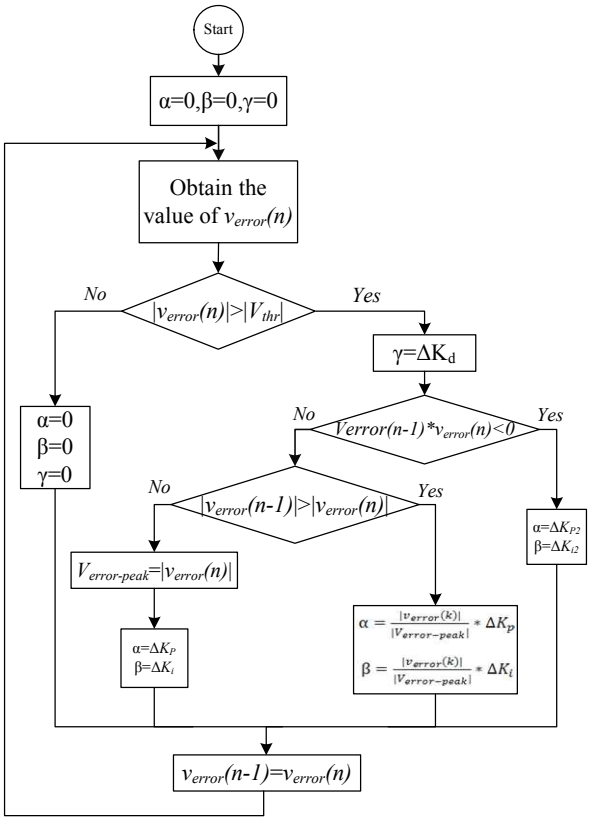


Fig. 5. The flowchart of MA-PID algorithm.

III. SIMULATION PROCESS OF THE DC-DC CONVERTER

A. The Selection of Parameters for the Digital Controller

Based on the MATLAB/Simulation platform, the universal model of a DC-DC buck converter can be built in the Simulink environment. The following parameters are taken into account for the model, as shown in Table I.

With the specified parameters, the open-loop gain function of the original ring based on equation (1) can be calculated. Hence, the open-loop gain function, which is translated into z-domain by the zero-order hold, can be given by:

$$G_O(z) = \frac{0.1469z - 0.04947}{z^2 - 1.87z + 0.8911} \tag{7}$$

Equation (7) can be used to design a PID controller. The cross-over frequency of the compensated loop should be

$$\beta = \begin{cases} 0, & |v_{error}(k)| < |V_{thr}| \\ \left.\begin{array}{ll} \Delta K_i, & |v_{error}(k-1)| \le |v_{error}(k)| \\ \dfrac{|v_{error}(k)|}{|V_{error-peak}|} * \Delta K_i, & |v_{error}(k-1)| > |v_{error}(k)| \end{array}\right\} & v_{error}(k) * v_{error}(k-1) > 0 \\ \Delta K_{i2}, & v_{error}(k) * v_{error}(k-1) \le 0 \end{cases} \left.\begin{array}{l}\\\\\\\end{array}\right\} |v_{error}(k)| \ge |V_{thr}| \tag{5}$$

$$\gamma = \begin{cases} 0, & |v_{error}(k)| < |V_{thr}| \\ \Delta K_d, & |v_{error}(k)| \ge |V_{thr}| \end{cases} \tag{6}$$

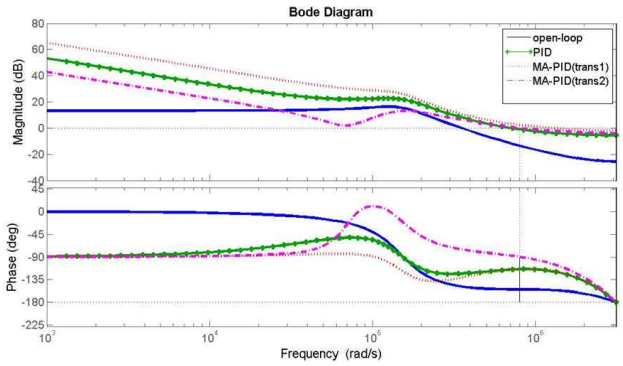


Fig. 6. Bode plot of converter with different control algorithms.

about one-tenth of the switching frequency, and the phase margin of the closed-loop system should be approximately 60 degrees [21]. The bode-plot-based technique and the root-locus technique are the common methods which can be operated using MATLAB's Single-Input Single-output (SISO) tool in a trial-and-error process. On the basis of equations (2) and (7), the compensated loop can be achieved by means of the above techniques whose cross-over frequency and phase margin meet the requirements. By adjustment and observation, the transfer function of the PID compensator is obtained as follows:

$$G_C(z) = 2 + \frac{0.1}{1 - Z^{-1}} + 4(1 - Z^{-1}) \tag{8}$$

Hence, the parameters of the PID controller are as follows: K_p=2, K_i=0.1, and K_d=4. Fig. 6 shows a bode plot of uncompensated and compensated closed-loop systems. It can be observed from Fig. 6 that the cross-over frequency of the compensated system is 114 kHz and that the phase margin is 65 degrees.

The parameters of the controller should be optimized to achieve a preferable dynamic response. Thus, the MA-PID control strategy is presented which smoothly transitions the PID parameters between steady state values and dynamic state values.

In order to obtain ΔK_p, ΔK_i and ΔK_d, the parameters during the steady state should be adjusted until the original bandwidth is increased to approximately one-fifth of the switching frequency and the low-frequency loop gain is increased by 10%~30%. Therefore, ΔK_p, ΔK_i and ΔK_d are the differences between the correspondingly newfound values and original values, respectively.

Based on the conventional PID parameters and the above design guidelines, the MA-PID parameters can be calculated. As a result, ΔK_p=0.7, ΔK_i=0.3, ΔK_d=2.3, ΔK_{p2}=-1.8, ΔK_{i2} =-0.02 and V_{thr} =60mV. When compared with the conventional PID controller, the MA-PID controller possesses an additional 9% bandwidth and a 23% increase in the low-frequency gain. Table II indicates the values of the parameters in the design example.

TABLE II

VALUES OF THE PARAMETERS IN THE DESIGN EXAMPLE

State	Para.	Values	GBW (kHz)	Low-freq. Gain (dB)	Phase margin
Steady	K_p	2	114	53.3	65°
	K_i	0.1			
	K_d	4			
Trans	ΔK_p	0.7	202	65.3	61°
	ΔK_i	0.3			
	ΔK_d	2.3			
	ΔK_{p2}	-1.8	120	42.8	88°
	ΔK_{i2}	-0.07			

TABLE III

CONVENTIONAL PID ALGORITHM DESCRIPTION

Step	Equation
	Initialization: v_{error}(k) = v_{error}(k-1) = v_{error}(k-2)=0, u(k) = u(k-1) =0
1	V_{oNow}=V_{ADC}
2	v_{error}(k-2) = v_{error}(k-1), v_{error}(k-1) = v_{error}(k), v_{error}(k) = V_{oNow}, Flag = 1
3	If Flag=1, then K_p=2, K_i=0.1, K_d=4
4	P=K_p*[v_{error}(k) - v_{error}(k-1)] I=K_i*v_{error}(k) D=K_d*[v_{error}(k)-2* v_{error}(k-1)+ v_{error}(k-2)]
5	u(k)=u(k-1)+P+I+D Flag=0
6	If Flag=0, repeat for step 1

B. The Establishment of a Simulation Model

Fig. 7 shows a MALAB/Simulink system model, which consists of an A/D converter, a compensator, a digital pulse width modulator and a power stage. The A/D converter is composed by delay, sample and hold, quantization and saturation blocks. Then, the DPWM module contains quantization, a limit block and a pulse width modulator which can generate the constant-frequency duty ratio signal to control the switch-tube. Buck converter block denotes the power stage which is realized by the state space averaging method, and can change the load resistor in order to simulate a transient response. The dynamic characteristics of the controller are reflected by applying a reduplicative step change in the load, which leads to a load current change.

As shown in Fig. 7, the compensator can be implemented by S-function code. S-function is a computer language to describe dynamic systems which can interact with the Simulink equation solver. As a rule, the algorithm is shown as:

$$\begin{aligned} u(k) = u(k-1) + K_P[e(k) - e(k-1)] + K_I e(k) \\ + K_D[e(k) - 2e(k-1) + e(k-2)] \end{aligned} \tag{9}$$

From equation (9), it can be seen that the controller just needs the current ($e(k)$), previous (i.e. $e(k-1)$, $e(k-2)$) samples of the error signal and previous values of the control output ($u(k-1)$). Table III shows the operational process of the conventional PID algorithm.

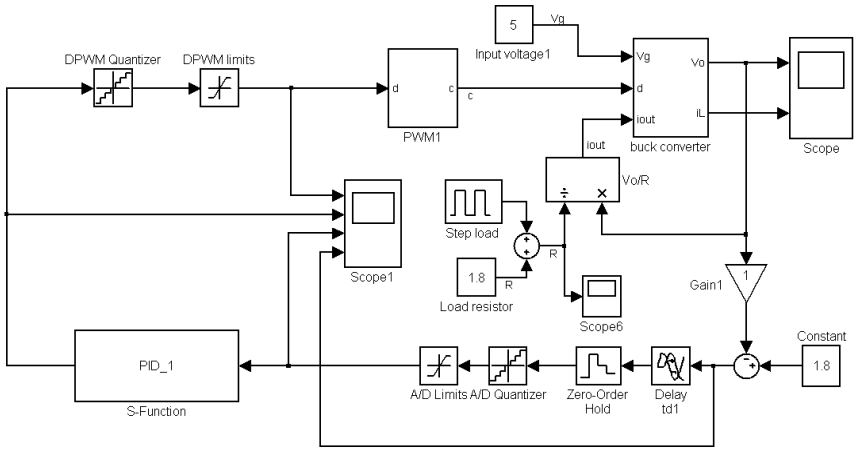
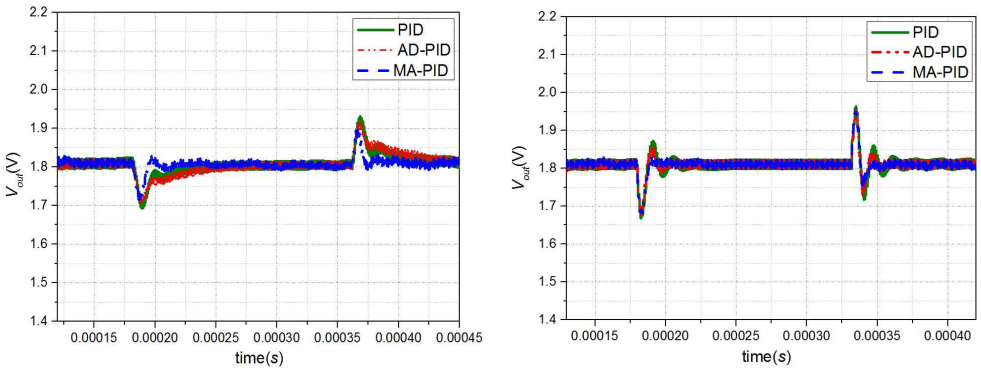
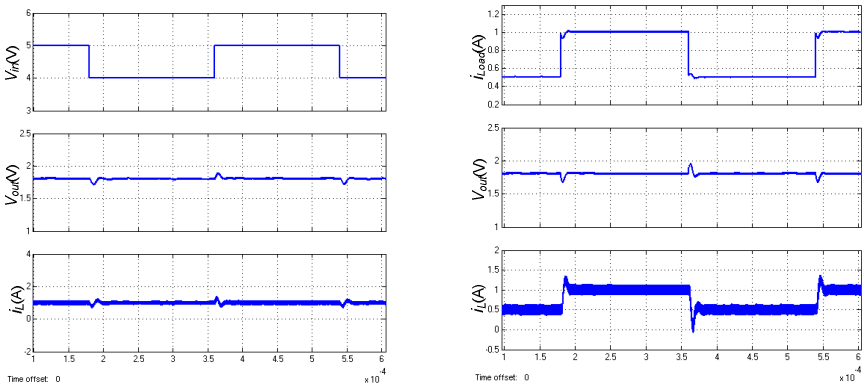


Fig. 7. MATLAB/Simulink model of a buck converter with a digital controller.



(a) (b)

Fig. 8. Comparison of transient response between PID, AD-PID and MA-PID. (a) Input voltage charge between 4V and 5V. (b) Load charge between 0.5A and 1A.



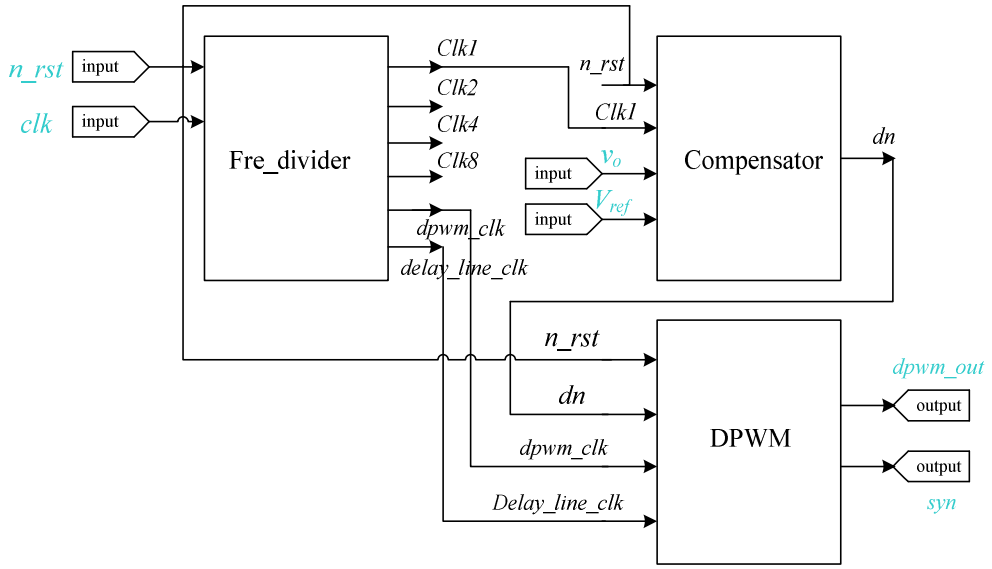
(a) (b)

Fig. 9. Transient simulation of the proposed MA-PID controller. Simulated (a) line transient response, (b) load transient response, top-to-bottom: input voltage, output voltage, inductor current.

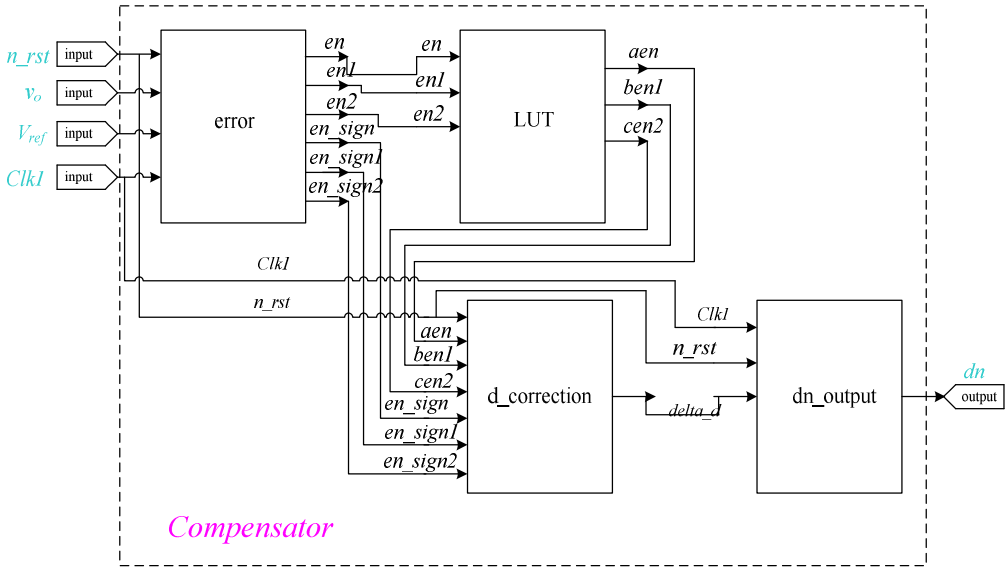
For simulations of the PID and MA-PID architecture, the parameters K_p, K_i and K_d should use the corresponding specific values. For example, equation (9) can be rewritten for the MA-PID architecture as:

$$u(k) = u(k-1) + (K_P + \alpha)[e(k) - e(k-1)] + (K_I + \beta)e(k) + (K_D + \gamma)[e(k) - 2e(k-1) + e(k-2)] \quad (10)$$

The transient response of the designed converter is shown in Fig. 8 in order to compare the PID control, the AD-PID control and the MA-PID control. The load transient response is simulated by producing a 500mA step in the Load. The line transient response is simulated with an input voltage change from 4V to 5V. It can be seen that there are no additional oscillations or ringing during the MA-PID operation, and that the MA-PID algorithm has a better line transient response than the AD-PID algorithm. Fig. 9 shows the simulated line and



(a)



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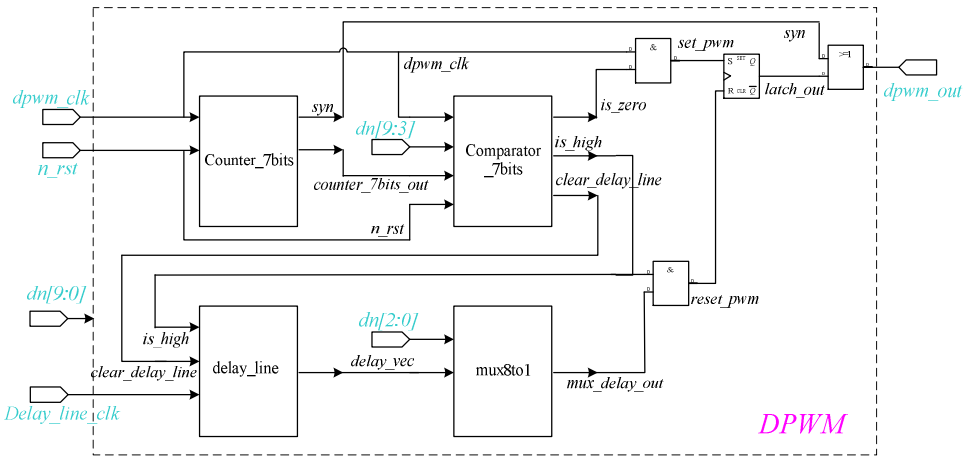


(c)

Fig. 10. HDL block for synthesized on the FPGA.

load transient responses with the MA-PID controller. Table IV summarizes the comparison results of the simulation recovery time. It can be observed that the MA-PID control algorithm reduces the recovery time by 25μs (>60%) in the overshoot and by 45μs (about 80%) in the undershoot under the line transient response. Meanwhile, for the load transient response, the recovery time is reduced by 15μs (about 50%) and 10μs (about 50%), respectively. Thus, the MA-PID algorithm immensely improves the dynamic response to enhance the system performance.

IV. FPGA Implementation of the MA-PID Control Algorithm

Digital controllers based on Field-Programmable Gate Arrays (FPGAs) are widely used in various applications. They have some advantages such as flexibility, parallel computing capability and integration. The digital compensator and DPWM are the main part of the implemented digital control circuit based on a FPGA. They are described using Hardware Description Language (HDL). Fig. 10 illustrates the HDL blocks which will be synthesized on the FPGA. It can be seen that compensator module uses a look-up table, and that the DPWM module uses a hybrid structure.

For the static voltage requirement, this paper requires that the output voltage V_{out} should be kept at 1% around the reference voltage V_{ref}=1.8V. In addition, according to the compensation method in section V, the actual controller parameters have a fractional part which cannot been realized directly using hardware description language. Therefore, the parameters should be amplified by a factor of 2^n and rounded to their nearest value [22]. The amplification factor decides the rounding error, and the larger the factor is, the smaller the rounding error becomes. However, if the amplification factor is larger, the area consumption increases. Therefore, the compromise between the factor and the area is particularly important. Finally, the duty command $u(k)$ in equations (9) and (10) should be scaled to $1/2^n$ to compute the actual duty ratio.

In order to test these two control algorithms, a buck converter prototype has been implemented as shown in Fig. 11. The power MOSFET transistor is a UPA2791, and the driver chip is a UCC27524. An Altera Cyclone II chip (EP2C50208C8N) is used to implement the conventional PID and MA-PID control algorithms. The input voltage v_{in} = 5V is set to the closed-loop to achieve an output voltage at 1.8V. Fig. 12 shows the output voltage transient waveforms of the converter with the conventional PID and MA-PID controllers under load current changes. The results indicate that the MA-PID control algorithm possesses a lower amplitude of overshoot/undershoot, a faster recovery time and a smaller voltage deviation. The recovery time of the MA-PID controller is about 300μs, which is a reduction of 60%, and the amplitude of the undershoot is 34mV, which is a reduction of 53%, when compared with the conventional PID controller.

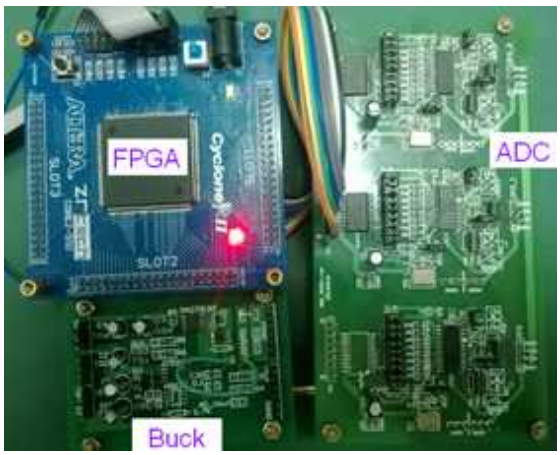
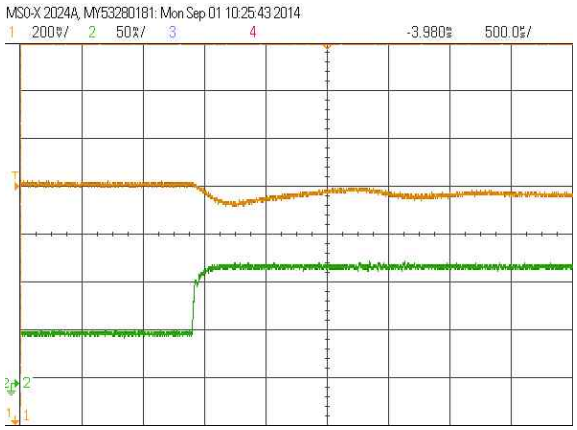


Fig. 11. A buck converter prototype and control system (FPGA+ADC).



(a)

(b)

Fig. 12. Transient waveforms under load change of 0.8 to 1.5A Top-to-bottom: output voltage, load current. (a)Conventional PID. (b)MA-PID.

Fig. 13 shows the corresponding steady-state output voltage under a different load current. It can be seen that the proposed MA-PID control algorithm achieves a smaller steady-state deviation (<18μV/mA), when compared with the conventional PID algorithm.

The specifications and performances of the proposed

TABLE IV
COMPARISON OF THE SIMULATION RECOVERY TIME OF BOTH METHODS

Algorithm	Line transient response(1V)		Load transient response(500mA)	
	overshoot	undershoot	overshoot	undershoot
PID	40μs	60μs	30μs	20μs
MA-PID	15μs	15μs	15μs	10μs

TABLE V
SUMMARY OF THE SPECIFICATIONS AND PERFORMANCES OF THE PROPOSED MA-PID CONTROL ALGORITHM AND PRIOR ARTS

	This paper	[23]	[24]	[25]	LTC3530
Control type	Digital	Digital	Digital	Digital	Analog
Control algorithm	Adaptive digital PID	Improved digital peak current	Adaptive PD+I DCD-RLS	Fist-order digital filter	NA
Switch frequency	1MHz	50kHz	20kHz	3.125MHz	1MHz
Input voltage	3.6-5V	5V	10V	0-3.3V	1.8-5.5V
Output voltage	1.8V	1.5V	3.3V	0.1-3.3V	3.3V
Filter inductor @DCR	4.7μH@200mΩ	20μH	220μH@63mΩ	2.2μH	4.7μH
Filter capacitor @ESR	10μF@100mΩ	1420μF	330μF@25mΩ	10μF	22μF
Number of A/D	1	2	1	1	0
The precision of A/D	8bit	8bit	12bit	10bit	NA
The precision of DPWM	10bit	10bit	>12bit	>10bit	NA
Load Step Response	0.43μs/mA 0.049 mV/mA	1.24μs/mA 0.07mV/mA	1.82μs/mA 0.38mV/mA	2μs/mA 0.08mV/mA	1μs/mA 0.33 mV/mA

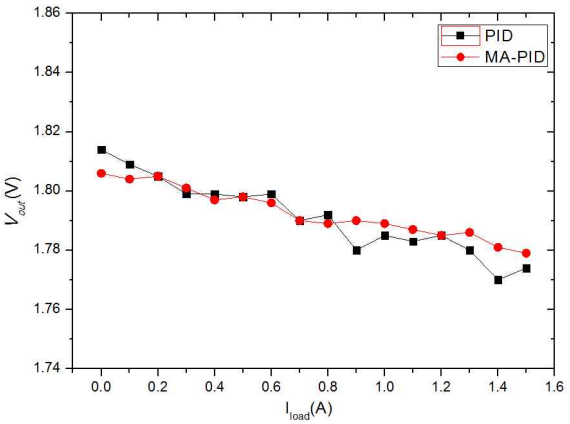


Fig. 13. Output voltages under different load currents.

MA-PID control algorithm are compared with those reported for DC-DC converters in recent studies. This comparison is summarized in Table V. It shows that the proposed MA-PID control algorithm achieves a better load step response than those of references [23]-[25] and a LTC3530 chip under the condition of reduced hardware requirements.

V. CONCLUSIONS

This paper presents a modified adaptive PID algorithm for digitally controlled DC/DC buck converters. The proposed algorithm does not require any additional components, and it does not detect any extra signals which reduces the complexity and cost of the controller. In addition, this paper also gives a step-by-step design flow of models, simulations and implementations based on FPGA for DC/DC converters. The simulation results indicate that the proposed control algorithm improves the line and load transient responses when compared with the conventional PID and AD-PID algorithms. Meanwhile, it can be seen from the experimental results that the proposed MA-PID algorithm possess better dynamic performance, such as a faster recovery time, a smaller steady-state deviation and a lower amplitude of the overshoot/undershoot.

Although this paper uses a Buck-type power converter topology as an example, a similar concept can be extended to other digital control switching converter systems.

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REFERENCES

[1] B. J. Patella, A. Prodic, A. Zirder, and D. Maksimovic, "High-frequency digital controller IC for DC/DC converters," in *Proc. Applied Power Electronics Conference and Exposition (APEC),* pp. 374-380, 2002.

[2] P. Zumel, C. Fernandez, M. Sanz, A. Lazaro, and A. Barrado, "Step-by-step design of an FPGA-based digital compensator for DC/DC converters oriented to an introductory course," *IEEE Trans. Educ.,* Vol. 54, No. 4, pp. 599-609, Nov. 2011.

[3] Y. F. Liu, E. Meyer, and X.D. Liu, "Recent developments in digital control strategies for DC/DC switching power converters," *IEEE Trans. Power Electron.*, Vol. 24, No. 11,

pp. 2567-2577, Nov. 2009.
[4] M. Mahdavian, M. B. Poudeh, and N. Wattanapongsakorn, "Improving the efficiency of power supplies with an adaptive control method," in *Proc. ECTI-CON*, pp. 1-4, 2013.
[5] H. Wangxin and J. A. A. Qahouq, "Tuning of a digital proportional-integral compensator for DC-DC power converter," in *Proc. APEC*, pp. 270-275, 2013.
[6] J. A. A. Qahouq and V. Arikatla., "Online closed-loop auto-tuning digital controller for switching power converters," *IEEE Trans. Ind. Electron.,* Vol. 60, No. 5 , pp. 1747-1758, May 2013.
[7] F. Kurokawa, R. Yoshida, Y. Maeda, K. Murata, "Transient response of novel fast digital PID control DC-DC converter," in *Proc. ICEMS,* pp. 1-4, 2011.
[8] F. Kurokawa, Y. Maeda, Y. Shibata, H. Maruta, T. Takahashi, K. Bansho, T. Tanaka, and K. Hirose, "Fast response digital PID control circuit for DC-DC converter," in *Proc. IEEE Region 10 Conference*, pp. 2159-2164, 2010.
[9] F. Kurokawa and R. Yoshida, "Transient response of fast digital PID control switching power supply," in *Proc. IEEE Vehicle Power and Propulsion Conference*, pp. 614-617, 2012.
[10] A. T. L. Lee Albert, J. K. O. Sin Johnny, P. C. H. Chan, "Adaptive high-bandwidth digitally controlled buck converter with improved line and load transient response," *IET Power Electron.,* Vol. 7, No. 3, pp. 515-526, Mar. 2014.
[11] Wang Qing, Chen Ning, Xu Shen, et al, "Trajectory prediction control for digital control DC-DC converters with fast transient response," *Microelectronics Journal*, Vol. 45, No. 6, pp. 767-774, Jun. 2014.
[12] V. Yousefzadeh, A. Babazadeh, B. Ramachandran, E. Alarcon, L. Pao, and D. Maksimovic, "Proximate time-optimal digital control for synchronous buck DC-DC Converters," *IEEE Trans. Power Electron.,* Vol. 23, No. 4, pp. 2018-2026, Jul. 2008.
[13] C. E. Carreio, E. Vidal-Idiarte, R. Giral, and L. Martinez-Salamero, "Predictive digital interpolation current control for DC-DC power converters," *IET Power Electron.*, Vol. 2, No. 5, pp. 545-554, Sep. 2009.
[14] J.-T. Su, D.-M. Liu, C.-W. Liu, and C.-W. Hung, "An adaptive control method for two-phase DC/DC converter," in *Proc. International Conference on Power Electronics and Drive Systems(PEDS)*, pp. 288-293, 2009.
[15] V. Arikatla and J. A. A. Qahouq, "Adaptive digital proportional-integral-derivative controller for power converters," *IET Power Electron.*, Vol. 5, No. 3, pp. 341-348, Mar. 2012.
[16] P. Ovidiu and L. Serban, "Switching mode power converters modeling with parasitic components," in *Proc. 30th International Spring Seminar on Electronics Technology,* pp. 545-550, 2007.
[17] Z. Xu and X. Shi, "Simulation study of buck converters based on Matlab/GUI," *Journal of East China Jiaotong University*, Vol. 29, No. 4, pp. 35-39, 2012.
[18] H. Cheng, C. Wang, and J. Wang, *Modeling, Control and Digital Controller Implementation of Switching Power Converters*, Tsinghua University Press, pp. 104-106, 2013.
[19] S. P. Li and Q. S. Jiang, "Study on PID Parameters Tuning Method Based on Matlab/Simulink," in *Proc. IEEE International Conference on Communication Software and Networks*, pp. 408-411, 2011.
[20] V. Arikatla and J. A. A. Qahouq, "DC-DC power converter with digital PID controller," in *Proc. Applied Power Electronics Conference and Exposition (APEC)*, 2011.
[21] J. H. Su, J. J. Chen, and D. S. Wu, "Learning feedback controller design of switching converters via Matlab/Simulink," *IEEE Trans. Educ.*, Vol. 45, No. 4, pp. 307-315, Nov. 2002.
[22] S. Chander, P. Agarwal, and I. Gupta, "FPGA-based PID controller for DC-DC converter," in *Proc. Joint International Conference on Power Electronics, Drives and Energy Systems*, pp. 1-6, 2010.
[23] G. Zhou, J. Xu, and Y. Jin, "Improved digital peak current predictive control for switching DC-DC converters," *IET Power Electron.*, Vol. 4, No. 2, pp. 227-234, Feb. 2011.
[24] A. Mather, A. Matthew, and G. Damian, "Adaptive PD+I control of a switch-mode DC-DC power using a recursive FIR predictor," *IEEE Trans. Ind. Appl.*, Vol. 47, No. 5, pp. 2135-2144, Sep./Oct. 2011.
[25] E. G. Soenen, A. Roth, J. Shi, M. Kinyua, J. Gaither, and E. Ortynska, "A robust digital dc-dc converter with rail-to-rail output range in 40nm CMOS," in *Proc. IEEE Int. Solid-State Circuits*, pp. 198-199, 2010.

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