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Switching Voltage Modeling and PWM Control in Multilevel Neutral-Point-Clamped Inverter under DC Voltage Imbalance

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Abstract

This paper presents a novel switching voltage model and an offset-based pulse width modulation (PWM) scheme for multilevel inverters with unbalanced DC sources. The switching voltage model under a DC voltage imbalance will be formulated in general form for multilevel neutral-point-clamped topologies. Analysis of the reference switching voltages from active and non-active switching voltage components in *abc* coordinates can enable voltage implementation for an unbalanced DC-source condition. Offset voltage is introduced as an indispensable variable in the switching voltage model for multilevel voltage-source inverters. The PWM performance is controlled through the design of two offset components in a subsequence. One main offset may refer to the common mode voltage, and the other offset restricts its effect on the quality of PWM control in related DC levels. The PWM quality can be improved as the switching loss is reduced in a discontinuous PWM mode by setting the local offset, which is related to the load currents. The validity of the proposed algorithm is verified by experimental results.

Key words: Decoupling offset, Multilevel inverter, PWM technique, Switching voltage, Unbalanced DC sources

I. INTRODUCTION

Multilevel inverters play an important role in current high-performance applications. Two topologies have become popular in practice, namely, multilevel neutral-point-clamped (NPC) inverter and multilevel cascaded inverter, as shown in Fig. 1. Well-known pulse width modulation (PWM) methods include carrier-based PWM (CPWM) and space vector PWM (SVPWM) techniques [1]-[8].

In the SVPWM method, the switching states in the switching sequences are selected after determining the three pivot vectors in the space vector diagram. The control process of the SVPWM is relatively complicated in a multilevel inverter [14], [15]. When the inverter level is high, the two main disadvantages of this PWM method are burden calculation and lookup table, both of which require large memory storage.

CPWM techniques are commonly used in practical applications because of their simple implementation. Algorithms of a SVPWM scheme with the nearest three voltage vectors can be completely realized by a corresponding CPWM method.

The offset feature in a two-level inverter has been extensively investigated in previous studies [9]-[11]. In multilevel inverters, a CPWM method can offer flexible control of vector redundancies through proper offset regulation [4], [20].

Offset voltage significantly affects converter performance. Offset adjustments can generate different PWM modes [1], [3], [26]-[31]. Proper selection of offset voltage can reduce switching amount and the harmonic distortion factor in different PWM techniques [4], [24], and its regulation with load currents may minimize switching losses [25]. Therefore, offset voltage is practically indispensable and is an important variable in the control model of a multilevel voltage-source inverter.

Offset control is also available in space vector modulation

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by redistributing the switching time duties of two redundant states [10]-[13]. However, in multilevel inverters, an algorithm based on the SVPWM method may generally be difficult to apply if the offset is used as a variable to control DC and neutral currents, and thus to balance DC voltages and reduce the effect of common mode voltages (CMVs) on electrical drives [16]-[18].

The unbalanced conditions of DC-link voltages that are fed to an inverter have a negative effect on the output quality. The imbalance, which is represented by the ripple on the DC link, causes distorted output waveforms with low-frequency harmonics. This phenomenon can lead to degradation in the load performance [38]. Solutions to cope with this problem can be found in [19], [23], [35]-[39]. The works in [35]-[37] focused on a two-level inverter and other classic topologies. In [38], a feed-forward SVPWM method was proposed to obtain balanced output voltages in a three-level NPC inverter. Other than the limitation represented by the complication of the control process in this method, the flexibility of the offset voltage has not been fully explored.

In [19], a simple carrier-based method with DC-link ripple feed-forward compensation in a multilevel inverter was introduced. The idea of this work was to modify the carriers according to the DC-link fluctuation. However, given that a sinusoidal reference was assumed and the offset voltage was constant, the maximum modulation index could not be greater than 0.866, which corresponded to the maximum modulation index of the conventional sine PWM method in a balanced condition.

In [23] and [39], a modified SVPWM method was applied to multilevel converters to solve the problem of unbalanced DC conditions. Under balanced and unbalanced conditions, the methods analyzed the control voltage in 3D coordinates and offered a simpler control process than the 2D-SVM in [38]. Nevertheless, the characteristics of the offset were not analyzed. In addition, given that no harmonic injection was considered, the modulation index limitation of 0.866 was unavoidable, as in [19].

The present study proposes a new CPWM technique for multilevel diode-clamped inverters under balanced and unbalanced conditions. The proposed algorithm is applicable to NPC inverters with arbitrary numbers of levels. With the actual conditions of the DC links considered, a novel approach to modeling switching voltages and an offset-based PWM scheme using *abc* coordinates are systematically analyzed. The switching voltages characterize the control characteristics of multilevel inverters, while the offset-based PWM quality control improves the output quality following some particular demands. In the proposed PWM scheme, the global offset component enables control of the draft CMV, and the local offset component sets the PWM modes. A current-based discontinuous PWM (DPWM) method that utilizes these two offset components to reduce switching loss is also proposed.

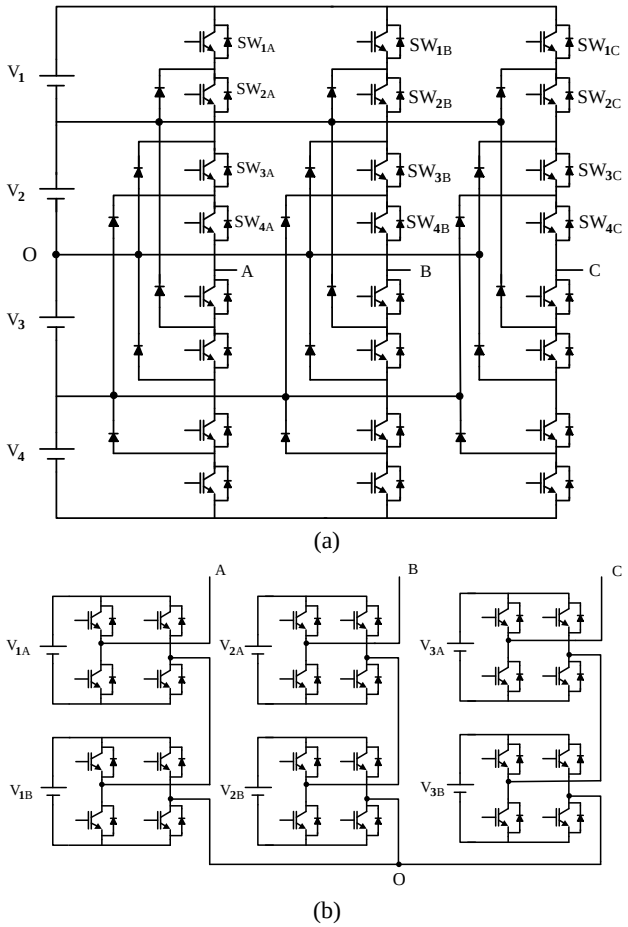


Fig. 1. Multilevel inverter circuits. (a) Five-level diode-clamped inverter. (b) Five-level cascaded inverter.

The modulation index control has been improved as compared with those in [19], [23], [39]. Therefore, the attainable maximum linear range of the output voltage control (under unbalanced input conditions) is always achieved.

The validity of the proposed feed-forward PWM method will be demonstrated through simulation and experimental results.

II. SWITCHING VOLTAGE FORMULATION FOR MULTILEVEL INVERTERS UNDER INPUT VOLTAGE IMBALANCE

A. Modeling of the Switching Voltage for a Multilevel NPC Inverter

In the five-level NPC topology in Fig. 1(a), the DC-link-fed inverter voltages are assumed to have the values V_1, V_2, V_3, and V_4. With a selected neutral point "O" and the designated switches in the X-phase (X = A,B,C) represented as SW_{1X}, SW_{2X} , SW_{3X}, and SW_{4X}, respectively, as in Fig. 1(a), the pole (leg) voltage V_{XO} can be determined as

$$V_{XO} = s_{1X}V_1 + s_{2X}V_2 + s_{3X}V_3 + s_{4X}V_4 - V_3 - V_4, \qquad (1)$$

where s_{1x}, s_{2x}, s_{3x}, and s_{4x} represent the switching states of SW_{1X},

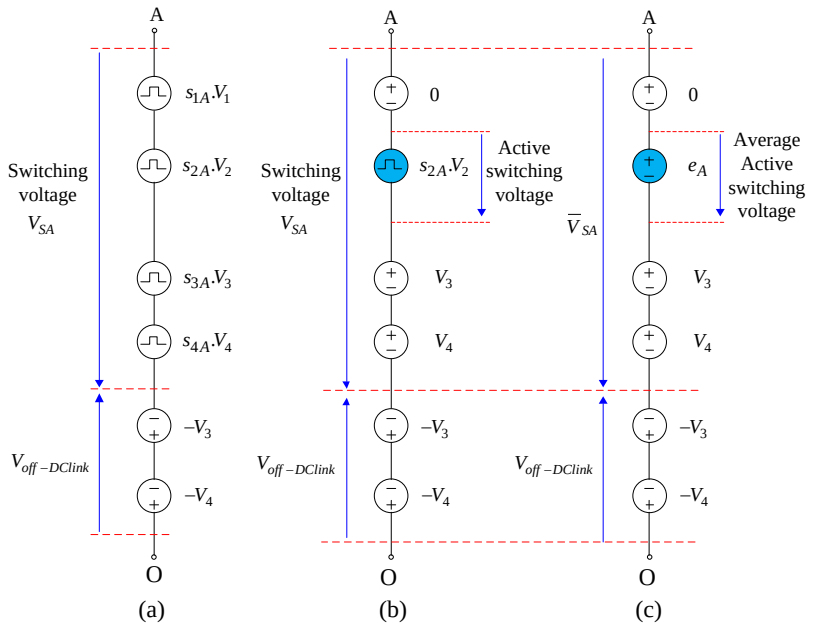


Fig. 2. (a) Relation between A-phase switching voltage and pole voltage. (b) A-phase switching voltage for non-active switches $s_{1A}=0$, $s_{3A}=1$, $s_{4A}=1$ and active switch s_{2A}. (c) Average voltage model of the A-phase switching voltage.

SW_{2X}, SW_{3X}, and SW_{4X}, respectively; s_{1A} is "1" if SW_{1A} is ON; otherwise, its value is "0."

We define the *X-phase switching voltage*, V_{SX}, (X = A,B,C), which is controlled by switches, as follows:

$$V_{SX}=\sum_{j=1}^{n-1}V_{SXj}=\sum_{j=1}^{n-1}s_{jX}V_j. \tag{2}$$

The switching voltage presents a switching-controlled voltage source to supply the load. Eq. (2) shows that the switching voltage consists of $(n-1)$ switching voltage components. j^{th} switching voltage component is defined as a product of j^{th} switching state and its corresponding DC voltage cell, that is,

$$V_{SXj}=s_{jX}V_j. \tag{3}$$

The constraint between switch states for the five-level NPC inverter shown in Fig. 1(a) is simply expressed as

$$0\le s_{1X}\le s_{2X}\le s_{3X}\le s_{4X}\le 1. \tag{4}$$

During a sampling period for an X-phase inverter leg, X = A,B,C, only one switch exists, called the active switch s_X; this switch is actively turned on and off. The states of the remaining $(n-2)$ switches, called the non-active switches, are unchanged ($s_{jX}=1$ or $s_{jX}=0$). Each non-active switch provides full voltage $V_{SXj}=V_j$ for $s_{jX}=1$ and zero voltage $V_{SXj}=0$ for $s_{jX}=0$. Among $(n-2)$ non-active switches, L switches are supposed to hold the ON state, and $(n-2-L)$ switches hold the OFF state. We define V_{LX} as the component of the non-active switching voltage provided by the non-active switches. For an active switch s_X, if ξ_X is defined as its average value in a sampling period and V_{DX} as its corresponding DC-link-fed inverter voltage, the instantaneous and average values of the switching voltages can be expressed in terms of two components, namely, non-active switching voltage and active switching voltage. These components are expressed as follows:

$$V_{SX}=V_{LX}+S_XV_{DX}, \tag{5}$$

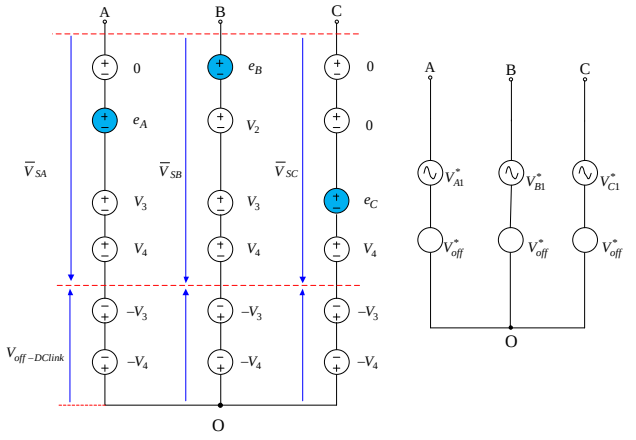
$$\bar{V}_{SX}=V_{LX}+\xi_XV_{DX}=V_{LX}+e_X. \tag{6}$$

The relation among average switching voltage $\bar{V}_{SX}$, non-active switching voltage V_{LX}, and DC voltage linked to active switch V_{DX} can be described as follows:

$$V_{LX}\le\bar{V}_{SX}\le V_{LX}+V_{DX}. \tag{7}$$

The instantaneous switching voltage model for a single leg relative to the pole voltage is presented in Fig. 2(a). Fig. 3(b) provides an example of the A-phase switching voltage model in Fig. 2(a) for the case in which switch s_{2A} is active and has a corresponding DC-link-fed inverter voltage V_2, and the other non-active switches s_{1A},s_{3A},s_{4A} have respective DC-link-fed inverter voltages of V_1,V_3,V_4, which receive values of 0, 1, and 1. The A-phase average voltage model of the example given in Fig. 2(b) is illustrated in Fig. 2(c).

Eq. (1) indicates that the sum of two DC-link-fed inverter voltages V_3,V_4 exists in the pole leg voltage formulation. This component presents an offset voltage $V_{off-DCLink}$, which is illustrated in the switching voltage model of the five-level NPC inverter in Fig. 2. In topologies with arbitrary numbers of



(a) (b)

Fig. 3. (a) Average voltage model of the three-phase pole voltages with active switches s_{2A}, s_{1B}, s_{3C} and non-active switches $(s_{1A},s_{3A},s_{4A}) = (0,1,1)$, $(s_{2B},s_{3B},s_{4B}) = (1,1,1)$, and $(s_{1C},s_{2C},s_{4C}) = (0,0,1)$. (b) Average voltage model of the three-phase pole voltages expressed in terms of the fundamental V^*_{X1} and the CMV V^*_{off}.

levels, $V_{off-DCLink}$ can be calculated as the voltage between the neutral point O and the lowest voltage point of the inverter.

The pole voltage V_{XO} can be analyzed in relation to the fundamental output phase voltage as follows:

$$V_{XO} = V_{X1} + V_{off}\,, \tag{8}$$

where

$$V_{A1} = \frac{2V_{AO} - V_{BO} - V_{CO}}{3};\quad V_{B1} = \frac{2V_{BO} - V_{CO} - V_{AO}}{3};$$

$$V_{C1} = \frac{2V_{CO} - V_{AO} - V_{BO}}{3};\quad V_{off} = \frac{V_{AO} + V_{BO} + V_{CO}}{3}.$$

Using Eq. (8) and in consideration of Eq. (1), the instantaneous switching voltage and average switching voltage in a sampling period can be expressed in other forms as follows:

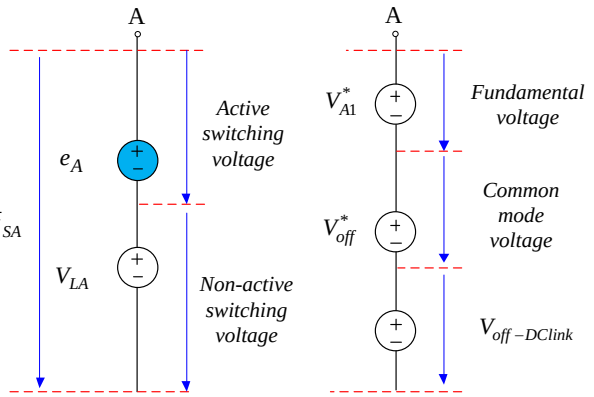
$$V_{SX} = V_{X1} + V_{off} + V_{off-DClink}\,, \tag{9}$$

$$\bar{V}_{SX} = V^*_{X1} + V^*_{off} + V_{off-DClink}\,, \tag{10}$$

where v^*_{X1} and v^*_{off} are the reference fundamental output phase voltage and reference CMV respectively. They satisfy

$$\bar{V}_{XO} = V^*_{X1} + V^*_{off}\,. \tag{11}$$

From the one-phase average pole voltage model expressed in terms of average switching voltage and $V_{off-DCLink}$ as in Fig. 2(c), as well as the average pole voltage obtained in Eq. (11), the three-phase average pole voltage models that use the two analytical approaches are described in Fig. 3. The voltage model in Fig. 3(a) corresponds to a specific case in which the active switches for the A, B, and C phases are s_{2A}, s_{1B}, and s_{3C}, respectively; the sets of non-active switches are



(a) (b)

Fig. 4. Multilevel NPC inverter: A brief description of the A-phase switching voltage from (a) the active and non-active switching voltage components and (b) the zero/non-zero sequence voltages.

$(s_{1A},s_{3A},s_{4A}) = (0,1,1)$, $(s_{2B},s_{3B},s_{4B}) = (1,1,1)$, and $(s_{1C},s_{2C},s_{4C}) = (0,0,1)$.

The relation of the two models in Figs. 3(a) and 3(b) shows that to obtain three-phase output voltages with a predefined CMV, the average switching voltages have to be the sum of the fundamental voltage V^*_{X1}, the CMV V^*_{off}, and a zero sequence voltage injected from the DC-link-fed inverter voltages $V_{off-DCLink}$. As a result, a new reference average switching voltage model of the A-phase is derived, as shown in Fig. 4(b). The complete PWM algorithm for multilevel NPC inverters under balanced and unbalanced conditions will be realized by using this switching voltage model and the model illustrated in relation to the active and non-active switching voltages in Fig. 4(a).

B. Fundamental Voltage Limit and the Global Reference CMV Design

The control limits of two parameters, namely, reference fundamental voltage and CMV, should be determined to completely master the switching voltage model in Fig. 4.

The maximum (minimum) value of the switching voltage will be obtained if all switches are turned "ON" ("OFF").
In a five-level NPC inverter, for example, these values are determined as follows:

$$V_{SWMAX} = V_1 + V_2 + V_3 + V_4\,, \tag{12}$$

$$V_{SWMIN} = 0\,. \tag{13}$$

As a result, the possible maximum fundamental voltage V^*_{X1} of the under-modulation limit is given as follows:

$$V^*_{1MAX} = \frac{V_{SWMX}}{\sqrt{3}}\,. \tag{14}$$

The reference CMV V^*_{off} can generally be expressed as a function of the variable η_1, that is,

$$V_{off}^{*} = \eta_1 V_{off-MX} + (1-\eta_1)V_{off-MN}\,;0 \le \eta_1 \le 1\,, \quad (15)$$

where V_{off-MX} and V_{off-MN} are the maximum and minimum values of V_{off}^{*} respectively. These values can be deduced from the switching voltage model in Fig. 4 and Eqs. (12) and (13) as follows:

$$\begin{aligned} V_{off-MX} &= Min(V_{SWMAX} - V_{X1}^{*}) - V_{off-DClink} \\ V_{off-MN} &= -Min(V_{X1}^{*}) - V_{off-DClink} \\ (X &= A,B,C) \end{aligned} \quad . \quad (16)$$

The "Min()" function returns the smallest value of the three given values inside the parentheses.

In practical applications, two popular reference average CMV designs are as follows:

Medium CMV [9]–[12]: This CMV approach is often used in two-level and multilevel inverters to maximize the linear PWM control range. In this case, the global offset is obtained by setting $\eta_1 = 0.5$ in Eq. (15) as follows:

$$V_{off}^{*} = V_{off-Med} = (V_{off-MX} + V_{off-MN})/2\,. \quad (17)$$

Minimum CMV [25]: The reference offset voltage is selected such that the absolute value of the obtained average CMV is at the minimum. The sinusoidal PWM method is a particular case of this PWM technique for a modulation index range lower than 0.866, that is,

$$V_{off}^{*} = V_{off-op} = \begin{cases} V_{off-MX} & \text{if} \quad V_{off-MN} \le V_{off-MX} \le 0 \\ V_{off-MN} & \text{if} \quad 0 \le V_{off-MN} \le V_{off-MX} \\ 0 & \text{if} \quad else \end{cases} . \quad (18)$$

III. SWITCHING VOLTAGE IMPLEMENTATION

A. Switching Voltage PWM Control

To implement the reference switching voltages, the active and non-active switching voltage components, as illustrated in Fig. 5(a), have to be calculated. On the basis of Eqs. (4)-(7), the non-active switching voltage components V_{LX} can be simply determined as follows:

$$V_{LX} = V_{SXk} \;\; if \;\; V_{SXk} \le \overline{V}_{SX} \le V_{SX(k+1)}; 1 \le k \le n-1\,, \quad (19)$$

where V_{SXk} is the k[th] discrete switching voltage, and n is the number of levels. For example, in a five-level NPC inverter, five discrete switching voltages are computed in increasing order as $V_{SX1} = 0$, $V_{SX2} = V_4$, $V_{SX3} = V_3 + V_4$, $V_{SX4} = V_2 + V_3 + V_4$, and $V_{SX5} = V_1 + V_2 + V_3 + V_4$.

The DC-link-fed inverter voltages V_{DX} (X = A,B,C), which correspond to the active switches on the three phases, can be determined as the DC cell between the two nearest discrete switching voltages of $\overline{V}_{SX}$.

For the active switches, their switching state sequence can be realized by the CPWM approach illustrated in Fig. 5 with the normalized modulating signals ξ_X, (X = A,B,C), which are calculated as follows:

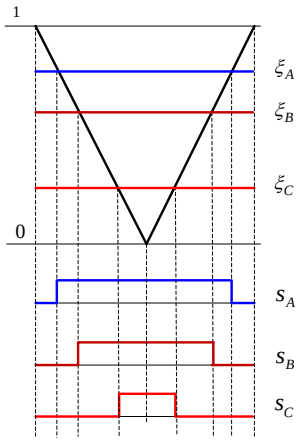


Fig. 5. Implementation of the active switching voltage switching sequence and the switching time diagram.

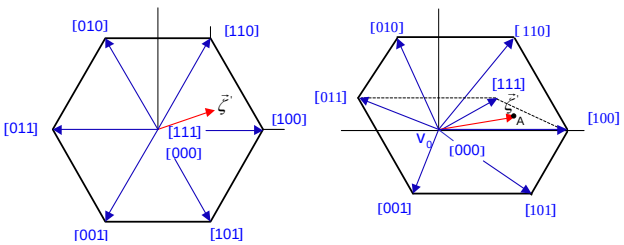


Fig. 6. Vector diagram of the active switching voltages for (a) balanced DC sources and (b) unbalanced DC sources ($V_{DA} > V_{DB} > V_{DC}$).

$$0 \le \xi_X = \frac{\overline{V}_{SX} - V_{LX}}{V_{DX}} \le 1\,. \quad (20)$$

The switching pattern in Fig. 5, from which the active switching states are directly derived, is similar to that of a two-level inverter. Supposing that in a sampling period the three-phase switching sequence in the first half of the pattern in Fig. 5 is (S_A, S_B, S_C) = (0,0,0) → (1,0,0) → (1,1,0) → (1,1,1), then the corresponding active switching sequence is derived as (0,0,0 → $(V_{DA},0,0)$ → $(V_{DA},V_{DB},0)$ → (V_{DA},V_{DB},V_{DC}). The switching voltage sequence is completely realized by using the information of the three-phase non-active voltage and active switching sequence. The switching time diagram of a virtual two level in Fig. 5 is directly imposed onto the switching voltage sequence to complete the switching voltage pattern. As a result, the characteristics of PWM control for a multilevel NPC inverter under unbalanced conditions are fully explored.

When analyzing in the αβ domain of the SVM method, eight switching states of the active switches will establish a voltage vector diagram (Fig. 6). Each discrete voltage vector is calculated as follows:

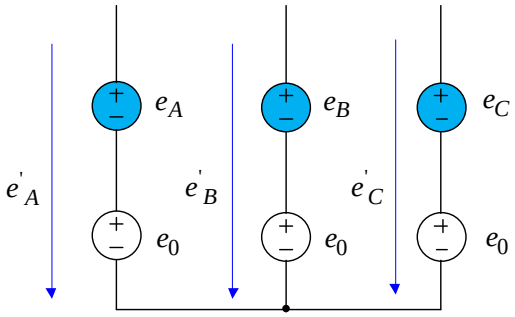


Fig. 7. Equivalent circuit of the modified average active switching voltages.

$$\vec{E} = \frac{2}{3}(S_A V_{DA} + S_B V_{DB} e^{j120} + S_C V_{DC} e^{j240}). \quad (21)$$

In Fig. 6, the discrete vector denoted as $[S_A,S_B,S_C]$ represents the active switching voltage state $(S_A.V_{DA},S_B.V_{DB},S_C.V_{DC})$. Under an unbalanced condition, the active switching voltage vector diagram forms an asymmetrical hexagon. The zero vector of [000] remains at the center of the old symmetrical hexagon in Fig. 6(a), whereas the zero vector of [111] deviates from its former position. As a result, for a reference vector, the PWM control with the three nearest vector principles cannot be implemented in some regions with minimum switching numbers. For example, when the reference vector has its tip located at point A, as illustrated in Fig. 6(b), the use of the three nearest vectors of [000], [100], and [111] will always require considerable switching. The switch from the continuous PWM mode to DPWM mode by simply removing the vector of [000] or [111] is also not allowed. For example, the active switching voltage vectors of [000]-[100]-[101]-[111] in continuous PWM after removing the vector [111] cannot implement the reference voltage vector in Fig. 6(b) because the area formed by the tips of the remaining vectors of [000]-[100]-[101] does not contain the A point.

B. Active Switching Voltage Control – Design of the Local Offset for Reduced Switching Loss

From the switching voltage model of the multilevel inverter shown in Fig. 4(a), the PWM performance can be improved by modifying the active switching voltages. A new equivalent circuit of the active switching voltages is obtained, as shown in Fig. 7, by adding an offset e_0, which is the local offset voltage, to the three-phase average active switching voltages.

Given that

$$e'_X = e_X + e_0 = \xi'_X V_{DX}; \quad X = A,B,C, \quad (22)$$

the modulating signals in Eq. (20) will be modified as follows:

$$0 \le \xi'_X = \frac{e_X + e_0}{V_{DX}} \le 1. \quad (23)$$

1) Reduced Switching Loss PWM under DC Voltage Imbalance: The control range of the local offset e_0 depends on the reference leg voltages of the virtual two-level inverter and the active DC cells of the DC-link-fed inverter voltages. The range can be as follows:

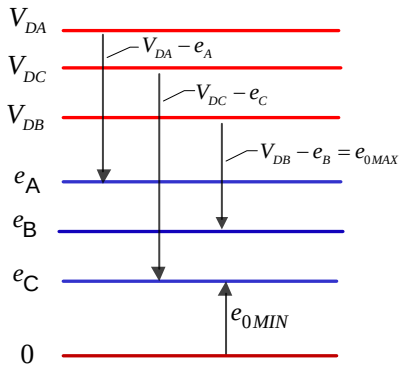


Fig. 8. Determination of local offset limits from the active voltages and related DC-link voltages.

$$e_{0MN} \le e_0 \le e_{0MX}, \quad (24)$$

where

$$e_{0MX} = Min(V_{DA} - e_A, V_{DB} - e_B, V_{DC} - e_C), \quad (25)$$

$$e_{0MN} = -Min(e_A, e_B, e_C). \quad (26)$$

The control limits of e_0 corresponding to a specific case of V_{DX} and e_X (X = A,B,C) are illustrated in Fig. 8.

From Eqs. (24)–(26), the local offset can be expressed as a function of the variable η_2 as follows:

$$e_0 = (1-\eta_2)e_{0MN} + \eta_2 e_{0MX}; \quad 0 \le \eta_2 \le 1. \quad (27)$$

The DPWM mode can be achieved if the value of the parameter η_2 in Eq. (27) is set to 1 or 0. We define i_X (X = A, B, C) as the three-phase output currents, and i_1 and i_2 as the absolute values of the two currents, the respective phases of which can achieve the DPWM by setting the local offset voltage to e_{0MX} and e_{0MN} respectively. I_{MX} and I_{MD} are also defined as the maximum and medium absolute values of the three-phase currents, respectively. The selection rule of e_0 for reduced switching loss can then be proposed as follows:

$$e_0 = \begin{cases} e_{0MX} & i_1 = I_{MX} \quad OR \quad (i_2 \ne I_{MX} \ and \ i_1 = I_{MD}) \\ e_{0MN} & i_2 = I_{MX} \quad OR \quad (i_1 \ne I_{MX} \ and \ i_2 = I_{MD}) \end{cases}. \quad (28)$$

Applying the local offset defined in Eq. (28) allows only the output phases of maximum or medium absolute currents for DPWM control. This condition helps to avoid commutation on the phase of a large current, thus reducing the switching loss of the power converter.

C. Proposed PWM Control Scheme

The proposed PWM control scheme for multilevel NPC inverters under a DC voltage imbalance is described in Fig. 9 on the basis of the theoretical analysis. A global offset voltage

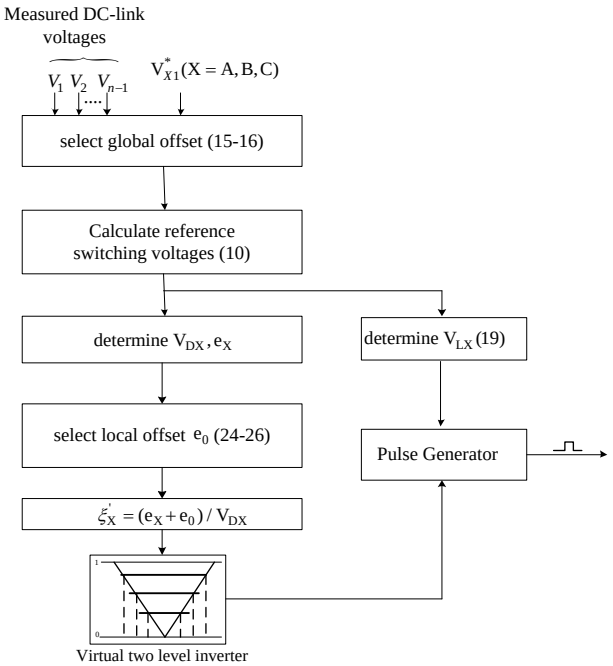


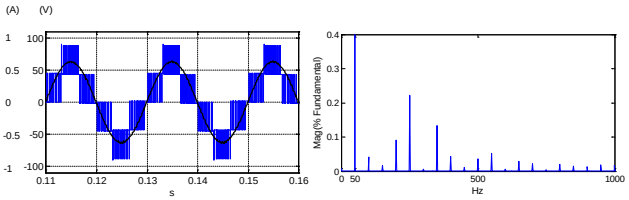
Fig. 9. Proposed feed-forward PWM control scheme for n-level NPC inverter under DC voltage imbalance conditions.

is designed by using the information of the feedback DC-link-fed inverter voltages and the reference fundamental voltages. The reference switching voltages and the respective active and non-active components can be calculated afterwards. (V_{DX}, e_X) helps to determine the local offset limits and simplifies the PWM control of n-level to that of a virtual two-level inverter. The resultant switching sequences and switching time diagrams of the active voltages are directly derived from those of the two-level inverter PWM. The final PWM patterns of n-level NPC are completely realized using this information and in consideration of V_{LX}.

IV. Simulation and Experimental Results

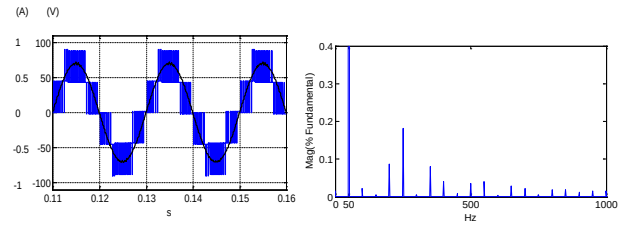
A. Simulation Results

Simulations are conducted for a five-level NPC inverter with unbalanced DC-link voltages and a three-phase load R–L in series, where R = 40 Ω and L = 85 mH. The switching frequency is set to $f_S = 2kHz$, and the output frequency is set to $f_0 = 50Hz$. Under the conditions of V_1 = 55 V, V_2 = 45 V, V_3 = 45 V, and V_4 = 55 V, two modulation indices of m = 0.3 and m = 0.75 are selected to analyze the typical conventional sinusoidal PWM method without compensation and with feed-forward compensation. For the uncompensated algorithm, the waveforms, including output line voltage and current (a) as well as the harmonic spectra of the current (b), are shown in Figs. 10 and 12. The obtained fundamental currents for the given loads are not correct, and the harmonic spectra in Figs. 10(b) and 12(b) show that the currents are influenced by



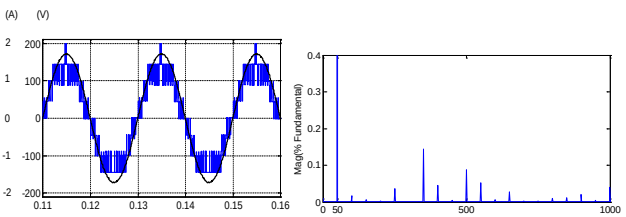
(a) (b)

Fig. 10. (a) Output line voltage and current waveforms. (b) Harmonic spectrum of output currents (Fundamental = 0.63 A, THD = 1.2%) when using conventional sinusoidal PWM without feed-forward compensation (m = 0.3).



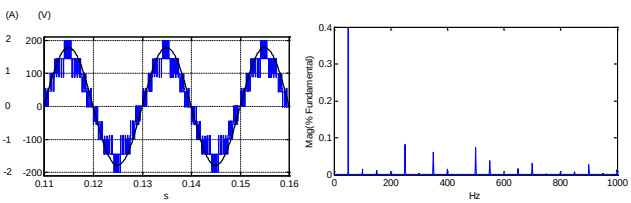
(a) (b)

Fig. 11. (a) Output line voltage and current waveforms. (b) Harmonic spectrum of output currents (Fundamental = 0.7018 A, THD = 1.09%) when using conventional sinusoidal PWM with feed-forward compensation (m = 0.3).



(a) (b)

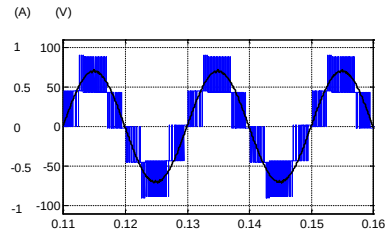
Fig.12. (a) Output line voltage and current waveforms; (b) harmonic spectrum of output currents (Fundamental = 1.721 A, THD = 0.58%) when using conventional sinusoidal PWM without feed-forward compensation (m = 0.75).



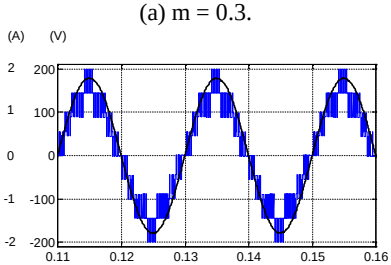
(a) (b)

Fig. 13. (a) Output line voltage and current waveforms; (b) harmonic spectrum of output currents (Fundamental = 1.79 A, THD = 0.52%) when using conventional sinusoidal PWM with feed-forward compensation (m = 0.75).

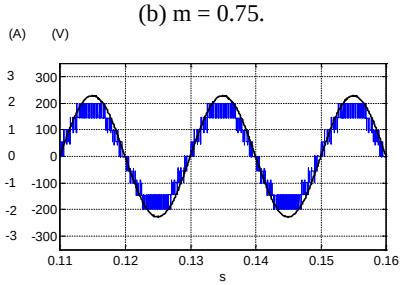
low-order harmonics with a large magnitude. For comparison, the same quantities are given for the sinusoidal PWM method with feed-forward compensation, as in Figs. 11(a) (m = 0.3) and 13(a) (m = 0.75). Improvements are obtained when the compensated algorithm yields output waveforms in Figs. 11(a) and 13(a) with correct fundamental components and low-order harmonics, as depicted in Figs. 11(b) and 13(b). The obtained total harmonic distortion (THD) values of the output currents are 1.09% (m = 0.3) and 0.52% (m = 0.75), whereas they are 1.2% and 0.58% in the uncompensated system.



(a) m = 0.3.



(b) m = 0.75.



(c) m = 0.95.

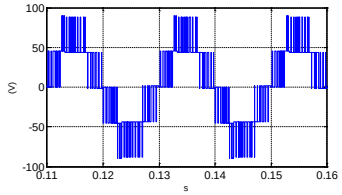
Fig. 14. Output line voltage and current waveforms when using PWM method with medium CMV and feed-forward compensation.

A medium CMV PWM method and a proposed PWM method with reduced switching loss are applied to a five-level NPC inverter with the previous configuration unchanged. The medium CMV PWM is achieved by using Equ. (17) and setting the local offset to zero. In the proposed PWM with reduced switching loss, the local offset is selected as the minimum CMV [Eq. (18)], and the local offset is selected as in Eq. (28).

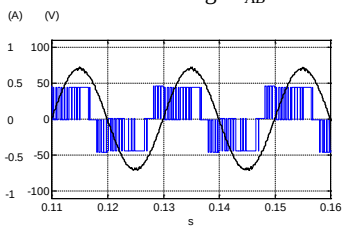
The waveforms obtained using the two PWM methods are shown in Figs. 14 and 15. The resulting THDs of the output currents when using the feed-forward PWM with the medium CMV are 0.99%, 0.56%, and 0.38%, which correspond to modulation index m values of 0.3, 0.75, and 0.95, respectively. By contrast, the THDs are 1.46%, 0.66%, and 0.59% with the proposed PWM method with reduced switching loss.

In the PWM with reduced switching loss, the waveforms of the pole voltage and its respective current for the three different modulation indices are illustrated in Fig. 15. No commutation on one phase occurs at some intervals of its maximum or medium absolute current. As a result of this proposed current-controlled DPWM mode, the switching loss can be significantly reduced, such as in the balanced input voltage case [25].

Figs. 16(a)–16(c) provide a detailed comparison of the line voltage THD when using the three feed-forward PWM control

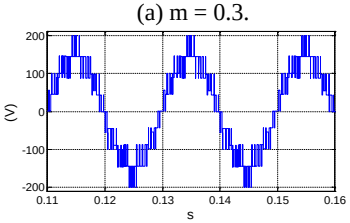


line voltage v_{AB}

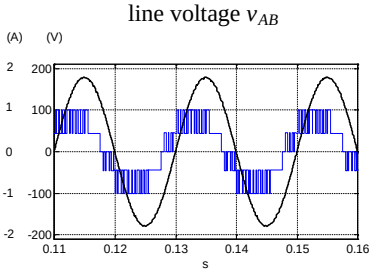


phase current i_A and pole voltage v_{AO}

(a) m = 0.3.

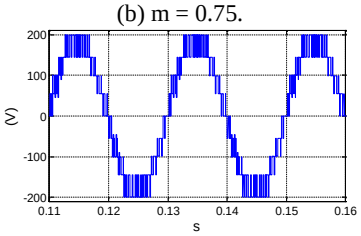


line voltage v_{AB}

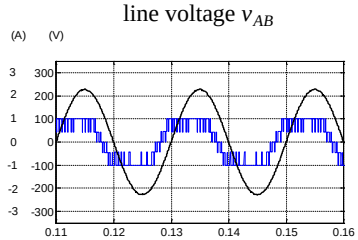


phase current i_A and pole voltage v_{AO}

(b) m = 0.75.



line voltage v_{AB}

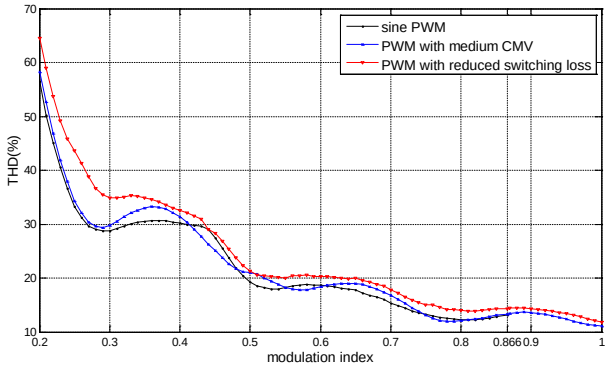


phase current i_A and pole voltage v_{AO}

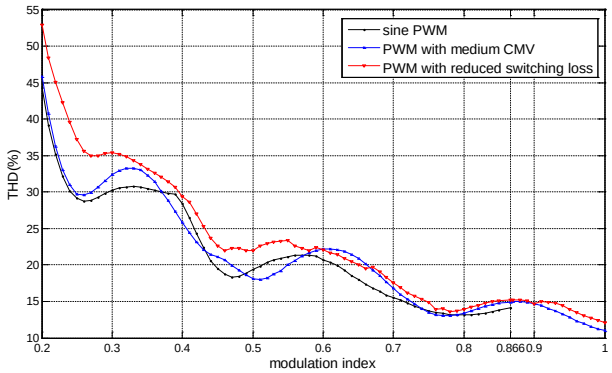
(c) m = 0.95.

Fig. 15. Waveforms of output line voltage and output pole voltage with its corresponding current when using the proposed feed-forward PWM method with reduced switching loss.

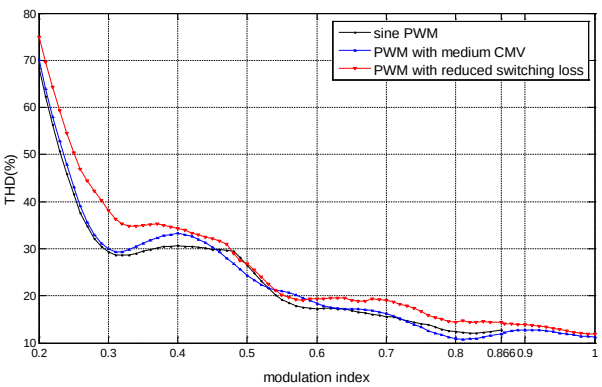
methods: the proposed PWM with reduced switching loss, the conventional sine PWM, and the medium CMV PWM. The THD is calculated up to the 100th harmonics of the output frequency. Each PWM method is analyzed to its maximum



(a) $V_1 = V_2 = V_3 = V_4 = 50$ V.



(b) $V_1 = 55$ V, $V_2 = 45$ V, $V_3 = 45$ V, $V_4 = 55$ V.



(c) $V_1 = 45$ V, $V_2 = 55$ V, $V_3 = 55$ V, $V_4 = 45$ V.

Fig. 16. THD comparison of the three feed-forward PWM methods ($f_S = 5$ *kHz*, $R = 40\,\Omega$, $L = 80$ *mH*).

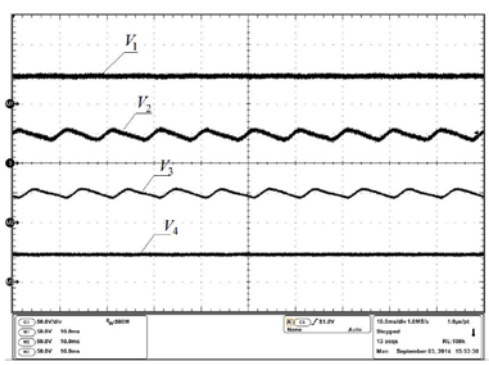
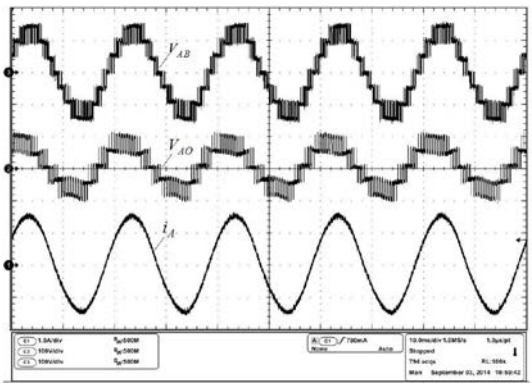
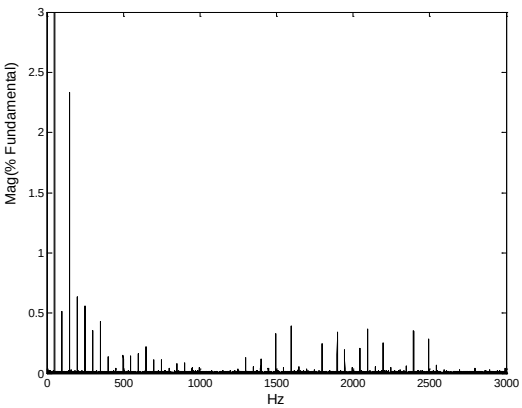


Fig. 17. Setup of the DC-link fed inverter voltages (X: 10 ms/div; Y: 50 V/div).



(Y-axis: Voltage: 100 V/div, Current: 1 A/div)

(a)



(b)

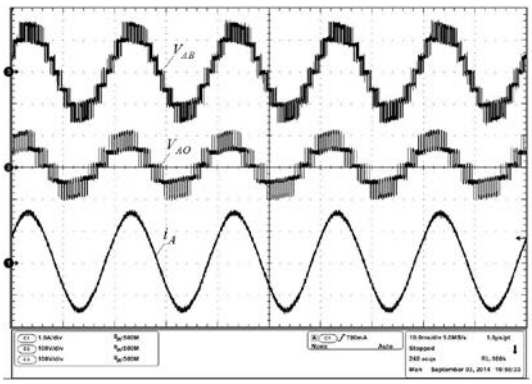
Fig. 18. (a) Waveforms include output line voltage V_{AB}, pole voltage V_{AO} and current i_A (X-axis:10 ms/div). (b) Harmonics spectrum of output current when using conventional sinusoidal PWM without feed-forward compensation (m = 0.7).

modulation index. For the sine PWM method, the maximum value of m is 0.866, whereas it is 1 for the other two methods. The DC-link voltages (V_1, V_2, V_3, V_4) for the THD analysis as in Figs. 16(a)–16(c) are set to (50 V, 50 V, 50 V, 50 V), (55 V, 45 V, 45 V, 55 V), and (45 V, 55 V, 55 V, 45 V), respectively.

B. Experimental Results

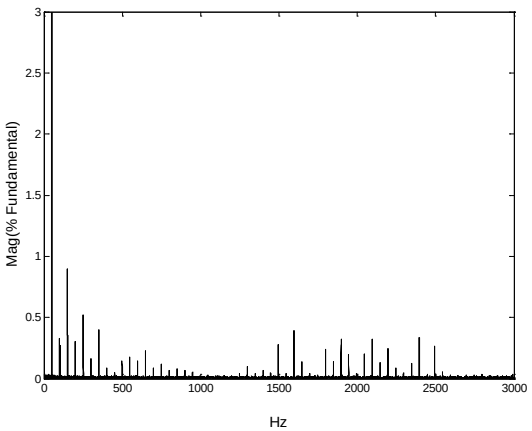
Experimental hardware is built for the five-level NPC inverter to validate the proposed theory. The algorithm is implemented using the eZdsp TMS320F28335 control kit. Four DC voltages are measured with LEM LV25 NP Hall sensors. For the switching loss PWM algorithm, three additional Hall LEM LA25NP current sensors are used to measure the phase load currents. The frequency of the triangle carrier waveform is 2 kHz, and the desired output frequency is 50 Hz. The experimental load parameters are set to $R = 40\Omega$ and $L = 85mH$.

In the first experiment, two DC-link voltages V_1, V_4 are held constant, and the others have large ripples (Fig. 17). Each DC-link voltage of V_1, V_4 is created by a three-phase



(Y-axis: Voltage: 100 V/div, current: 1 A/div)

(a)



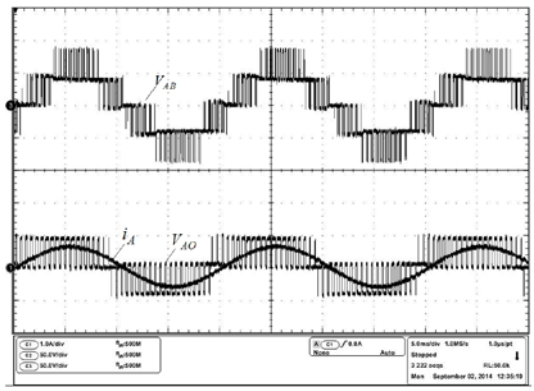
(b)

Fig. 19. (a) Waveforms including output line voltage V_{AB}, pole voltage V_{AO}, and current i_A (X-axis:10 ms/div). (b) Harmonic spectrum of output current when using conventional sinusoidal PWM with feed-forward compensation (m = 0.7).

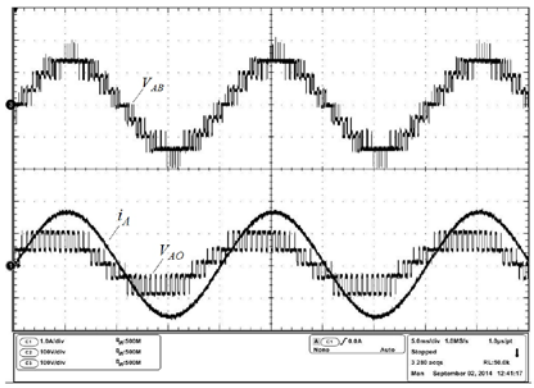
full-wave diode bridge rectifier and a 6800 μ F capacitor. Two middle DC-link voltages V_2, V_3, each of which is created by one single-phase full-wave diode bridge rectifier and a 680 μ F capacitor, have a measured ripple in the range from 42 V to 60 V] when the inverter is in operation at the analyzed modulation index of 0.7.

The different capacitors produced different DC sources, which, in turn, caused asymmetrical output voltages. As shown in Fig. 18(a), without compensation, the distortion of the output current leads to significant low-order harmonics, as depicted in the harmonic spectrum in Fig. 18(b). The sinusoidal current is obtained as in Fig. 19(a) by using the compensated algorithm. The harmonic spectrum of the current in Fig. 19(b) also demonstrates a great reduction in low-order harmonics. The measured THD of the current with the compensated algorithm is 1.72%, whereas it is 2.725% in the uncompensated system.

In the second experiment, the DC-link voltages are set to $V_1 = 55V, V_2 = 45V, V_3 = 45V, V_4 = 55V$. Figs. 20-22 depict the experimental waveforms of the output line voltage and the output current with its respective pole voltage when the



(a) m = 0.3 (Y-axis: Voltage: 50 V/div, Current: 1 A/div).



(b) m = 0.75 (Y-axis: Voltage: 100 V/div, Current: 1 A/div).

Fig. 20. Waveforms of output line voltage and pole voltage with its corresponding current when using sine PWM method with feed-forward compensation (X-axis:5ms/div).

feed-forward PWM methods of the sine PWM, the PWM with medium CMV, and the proposed DPWM are applied. The pole voltage waveform in Fig. 22 shows that similar to the simulation results, the implemented DPWM mode that depends on the phase load currents sets the non-commutation phase at intervals, in which its current attains the maximum or medium absolute value.

A comparison of the experimental line voltage THD (calculated up to the 100th harmonics) of the proposed feed-forward DPWM method with the feed-forward sine PWM and medium CMV PWM is illustrated in Figs. 23(a)-23(c). modulation index. For the sine PWM method, the maximum value of m is 0.866, whereas it is 1 for the other two methods. The DC-link voltages (V_1, V_2, V_3, V_4) for the THD analysis as in Figs. 16(a)–16(c) are set to (50 V, 50 V, 50 V, 50 V), (55 V, 45 V, 45 V, 55 V), and (45 V, 55 V, 55 V, 45 V), respectively.

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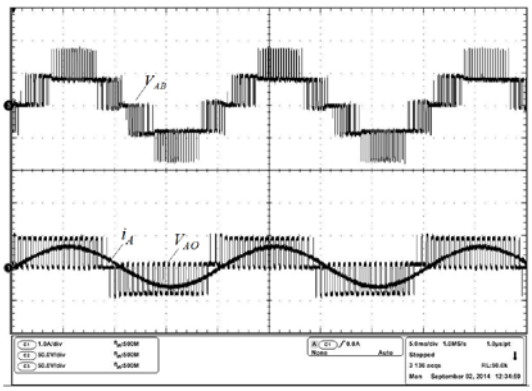
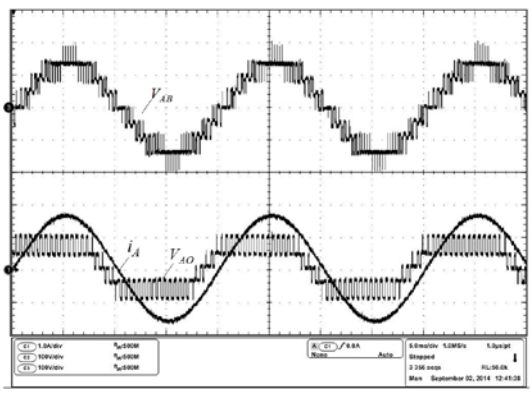
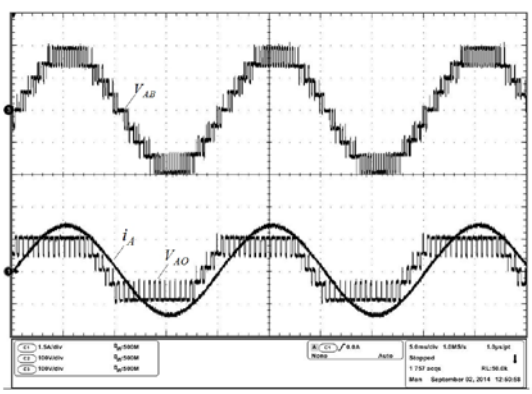


(a) m = 0.3 (Y-axis: Voltage: 50 V/div, Current: 1 A/div).

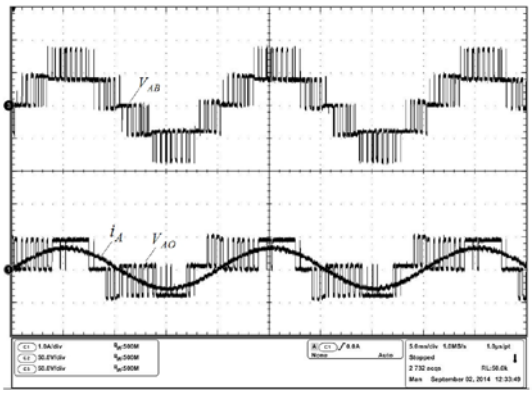


(b) m = 0.75 (Y-axis: Voltage: 100 V/div, Current: 1 A/div).

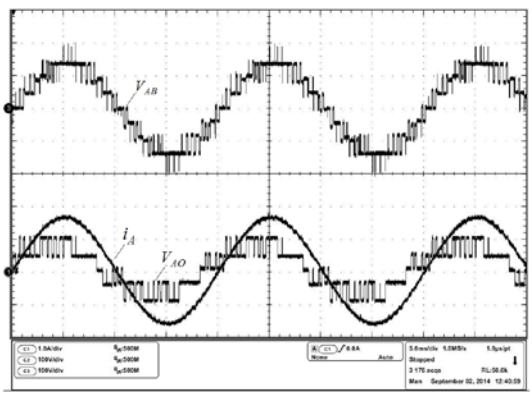


(c) m = 0.95(Y-axis: Voltage: 100 V/div, Current: 1.5 A/div).

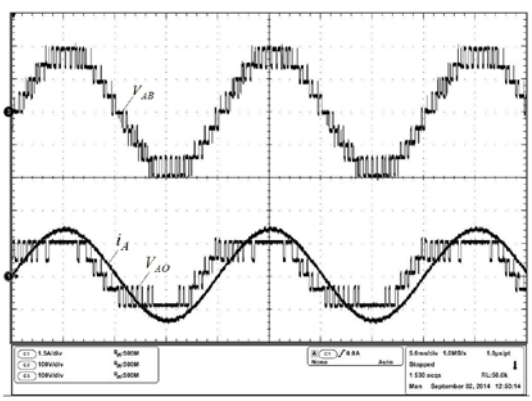
Fig. 21. Waveforms of output line voltage and pole voltage with its corresponding current when using PWM method with medium CMV and feed-forward compensation (X-axis: 5 ms/div).



(a) m = 0.3 (Y-axis: Voltage: 50 V/div, Current: 1 A/div).



(b) m = 0.75 (Y-axis: Voltage: 100 V/div, Current: 1 A/div).



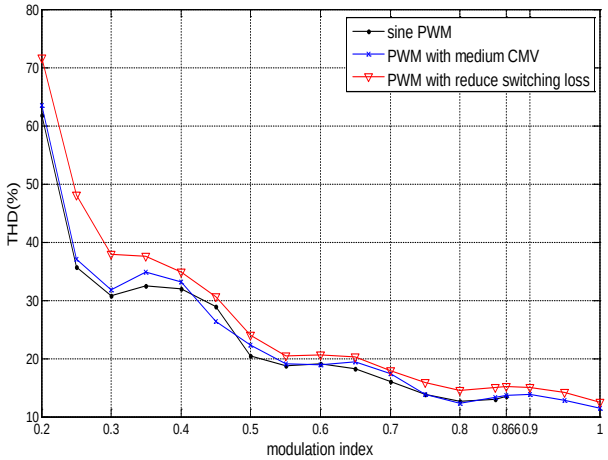
(c) m = 0.95 (Y-axis: Voltage: 100 V/div, Current: 1.5 A/div).

Fig. 22. Waveforms of output line voltage and pole voltage with its corresponding current when using feed-forward PWM method with reduced switching loss (X-axis: 5 ms/div).

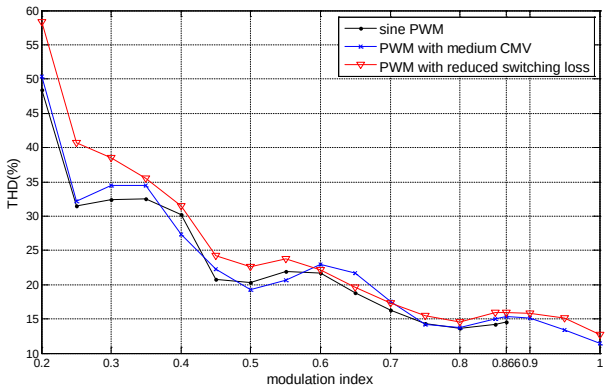
additional Hall LEM LA25NP current sensors are used to measure the phase load currents. The frequency of the triangle carrier waveform is 2 kHz, and the desired output frequency is 50 Hz. The experimental load parameters are set to $R = 40\Omega$ and $L = 85mH$.

In the first experiment, two DC-link voltages V_1, V_4 are held constant, and the others have large ripples (Fig. 17). Each DC-link voltage of V_1, V_4 is created by a three-phase full-wave diode bridge rectifier and a 6800 μ F capacitor. Two middle DC-link voltages V_2, V_3, each of which is created by one single-phase full-wave diode bridge rectifier and a 680 μ F capacitor, have a measured ripple in the range from 42 V to 60 V] when the inverter is in operation at the analyzed modulation index of 0.7.

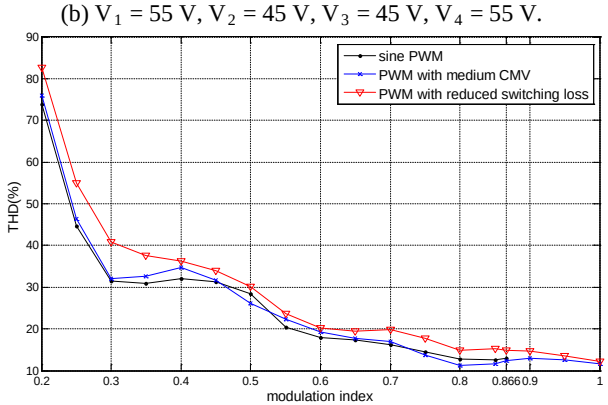
The different capacitors produced different DC sources, which, in turn, caused asymmetrical output voltages. As shown in Fig. 18(a), without compensation, the distortion of the output



(a) $V_1 = V_2 = V_3 = V_4 = 50$ V.



(b) $V_1 = 55$ V, $V_2 = 45$ V, $V_3 = 45$ V, $V_4 = 55$ V.



(c) $V_1 = 45$ V, $V_2 = 55$ V, $V_3 = 55$ V, $V_4 = 45$ V.

Fig. 23. Experimental THD comparison of the three feed-forward PWM methods ($f_S = 5$ *kHz*, $R = 40\ \Omega$, $L = 80$ *mH*).

current leads to significant low-order harmonics, as depicted in the harmonic spectrum in Fig. 18(b). The sinusoidal current is obtained as in Fig. 19(a) by using the compensated algorithm. The harmonic spectrum of the current in Fig. 19(b) also demonstrates a great reduction in low-order harmonics. The measured THD of the current with the compensated algorithm is 1.72%, whereas it is 2.725% in the uncompensated system.

In the second experiment, the DC-link voltages are set to $V_1 = 55V, V_2 = 45V, V_3 = 45V, V_4 = 55V$. Figs. 20-22 depict the experimental waveforms of the output line voltage and the output current with its respective pole voltage when the feed-forward PWM methods of the sine PWM, the PWM with medium CMV, and the proposed DPWM are applied. The pole voltage waveform in Fig. 22 shows that similar to the simulation results, the implemented DPWM mode that depends on the phase load currents sets the non-commutation phase at intervals, in which its current attains the maximum or medium absolute value.

A comparison of the experimental line voltage THD (calculated up to the 100th harmonics) of the proposed feed-forward DPWM method with the feed-forward sine PWM and medium CMV PWM is illustrated in Figs. 23(a)-23(c).

The characteristics of the line voltage THD using the three PWM methods under the same conditions of DC voltages as in Figs. 16(a)–16(c) yield acceptable results in comparison with those obtained by simulation (Fig. 16). The experimental THD characteristics indicate that the proposed DPWM method under three given DC-link voltage conditions yield higher THD values than the two other PWM methods in nearly the entire region of the modulation index.

V. CONCLUSIONS

In this study, a model of switching voltages and an offset-based PWM scheme for multilevel NPC inverters under a DC voltage imbalance are proposed. In the proposed scheme, the global offset extends the maximized output voltage range in the under-modulation range and defines a draft CMV. The local offset can be flexibly modified to establish different PWM modes related to the PWM quality, such as switching loss and current ripple. A DPWM that utilizes these flexible offsets and the feedback information of the currents is proposed to reduce switching loss. The proposed PWM for switching loss reduction can be analyzed in relation to other carrier-based methods using the same switching voltage model. Simulations and experiments are conducted to confirm the validity of the proposed switching voltage modeling and the proposed DPWM control method.

ACKNOWLEDGMENT

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