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Steady-State Analysis of ZVS and NON-ZVS Full-Bridge Inverters with Asymmetrical Control for Induction Heating Applications

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Abstract

This paper presents a steady-state operation analysis of full-bridge series-resonant inverters focusing on the distorted load current due to low-quality-factor resonant circuits in induction heating and other applications. The regions of operation based on the zero-voltage switching (ZVS) and non-zero-voltage switching (NON-ZVS) operations of the asymmetrical voltage-cancellation control technique are identified. The effects of a distorted load current under a wide range of output powers are also analyzed for achieving a precise ZVS operating region. An experimental study is performed with a 1kW prototype. Simulation and experimental studies have confirmed the validity of the proposed method. An efficiency comparison between the variable frequency method and the conventional fixed-frequency method is provided.

Key words: Asymmetrical voltage-cancellation, Induction heating, Non-zero- voltage switching, Series-resonant inverter, Zero-voltage switching

I. INTRODUCTION

High-frequency resonant inverters for induction heating (IH) technologies have been widely used in industrial, automotive, pipeline and consumer applications where high efficiency, system reliability, safety, cleanliness, compactness in volumetric physical size, light weight, and performance are required [1]. The use of a higher switching frequency results in higher switching losses, resulting in a lowered efficiency. However, this switching loss can greatly be reduced by the soft-switching technique [2]-[6]. The zero-voltage switching (ZVS) technique is one of the soft-switching techniques. It is the representative feature of resonant inverters and is suitable for high-switching frequency operation. The ZVS operation avoids switching losses, reduces electromagnetic interference (EMI) and device stresses, and allows for the possibility of snubberless operation [4], [7]-[10]. Voltage-source resonant inverter topologies have received a great deal of attention because of their output power control capability under ZVS operation. Several switching techniques have been reported in high-frequency IH applications such as the pulse-frequency modulation (PFM) [11]-[13], pulse-density modulation (PDM) [14], [15], asymmetrical duty-cycle (ADC) [16], [17], phase-shift (PS) [18]-[20], and asymmetrical voltage-cancellation (AVC) [21]-[24]. In [24], the variable-frequency AVC control is used in a full-bridge resonant inverter with a low-quality-factor resonant circuit (Q_r) to identify the condition of ZVS operation by the fundamental harmonic approximation technique. However, this technique may not guarantee ZVS operation in the entire range of output power. By using the AVC technique in the case of a low Q_r resonant circuit (less than 2.5 [25]), the output current (load current) is non-sinusoidal due to a high damping factor (α) value. The

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transient response is oscillatory and exponentially damped in nature. The output current is unavoidably distorted and may result in hard-switching conditions during switching transitions at the end of the positive cycle, causing the so-called non-zero-voltage switching (NON-ZVS). Consequently, an increase in the switching losses and device stresses results in a lower efficiency.

In practice, the switching loss due to the effect of the parasitic capacitances associated with the charging and discharging of switching devices has been observed during a switching transition period. To mitigate this switching loss, the positive output current diverted from the resonant circuit should be large enough to completely discharge the parasitic capacitors and the switching frequency must be suitably increased above the resonant frequency.

The regions of ZVS and NON-ZVS operations of the full-bridge inverters for IH applications with a low Q_r resonant circuit based on the asymmetrical control technique have been identified in this paper. The influence of parasitic capacitors are taken into consideration through computer simulations and verified by experimental results. The remainder of this paper consists of six sections. The circuit configurations and operations are described in Section II. Section III presents a steady state circuit analysis. In Section IV, an analysis of the soft-switching operation is provided. The experimental setup and results are provided in Section V. Section VI concludes the work.

II. CIRCUIT CONFIGURATION AND OPERATIONS

A. Circuit Configuration

Fig. 1 shows a full-bridge series-resonant inverter circuit for induction heating applications. A voltage-source inverter consisting of four IGBTs (S_1-S_4) with antiparallel diodes (D_1-D_4) and parasitic capacitors (C_1-C_4 or C_o), is connected with a series-resonant load. To eliminate the turn-on switching loss, all of the switches (S_1-S_4) are operated at a frequency slightly higher than the resonant frequency under the ZVS condition.

B. Steady-State ZVS Operation

The gate signals for the switching devices (S_1-S_4) and typical steady-state waveforms of the output voltage and current of the inverter for ZVS and NON-ZVS operations are shown in Fig. 2. As shown in Fig. 2(a), the inverter operates with the desired ZVS operation. Figs. 2(b) and (c) show steady-state waveforms for the NON-ZVS operations. The output power P_o is adjusted by varying the shifted angle β through switch S_4. The output voltage v_o of the inverter assumes the form of a square wave while the output current i_o is lagging the output voltage by the angle θ_{io} at the end of the positive cycle of i_o. θ_{Co} is an angle defined at the completion of charging and discharging processes of C_1 and C_2, respectively. The fundamental components of the output voltage and

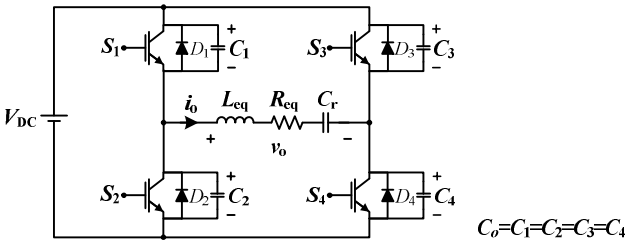

Fig. 1. Circuit configuration of full-bridge series-resonant inverter.

current are illustrated by the sinusoidal signals V_{o1} and I_{o1}, respectively. The I_{o1} signal lags the V_{o1} signal by the phase angle θ_{z1}. The modes of operation with ZVS are described in eight stages (t_0-t_4), as illustrated in Fig. 3 by the solid arrows.

Mode 1 (t_0–t'_0): The switches S_2 and S_3 are already turned off, and the switches S_1 and S_4 are still off. Negative output current flows through the parasitic capacitors C_1, C_2, C_3 and C_4. The parasitic capacitors C_2 and C_3 are completely charged by the L_{eq}-C_r resonant circuit while the parasitic capacitors C_1 and C_4 are completely discharged. At the same time, the output voltage increases from $-V_{DC}$ to $+V_{DC}$. From the Laplace transform, the output current i_o and voltage v_o during this mode are given as follows:

$$\left.\begin{aligned} i_o(t) &= \left(\frac{A1 - R_{eq}I_8}{2L_{eq}\omega_{d1}}\right)e^{-\alpha t}\sin\omega_{d1}t + I_8 e^{-\alpha t}\cos\omega_{d1}t \\ v_o(t) &= \left[\begin{aligned} &\frac{(\alpha A1 - (\omega_{d1}^2+\alpha^2)2L_{eq}I_8)(L_{eq}C_r(\omega_{d1}^2+\alpha^2)-1)}{2\omega_{d1}L_{eq}C_r(\omega_{d1}^2+\alpha^2)}e^{-\alpha t}\sin\omega_{d1}t \\ &+\frac{A1(L_{eq}C_r(\omega_{d1}^2+\alpha^2)-1)}{2L_{eq}C_r(\omega_{d1}^2+\alpha^2)}e^{-\alpha t}\cos\omega_{d1}t + \frac{A1}{2L_{eq}C_r(\omega_{d1}^2+\alpha^2)} \end{aligned}\right] + V_0 \end{aligned}\right\} \quad (1)$$

where: $\alpha = \dfrac{R_{eq}}{2L_{eq}}$, $\omega_{d1} = \sqrt{\dfrac{C_r + C_o}{L_{eq}C_rC_o} - \left(\dfrac{R_{eq}}{2L_{eq}}\right)^2}$, $I_8 = i_o(t_4)$ is the initial value of the output current i_o, and $A1 = -2V_0 - V_{C1} + V_{C2} + V_{C3} - V_{C4}$ is the total initial voltage of the capacitor in each mode when V_0 is the initial voltage of the resonant capacitor C_r. V_{C1}, V_{C2}, V_{C3}, and V_{C4} are the initial voltages of the parasitic capacitors C_1, C_2, C_3, and C_4, respectively.

Mode 2 (t'_0–t_1): At t'_0, the switches S_2 and S_3 are still off. The negative output current is diverted from the parasitic capacitors C_1 and C_4 to the antiparallel diodes D_1 and D_4. Then it reaches zero at t_1. After the switch dead time t_d, the switches S_1 and S_4 receive positive gating signals and the output voltage is equal to $+V_{DC}$. The current i_o and voltage v_o in this mode are expressed as:

$$\left.\begin{aligned} i_o(t) &= \left(\frac{A2 - R_{eq}I_1}{2L_{eq}\omega_{d2}}\right)e^{-\alpha t}\sin\omega_{d2}t + I_1 e^{-\alpha t}\cos\omega_{d2}t \\ v_o(t) &= \left[\begin{aligned} &\frac{(\alpha A2 - (\omega_{d2}^2+\alpha^2)2L_{eq}I_1)(L_{eq}C_r(\omega_{d2}^2+\alpha^2)-1)}{2\omega_{d2}L_{eq}C_r(\omega_{d2}^2+\alpha^2)}e^{-\alpha t}\sin\omega_{d2}t \\ &+\frac{A2(L_{eq}C_r(\omega_{d2}^2+\alpha^2)-1)}{2L_{eq}C_r(\omega_{d2}^2+\alpha^2)}e^{-\alpha t}\cos\omega_{d2}t + \frac{A2}{2L_{eq}C_r(\omega_{d2}^2+\alpha^2)} \end{aligned}\right] + V_0 \end{aligned}\right\} \quad (2)$$

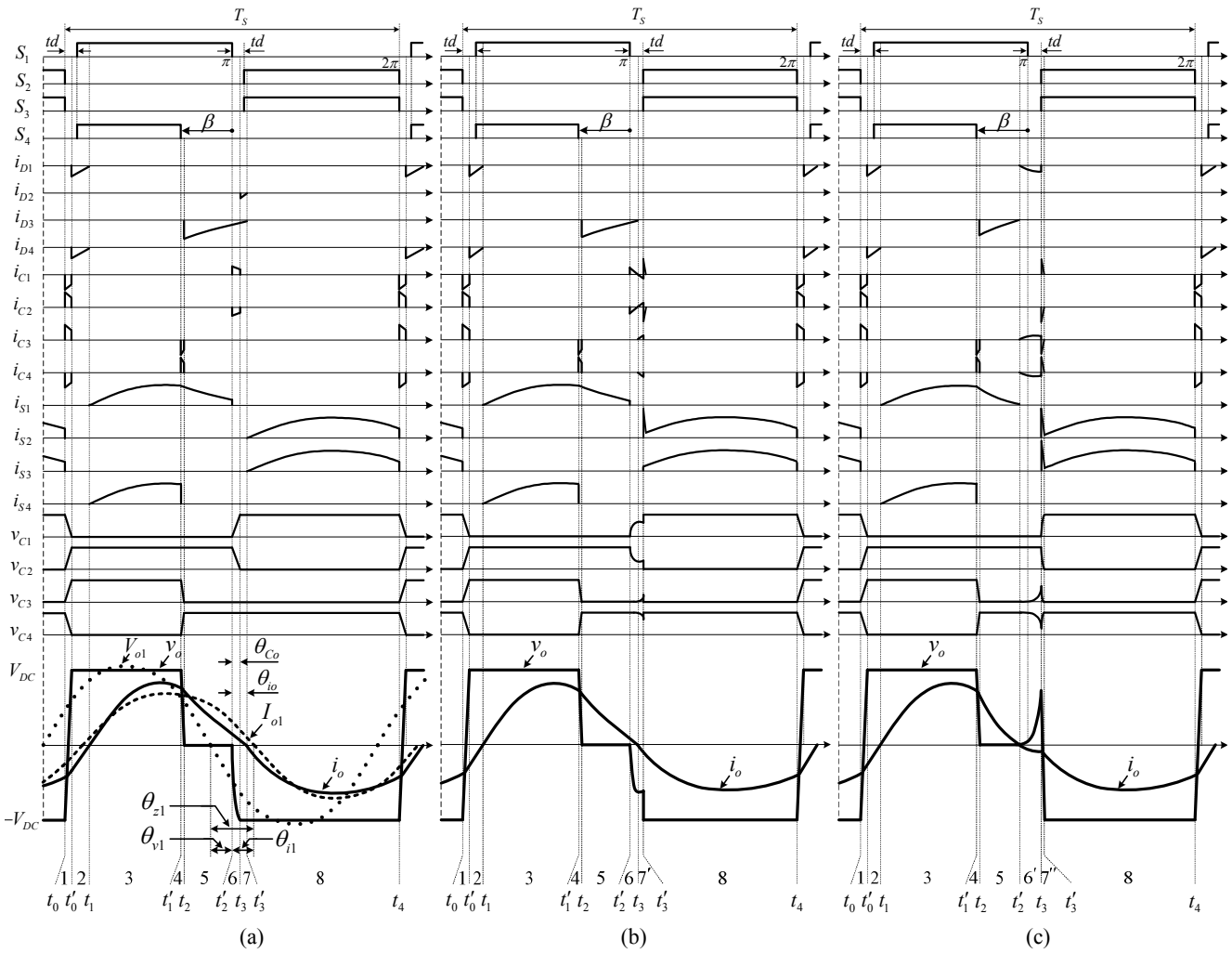

Fig. 2. The gate signals for all switches and typical steady-state waveforms of the output voltage and current. (a) Desired ZVS. (b) NON-ZVS *I*. (c) NON-ZVS *II*.

where: $I_1 = i_o(t_0'),\ A2 = 2(V_{DC} - V_0),\ \omega_{d2} = \sqrt{\frac{1}{L_{eq}C_r} - \left(\frac{R_{eq}}{2L_{eq}}\right)^2}$

Mode 3 (t_1–t'_1): At t_1, the switches S_1 and S_4 start conducting after the antiparallel diodes D_1 and D_4 are turned off, and the ZVS operation is obtained. The positive output current flows from zero until t'_1, and the output voltage is still equal to $+V_{DC}$. At this stage, the current i_o and voltage v_o in this mode are expressed as:

$$\left.\begin{aligned} i_o(t) &= \left(\frac{A3 - R_{eq}I_2}{2L_{eq}\omega_{d3}}\right)e^{-\alpha t}\sin\omega_{d3}t + I_2 e^{-\alpha t}\cos\omega_{d3}t \\ v_o(t) &= \left[\begin{aligned} &\frac{(\alpha A3 - (\omega_{d3}^2+\alpha^2)2L_{eq}I_2)(L_{eq}C_r(\omega_{d3}^2+\alpha^2)-1)}{2\omega_{d3}L_{eq}C_r(\omega_{d3}^2+\alpha^2)}e^{-\alpha t}\sin\omega_{d3}t \\ &+\frac{A3(L_{eq}C_r(\omega_{d3}^2+\alpha^2)-1)}{2L_{eq}C_r(\omega_{d3}^2+\alpha^2)}e^{-\alpha t}\cos\omega_{d3}t + \frac{A3}{2L_{eq}C_r(\omega_{d3}^2+\alpha^2)} \end{aligned}\right] + V_0 \end{aligned}\right\} (3)$$

where: $I_2 = i_o(t_1),\ A3 = 2(V_{DC} - V_0),\ \omega_{d3} = \sqrt{\frac{1}{L_{eq}C_r} - \left(\frac{R_{eq}}{2L_{eq}}\right)^2}$

Mode 4 (t'_1–t_2): At t'_1, while the switch S_1 still conducts, the switch S_4 is turned off due to the shifted angle β that is adjusted to control the output power. During this mode, the output current flows in the same direction. The parasitic capacitor C_4 is charged while the parasitic capacitor C_3 is discharged. At this stage, the output voltage decreases to zero. The current i_o and voltage v_o are expressed as:

$$\left.\begin{aligned} i_o(t) &= \left(\frac{A4 - R_{eq}I_3}{2L_{eq}\omega_{d4}}\right)e^{-\alpha t}\sin\omega_{d4}t + I_3 e^{-\alpha t}\cos\omega_{d4}t \\ v_o(t) &= \left[\begin{aligned} &\frac{(\alpha A4 - (\omega_{d4}^2+\alpha^2)2L_{eq}I_3)(L_{eq}C_r(\omega_{d4}^2+\alpha^2)-1)}{2\omega_{d4}L_{eq}C_r(\omega_{d4}^2+\alpha^2)}e^{-\alpha t}\sin\omega_{d4}t \\ &+\frac{A4(L_{eq}C_r(\omega_{d4}^2+\alpha^2)-1)}{2L_{eq}C_r(\omega_{d4}^2+\alpha^2)}e^{-\alpha t}\cos\omega_{d4}t + \frac{A4}{2L_{eq}C_r(\omega_{d4}^2+\alpha^2)} \end{aligned}\right] + V_0 \end{aligned}\right\} (4)$$

where:

$$I_3 = i_o(t_1'),\ A4 = V_{DC} - 2V_0 + V_{C3} - V_{C4},\ \omega_{d4} = \sqrt{\frac{C_r + 2C_o}{2L_{eq}C_rC_o} - \left(\frac{R_{eq}}{2L_{eq}}\right)^2}$$

Mode 5 (t_2–t'_2): At t_2, with a given value of the shifted angle β, the switch S_4 is already turned off while the switch S_1 still

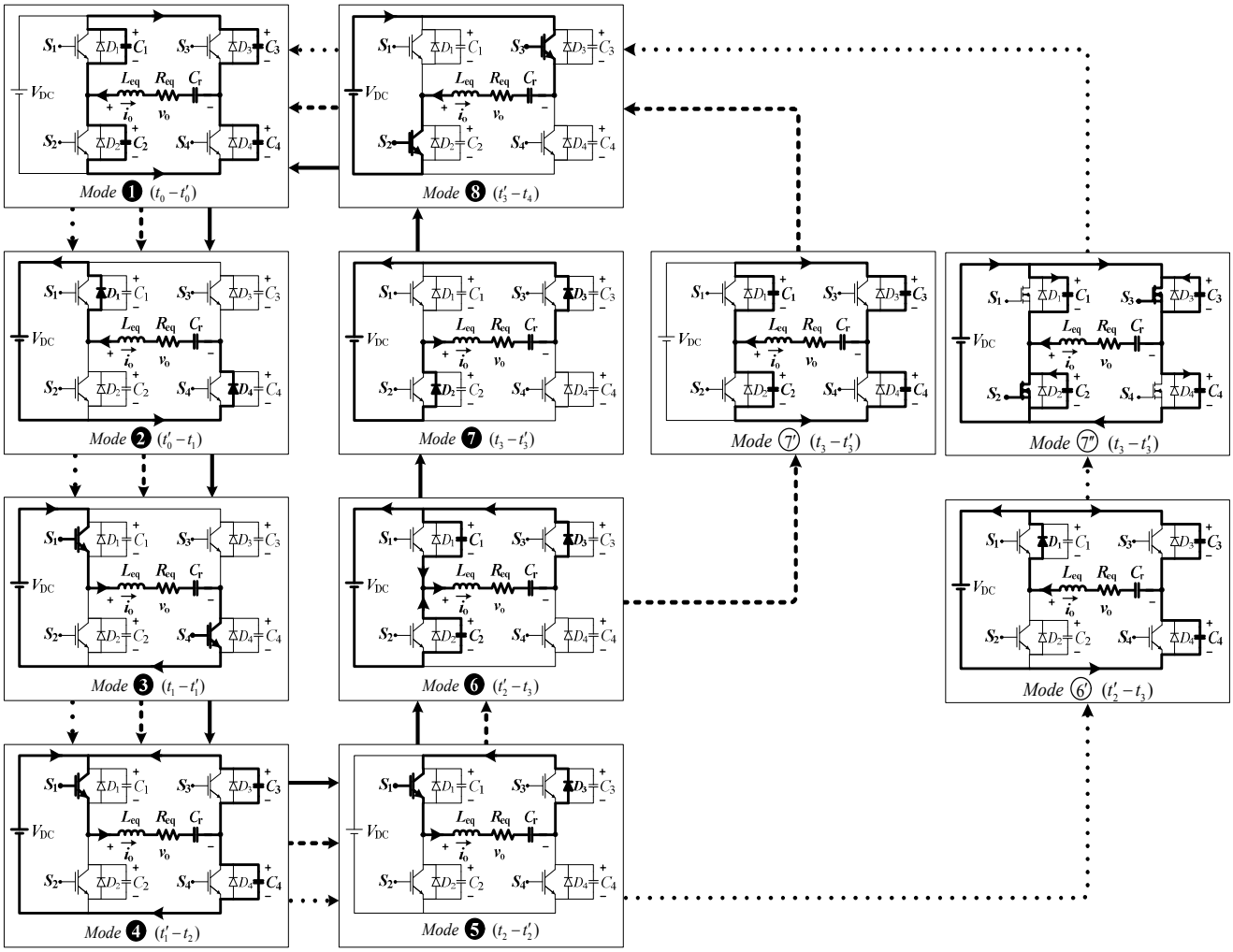

Fig. 3. Operation modes of a full-bridge resonant inverter: (a) ⟶ desired ZVS, (b) - - → NON-ZVS *I*, and (c) • • • ▶ NON-ZVS *II*.

conducts and the output current flows through the antiparallel diode D_3. During this stage, the output voltage is already zero and the positive output current is decreasing. The current i_o and voltage v_o become:

$$\left.\begin{aligned} i_o(t) &= \left(\frac{A5 - R_{eq}I_4}{2L_{eq}\omega_{d5}}\right)e^{-\alpha t}\sin\omega_{d5}t + I_4 e^{-\alpha t}\cos\omega_{d5}t \\ v_o(t) &= \left[\begin{aligned} &\frac{(\alpha A5 - (\omega_{d5}^2+\alpha^2)2L_{eq}I_4)(L_{eq}C_r(\omega_{d5}^2+\alpha^2)-1)}{2\omega_{d5}L_{eq}C_r(\omega_{d5}^2+\alpha^2)}e^{-\alpha t}\sin\omega_{d5}t \\ &+\frac{A5(L_{eq}C_r(\omega_{d5}^2+\alpha^2)-1)}{2L_{eq}C_r(\omega_{d5}^2+\alpha^2)}e^{-\alpha t}\cos\omega_{d5}t + \frac{A5}{2L_{eq}C_r(\omega_{d5}^2+\alpha^2)} \end{aligned}\right] + V_0 \end{aligned}\right\} (5)$$

where: $I_4 = i_o(t_2),\ A5 = -2V_0,\ \omega_{d5} = \sqrt{\dfrac{1}{L_{eq}C_r} - \left(\dfrac{R_{eq}}{2L_{eq}}\right)^2}$

Mode 6 (t_2'–t_3): At t_2', all of the switches are off. A part of the positive output current flows through the antiparallel diode D_3 and the parasitic capacitors C_1 and C_2. At the same time, the capacitor voltage V_{C1} increases from zero to $+V_{DC}$, whereas the capacitor voltage V_{C2} decreases from $+V_{DC}$ to zero. In this mode, the output voltage reduces from zero to $-V_{DC}$ at t_3. The current i_o and voltage v_o are:

$$\left.\begin{aligned} i_o(t) &= \left(\frac{A6 - R_{eq}I_5}{2L_{eq}\omega_{d6}}\right)e^{-\alpha t}\sin\omega_{d6}t + I_5 e^{-\alpha t}\cos\omega_{d6}t \\ v_o(t) &= \left[\begin{aligned} &\frac{(\alpha A6 - (\omega_{d6}^2+\alpha^2)2L_{eq}I_5)(L_{eq}C_r(\omega_{d6}^2+\alpha^2)-1)}{2\omega_{d6}L_{eq}C_r(\omega_{d6}^2+\alpha^2)}e^{-\alpha t}\sin\omega_{d6}t \\ &+\frac{A6(L_{eq}C_r(\omega_{d6}^2+\alpha^2)-1)}{2L_{eq}C_r(\omega_{d6}^2+\alpha^2)}e^{-\alpha t}\cos\omega_{d6}t + \frac{A6}{2L_{eq}C_r(\omega_{d6}^2+\alpha^2)} \end{aligned}\right] + V_0 \end{aligned}\right\} (6)$$

where:

$$I_5 = i_o(t_2'),\ A6 = -V_{DC} - 2V_0 + V_{C1} - V_{C2},\ \omega_{d6} = \sqrt{\frac{C_r + 2C_o}{2L_{eq}C_rC_o} - \left(\frac{R_{eq}}{2L_{eq}}\right)^2}$$

Mode 7 (t_3–t_3'): At t_3, the switch S_1 is still off during the dead time. The antiparallel diodes D_2 and D_3 naturally conduct while the positive output current decreases to zero at t_3'. At this stage, the output voltage is equal to $-V_{DC}$. The switches S_2 and S_3 receive the same positive gating signal. Therefore, the current i_o and voltage v_o in this mode are:

$$\left.\begin{aligned} i_o(t) &= \left(\frac{A7 - R_{eq}I_6}{2L_{eq}\omega_{d7}}\right)e^{-\alpha t}\sin\omega_{d7}t + I_6 e^{-\alpha t}\cos\omega_{d7}t \\ v_o(t) &= \left[\begin{aligned} &\frac{(\alpha A7 - (\omega_{d7}^2+\alpha^2)2L_{eq}I_6)(L_{eq}C_r(\omega_{d7}^2+\alpha^2)-1)}{2\omega_{d7}L_{eq}C_r(\omega_{d7}^2+\alpha^2)}e^{-\alpha t}\sin\omega_{d7}t \\ &+\frac{A7(L_{eq}C_r(\omega_{d7}^2+\alpha^2)-1)}{2L_{eq}C_r(\omega_{d7}^2+\alpha^2)}e^{-\alpha t}\cos\omega_{d7}t + \frac{A7}{2L_{eq}C_r(\omega_{d7}^2+\alpha^2)} \end{aligned}\right] + V_0 \end{aligned}\right\} \quad (7)$$

where: $I_6 = i_o(t_3),\ A7 = -2(V_{DC} - V_0),\ \omega_{d7} = \sqrt{\frac{1}{L_{eq}C_r} - \left(\frac{R_{eq}}{2L_{eq}}\right)^2}$

Mode 8 (t'_3–t_4): At t'_3, as soon as the antiparallel diodes D_2 and D_3 are turned off, the switches S_2 and S_3 conduct under ZVS operation. During this stage, the output current and voltage are both negative and a full cycle of waveform is achieved. This can be expressed by:

$$\left.\begin{aligned} i_o(t) &= \left(\frac{A8 - R_{eq}I_7}{2L_{eq}\omega_{d8}}\right)e^{-\alpha t}\sin\omega_{d8}t + I_7 e^{-\alpha t}\cos\omega_{d8}t \\ v_o(t) &= \left[\begin{aligned} &\frac{(\alpha A8 - (\omega_{d8}^2+\alpha^2)2L_{eq}I_7)(L_{eq}C_r(\omega_{d8}^2+\alpha^2)-1)}{2\omega_{d8}L_{eq}C_r(\omega_{d8}^2+\alpha^2)}e^{-\alpha t}\sin\omega_{d8}t \\ &+\frac{A8(L_{eq}C_r(\omega_{d8}^2+\alpha^2)-1)}{2L_{eq}C_r(\omega_{d8}^2+\alpha^2)}e^{-\alpha t}\cos\omega_{d8}t + \frac{A8}{2L_{eq}C_r(\omega_{d8}^2+\alpha^2)} \end{aligned}\right] + V_0 \end{aligned}\right\} \quad (8)$$

where: $I_7 = i_o(t'_3),\ A8 = -2(V_{DC} - V_0),\ \omega_{d8} = \sqrt{\frac{1}{L_{eq}C_r} - \left(\frac{R_{eq}}{2L_{eq}}\right)^2}$

C. NON-ZVS Operation

Two NON-ZVS operations have been observed as illustrated in Fig. 3. The first one emanated from an increase in the shifted angle β with the aim of reducing the output power without varying the switching frequency f_s. The first category of NON-ZVS operations (NON-ZVS *I*) is indicated by the dashed arrows where the previously described operation of mode 7 is replaced by mode 7′. Mode 6 begins after the gate signal of S_1 is removed at t'_2, as depicted in Fig. 2(b). The positive output current flows through the circuit formed by C_1, C_2, D_3, and the DC input voltage source. During this interval, the capacitor voltage V_{C1} increases whereas the capacitor voltage V_{C2} decreases. The output voltage becomes negative in this mode. At the beginning of mode 7′, after the antiparallel diode D_3 is turned off at t_3 with no gate signals of S_2 and S_3, the output current becomes negative and flows through the parasitic capacitors C_1, C_2, C_3 and C_4. Therefore, the voltages across the switches S_2 and S_3 increase. At t'_3, the switches S_2 and S_3 start conducting under the NON-ZVS. The parasitic capacitors C_1 and C_2 experience an instantaneous voltage change. This results in high current spikes in the switches S_1 and S_2. In this case, the modes of operation are sequenced as ❶❷❸❹❺❻⑦❽.

The second category of NON-ZVS operations (NON-ZVS *II*) is indicated by the dotted arrows in Fig. 3. It can also be divided into eight stages as ❶❷❸❹❺⑥′⑦″❽. The original operations of modes 6 and 7 in the ZVS operation are changed to modes 6′ and 7″, respectively. The operation in mode 6′ begins when the positive output current becomes zero at t'_2 before the end of the gate signal of S_1, depicted in Fig. 2(c). The negative output current flows through the antiparallel diode D_1 and the parasitic capacitors C_3 and C_4. During this mode, the capacitor voltage V_{C3} increases whereas the capacitor voltage V_{C4} decreases, adding up to a high value for the output voltage depending on the operating frequency. At the same time, the capacitor voltages V_{C1} and V_{C2} remain unchanged at zero and $+V_{DC}$, respectively. Mode 7″ begins at t_3. The switches S_2 and S_3 start conducting instantaneously under the NON-ZVS operation. Since the capacitor voltage V_{C1} is initially zero, this creates a short-circuit path of the input voltage source through the switch S_2. All of the parasitic capacitors suffer from a sudden voltage change that results in current spikes in the capacitors (C_1-C_4) and the switches S_2 and S_3 for a short interval. Such an operation reduces the inverter efficiency due to the high turn-on switching loss and it causes device stress, which may destroy all of the switches.

Therefore, for the case of a low Q_r resonant circuit, the damping frequency ω_d of the series-resonant circuit is less than the resonant angular frequency ω_r due to a high damping factor α. Two NON-ZVS operations on the switches S_2 and S_3 are likely to be encountered if the inverter is operated at an unsuitable switching frequency.

III. STEADY STATE CIRCUIT ANALYSIS

The induction heating load can be modeled as an equivalent resistor (R_{eq}) and inductor (L_{eq}). The resonant circuit is formed by adding a resonant capacitor (C_r), as shown in Fig. 1. The load quality factor of the resonant circuit is defined as:

$$Q_r = \frac{2\pi f_r L_{eq}}{R_{eq}} = \frac{1}{2\pi f_r R_{eq} C_r} \quad (9)$$

where f_r is the resonant frequency, and $f_r = 1/2\pi\sqrt{L_{eq}C_r}$.

A steady-state analysis of the series-resonant circuit is based on the equivalent parameters and typical waveforms under the ZVS operation as shown in Fig. 1 and Fig. 2(a), respectively. To simplify the analysis, the conventional assumptions are made for the analysis in this section as follows.

1) The converter elements are ideal.
2) The effect of the ripples from the DC input voltage is neglected.
3) The parasitic inductance and capacitance in the switches are neglected.

With the stated assumption, the magnitude of the impedance $\hat{Z}_{eq}$ of the series-resonant circuit can be obtained as:

$$\hat{Z}_{eq} = R_{eq}\sqrt{1+Q_r^2\left(hf_n-\frac{1}{hf_n}\right)^2} \tag{10}$$

where h is the order of harmonic components, and f_n is the normalized frequency (f_s/f_r).

The impedance phase angle of the harmonic components is given by:

$$\theta_{zh} = \tan^{-1}\left[Q_r\left(hf_n-\frac{1}{hf_n}\right)\right] \tag{11}$$

The output voltage is given by:

$$v_o(t)=\sum_{h=0}^{\infty}\hat{V}_{oh}\sin(h\omega t+\theta_{vh}) \tag{12}$$

The amplitude of the harmonic components of the output voltage can be written by means of the Fourier series as:

$$\hat{V}_{oh}=\begin{cases}\frac{V_{DC}}{h\pi}\sqrt{10+6\cos h\beta} & ;h=1,3,5,7,...\\ \frac{V_{DC}}{h\pi}\sqrt{2-2\cos h\beta} & ;h=2,4,6,8,...\end{cases} \tag{13}$$

where β is the shifted angle of the switch S_4 with a value from 0º to 180º, and V_{DC} is the DC bus voltage. The angle θ_{vh} between the output voltage v_o and its harmonic voltage (V_{oh}) can be determined by:

$$\theta_{vh}=\begin{cases}\tan^{-1}\frac{\sin h\beta}{3+\cos h\beta} & ;h=1,3,5,7,...\\ \tan^{-1}\frac{\sin h\beta}{\cos h\beta-1} & ;h=2,4,6,8,...\end{cases} \tag{14}$$

The output current can also be written by:

$$i_o(t)=\sum_{h=0}^{\infty}\hat{I}_{oh}\sin(h\omega t-\theta_{ih}) \tag{15}$$

where the angle θ_{ih} is the phase difference between the output voltage and the impedance phase angle ($\theta_{ih}=\theta_{vh}-\theta_{zh}$). The amplitude of the harmonic components of the output current is given by:

$$\hat{I}_{oh} = \frac{\hat{V}_{oh}}{R_{eq}\sqrt{1+Q_r^2\left(hf_n-\frac{1}{hf_n}\right)^2}} \tag{16}$$

Note that if the load quality factor is sufficiently high (more than 2.5), the output current i_o flowing through the series-resonant circuit assumes the form of a sinusoidal wave. In addition, the angle θ_{io} in Fig. 2(a) can be reasonably approximated by the phase difference θ_{i1}.

From (16), the average output power P_o is given as:

$$P_o \simeq \sum_{h=0}^{\infty} I_{oh,rms}^2\cdot R_{eq} \simeq \sum_{h=0}^{\infty}\frac{\hat{V}_{oh}^2}{2R_{eq}\left(1+Q_r^2\left(hf_n-\frac{1}{hf_n}\right)^2\right)} \tag{17}$$

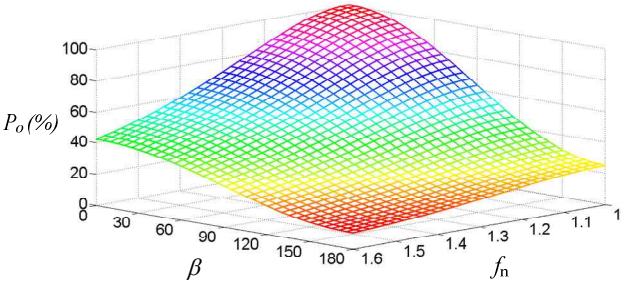

Fig. 4. The relationship of percent output power, β, and f_n.

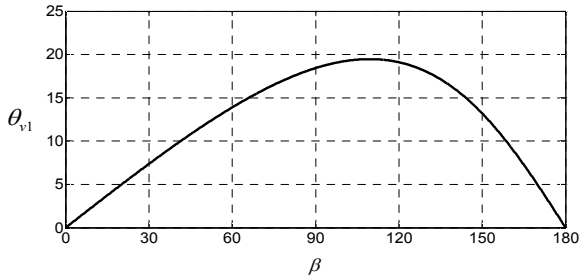

Fig. 5. The angle θ_{v1} as a function of shifted angle β.

The maximum value of the output power in (17) occurs at f_n = 1 and β = 0. Clearly, if the normalized frequency f_n and β are increased, the output power is reduced, as shown in Fig. 4 (i.e., an increase of β will result in a reduction of the output power). However, the minimum output power is limited to 25% of the maximum output power at β =180º since the output voltage control is through an adjustment of the positive cycle and the minimum achievable output voltage is at 50% of its rated value [21].

IV. Analysis of the Soft-Switching Operation

A necessary requirement for the ZVS operation of a full-bridge resonant inverter with the asymmetrical voltage-cancellation control technique is that the applied voltage across the switches must be zero during the turn-on operation. Although, the switching frequency of the series-resonant inverter is higher than the resonant frequency, the NON-ZVS operations may occur due to an increase in the shifted angle β, resulting in a variation of the angle θ_{v1}, as shown in Fig. 5. From Fig. 2(a), neglecting the parasitic capacitances, the ZVS condition requires that the angle θ_{io} must be greater than zero. This means that the positive output current waveforms become zero after the end of the gate signal S_1 (i.e., the antiparallel diodes D_2 and D_3 provide a path for the energy stored in the resonant circuit that must be conducted at t'_2).

In practice, the inverter is operated at high frequencies and the effects of the parasitic capacitors can be significant. They can alter the predetermined ZVS operation during a switching transition at the end of the positive cycle of i_o. The discharging processes of the parasitic capacitor C_2 must be

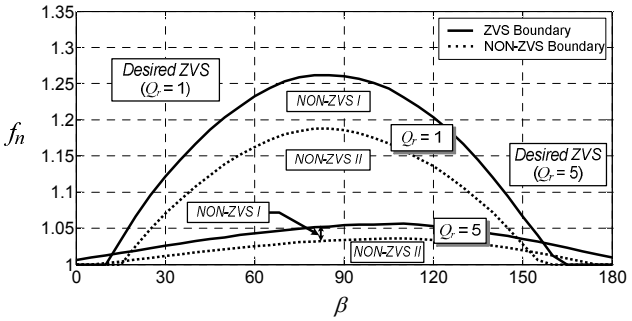

Fig. 6. Regions of ZVS and NON-ZVS operations in terms of f_n.

complete before the output current reaches zero (i.e., the output current should be large enough to ensure the ZVS condition). Therefore, the output current continues to flow through the antiparallel diodes D_2 and D_3. The critical angle of the parasitic capacitors is calculated by:

$$\theta_{Co,cri} = \frac{4\pi f_s C_o V_{DC}}{i_o(t)\big|_{t=\pi}} \tag{18}$$

where C_o is the parasitic capacitor of the switch, and $i_o(t)\big|_{t=\pi}$ is the output current at 180º.

The angle $\theta_{Co,cri}$ may be used to define a proper dead time interval. The critical ZVS boundary of operation is obtained by setting $\theta_{io} = \theta_{Co,cri} = \theta_{td}$ in (15) where θ_{td} is an angle of the dead time t_d. The critical ZVS boundary under the effect of C_o is obtained as indicated by the solid line while neglecting C_o as indicated by the dotted line in Fig. 6. If the load quality factor is high, for example Q_r = 5, the boundary line is rather flat with f_n around 1.06 at 110º of the shifted angle β. On the other hand, at Q_r = 1, the highest boundary value of f_n will shift to around 80º of the shifted angle β. Therefore, the regions of ZVS and the two NON-ZVS operations can be identified in terms of f_n as described in Section II. Again, the dotted line is the boundary between the NON-ZVS *I* and the NON-ZVS *II* operations (where θ_{io} = 0) whereas the solid line is the boundary between the desired ZVS and the NON-ZVS *I* operations. This implies that a switching frequency higher than the solid line will ensure the ZVS operation. If the shifted angle β is adjusted to 60º, f_n must be more than 1.24 to guarantee the ZVS operation. In addition, the conventional AVC control with fixed frequency control requires the inverter to operate above the resonant frequency (i.e. $f_s > f_r$) and the highest boundary value of f_n, specifically $f_n > 1.26$ for this case, at all times.

V. Experimental Setup and Results

A. Experimental Setup

A hardware prototype is created where an induction cooker is used to illustrate the proposed analysis on the low Q_r resonant circuit. The system controller is an STM32F4 discovery board. To avoid acoustic noise from the induction coil and the cooking vessel, the resonant frequency must be over 20 kHz. The material used in the cooking vessel is essential in terms of efficiency. The cooking vessel is an off-the-shelf low-cost vessel made of stainless steel that measures 235 mm in diameter and 75 mm in height. The bottom and wall thicknesses are 1.4 mm and 0.8 mm, respectively.

TABLE I
Inverter Specifications and Circuit Parameters

Symbol	Quantity	Value
V_{DC}	DC input voltage	135 V
f_r	Resonant frequency	33 kHz
f_s	Switching frequency	33.75-45.5 kHz
C_r	Resonant capacitance	300 nF
L_{eq}	Equivalent inductance	77 µH
R_{eq}	Equivalent resistance	14 Ω
S_1 - S_4	Switches	IRG4PC50UD

The induction coil is a 29-turn flat spiral made of a litz wire consisting of 35 strands of 26 SWG wire to reduce the skin effect losses and the consequent increase of heat in the coil. The maximum coil current is approximately 12 A rms. A resonant capacitor C_r of 300 nF, 1000 V has been selected to provide the resonant frequency at 33 kHz, and the quality factor Q_r at resonance is approximately one. Note that the resonant capacitor needs to withstand the peak voltage, which may be greater than the DC input voltage because of voltage magnification due to the circuit quality factor.

The inverter specifications and circuit parameters are given in Table I. The dead time interval t_d is chosen as 320 ns based on the manufacturer's data sheet. For the complete ZVS condition, the angle θ_{io} must be higher than the angle θ_{td}, as shown in Fig. 2(a). As mentioned before, an increase of the shifted angle β will cause a reduction of the angle θ_{io}. In this experiment, the angle θ_{io} is set at 7º by controlling the switching frequency. In the worst case scenario, where the shifted angle β is around 80º, the switching frequency must increase to 45.5 kHz (f_n = 1.37) so that the angle θ_{io} becomes 7º (425 ns). Thus, the switching frequency of the inverter is varied between 33.75 kHz and 45.5 kHz to assure operation in the desired ZVS region as shown in Fig. 6.

B. Simulation and Experimental Results

A computer simulation is performed to illustrate the proposed boundaries of the ZVS and NON-ZVS operations using the inverter specifications and circuit parameters from Table I. To demonstrate the inverter operation in the ZVS, critical ZVS, NON-ZVS *I*, and NON-ZVS *II* regions, the corresponding switching frequencies are set to 45.5, 40.5, 39.5 and 36 kHz, respectively. In addition, the shifted angle β is initially set at 80º.

The steady-state phase plane trajectories of the current and voltage of the inverter (i_o and v_o) and the switches (i_{S2} and

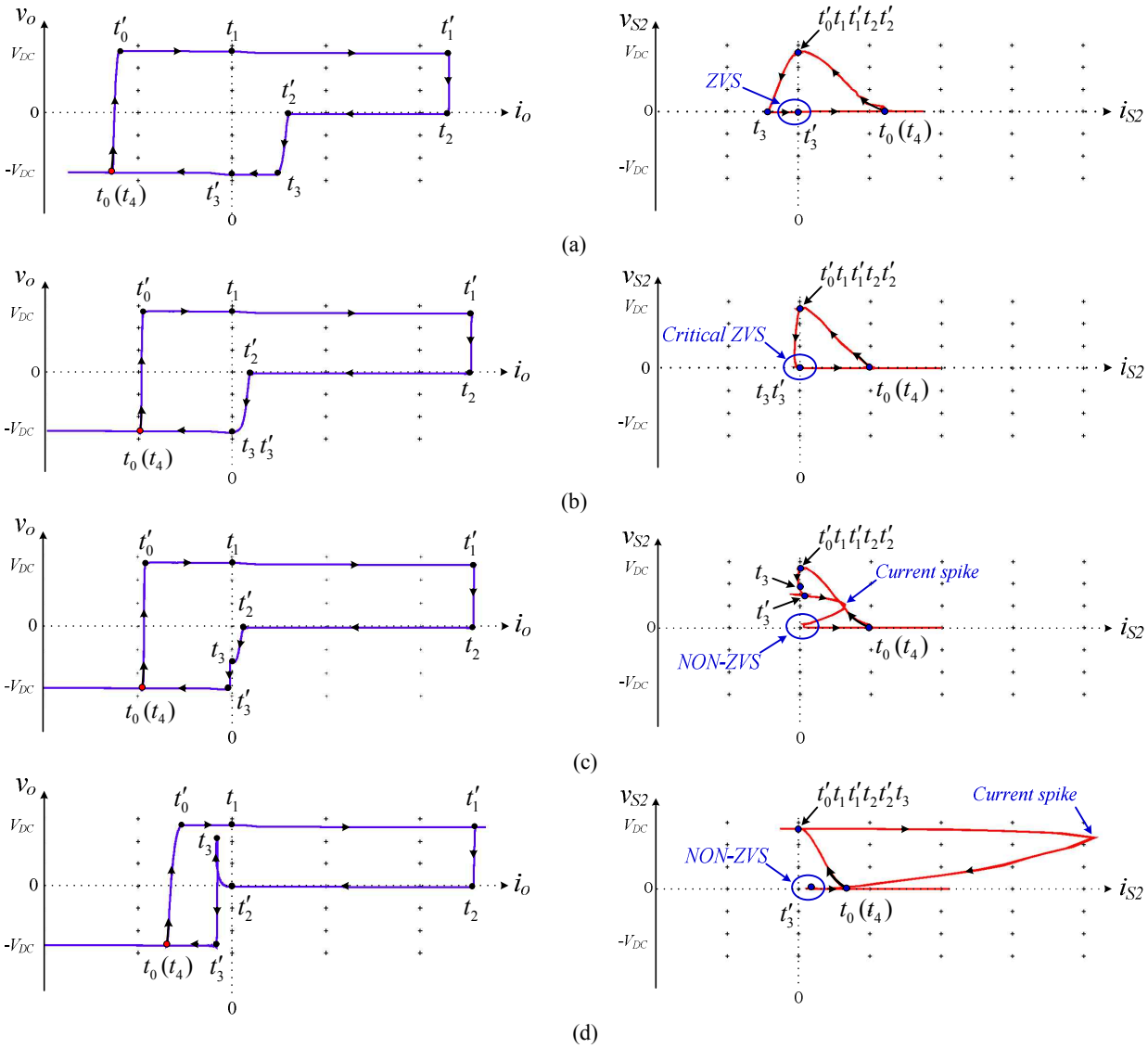

Fig. 7. Phase-plane trajectories of the current and voltage of the inverter and the switch S_2. (a) Desired ZVS. (b) Critical ZVS. (c) NON-ZVS *I*. (d) NON-ZVS *II*.

v_{S2}) for the desired ZVS, critical ZVS, and two NON-ZVS operations are shown in Fig. 7. In Fig. 7(a), the switch current i_{S2} is negative while the switch voltage v_{S2} decreases from $+V_{DC}$ to zero at t_3. The negative current i_{S2} flows through the diode D_2 then reaches zero at t'_3, and ZVS operation is achieved. Under the critical ZVS operation, it can be seen that the switch voltage v_{S2}, indicated in Fig. 7(b), decreases from $+V_{DC}$ to zero while the small negative value of the switch current i_{S2} also flows through the capacitor C_2. With an increase in the shifted angle β to reduce the output power, the angle θ_{io} decreases and becomes less than the angle θ_{td}. The inverter operates in the NON-ZVS *I* region as indicated in Fig. 7(c). The negative switch current i_{S2} crosses zero and becomes positive while the switch voltage v_{S2} is still positive. This causes a current spike in the switch S_2 during the turn-on transition. Although this current spike is not likely to damage the switch, the inverter's efficiency is sacrificed. Fig. 7(d)

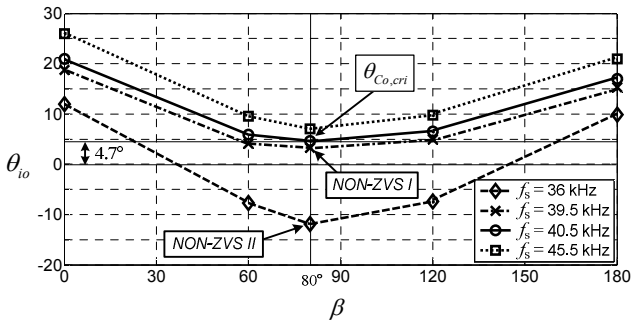

Fig. 8. Relationship between the angle θ_{io} and the shifted angle β at various switching frequencies f_s.

shows the phase plane trajectory under the operation of the NON-ZVS *II*. At t'_2, the output current i_o is negative flowing through the diode D_1, before the switch S_1 is turned off. The output voltage v_o is exposed to the increasing voltage across

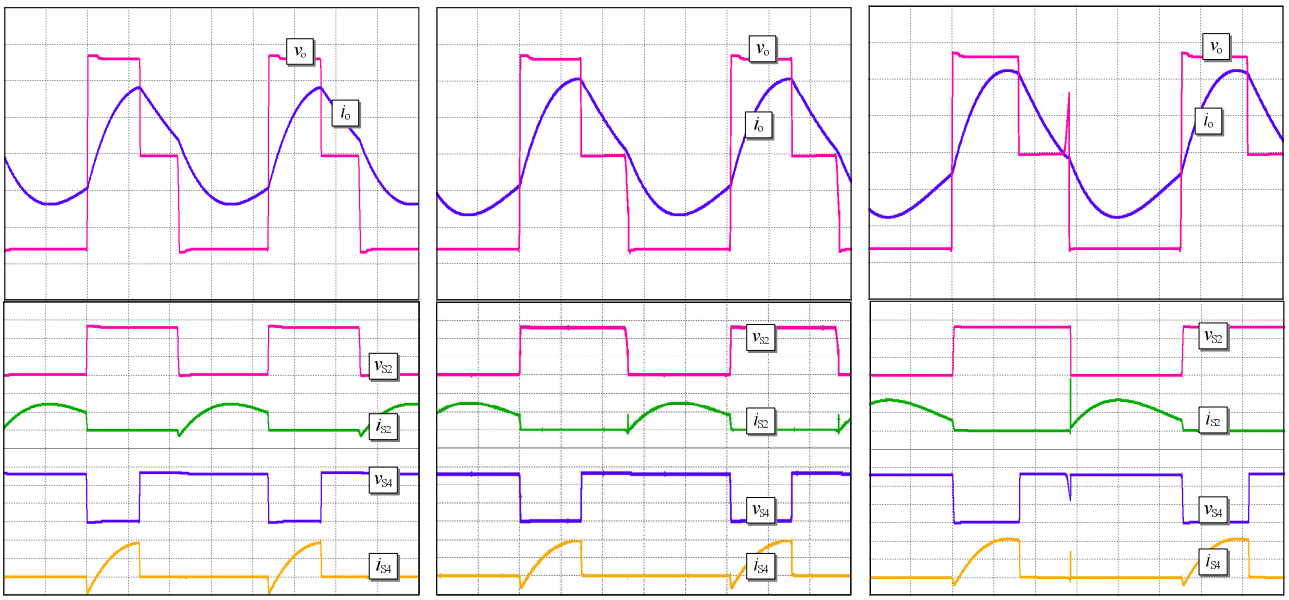

Fig. 9. Simulation waveforms of v_o, i_o, v_{S2}, i_{S2}, v_{S4} and i_{S4} at β = 80º for: (a) Desired ZVS region with f_s = 45.5 kHz. (b) NON-ZVS *I* region with f_s = 39.5 kHz. (c) NON-ZVS *II* region with f_s = 36 kHz. (v_o: 50V/div, i_o: 5A/div,v_{S2}: 50V/div, i_{S2}: 5A/div, v_{S4}: 50V/div, i_{S4}: 5A/div and Time: 5us/div.).

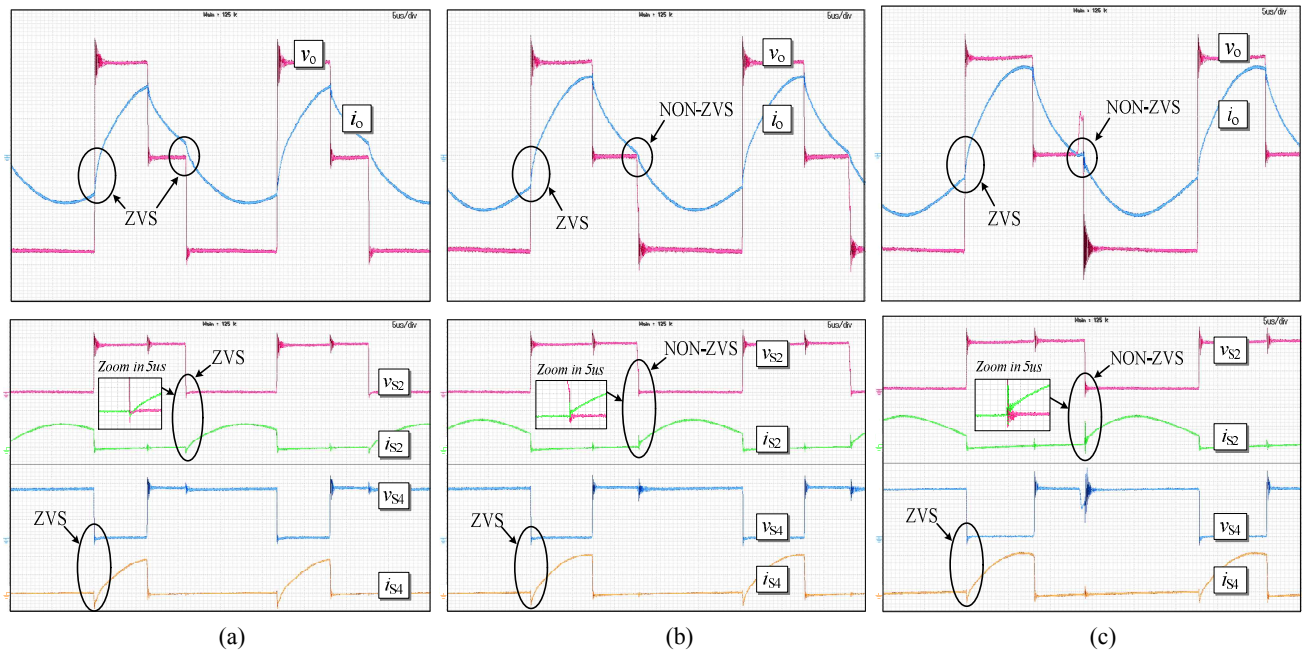

Fig. 10. Experimental waveforms of v_o, i_o, v_{S2}, i_{S2}, v_{S4} and i_{S4} at β = 80º for: (a) Desired ZVS region with f_s = 45.5 kHz. (b) NON-ZVS *I* region with f_s = 39.5 kHz. (c) NON-ZVS *II* region with f_s = 36 kHz. (v_o: 50V/div, i_o: 5A/div,v_{S2}: 50V/div, i_{S2}: 5A/div, v_{S4}: 50V/div, i_{S4}: 5A/div and Time: 5us/div.).

the capacitor C_3, causing a current spike several times the normal current on the switches S_2 and S_3. Clearly, the current spike in the NON-ZVS *II* operation can cause damage to the switches.

The relationship between the angle θ_{io} and the shifted angle β at various switching frequencies f_s is shown in Fig. 8. The output power regulation through the shifted angle β has an obvious effect on the angle θ_{io}. An unsuitable switching frequency can lead to ZVS or NON-ZVS operations. For instance, if the output power is set to the desired value at β = 80º. The switching frequency f_s at 45.5 kHz yields an operation in the ZVS region because the angle θ_{io} is greater than the angle $\theta_{Co,cri}$ at 4.7º (where f_s = 40.5 kHz). On the other hand, a switching frequency f_s at 39.5 kHz causes the

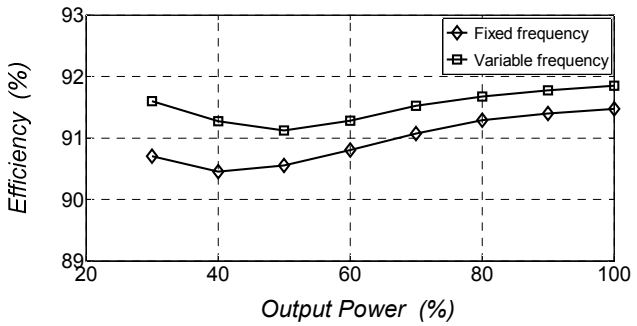

Fig. 11. Efficiency comparison between the variable frequency and the conventional fixed-frequency methods.

angle θ_{io} to become less than the angle $\theta_{Co,cri}$. This is an operation in the NON-ZVS *I* region. Note that if the angle θ_{io} is further decreased, through a switching frequency reduction, the inverter is operated in the NON-ZVS *II* region. In other words, the angle θ_{io} becomes negative as indicated by the dashed line.

The simulation and experimental results under the desired ZVS and two NON-ZVS operations are shown in Figs. 9 and 10. The results under the ZVS operation are shown in Figs. 9(a) and 10(a). The switching frequency of the inverter is then adjusted (45.5 kHz), according to Fig. 6, where the angle θ_{io} becomes 7º over the angle $\theta_{Co,cri}$ to assure operation in the desired ZVS region. The results under the operation of the NON-ZVS *I* are shown in Figs. 9(b) and 10(b) where the angle θ_{io} is at 3.2º to allow for operation in the NON-ZVS *I* region. In addition, the NON-ZVS *II* results are shown in Figs. 9(c) and 10(c) where the angle θ_{io} is -11º. For the NON-ZVS operations, as observed in the results, the switches S_1 and S_4 are turned on at zero voltage, but the switches S_2 and S_3 are turned on at non-zero voltage due to the load parameters and unsuitable switching frequency. This results in high switching losses in switches S_2 and S_3 which in turn reduces the inverter efficiency. In the case of the NON-ZVS *II*, the current spikes at the turn-on switching period may cause damages to the switches S_2 and S_3.

C. Efficiency

An efficiency comparison between the proposed variable frequency and conventional fixed-frequency methods for AVC schemes are provided as shown in Fig. 11. As mentioned earlier, the switching frequency of the fixed-frequency method is set to 45.5 kHz while the switching frequency of the variable frequency method is in the range of 33.75-45.5 kHz. Clearly, the variable frequency control yields a higher efficiency, especially in the low output power range, since the switching frequency is allowed to decrease. The benefits of knowing the regions of operation are the insight into the optimal operation as a systematic approach while maintaining the ZVS operation throughout all of the output power levels.

VI. CONCLUSION

This paper addresses the issue of the regions of ZVS and NON-ZVS operations of a full-bridge inverter focusing on the distorted load current due to a low-quality-factor resonant circuit in induction heating and other applications. The steady-state circuit analysis is based on the asymmetrical control scheme and a Fourier series analysis. The operations of ZVS and NON-ZVS are analyzed in terms of the typical waveform phenomenon of the inverter and the analytical equations in the operation modes. Under the ZVS operating criteria, the parasitic capacitances must also be taken into account. The presented circuit configurations and operations provide insight into the selection of optimal operation with the soft-switching technique to achieve a high efficiency. In addition, this method can be applied to other applications.

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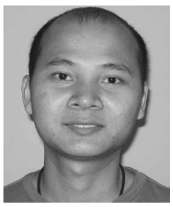

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