LED Driver with TRIAC Dimming Control by Variable Switched Capacitance for Power Regulation

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Abstract

A TRIAC dimming LED driver that can control the brightness of LED arrays for a wide range of source voltage variations is proposed in this paper. Unlike conventional PWM LED drivers, the proposed LED driver adopts a TRIAC switch, which inherently guarantees zero current switching and has been proven to be quite reliable over its long lifetime. Unlike previous TRIAC type LED drivers, the proposed LED driver is composed of an LC input filter and a variable switched capacitance, which is modulated by the TRIAC turn-on timing. Thus, the LED power regulation and dimming control, which are done by a volume resistor in the same way as the conventional TRIAC dimmers, can be simultaneously performed by the TRIAC control circuit. Because the proposed LED driver has high efficiency and a long lifetime with a high power factor (PF) and low total harmonic distortion (THD) characteristics, it is quite adequate for industrial lighting applications such as streets, factories, parking garages, and emergency stairs. A simple step-down capacitive power supply circuit composed of passive components only is also proposed, which is quite useful for providing DC power from an AC source without a bulky and heavy transformer. A prototype 60 W LED driver was implemented by the proposed design procedure and verified by simulation and experimental results, where the efficiency, PF, and THD are 92%, 0.94, and 6.3%, respectively. The LED power variation is well mitigated to below ± 2% for 190 V < V_s < 250 V by using the proposed simple control circuit.

Key words: Controlled current mirror, DC power supply circuit, TRIAC dimming control, Variable switched capacitance

I. INTRODUCTION

Light emitting diodes (LEDs) are gradually replacing conventional fluorescent lamps and incandescent lights due to their higher efficacy and longer lifespans [1]-[8]. LED drivers provide regulated or controlled currents to LEDs for constant lighting or dimming, regardless of source voltage changes and temperature variations. Switch mode power supply (SMPS)-type LED drivers with pulse width modulation (PWM) switching, in the hundreds of kHz range, are widely used due to their compact filter size and fair total harmonic distortion (THD) characteristics. However, the SMPS-type LED drivers suffer from large switching losses and shorter lifespans than the LED itself due to the high junction temperature of the main switches [9]-[20]. As an alternative solution, passive-type LED drivers are preferred due to their very high efficiency and extremely long lifespan [21]-[24]. However, the inherent drawbacks of the passive-type LED drivers include their lack of current regulation capability and a relatively large filter size, where this filter size problem can be mitigated by virtue of a reduced heat sink and a compact coil design. Therefore, the passive-type LED drivers may not be a good solution for the applications requiring a constant LED current regardless of source voltage variations.

LED dimming is widely used. It is generally achieved with by PWM switches [25]-[28] or TRIAC switches [29]-[32]. LED dimmers composed of a TRIAC and a DIAC with a variable resistor [29]-[32] have many merits such as a simple structure, high reliability, low cost, and high efficiency. However, these conventional TRIAC dimming LED drivers generally have poor THD characteristics because they are directly connected to the primary side of the source line. Though their power factor (PF) can be mitigated by using appropriate power converters [29]-[31], this type of dimmer
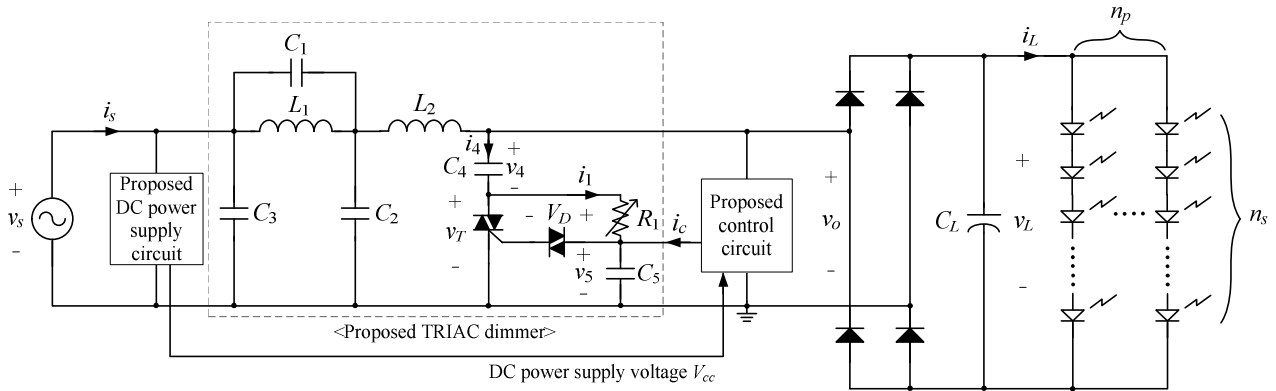
Fig. 1. Overall circuit diagram of the proposed TRIAC dimming LED driver.

is not adequate for high power LED applications due to THD and PF problems.

In this paper, a novel TRIAC dimming LED driver with a passive input filter is proposed, as shown in Fig. 1. This LED driver is based on the LC^3 passive-type LED driver configuration [24] to achieve a high efficiency and an extremely long lifespan. A dynamically variable switched capacitance is adopted to modulate the TRIAC turn-on timing so that the LED power can be controlled. Unlike the SMPS-type LED drivers, the proposed LED driver uses a TRIAC, which is a proven and quite robust device in home appliances, that inherently guarantees zero current switching (ZCS) with no additional circuits. The LED dimming is done by a volume resistor, which is similar to conventional manual TRIAC dimmers [29]-[32]. The validity of the proposed LED driver design is verified by simulation and experimental results. They show a successful regulation of LED power, and meet PF and THD standards over a wide range of source voltages.

II. ANALYSIS OF THE PROPOSED TRIAC DIMMING LED DRIVER

A. Operating Principle of the Main Power Circuit in the Steady State

The power circuit of the proposed LED driver, as shown in Fig. 1, is derived from the temperature-robust LC^3 LED driver [24], which is a novel passive-type LED driver, that satisfies PF and THD regulations. In order to provide the power control function with the LED driver, a TRIAC switch with a DIAC is inserted in series with C_4 to vary the connecting time portion, which results in a variation of the equivalent capacitance, unlike with conventional variable capacitances [33]-[36]. An additional inductor L_2 is newly introduced in the proposed LED driver to prevent the TRIAC from having a large inrush current when it is turned on. Note that n_s and n_p are the numbers of LEDs in series and parallel, respectively. In this paper, all of the circuit components are assumed to be ideal unless otherwise specified.
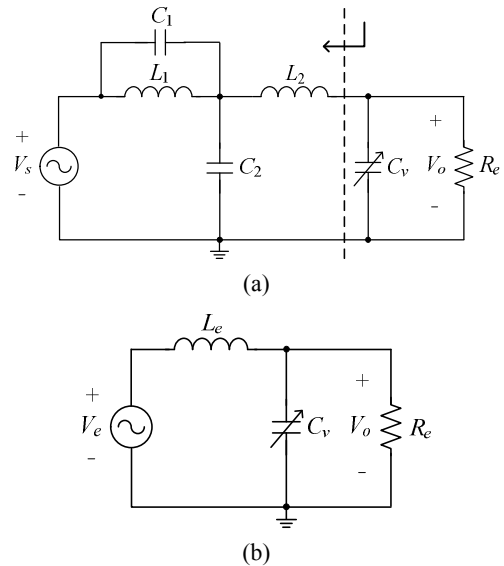

(a)

(b)

Fig. 2. A simplified static circuit of the proposed LED driver, neglecting harmonic components. (a) Simplified equivalent circuit of the proposed LED driver. (b) Further simplified circuit of (a).

As shown in Fig. 2(a), the simplified equivalent main power circuit of the proposed LED driver can be obtained by regarding the switched capacitor circuit of C_4 and the TRIAC as an equivalent variable capacitor C_v and by simplifying the diode rectifier and DC load circuit as an equivalent resistor [23]-[24], [37]-[38] as follows:

$$R_e \cong \alpha^2 R_L \quad \because R_L = V_L / I_L \quad \alpha \cong 2\sqrt{2} / \pi \cong 0.90 \text{ , (1)}$$

where α is the DC to AC voltage conversion ratio when a bridge diode is converted to an equivalent auto-transformer [39]-[42].

In this section, the high-order switching harmonics are neglected from discussions and only the fundamental components of the voltages and currents are considered for simplification.

By applying Thevenin's theorem to the left part of the circuit in Fig. 2(a) in the steady state at the source angular frequency ω_s, the proposed LED circuit can be converted to
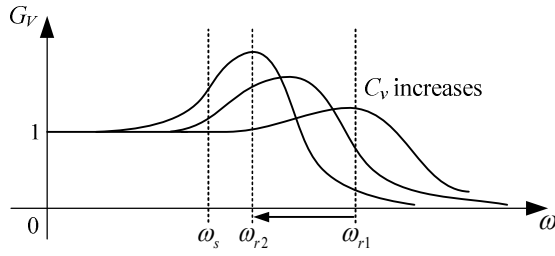
Fig. 3. The LED power regulation principle by variable switched capacitance.

that shown in Fig. 2(b), since C_1 and C_2 are small. Thus, V_e and L_e are found as follows:

$$V_e = \frac{V_s}{1 - \omega_s^2 L_p C_2}, \quad L_e = \frac{L_p}{1 - \omega_s^2 L_p C_2} + L_2 \quad (2a)$$

$$\because L_p = \frac{L_1}{1 - \omega_s^2 L_1 C_1} \quad . \quad (2b)$$

Therefore, the DC voltage gain G_V, which is the ratio of the output voltage V_o and the source voltage V_s, is then determined as follows:

$$G_V(C_v) \equiv \left| \frac{V_o}{V_s} \right| = \left| \frac{V_e}{V_s} \cdot \frac{V_o}{V_e} \right|$$

$$= \frac{1}{(1 - \omega_s^2 L_p C_2)} \cdot \frac{R_e}{\sqrt{R_e^2 (1 - \omega_s^2 L_e C_v)^2 + \omega_s^2 L_e^2}} \quad (3)$$

As identified from (3), G_V increases when C_v increases as long as the source angular frequency ω_s is less than the resonant angular frequency ω_r, which is exactly the case of the proposed design, i.e.:

$$\omega_s < \omega_r, \quad \omega_r = \frac{1}{\sqrt{L_e C_v}} \quad . \quad (4)$$

The LED dissipating power, which is proportional to V_o, can be accordingly controlled by changing C_v, as shown in Fig. 3.

B. Operating Principle of the TRIAC Dimmer in the Transient State

The method for changing the capacitance C_v by the proposed TRIAC dimmer, as shown in Fig. 1, is explained in this section.

When the TRIAC is completely turned off, as shown in Fig. 4(a), there is no capacitance, assuming the loading effect of R_1-C_5 is negligible. As a result, $C_v = 0$. When the TRIAC is completely turned on, as shown in Fig. 4(b), the capacitance becomes $C_v = C_4$. If the TRIAC is appropriately turned on with a delay time of T_c for every half cycle of the power source T_s, as shown in Fig. 5, the equivalent capacitance C_v can be varied as follows:

$$0 \le C_v < C_4 \quad \text{for} \quad T_s / 2 \ge T_c > 0 \quad . \quad (5)$$

Unfortunately, it is not possible to find an analytical expression of C_v for an arbitrary control time of T_c. This is due to difficulties in finding the dynamics of the fourth-order
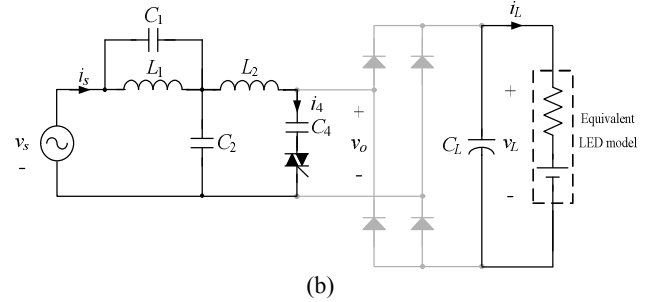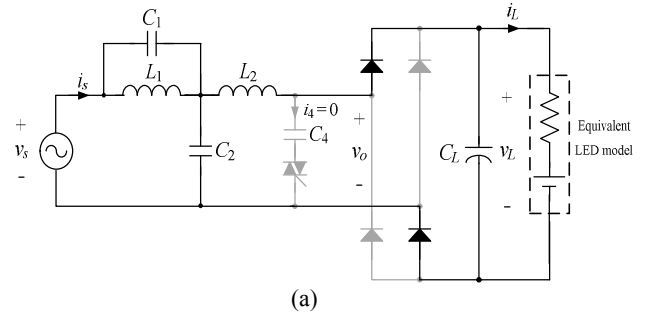

(a)

(b)

Fig. 4. Dynamic circuits of the proposed LED driver for a positive half cycle of the v_s, assuming the v_L is constant due to a large load capacitor. (a) The TRIAC is turned off. (b) The TRIAC is turned on.

power circuit. Therefore, the dynamic characteristics and the DC gain of (3) are simulated for each T_c in the subsequent section. Instead, the method for changing the value of T_c is suggested in this section.

TRIAC-Off Mode [t_1, t_2]: As shown in Fig. 4(a), the DIAC control input voltage v_5 is charged, when the TRIAC is turned off, as follows:

$$C_5 \frac{dv_5}{dt} = i_1 - i_c = \frac{v_T - v_5}{R_1} - i_c \cong \frac{v_T}{R_1} - i_c \cong \frac{2V_L}{R_1} - i_c \quad (6a)$$

$$\because |v_5| \le V_D << V_L < 2V_L \cong |v_T| \quad . \quad (6b)$$

In (6), it is assumed that the LED voltage and capacitor voltage are unchanged, i.e. $v_o = v_L = V_L$ and $v_4 = -V_L$, respectively. As a result, the TRIAC voltage is determined as $v_T = v_o - v_4 \approx V_L - (-V_L) = 2V_L$. Moreover, v_4 is nearly constant because R_1 is set to be as high as several MΩ. The DIAC triggering voltage V_D is set to be 32 V in this paper, which is much less than $V_L \approx 210$ V. The capacitor voltage v_4 has been determined by the previous switching stage, which will be explained in the next few paragraphs.

TRIAC-On Mode [t_2, t_3]: As v_5 reaches V_D, the DIAC and TRIAC are turned on, and C_5 is immediately discharged so that v_5 becomes zero, as shown in Fig. 4(b). At the same time, the capacitor voltage of C_4 is resonated with L_2 and other filter elements, and its voltage v_4 is increased from $-V_L$ at t = t_2 to V_L at t = t_3, as shown in Fig. 5. Note that v_4 is kept constant until the TRIAC is turned on again at the next negative polarity of source voltage. As soon as v_4 reaches V_L, the TRIAC is turned off because the time derivative of the
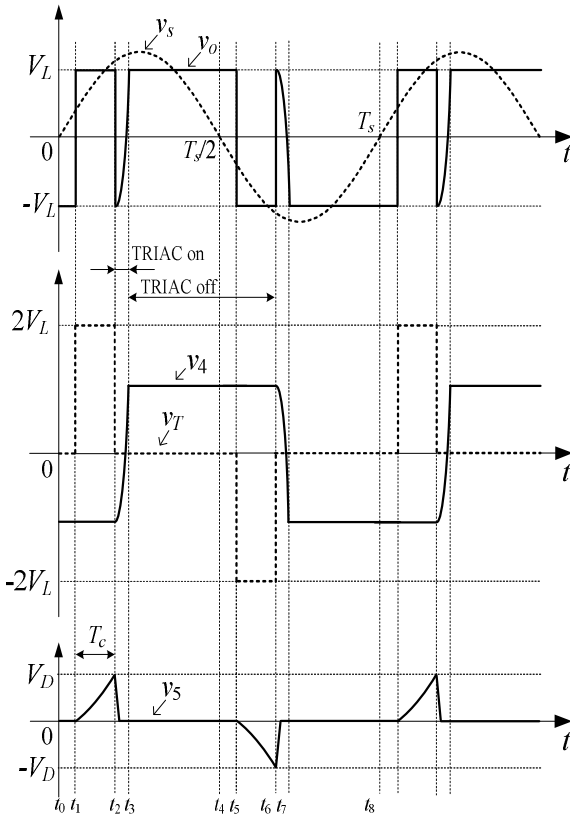
Fig. 5. Waveforms of the TRIAC dimmer.

Fig. 6. An example of theoretical normalized control time $T_c/(R_1C_5)$ w.r.t. I_c for various R_1 when V_D =32 V and V_L = 210 V.

capacitor voltage is eventually zero, i.e., $i_4 = C_4 \dfrac{dv_4}{dt} = C_4 \dfrac{dV_L}{dt} = 0$. Therefore, the TRIAC is kept turned off during $[t_3, t_6]$, where its voltage becomes negative at t = t_5 due to a reversed turning on of the full bridge diode.

The control time T_c, as shown in Fig. 5, can be derived from (6), assuming $i_c = I_c$ for a half cycle, as follows:

$$C_5 \frac{V_D}{T_c} \cong \frac{2V_L}{R_1} - I_c \quad \rightarrow \quad T_c = \frac{V_D R_1 C_5}{2V_L - I_c R_1} \quad . \tag{7}$$

From (7), T_c can be normalized by R_1C_5, as follows:

$$\beta \equiv \frac{T_c}{R_1 C_5} = \frac{V_D}{2V_L - I_c R_1} \quad . \tag{8}$$

As shown in Fig. 6, β, which is proportional to T_c, can be controlled by either the manual dimming volume resistor R_1 or the control current I_c so that the LED power can eventually be varied.

C. Operating Principle of the Control Circuit

In order to feed an appropriate I_c of (8) against variations in the LED voltage V_L, a control circuit is introduced, as shown in Fig. 7, where the input and output of the proposed circuit are connected to v_o and v_5 of Fig. 1, respectively.

The proposed control circuit is composed of a negative peak detector for detecting the envelope of the load voltage, a low pass filter for eliminating harmonic voltage ripples higher than th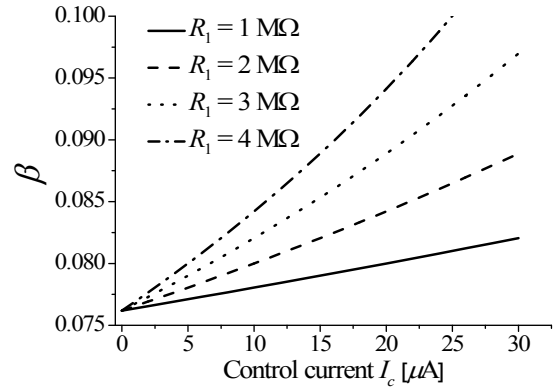e source frequency of 50 Hz or 60 Hz, an integrator to accumulate the control error signals, and a current mirror for converting the control voltage v_c to the control current i_c.

As shown in Fig. 5, v_o and v_5 alternatively change every half cycle. Therefore, it is not feasible to derive a transfer function from the proposed control circuit as it is. Instead, the envelope behavior of v_o and v_5 is considered in this section.

The resistors R_6 and R_7 constitute a mathematical comparator as follows:

$$v_{f1} = \frac{R_6}{R_6 + R_7} V_{cc} + \frac{R_7}{R_6 + R_7} v_o \equiv V_{ref} + Kv_o \tag{9a}$$

$$\because V_{ref} = \frac{R_6}{R_6 + R_7} V_{cc} , \quad K = \frac{R_7}{R_6 + R_7}$$

$$v_{f2} \cong \frac{R_6}{R_6 + R_7} V_{cc} - \frac{R_7}{R_6 + R_7} v_o^* = V_{ref} - Kv_o^* \tag{9b}$$

$$\Rightarrow \quad V_{f2}(s) \cong V_{ref}(s) - KV_o^*(s), \tag{9c}$$

where the constant DC supply voltage V_{cc} is used to generate the reference voltage V_{ref}. In (9b), a non-linear negative peak detector is approximated to a rectifier for the envelope of each peak voltage v_o^*.

The low pass filter and integrator have the following transfer functions, respectively:

$$G_1(s) \equiv \frac{V_{f3}(s)}{V_{f2}(s)} = \frac{R_3 // R_5}{R_3 // R_5 + R_4} \cdot \frac{1}{1 + sC_7(R_3 // R_4 // R_5)} \tag{10a}$$

$$G_2(s) \equiv \frac{V_c(s)}{V_{f3}(s)} = -\frac{1}{sR_3 C_6} \quad , \tag{10b}$$

where a positive offset current is provided through R_5 in the low pass filter because the negative peak detector is a current sink.

The current mirror provides the control current I_c of (8), regardless of the polarity, in proportion to v_c as follows:

$$i_c = i_m \quad \text{for} \quad v_5 > V_\gamma + V_\sigma \quad (\because D_1 = D_2 = \text{OFF}, D_3 = D_4 = \text{ON}) \tag{11a}$$

$$i_c = -i_m \quad \text{for} \quad v_5 < -V_\gamma \quad (\because D_1 = D_2 = \text{ON}, D_3 = D_4 = \text{OFF}) \tag{11b}$$

$$i_c = 0 \quad \text{for} \quad -V_\gamma \leq v_5 \leq V_\gamma + V_\sigma \quad (\because D_1 = D_2 = D_3 = \text{OFF}, D_4 = \text{ON}) \tag{11c}$$
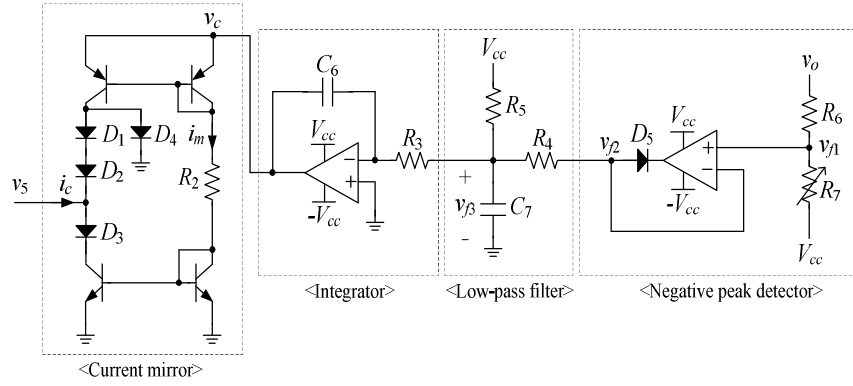
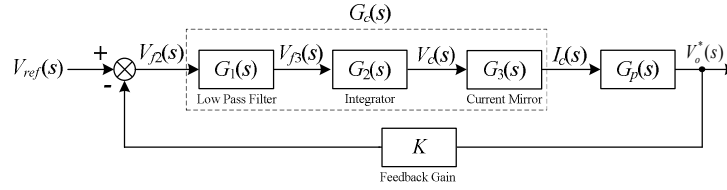Fig. 7. Proposed control circuit for LED power regulation.

Fig. 8. Overall block diagram of the proposed TRIAC dimming LED driver including the control circuit.

$$\because i_m = \frac{v_c - 2V_\gamma}{R_2} \qquad (11d)$$

$$\Rightarrow I_c(s) = \Delta I_m(s) = \frac{1}{R_2}V_c(s) \qquad (11e)$$

$$\therefore \ G_3(s) \equiv \frac{I_c(s)}{V_c(s)} = \frac{1}{R_2} \ , \qquad (11f)$$

where V_γ and V_σ are the cut-in voltage ($\cong 0.6$ V) and saturation voltage ($\cong 0.2$ V) of a bipolar junction transistor, respectively.

As can be seen from (11a) and (11b), the current mirror operates nearly symmetrically w.r.t. v_5, which is essential for symmetrical control of each half cycle. In (11e), the DC offset term of (11d) is omitted from the transfer function of $I_c(s)$ of (8) because this offset is relatively small and can be cancelled by the integrator. Therefore, only the change of the mirror current i_m is considered.

As shown in Fig. 8, the overall closed-loop transfer function of the proposed TRIAC dimming LED driver can be found from (9)-(11) as follows:

$$G_s(s) \equiv \frac{V_o^*(s)}{V_{ref}(s)} = \frac{G_c(s)G_p(s)}{1 + KG_c(s)G_p(s)} \qquad (12a)$$

$$\because \ G_p(s) \equiv \frac{V_o^*(s)}{I_c(s)} \ , \qquad (12b)$$

$$G_c(s) \equiv G_1(s) \cdot G_2(s) \cdot G_3(s)$$
$$= \frac{R_3 /\!/ R_5}{R_3 /\!/ R_5 + R_4} \cdot \frac{1}{1 + sC_7(R_3 /\!/ R_4 /\!/ R_5)} \cdot \frac{-1}{sR_3C_6} \cdot \frac{1}{R_2} \qquad (12c)$$

In (12), the LED system transfer function $G_p(s)$ has a negative gain as identified from (3) and (8). In other words, T_c increases as I_c increases, which results in decreases of C_v

and V_o. The LED voltage V_L, which is the final control goal, is indirectly controlled by V_o ($\cong \alpha V_L$) from (12).

In many cases, the power regulation of LED drivers is not necessarily very fast. Thus, the proposed control circuit is designed to be slow enough so that it can be quite robust to switching noise and disturbances. Then, assuming that the low pass filter and LED system are fast enough when compared to the integrator, the loop gain of (12a) becomes as follows:

$$LG(s) \equiv 1 + KG_c(s)G_p(s)$$
$$= 1 + KG_1(s) \cdot G_2(s) \cdot G_3(s)G_p(s) \qquad (13a)$$
$$\cong 1 + KG_2(s) \cdot G_3(s)G_{p0} = 1 + \frac{KG_{p0}}{sR_3C_6R_2} = 0$$

$$\because \ G_{p0} \equiv -G_p(0) > 0 \ , \ G_1(s) \cong 1 \qquad (13b)$$

$$\Rightarrow s_o = -\frac{KG_{p0}}{R_2R_3C_6} \ \text{ or } \Rightarrow \tau = \frac{R_2R_3C_6}{KG_{p0}} \ . \qquad (13c)$$

As identified from (13c), the proposed LED driver is always stable and its first-order time constant can be adjusted by the control gain.

III. Design of the Proposed TRIAC Dimming LED Driver

A. Main Circuit

As shown in Fig. 1, the proposed LED driver includes a passive-type LC^3 LED driver [24]; hence, the main power circuit parameters for 60 W of power were chosen in a similar way to those of the references [24], as listed in the Table I.

Concerning the TRIAC dimmer in Fig. 1, a small value of

TABLE I
CIRCUIT PARAMETERS OF THE PROPOSED MAIN POWER CIRCUIT

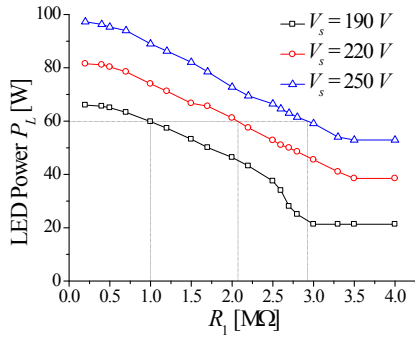| Parameters	Values	Parameters	Values
L_1	0.6 H	C_5	10 nF
L_2	0.6 H	C_L	100 μF
C_1	0.47 μF	R_1	1.0 MΩ
C_2	0.68 μF	V_D	32 V
C_3	1.68 μF	n_s	70
C_4	1.0 μF	n_p	4

Fig. 9. Simulation results of the LED power w.r.t. R_1 for various V_s.

C_5 and a large value of R_1 are highly recommended for reducing the capacitor size and power loss in R_1. Thus, C_5 and R_1 are chosen as 10 nF and 1.0 ~ 3.0 MΩ, respectively. The worst case power dissipation in R_1 is roughly $(2V_L)^2 / R_1 \cong (2 \cdot 210)^2 / 1M \cong 176.4 \ m$W, which is well below 1/4 W. The value of C_4 is selected as 1.0 μF, considering the range of variable switched capacitance. The breakover voltage V_D of the DIAC is selected as 32 V, considering the commercial availability of the DIAC.

To confirm LED dimming by a volume resistor R_1, a PSIM simulation was performed, as shown in Fig. 9. As R_1 increases, T_c increases according to (7), and C_v decreases, which results in a decrease of the LED power, as shown in Fig. 9. In this way, LED dimming by a volume resistor can be achievable for a wide range of source voltages, like a conventional dimming lamp. For a constant LED power $P_L = 60$ W, R_1 should be appropriately varied between 1.0 and 3.0 MΩ for a source voltage of 190 V < V_s < 250 V, which is a ± 30 V variation of the rated source voltage of 220 V. For a constant source voltage of $V_s = 220$ V, the LED power can be varied from 40 W to 80 W.

B. Control Circuit

To sense the envelope of each peak voltage v_o^*, as shown in Fig. 7, a large value for R_6 is recommended for reducing the power loss in the resistor; hence, R_6 is set to 4.7 MΩ so that the worst case power dissipation in R_6 can be roughly 10 mW. In other words, $V_L^2 / R_6 \cong 210^2 / 4.7M \cong 9.4 \ m$W , which is much lower than 1/4 W. In the steady state, the v_{f2} of

(9b) should be zero, assuming that R_5 is large enough, so that the input voltage of the integrator can be zero. Thus, for a given V_L that is determined from [24], R_7 is calculated as 336 $k\Omega$, as follows:

$$\frac{R_6}{R_6 + R_7} V_{cc} \cong \frac{R_7}{R_6 + R_7} V_o^* \quad (\because V_{f2} = 0)$$

$$\to R_7 \cong \frac{V_{cc}}{V_o^*} R_6 \cong \frac{V_{cc}}{V_L} R_6 = \frac{15}{210} 4.7M = 336 \ k\Omega \quad (14)$$

Harmonic voltage components higher than the third harmonic of the source frequency f_s are assumed to be eliminated by the low pass filter. In other words, the time constant of the low pass filter, $R_4 C_7$ is approximately 1 ms, which results in the selection of $R_4 = 10 \ k\Omega$ and $C_7 = 0.1 \ \mu$F. For $V_{cc} = 15$V, R_5 is selected as 2.0 MΩ to provide a positive offset current of about 7.5 μA, which is a requisite for maintaining the non-negative polarity of v_{f3}.

In the current mirror of Fig. 7, the maximum value for I_1 of Fig. 1 is calculated as 0.42 mA from (6) when $R_1 = 1.0$ MΩ and $V_L = V_o^* = 210$ V. As can be seen from Fig. 9, the maximum value of R_1 for 190 V < V_s < 250 V is 2.9 MΩ, which corresponds to almost a third of I_1, i.e. 0.14 mA; hence, the maximum control current $I_{c,max} = I_{m,max}$ becomes 0.28 mA to give this current difference. Then, R_2 is approximately calculated from (11d) as 43.2 $k\Omega$, where $V_\gamma = 0.7$ V and the maximum value of v_c is 13.5 V.

Finally, the integrator is designed, where the time constant of this integrator $R_3 C_6$ can be determined from (13c). From (9a), K is calculated to be 0.0667, and the system gain G_{p0} is experimentally determined to be 2.3 × 10⁵. Therefore, $R_3 C_6$ becomes 14 ms, and the values of R_3 and C_6 are selected as 300 $k\Omega$ and 47 nF, respectively, considering a sufficiently slow response time of 400 ms.

C. DC Power Supply

To provide the control circuit with supply voltages of V_{cc} and -V_{cc}, a new DC power supply circuit is introduced, as shown in Fig. 10. Because the source voltage is very high when compared to the DC supply voltage, a new capacitive voltage divider of C_8 and C_9 is used. This simple circuit constitutes a step-down capacitive transformer, which may be replaced with a conventional inductive transformer and provides a galvanic isolation from the source voltage. In this paper, it is assumed that V_{cc} and -V_{cc} are symmetrical. In other words, $C_{10} = C_{11}$, and the zenor diode voltage V_z is the same.

By applying Thevenin's theorem to Fig. 10(a), an equivalent circuit is obtained, as shown in Fig. 10(b), where the parameters are determined as follows:

$$v_{th} = \frac{C_8}{C_8 + C_9} v_s \quad \text{and} \quad C_{th} = C_8 + C_9 . \quad (15)$$

The analysis of Fig. 10(b) is straightforward if the input current of a half cycle is found for a given V_z. This analysis is already available [43]-[44], assuming that $C_{10} >> C_{th}$ and that
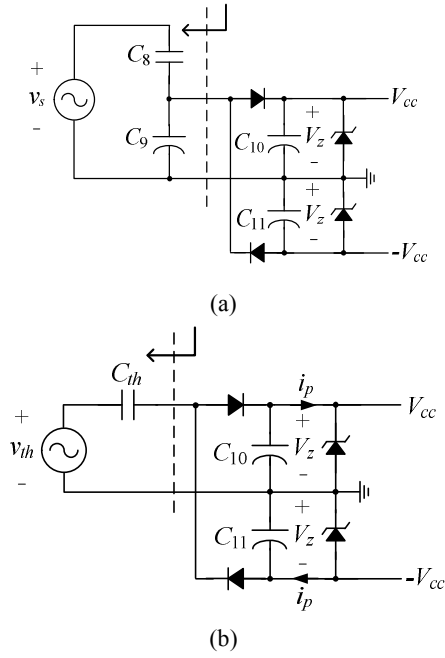
Fig. 10. Proposed capacitive transformer type DC power supply. (a) Original circuit. (b) Thevenin's equivalent circuit.
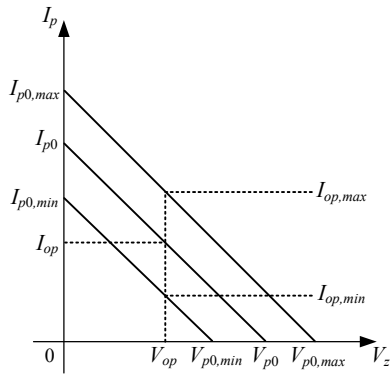

Fig. 11. The V_z - I_p curve of the proposed DC power supply circuit.

the full bridge rectifier circuit is replaced with the proposed positive and negative rectifiers. Then, the average current of the positive DC side power supply I_p becomes as follows, neglecting the diode forward voltage drop [44]-[45]:

$$I_p = I_{p0}\left(1 - \frac{V_z}{V_{p0}}\right) \qquad (16a)$$

$$\therefore I_{p0} = \frac{V_{th}/2}{1/(\omega_s C_{th})} = \frac{\omega_s C_{th} V_{th}}{2} \quad \text{and} \quad V_{p0} = \sqrt{2}V_{th} \quad . \quad (16b)$$

In (16), I_{p0} corresponds to the shorted load circuit where $V_z = 0$, and V_{p0} corresponds to an open load circuit where $I_p = 0$.

As can be seen from Fig. 11, the average DC current I_p varies as the source voltage changes for $V_s = 190$ V, 220 V, and 250 V, respectively. When $V_s = 190$ V, for a given $V_z = V_{cc} = 15$ V, I_p becomes its minimum value $I_{op,min}$, which should be larger than the required load current of the positive power supply $I_{p,req}$. Meanwhile, when $V_s = 250$ V, I_p becomes

TABLE II
CIRCUIT PARAMETERS OF THE PROPOSED CONTROL CIRCUIT AND DC POWER SUPPLY

Parameters	Values	Parameters	Values
R_2	43.2 $k\Omega$	C_7	0.1 μF
R_3	300 $k\Omega$	C_8	0.1 μF
R_4	10 $k\Omega$	C_9	1.0 μF
R_5	2.0 $M\Omega$	C_{10}	10 μF
R_6	4.7 $M\Omega$	C_{11}	10 μF
R_7	336 $k\Omega$	V_z	15 V
C_6	47 nF		

its maximum $I_{op,max}$, which means that the zenor diode current, which is the difference between I_p and the required load current, becomes large. Because the zenor diode current should be neither zero nor too large, the operating voltage V_{op} and the operating current I_{op} are chosen to be half of V_{p0} and I_{p0} at the normal source voltage of $V_{s,norm} = 220$ V, as follows:

$$V_{op} = V_{cc} = \frac{V_{p0}}{2} = \frac{\sqrt{2}V_{th,norm}}{2} = \frac{V_{th,norm}}{\sqrt{2}} \qquad (17a)$$

$$\because V_{th,norm} = \frac{C_8}{C_8 + C_9}V_{s,norm} \quad . \qquad (17b)$$

On the other hand, the minimum DC current $I_{op,min}$ at the minimum source voltage of $V_{s,min} = 190$ V should always be larger than the required load current $I_{p,req}$, as follows:

$$I_{op,min} \equiv I_{p0,min}\left(1 - \frac{V_{op}}{V_{p0,min}}\right) \geq I_{p,req} \qquad (18a)$$

$$\because I_{p0,min} = \frac{\omega_s C_{th} V_{th,min}}{2}, \quad V_{p0,min} = \sqrt{2}V_{th,min} = \frac{\sqrt{2}C_8}{C_8 + C_9}V_{s,min} . \quad (18b)$$

In this paper, the required DC power is identified as $V_{op} = V_{cc} = 15$ V and $I_{p,req} = 1.5$ mA at $f_s = 60$ Hz; hence, V_{p0} is selected as 30 V. From (17)-(18), C_8 and C_9 are calculated as 0.099 μF and 0.932 μF, respectively. Hence, C_8 and C_9 are selected as 0.1 μF and 1.0 μF, considering commercial product availability. To filter out the ripple in the supply voltage V_{cc}, both C_{10} and C_{11} are selected as 10 μF, which is about ten times greater than C_{th}.

The design parameters of the proposed control circuit and DC power circuit are summarized in Table II.

IV. EXPERIMENTAL VERIFICATIONS

As shown in Fig. 12, a prototype of the proposed LED driver was fabricated in accordance with the proposed design procedure, as listed in Tables I and II. The core material in the two inductors L_1 and L_2 of Fig. 12 was silicon steel plate core, and the internal resistance of the fabricated inductors was measured as 7 Ω. Because the proposed LED driver can be used for high LED power applications whose power level
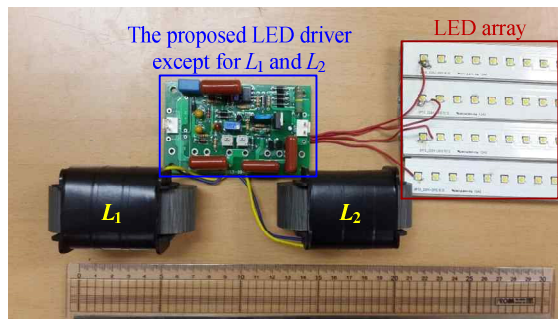
Fig. 12. A prototype of the proposed LED driver with two inductors L_1 and L_2 and an LED array.
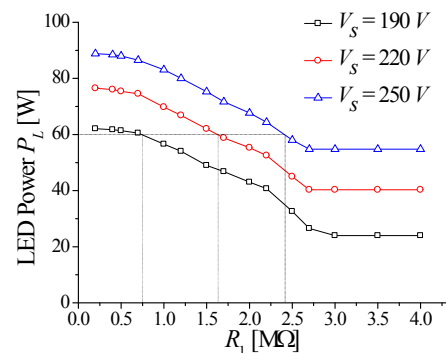

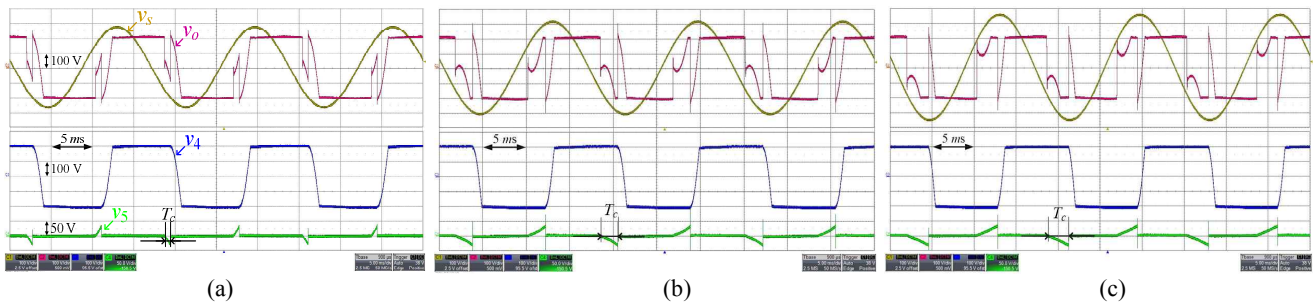Fig. 13. Experimental results of LED power with respect to R_1 for various V_s.

Fig. 14. The experimental waveforms of v_s, v_o, v_4, and v_5 for V_s = 190 V, 220 V, and 250 V at f_s = 60 Hz. (a) V_s = 190 V: R_1 = 0.75 MΩ. (b) V_s = 220 V: R_1 = 1.63 MΩ. (c) V_s = 250 V: R_1 = 2.4 MΩ.
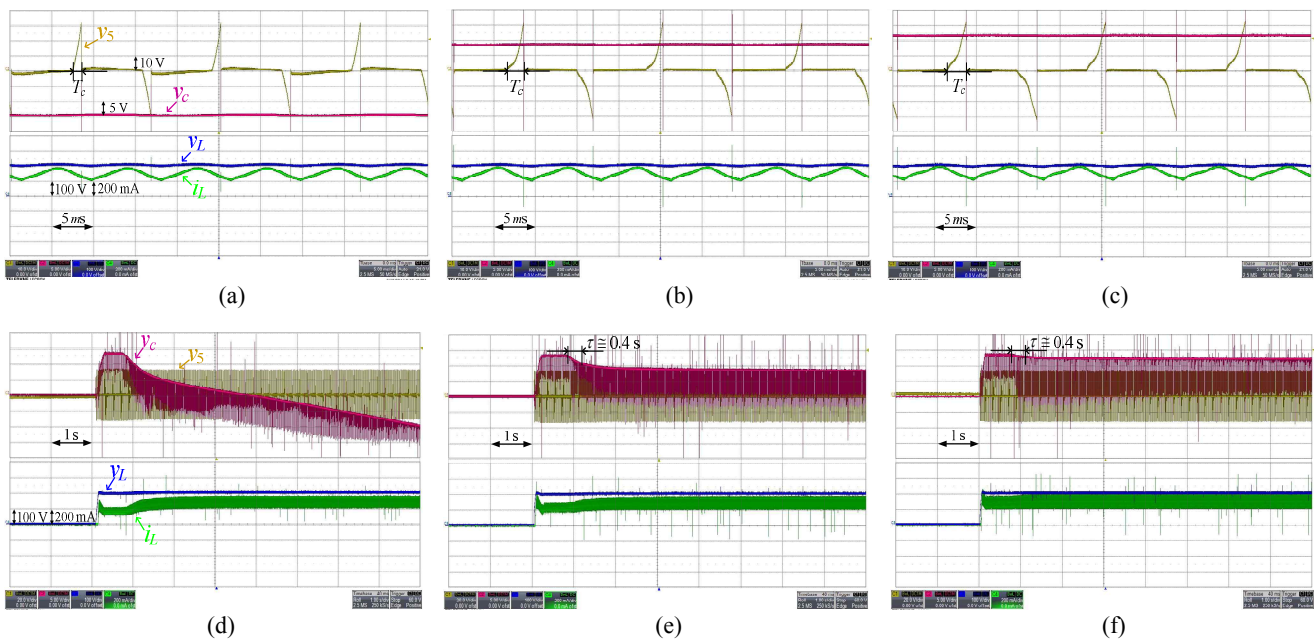

Fig. 15. The experimental waveforms of v_5, v_c, i_L, and v_L for V_s = 190 V, 220 V, and 250 V at f_s = 60 Hz. (a) V_s = 190 V: time scale = 5 ms. (b) V_s = 220 V: time scale = 5 ms. (c) V_s = 250 V: time scale = 5 ms. (d) V_s = 190 V: time scale = 1 s. (e) V_s = 220 V: time scale = 1 s. (f) V_s = 250 V: time scale = 1 s.

is as high as 60 ~ 100 W, two slightly large inductors are of no practical concern due to the large accommodation space of industrial lighting applications. These applications generally require high efficiency and a long lifespan for an LED driver.

A. LED Dimming

As shown in Fig. 13, the LED dimming of the proposed LED driver without a control circuit is experimentally verified. It is well matched with the simulation results of Fig. 9. Slight discrepancies between the experimental and simulation results come mainly from the internal resistances of L_1 and L_2. The value of P_L can be set appropriately by

TABLE III
MEASURED RESULTS FOR SOURCE VOLTAGE VARIATION
(190 V < V_s < 250 V)

Measured Parameters	Source voltage (V_s)		
	190 V$_{rms}$	220 V$_{rms}$	250 V$_{rms}$
P_s	62.6 W	63.7 W	66.5 W
P_L	58.4 W	58.8 W	60.6 W
PF	0.979	0.940	0.912
THD	7.0%	6.3%	10.8%
Efficiency	93.3%	92.3%	91.1%
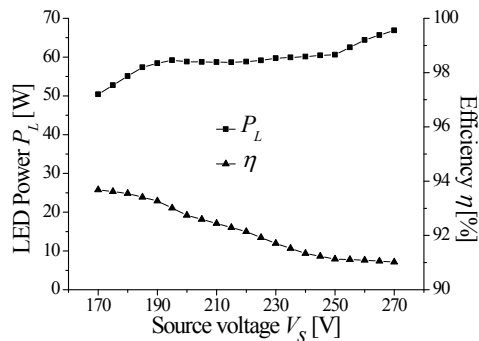
(a)
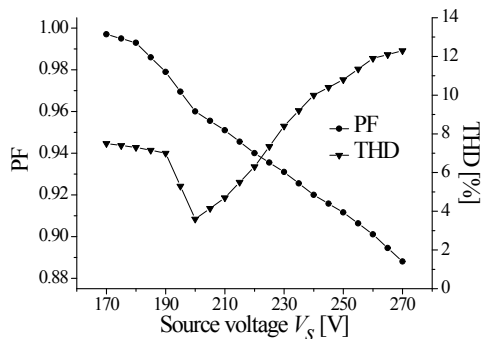
(b)

Fig. 16. Experimental results of the P_L, η, PF, and THD w.r.t. the V_s at f_s = 60 Hz. (a) The LED power P_L and efficiency η. (b) The PF and THD.

modulating the volume resistor R_1. For instance, P_L can be changed from 76 W to 40 W at V_s = 220 V, where over 2.7 MΩ of R_1 cannot be used for the LED dimming range because v_5 in Fig. 5 cannot reach V_D within the control time T_c.

As can be seen from Fig. 13, R_1 was selected to satisfy P_L = 60 W: R_1 = 0.75 MΩ, 1.63 MΩ, and 2.4 MΩ for V_s = 190 V, 220 V, and 250 V, respectively. Based on these values, the experimental waveforms of v_s, v_o, v_4, and v_5 were measured, as shown in Fig. 14, where T_c increased as V_s increased, as anticipated from Fig. 5.

B. LED Power Regulation

As shown in Fig. 15, the experimental waveforms of v_5, v_c, i_L, and v_L were measured to verify the LED power regulation

by the proposed control circuit. When V_s = 190 V, V_c became -15.0 V, which is the minimum value of v_c. However, when V_s > 190 V, the LED power regulation began, which is identified by v_c > 0. For instance, v_c = 8.5 V for V_s = 220 V, and v_c = 12.3 V for V_s = 250 V. In this way, P_L was found to be well regulated for 190 V < V_s < 250 V by the proposed control circuit. The time constant of the control circuit was measured as 0.4 s, as shown in Figs. 15(e) and (f), which can be varied, as can be seen from (13c).

The LED power and total efficiency of the proposed LED driver were also measured, as shown in Fig. 16(a), where the maximum LED power variation was well mitigated to within ± 2% and the maximum efficiency was between 93.3% and 91.1% for 190 V < V_s < 250 V. This power variation, ± 2%, of the proposed LED driver is quite negligible in practice. As shown in Fig. 16(b), the measured results of the PF and THD satisfy the global standards for 190 V < V_s < 250 V [45]-[46]. Furthermore, all of the harmonics of the source current i_s satisfy the IEC61000-3-2 class C standard, as shown in Fig. 17. The measurement results for each V_s are summarized in Table III.

V. CONCLUSION

The proposed TRIAC dimming LED driver by variable switched capacitance has been verified for 60 W LED applications. The LED power can be successfully regulated to within ± 2% for a wide range of 190 V < V_s < 250 V. The measured THD, PF, and power efficiency were 6.3%, 0.94, and 92.3% at V_s = 220 V, respectively. The temperature increase of the LED driver was merely 6°C. With this novel TRIAC dimming LED driver, high efficiency and a long lifespan were achieved, since these are inherent merits of passive-type LED drivers. In addition, LED dimming and LED power regulation were successfully realized. Thus, the proposed LED driver is expected to be utilized in industrial lighting applications such as streets, factories, parking garages, and emergency stairs.

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