JPE 15-2-26

http://dx.doi.org/10.6113/JPE.2015.15.2.567
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

An Improved Topology for the Current Fed Parallel Resonant Half Bridge Circuits Used in Fluorescent Lamp Electronic Ballasts

Qingsong Wang*, Ming Cheng†, and Bing Zhang*

†*School of Electronic Engineering, Southeast University, Nanjing, China

Abstract

An improvement in the current fed parallel resonant half bridge (CFPRHB) circuits used in fluorescent lamp electronic ballasts is provided in this paper. The CFPRHB belongs to the self-oscillating family which includes the current fed push-pull and series resonant inverters, most of which are used in instant-start applications. However, many failure modes are related to the bypass capacitor according to an analysis of failed samples. In this paper, the operating functions of the existing topology in the steady state are analyzed and the main root cause of failure modes has been found. Comparisons between the two topologies are conducted in terms of the voltage stress of the bypass capacitor as well as the thermal and performance of the ballasts to verify the advantages of the proposed topology. It is found that the improved topology is capable of enhancing the reliability and reducing the cost of products without having a negative influence on the system performance.

Key words: Current fed, Electronic ballasts, Fluorescent lamp, Independent lamp operation, Instant start, Lighting, Parallel resonant

I. INTRODUCTION

Fluorescent lamps of many types have been studied in [1]-[4], and various kinds of electronic ballasts have been designed as lamp drivers in [5]-[12]. Many topologies have been developed to improve the performance of fluorescent lamps in lighting systems. They can generally be separated into self-oscillating series and IC-controlled series. The self-oscillating ballasts as described in [13]-[17] have been widely used in the market since they have fewer components and lower cost. The self-oscillating families include the current fed push-pull, series and parallel resonant inverters, etc. [18]. The current fed push-pull and series resonant topologies have been well studied. Conversely, the current fed parallel resonant topologies need to be explored further.

The traditional topology for current fed parallel resonant half bridge (CFPRHB) circuits, as shown in Fig. 1, is dealt with in this paper. This topology is often used in ballasts to drive T8 lamps, such as F32T8, F25T8 and F17T8 lamps. It is widely used by international companies in fluorescent lamp electronic ballasts because of its independent lamp operation (ILO), simple structure, perfect isolation between the input and output, fewer components and lower cost.

It is recorded that many of the failure modes of failed samples returned from applications are related to the bypass capacitor C_8 in Fig. 1. Too high of a voltage stress was found on the capacitor at the steady and transient states, which can reduce the lifetime of the capacitor and result in failures of the ballasts.

This paper is organized as follows. Issues and the main root cause of traditional CFPRHBs are described in Section II. An improved topology is proposed and analyzed in Section III. Simulations are presented in Section IV. Experiments and discussions are provided in Section V. Conclusions are given in Section VI.

II. ISSUES OF THE TRADITIONAL CFPRHB

A. Operating Principles of the Traditional CFPRHB

The operating principles of the traditional CFPRHB are described as follows. Only the half bridge circuit is depicted in Fig. 1. Before that, there is a power factor correction

Manuscript received Oct. 15, 2014; accepted Jan. 9, 2015
Recommended for publication by Associate Editor Bor-Ren Lin.
†Corresponding Author: mcheng@seu.edu.cn
Tel: +8613701402059, Southeast University
*School of Electronic Engineering, Southeast University, China

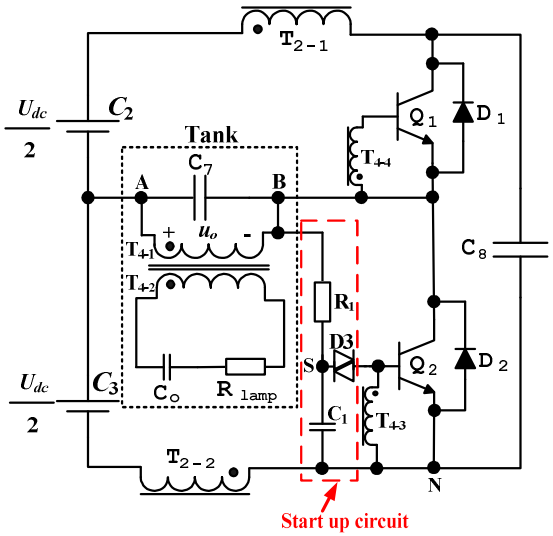


Fig. 1. Traditional topology of CFPRHB circuit.

(PFC) circuit within a single ballast. Since the PFC circuit is not depicted in Fig. 1, the symbols used in the CFPRHB may seem discontinuous. These symbols are defined as follows. U_{dc} is the output voltage of the PFC circuit, which is called the DCBUS. C_2 and C_3 are in series and each voltage is $0.5U_{dc}$. Q_1 and Q_2 are the transistors used as switches. D_1 and D_2 are the avalanche and freewheeling diodes. The input AC voltage is from 120V to 277V. When power is on, PFC starts to work and U_{dc} is built up first. Then the startup capacitor C_1 is charged by $0.5U_{dc}$ through $T_{4\text{-}1}$ and R_1. Once C_1 is charged to the threshold, D_3 is on and C_1 is discharged through D_3 and the base to the emitter junction of Q_2. Then, Q_2 is on. T_2 is the current fed transformer and the primary winding of T_4 acts as a resonant inductor, where the self inductance is much smaller than T_2. $T_{4\text{-}3}$ and $T_{4\text{-}4}$ are designed as drive windings. $T_{4\text{-}2}$ is the output winding to withstand the Open Circuit Voltage (OCV). There are many branches in parallel with $T_{4\text{-}2}$, each of which consists of a lamp in series with a ballasting capacitor. C_o and R_{lamp} denote the total equivalent ballasting capacitor and the total equivalent resistor of all of the lamps, respectively. C_8 is the bypass capacitor and it works with C_7 and C_o. The parameters used in this paper are listed in Table I. When Q_2 is on and Q_1 is off, current flows through C_3, the tank, Q_2, $T_{2\text{-}2}$ and then back to C_3. Q_2 will saturate as the drive signal is enhanced according to the induced voltage in $T_{4\text{-}3}$. Since the voltage on $T_{4\text{-}1}$ is sinusoidal, the drive signals are also sinusoidal and Q_2 will be turned off when the voltage on $T_{4\text{-}3}$ drops below the threshold. Meanwhile, Q_1 is on. The freewheeling current flows through C_3, the tank, D_1, C_8, $T_{2\text{-}2}$ and back to C_3. When it reverses, the current loop includes C_2, $T_{2\text{-}1}$, Q_1 and the tank. The same analogy applies to the function when Q_1 is on. Then, the circuit enters the self-oscillating mode.

TABLE I

PARAMETERS OF THE CIRCUIT

DCBUS (U_{dc})	460V
Turn ratio of T_2	1:1
Turn ratio of T_4	60:138:1:1
Inductance of T_2 (T_m)	2.05mH
Inductance of $T_{4\text{-}1}$ (T_r)	408μH
C_7	4.7nF
C_8	1nF
Q_1 and Q_2	1100V/4A
Open Circuit voltage (OCV)	585V
Each ballasting capacitor	1.2nF
Lamp type	4xF32T8
Start mode	Instant-start
Operating frequency	42kHz

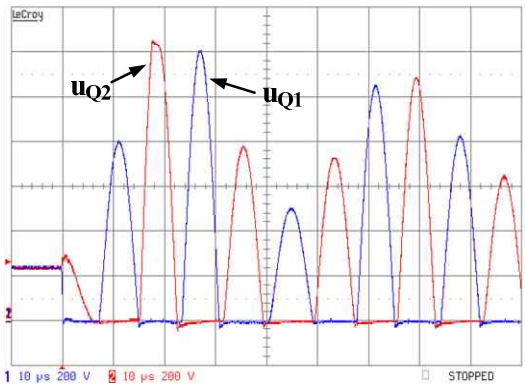


Fig. 2. Voltage spikes on switches (200V/div, 10μs/div).

B. Issues Occurred in the Traditional CFPRHB

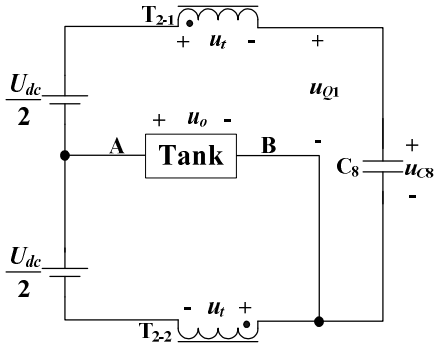
V-I mapping tests of key components have been implemented and voltage spikes as high as 1.2kV on two switches have been observed before ignition at the worst case, as shown in Fig. 2. Voltages on Q_1 and Q_2 have been recorded in channels 1 and 2. As analyzed after, these high voltage spikes are also on C_8. Their RMS and maximum voltages of are 511V and 722V, respectively, which means that the existing type of MKP21 (700V) can not last long in the applications since it is out of spec.

To solve this issue, capacitors of higher voltage ratings must be used, which may result in higher cost.

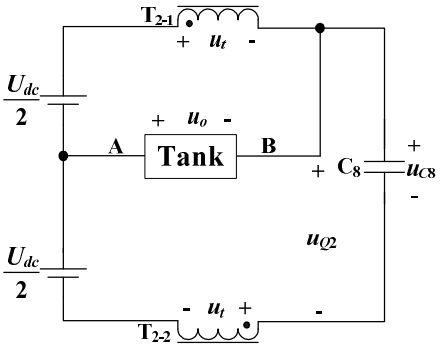
C. Root Cause Analysis of the Failure Modes in the Traditional CFPRHB

To find out the root cause, an analysis of the topology is needed. The operating functions can be separated into two stages. In this paper, stage 1 means Q_2 is on and Q_1 is off, and stage 2 means Q_1 is on and Q_2 is off, as shown in Fig. 3. All of the variables are defined in the related figures.

According to Kirhhoff's Voltage Law (KVL), the equations can be obtained from Fig. 3(a) as:



(a) Scenario of stage 1.



(b) Scenario of stage 2.

Fig. 3. Equivalent circuits of the traditional CFPRHB at different stages.

$$\frac{1}{2}U_{dc} = u_o + u_t \tag{1}$$

$$u_{C8} = U_{dc} - 2u_t \tag{2}$$

$$u_{C8} = u_{Q1} \tag{3}$$

where u_o denotes the voltage on $T_{4\text{-}1}$, u_t represents the voltage on each of the windings of T_2, u_{C8} denotes the voltage on C_8, and u_{Q1} denotes the voltage on Q_1.

Substituting Eqns. (1)-(2) into Eq. (3) gives:

$$u_{C8} = u_{Q1} = 2u_o \tag{4}$$

According to KVL, the equations of Fig. 3 (b) are:

$$\frac{1}{2}U_{dc} = u_t - u_o \tag{5}$$

$$u_{C8} = U_{dc} - 2u_t \tag{6}$$

$$u_{C8} = u_{Q2} \tag{7}$$

Substituting Eqns. (5)-(6) into Eq. (7) gives:

$$u_{C8} = u_{Q2} = -2u_o \tag{8}$$

In Fig. 1, u_o is the AC voltage, the mean value of which is zero. The power direction is from A to B at stage 1, while it is opposite at stage 2. Thus, Eq. (4) and Eq. (8) can be rewritten into a uniform equation, which is expressed as:

$$u_{C8} = u_Q = 2|u_o| \tag{9}$$

It is observed from Eq. (9) that the transient voltage on C_8 is always twice that of u_o, which explains the reason why the peak voltage on C_8 is over 1kV at the worst case. Such high voltage spikes may damage the bypass capacitor.

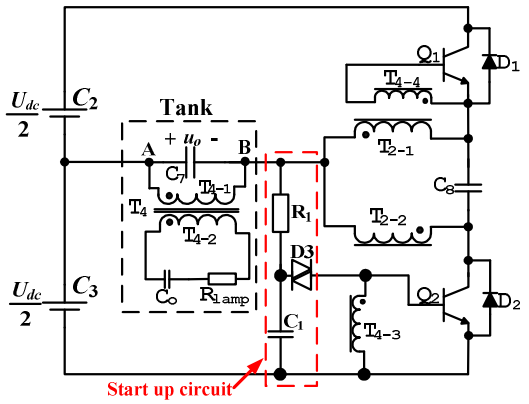


Fig. 4. The improved topology of CFPRHB.

III. Proposed Topology of the CFPRHB

A. Improved Topology and Its Operation Principle

The key concept is to find a way to change the form of Eq. (9), so that it can reduce the absolute value of u_{C8}.

An improved topology is proposed, as shown in Fig. 4. When compared with the traditional topology, the positions of T_2 and C_8 are changed, while all of the other parameters in the main circuit are kept the same.

B. Comparison of the Operating Functions between the Two Topologies

Similarly, the analysis of the operating functions can also be separated into two stages, as shown in Fig. 5. The equations can be obtained from Fig. 5 (a) as:

$$\frac{1}{2}U_{dc} = u_o - u_t \tag{10}$$

$$u_{C8} = -2u_t \tag{11}$$

$$u_{Q1} = \frac{1}{2}U_{dc} + u_o + u_t \tag{12}$$

By substituting Eq. (10) into Eq. (12) and Eq. (11), the following is obtained:

$$u_{Q1} = 2u_o \tag{13}$$

$$u_{C8} = U_{dc} - 2u_o \tag{14}$$

In Fig. 5 (b), the equations can be expressed as:

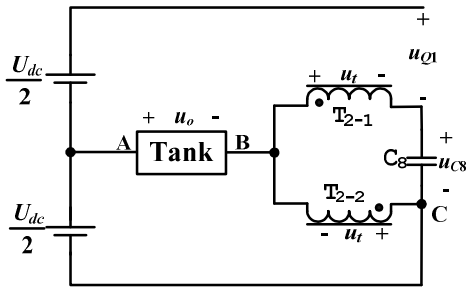
$$\frac{1}{2}U_{dc} = -u_t - u_o \tag{15}$$

$$u_{C8} = -2u_t \tag{16}$$

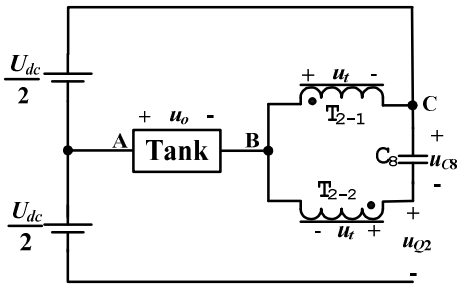
$$u_{Q2} = \frac{1}{2}U_{dc} - u_o + u_t \tag{17}$$

Substituting Eq. (15) into Eq. (16) and Eq. (17) gives:

$$u_{Q2} = -2u_o \tag{18}$$



(a) Scenario of stage 1.



(b) Scenario of stage 2.

Fig. 5. Operating stages of the improved CFPRHB.

$$u_{C8} = U_{dc} + 2u_o \tag{19}$$

Eq. (13) and Eq. (18) can be rewritten into a united form to get the voltage formula of the switches, which can be expressed as:

$$u_Q = 2|u_o| \tag{20}$$

Similarly, the following can be obtained:

$$u_{C8} = U_{dc} - 2|u_o| \tag{21}$$

A great change in the voltage on C_8 can be observed by comparing Eq. (9) and Eq. (21). In the traditional topology, the peak voltage value of C_8 is always twice that of u_o while it is changed to be less than U_{dc} in the improved topology.

C. An Example of the Solution

With the example and parameters in Table I, it is possible to obtain $U_o = U_{C7RMS} = 255$ V.

Let $u_o = \sqrt{2}U_o \sin(\omega t + \varphi) = \sqrt{2}U_o \sin\theta$, then in the proposed topology, the voltage of C_8 can be expressed as:

$$u_{C8} = U_{dc} - 2\sqrt{2}U_o|\sin\theta| \tag{22}$$

which means:

$$U_{dc} - 2\sqrt{2}U_o \le u_{C8} \le U_{dc} \tag{23}$$

Eq. (23) indicates that transient voltage on C_8 will not exceed $\max\{|U_{dc} - 2\sqrt{2}U_o, U_{dc}|\}$, which means that the peak value is less than U_{dc}. When compared to the 722V in the traditional CFPRHB, the improved CFPRHB has an overwhelming advantage on reducing voltage stress of C_8.

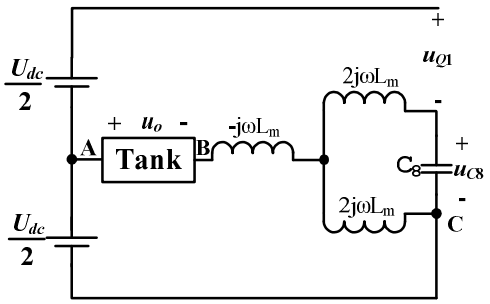


Fig. 6. Equivalent circuit of Fig. 5 (a).

The RMS voltage of C_8 in the improved topology can be calculated through Eq. (22), which is:

$$\begin{aligned} U_{C8new} &= \sqrt{\frac{1}{2\pi}\int_0^{2\pi}(U_{dc} - 2\sqrt{2}U_o|\sin\theta|)^2 d\theta} \\ &= \sqrt{U_{dc}^2 + 4U_o^2 - \frac{8\sqrt{2}U_o U_{dc}}{\pi}} \end{aligned} \tag{24}$$

Based on Eq. (24) and the parameters in Table I, the calculated RMS voltage of C_8 is 221.6V, which is much less than the 511V in the traditional CFPRHB.

D. Modeling of the Improved Topology

The main concept is to build up equivalent circuits of each stage using Thevenin's theorem.

The impedance between B and C in Fig. 6 is expressed as:

$$\begin{aligned} Z_0 &= -j\omega L_m + (2j\omega L_m)//(2j\omega L_m + \frac{1}{j\omega C_8}) \\ &= \frac{j\omega L_m \cdot \frac{1}{j\omega(4C_8)}}{j\omega L_m + \frac{1}{j\omega(4C_8)}} \\ &= (j\omega L_m)//(\frac{1}{j\omega(4C_8)}) \end{aligned} \tag{25}$$

According to Eq. (25), the simplified operating function can be depicted as Fig. 7.

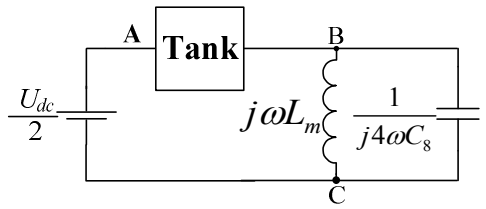
The two operating functions can be further united as shown in Fig. 8.

In Fig. 8, L_r denotes the inductance of the primary winding of T_4, L_m denotes the inductance of each winding of T_2, R_{la} and C_{la} are the equivalent resistor and capacitor looking from the primary side to the secondary side of T_4, which are:

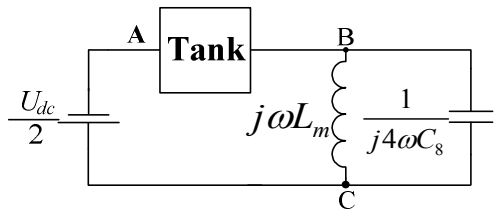
$$R_{la} = \frac{R_{lamp}}{2.3^2} \tag{26}$$

$$C_{la} = 2.3^2 C_o \tag{27}$$

With respect to the equivalent circuits in Fig. 8 (b), the relationship between the self-oscillating frequency and the circuit parameters can be expressed as:

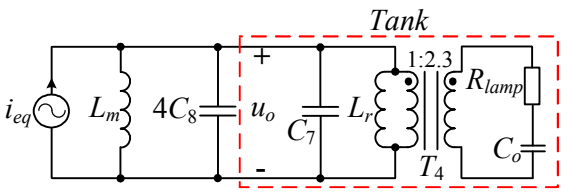


(a) Scenario of stage 1.

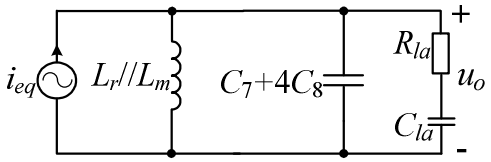


(b) Scenario of stage 2.

Fig. 7. Simplified operating stages of the improved CFPRHB.



(a) Equivalent circuit of the improved CFPRHB.



(b) Simplified circuit of (a).

Fig. 8. Equivalent circuits of the improved CFPRHB.

$$\omega = \frac{1}{\sqrt{\frac{L_r L_m}{L_r + L_m}(C_7 + 4C_8 + 2.3^2 mC_o)}} \tag{28}$$

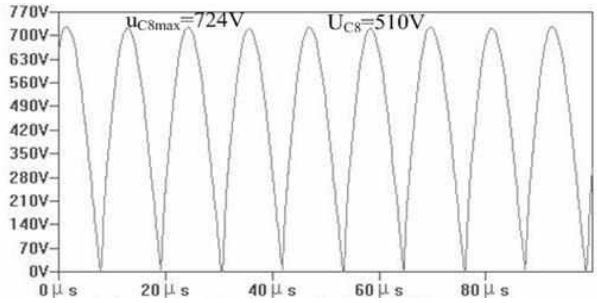
Where, m denotes the numbers of ballasting capacitors. In this paper, m is equal to 4.

IV. Simulation

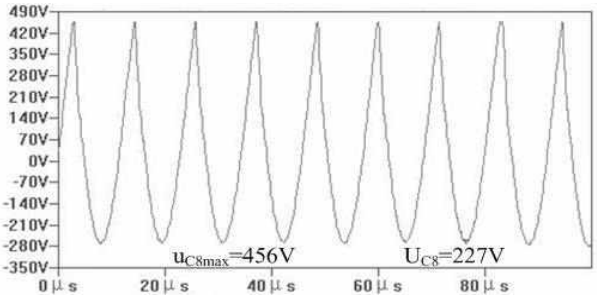
To verify the aforementioned analysis, simulations are carried out by LTSpice. The parameters of the main circuit are the same in the two topologies, as described in Table I. All of the lamps are regarded as pure resistors in the simulation.

A. Verification of the Voltages of C_8

The simulated voltage waveforms are shown in Fig. 9, where (a) and (b) are the results of the traditional and improved topologies, respectively. It can be seen that the



(a) In the traditional CFPRHB.



(b) In the proposed CFPRHB.

Fig. 9. Simulated voltage waveforms of C_8 at steady state.

shapes of the two waveforms are different. The waveform in Fig. 9 (b) is the inverse type of Fig. 9 (a). Both the peak and RMS voltages of the improved topology are much less than the traditional one. This is in agreement with the theoretical analysis.

B. Verification of the Lamp Current

The lamp current in each topology at the steady state is compared in Fig. 10 to double check whether it is influenced or not after the topology improvement. Obviously, the simulation results show that the lamp current is not affected based on the same parameters of the main circuit.

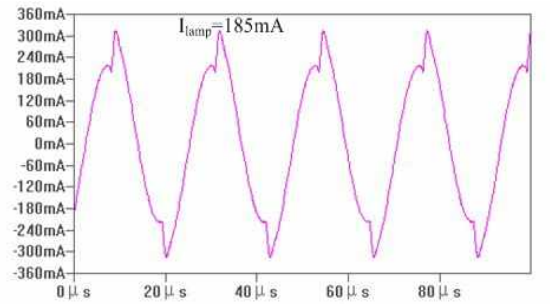
V. Experiments and Discussions

A. Voltage Comparison

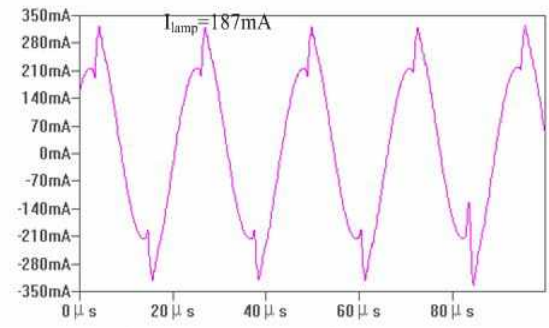
To double check the effectiveness of the proposed topology, an experimental study has been conducted. The switches are 1.1kV/4A transistors and the diodes are 1kV/1A avalanche types. Their parameters are the same as those in Table I.

The experimental waveforms of the voltage of C_8 at the steady state are shown in Fig. 11. In the traditional topology, the peak value is 730V and the RMS value is 514V, while they are 450V and 237V in the improved topology. The test results are consistent with both the simulation results and the theoretical analysis.

The start-up state is also checked as shown in Fig. 12. The solution behaves well at the worst case when the input voltage is 305VAC and at the start-up state. The voltage

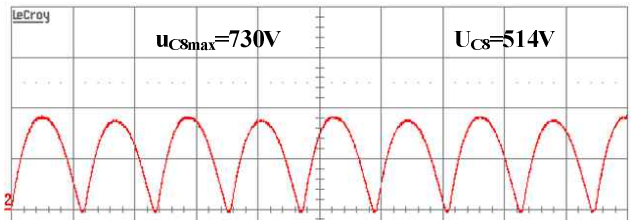


(a) In the traditional CFPRHB.

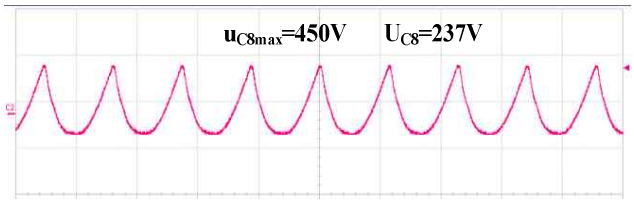


(b) in the proposed CFPRHB.

Fig. 10. Simulated waveforms of lamp current at steady state.



(a) In traditional topology (400V/div, 10μs/div).



(b) In the proposed topology (400V/div, 10μs/div).

Fig. 11. Measured voltage waveforms of C_8 at steady state.

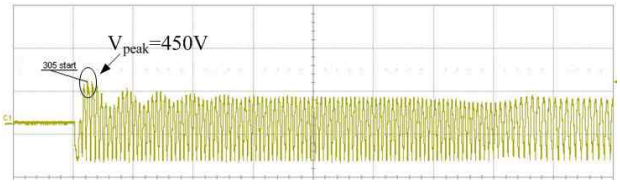


Fig. 12. Measured voltage waveform of C_8 at start-up state@305 VAC input (500V/div, 0.5s/div).

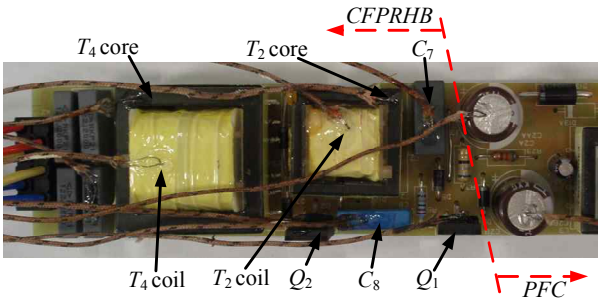


Fig. 13. Experimental setup for thermal tests.

TABLE II
THERMAL DATA OF TWO TOPOLOGIES

	Traditional CFPRHB	Improved CFPRHB
Input voltage (V)	120	120
Input power (W)	118.57	118.7
Ambient Temperature (ºC)	25	25
T_2 coil (ºC)	74.8	75.3
T_2 core (ºC)	62.2	62.7
T_4 coil (ºC)	80.7	81.6
T_4 core (ºC)	78.7	79.5
C_7 (ºC)	61.7	60.8
C_8 (ºC)	60.7	55.2
Self-rise of C_8 (ºC)	5.5	2.5

spike of C_8 is 450V which is clamped by the DC voltage according to Eq. (23). This is also consistent with the theoretical analysis.

B. Thermal Comparison

As mentioned, there are two parts in the tested sample, one is the boost PFC and the other one is the half bridge circuit, as shown in Fig. 13.

Thermal tests have been implemented on the same ballast. Some traces in the printed circuit board (PCB) are modified to change the traditional topology into the improved one. However, the positions of all of the components have not been changed in the PCB. Two thermal tests are conducted for the self-rise test of C_8. The thermal couple is located at the same capacitor and the capacitor is also located at the same position in the ballast. The only difference is that the capacitor works normally in the first test but does not work in the second test, while an additional capacitor is working at another place instead. The thermal gap of the capacitor between the two tests is defined as the self-rise of C_8.

The thermal tests are conducted at room temperature and the results are shown in Table II. All of the data are close except for the self-rise of C_8 which decreases from 5.5 ºC to 2.5 ºC based on the same input power. It is known that the thermal tests of C_8 are related to its RMS voltage. The reason why they decrease is that voltage stress is reduced in

TABLE III

PERFORMANCE DATA OF TWO TOPOLOGIES

	Traditional CFPRHB	Improved CFPRHB
Input voltage (V)	277	277
Input power (W)	115.59	115.60
THD (%)	5.52	5.28
Lamp current1 (mA)	183.3	185.1
Lamp current2 (mA)	182.5	183.0
Lamp current3 (mA)	182.6	183.0
Lamp current4 (mA)	183.9	185.5
Crest factor1	1.65	1.63
Crest factor2	1.63	1.62
Crest factor3	1.62	1.61
Crest factor4	1.64	1.63

the improved CFPRHB. This validates the effectiveness of the topology improvement.

C. Performance Comparison

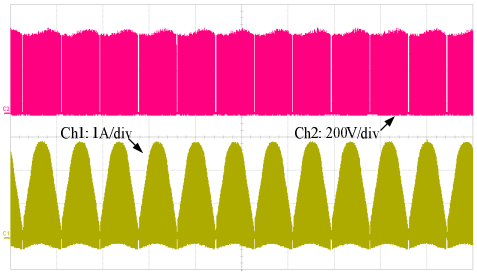
Tests are also conducted to double check the performance under 277V of input, as shown in Table III. The crest factor is defined as the ratio of the maximum value to the RMS value of the lamp current, which is the key objective in the design and should be less than 1.7. There is no obvious difference in the tested performance data between the two topologies with the same parameters, which are shown in Table I.

Considering parts A, B and C in this section, it is validated by the experimental results that the topology improvement can solve the issue of the voltage stress on C_8 and with less influence on the system performance.

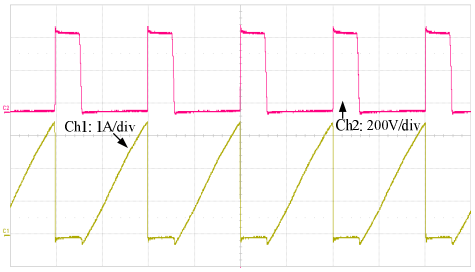
D. Other V-I mapping Tests

To validate the performance of the designed prototype, more current and voltage waveforms with descriptions are presented in Fig. 14 to Fig. 18.

The waveforms of the MOSFE in the boost PFC circuit are shown in Fig. 14 where the current and voltage waveforms are shown in Ch1 and Ch2, respectively. The tested results of the MOSFET at the steady state when the input voltage is 120V are recorded in Fig. 14(a). It can be seen that the frequency of the envelopes of both of the waveforms is 100Hz which is twice that of the AC source. The input voltage of the PFC circuit is 100Hz since it is obtained through a single-phase rectifier from the AC source. The PFC circuit is designed at the critical continuous mode which can be further validated by Fig. 14(b), the zooming of Fig. 14(a) and the fact that the input voltage is 108V. When the MOSFET is off, its voltage rises to a high level and the current decreases to zero. When it starts to be turned on, the current increases linearly and starts from zero which indicates that the current through the

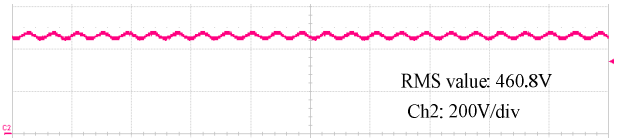


(a) At steady state@ 120V input (10ms/div).

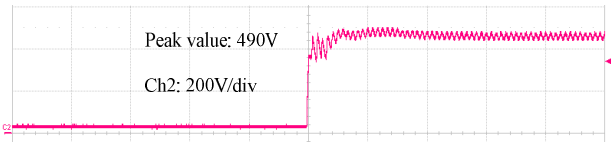


(b) At steady state@ 108V input (10μs/div).

Fig. 14. Measured waveforms of the PFC MOSFET. Ch1: Current waveform, 1A/div, Ch2: Voltage waveform, 200V/div.



(a) At steady state@ 120V input (200V/div, 10ms/div).



(b) At start-up state@ 305V input (200V/div, 10ms/div).

Fig. 15. Measured waveforms of DCBUS of PFC circuit.

boost inductor increases from zero during each switching period.

The DC output of the PFC circuit is called the DCBUS, as shown in Fig. 15. It can be seen from Fig. 15(a) that the RMS value of the DCBUS is 460.8V at the steady state. The transient response is shown in Fig. 15(b). The peak value is 490V which is within the specs of the electrolytic capacitor used in the prototype.

The voltage and current waveforms of a single ballasting capacitor are presented in Fig. 16. The ballasting capacitors are in series with lamps which means they have the same current. It can be seen from Ch1 that the RMS value of the tested voltage is 551V, which supports more voltage pressure than the lamp after ignition. This is the same as the design.

The voltage and current waveforms of the switch Q_2 are shown in Fig. 17. The voltage and current waveforms from

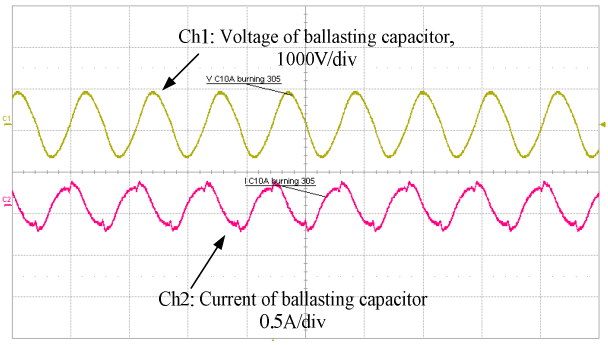
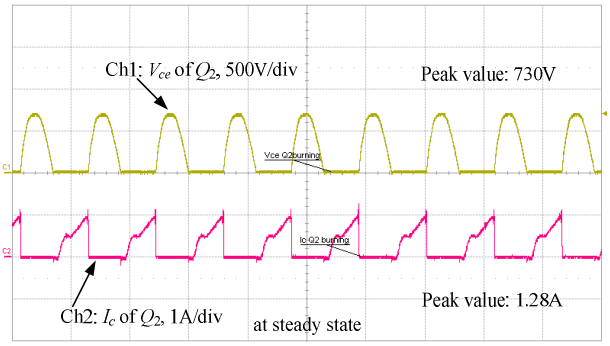
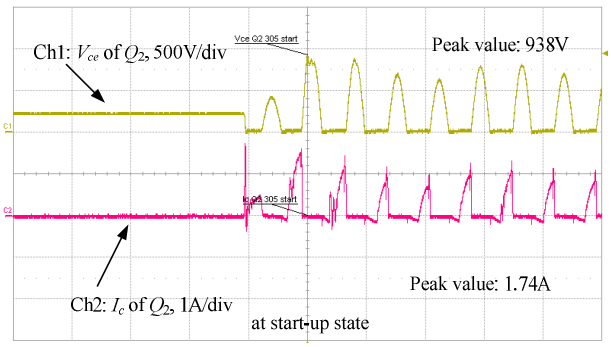


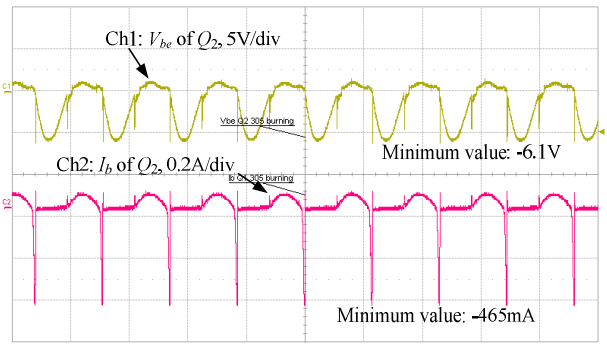
Fig. 16. Measured waveforms of each ballasting capacitor at steady state. Ch1: Voltage waveform, 1000V/div, Ch2: Current waveform, 0.5A/div.



(a) V_{ce} and I_c of Q_2 at steady state@ 305V input (20μs/div).



(b) V_{ce} and I_c of Q_2 at start-up state@ 305V input (20μs/div).



(c) V_{be} and I_b of Q_2 at steady state@ 305V input (20μs/div)

Fig. 17. Measured waveforms of Q_2. Ch1: Voltage waveform, Ch2: Current waveform.

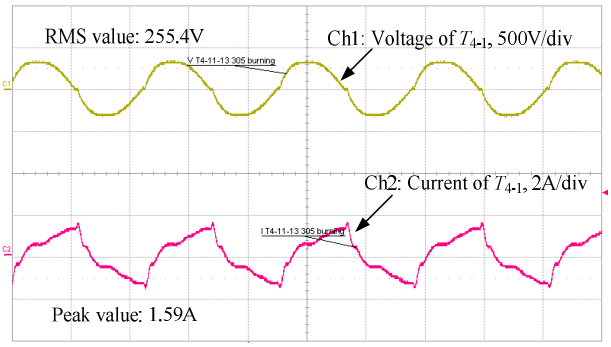


Fig. 18. Measured waveforms of $T_{4\text{-}1}$. Ch1: Voltage waveform, 500V/div, Ch2: Current waveform, 2A/div.

the collector to the emitter at both the steady and transient states are shown in Fig. 17(a) and 17(b), respectively. It can be seen that the peak values at the transient state are much larger than that those at the steady state. However, both are within the specs. The voltage and current waveform from the base to the emitter are shown in Fig. 17(c). As described in Section II, the driving winding $T_{4\text{-}3}$ is designed for Q_1 and $T_{4\text{-}4}$ is for Q_2, each of which is only 1 turn and the driving signal is sinusoidal. When the driving voltage rises to the threshold of the base to the emitter junction, Q_2 will be on and the base current I_b is kept sinusoidal, as seen in Ch1 of Fig. 17(c). It can also be observed that when V_{be} decreases to the threshold, there is a huge reversing recovery current of I_b. However, a peak value of -465mA can meet the specifications. All of the waveforms of the other switch Q_1 are similar.

The voltage and current waveforms of $T_{4\text{-}1}$ are shown in Fig. 18. The tested RMS voltage value is 255.4V, which is the same as that analyzed in Part C of Section III. It can be seen that the current rises when the voltage is positive and reverses when the voltage is negative. The tested peak value of the current is about 1.59A under which T_4 doesnot saturate and can work well.

VI. Conclusion

This paper analyzes the high voltage stress on the bypass capacitor in a traditional CFPRHB. This reveals the root cause of the failure modes of ballasts with this topology. An improved topology of a CFPRHB is then proposed. The operating principles and modeling of the proposed topology are also provided. Both a theoretical analysis and simulations have been carried out. They show that the voltage stress on C_8 in the proposed CFPRHB is significantly reduced without having a negative influence on the system performance. Hence, a capacitor with lower voltage ratings for C_8 can be used and the cost will be reduced accordingly. The proposed topology offers the advantages of higher reliability and lower cost when compared with the traditional one. Several experiments have

also been carried out. They verify both the theoretical analysis and the effectiveness of the proposed CFPRHB.

ACKNOWLEDGMENT

This work was supported by the National Natural Science Foundation of China under project 51320105002, and by the Specialized Research Fund for the Doctoral Program of Higher Education of China under project 20120092130008.

REFERENCES

[1] E. E. Hammer and T. K. Mcgowan, "Characteristics of Various F40 Fluorescent Systems at 60 Hz and High Frequency," *IEEE Trans. Ind. Applicat.*, Vol. 21, No. 1, pp. 11-16, Jan./Feb. 1985.

[2] M. Sun and B. L. Hesterman, "PSpice high-frequency dynamic fluorescent lamp model," *IEEE Trans. Power Electron.*, Vol. 13, No. 2, pp. 261-272, Mar. 1998.

[3] M. Cervi, A. R. Seidel, F. E. Bisogno, and R. N. do Prado, "Fluorescent lamp model based on the equivalent variation," in *Conf. IAS 2002*, Vol. 1, pp. 680-684, 2002.

[4] W. Yan, E. Tam, and S. Y. R. Hui, "A semi-theoretical fluorescent lamp model for time-domain transient and steady-state simulations," *IEEE Trans. Power Electron.*, Vol. 22, No. 6, pp. 2106-2115, Nov. 2007.

[5] R. L. Steigerwald, "A comparison of half-bridge resonant converter topologies," *IEEE Trans. Power Electron.*, Vol. 3, No. 2, pp. 174-182, Apr. 1988.

[6] R.-L. Lin and Y.-T. Chen, "Electronic ballast for fluorescent lamps with phase-locked loop control scheme," *IEEE Trans. Power Electron.*, Vol. 21, No. 1, pp. 254-262, Jan. 2006.

[7] L. Laskai, P. N. Enjeti, and I. J. Pitel, "White-noise modulation of high-frequency high-intensity discharge lamp ballasts," *IEEE Trans. Ind. Applicat.*, Vol. 34, No. 3, pp. 597-605, 1998.

[8] S. Ben-Yaakov, M. Shvartsas, and S. Glozman, "Statics and dynamics of fluorescent lamps operating at high frequency: modeling and simulation," *IEEE Trans. Ind. Applicat.*, Vol. 38, No. 6, pp.1486-1492, Nov./Dec. 2002.

[9] J. M. Alonso, A. J. Calleja, J. Ribas, E. L. Corominas, and M. Rico-Secades, "Analysis and design of a novel single-stage high-power-factor electronic ballast based on integrated buck half-bridge resonant inverter," *IEEE Trans. Power Electron.*, Vol. 19, No. 2, pp. 550-559, March 2004.

[10] J. M. Alonso, J. Cardesin, A. J. Calleja, M. Rico-Secades, and J. Garcia, "A fluorescent lamp electronic ballast for railway applications based on low-cost microcontroller," *IEEE Trans. Ind. Applicat.*, Vol. 41, No. 5, pp. 1391-1400, Sep./Oct. 2005.

[11] A. S. de Morais, V. J. Farias, L. C. de Freitas, E. A. Alves Coelho, and J., Jr. Batista Vieira, "A high power factor ballast using a single switch with both power stages integrated," *IEEE Trans. Power Electron.*, Vol. 21, No. 2, pp. 524-531, Mar. 2006.

[12] F. J. Diaz, F. J. Azcondo, R. Casanueva, C. Branas, and R. Zane, "Digital control of a low-frequency square-wave electronic ballast with resonant ignition," *IEEE Trans. Ind. Electron.*, Vol. 55, No. 9, pp. 3180-3191, Sep. 2008.

[13] C. Chang, J. Chang, and G. W. Bruning, "Analysis of the Self-Oscillating Series Resonant Inverter for Electronic Ballasts," *IEEE Trans. Power Electron.*, Vol. 14, No. 3, pp. 533-540, May 1999.

[14] J. Ribas, J. M. Alonso, A. J. Calleja, E. L. Corominas, M. Rico-Secades, and J. Cardesin, "Low cost single-stage electronic ballast based on a self oscillating resonant inverter integrated with a buck-boost PFC circuit," *IEEE Trans. Ind. Electron.*, Vol. 48, No. 6, pp. 1196-1204, Dec. 2001.

[15] A. R. Seidel, F. E. Bisogno, H. Pinheiro, and R. N. do Prado, "Self-oscillating dimmable electronic ballast," *IEEE Trans. Ind. Electron.*, Vol. 50, No. 6, pp. 1267-1274, Dec. 2003.

[16] A. Campos, M. A. Dalla Costa, R. A. Pinto, and R. N. Prado, "Fixed frequency self-oscillating electronic ballast to supply multiple lamps," in *Conf. PESC 2004,* pp. 413-418, 2004.

[17] R.-L. Lin and Z.-Q. Wang, "2.56-MHz self-oscillating electronic ballast with constant-lamp current control for metal halide lamp," *IEEE Trans. Power Electron.*, Vol. 22, No. 3, pp. 839-844, May 2007.

[18] T.-H. Yu, L.-M. Wu, and T.-F. Wu, "Comparisons among self-excited parallel resonant, series resonant and current-fed push-pull electronic ballast," in *Proc. APEC 1994*, Vol. 1, pp. 421-426, 1994.

Qingsong Wang received his B.S. and M.S. degrees in Electrical Engineering from Zhejiang University, Hangzhou, China, in 2004 and 2007, respectively. He is presently working toward his Ph.D. degree in Electrical Engineering at Southeast University, Nanjing, China. From July 2004 to July 2005, he was an Engineer at Shihlin Electronic & Engineering Co., Ltd, Suzhou, China. From July 2007 to August 2011, he was an Engineer in the Global Development Center of Philips Lighting Electronics, Shanghai, China. In October 2010, he was promoted to a Senior Engineer. From August 2011 to September 2013, he was a Lecture in the PLA University of Science and Technology, Nanjing, China. He is a student member of the IEEE. His current research interests include electronic ballasts, the multilevel rectifiers of current sources, and the application of power electronics to power systems.

Ming Cheng received his B.S. and M.S. degrees from the Department of Electrical Engineering, Southeast University, Nanjing, China, in 1982 and 1987, respectively, and his Ph.D. degree from the Department of Electrical and Electronic Engineering, University of Hong Kong, Hong Kong SAR, China, in 2001. Since 1987, he has been with Southeast University, Nanjing, China, where he is currently a Distinguished Professor in the School of Electrical Engineering and the Director of the Research Center for Wind Power Generation. His current teaching and research interests include electrical machines, motor drives for electric vehicles, and renewable energy generation. He has authored or coauthored more than 300 technical papers and four books. He is also the holder of 55 patents in these areas. Professor Cheng is a Fellow of the IET and IEEE. He has served as Chair and Organizing Committee Member for many international conferences. He is a Distinguished Lecturer of the IEEE Industry Applications Society (IAS) in 2015/2016.

Bing Zhang received his B.S. degree in Electrical Engineering from the Shangdong University of Technology, Zibo, China, in 2012. He is presently working toward his M.S. degree in Electrical Engineering at Southeast University, Nanjing, China. His current research interests include topologies, devices, modeling and control for high-power conversion.