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Analysis and Design of a DC-Side Symmetrical Class-D ZCS Rectifier for the PFC of Lighting Applications

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Abstract

This paper proposes the analysis and design of a DC-side symmetrical zero-current-switching (ZCS) Class-D current-source driven resonant rectifier to improve the low power-factor and high line current harmonic distortion of lighting applications. An analysis of the junction capacitance effect of Class-D ZCS rectifier diodes, which has a significant impact on line current harmonic distortion, is discussed in this paper. The design procedure is based on the principle of the symmetrical Class-D ZCS rectifier, which ensures more accurate results and provides a more systematic and feasible analysis methodology. Improvement in the power quality is achieved by using the output characteristics of the DC-side Class-D ZCS rectifier, which is inserted between the front-end bridge-rectifier and the bulk-filter capacitor. By using this symmetrical topology, the conduction angle of the bridge-rectifier diode current is increased and the low line harmonic distortion and power-factor near unity were naturally achieved. The peak and ripple values of the line current are also reduced, which allows for a reduced filter-inductor volume of the electromagnetic interference (EMI) filter. In addition, low-cost standard-recovery diodes can be employed as a bridge-rectifier. The validity of the theoretical analysis is confirmed by simulation and experimental results.

Key words: Class-D ZCS rectifier, Electronic ballast, Lighting applications, Line harmonic, Power-factor correction, Power quality, Symmetrical circuit

I. INTRODUCTION

It is very well known that line current harmonic distortion causes several problems such as a voltage distortion, noise, heating that reduces efficiency, and reduced capacity of energy suppliers. In order to overcome these drawbacks, the need to comply with standards has forced the use of power-factor correction (PFC) in power converters. The development of high power-factor converters with minimized current total harmonics distortion (THD_i) for lighting applications such as the electronic ballasts for gas-discharge lamps [1]-[18] and the drivers for light-emitting diodes (LED) [19]-[25] have to meet the lighting standard regulations of the International Electrotechnical Commission (IEC) 61000-3-2 Class-C limit for harmonic current emissions [26].

Recently, the use of resonant rectifiers for the PFC of single-stage converters has become attractive, due to the advantages of resonant-rectifier based PFC since a theoretical analysis can be used to provide a systematic, simple, and feasible solution. Examples of this are the zero-voltage-switching (ZVS) AC-side Class-E current-source driven rectifier for PFC (CECS-RPFC) [4], and the ZVS AC-side Class-DE current-source driven rectifier for PFC

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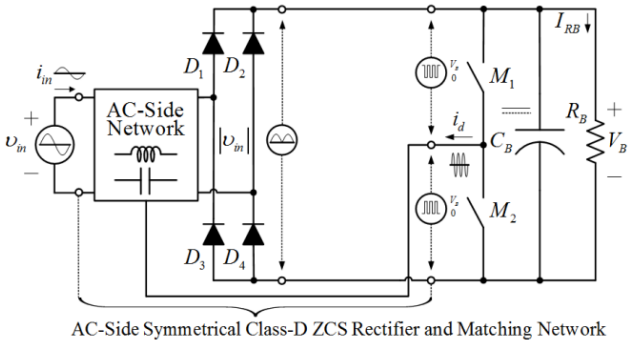

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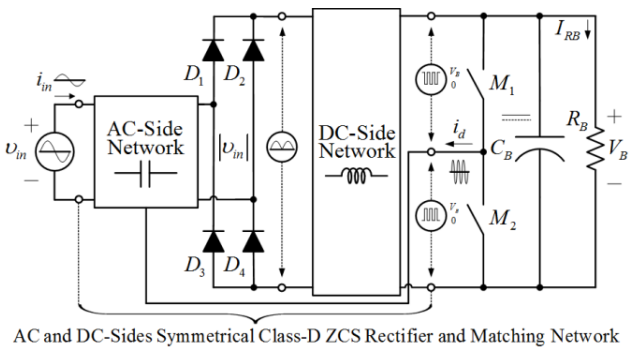

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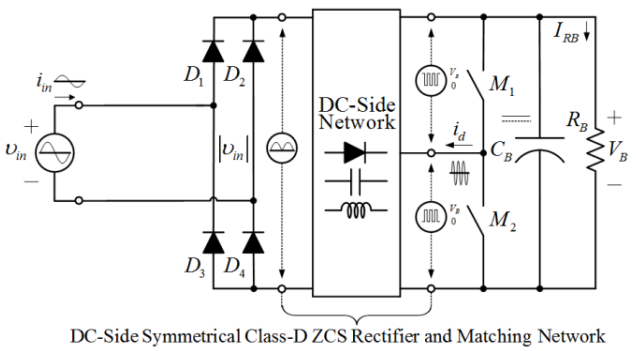

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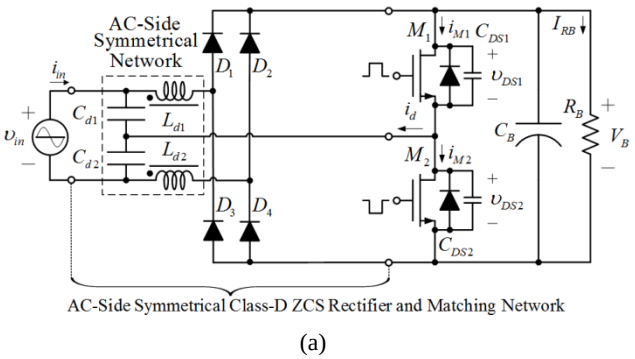
Fig. 1. Circuit diagram of symmetrical CDCS-RPFCs.



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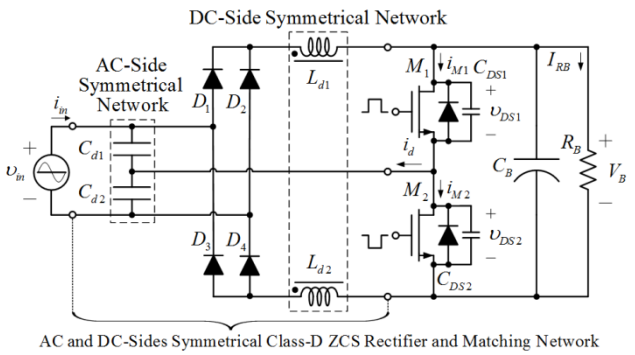

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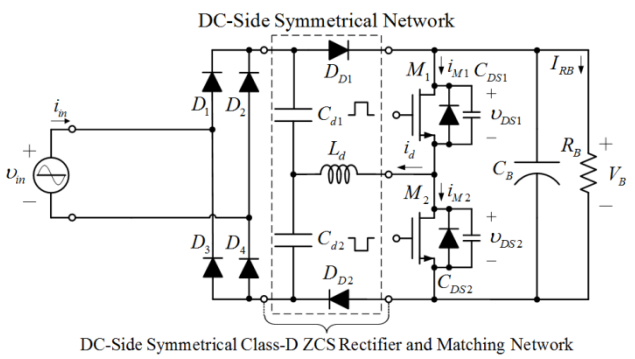

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Fig. 2. Family of symmetrical CDCS-RPFCs.

(CDECS-RPFC) [5], [8]. However, the main drawbacks of the previously proposed CECS-RPFC and CDECS-RPFC topologies are their low efficiency because they suffer from high current stresses in the power switches near the zero-crossing of the line voltage, and the fact that fast recovery diodes are required for the bridge-rectifier. As a result, these ballast topologies are unattractive for low-cost commercial applications. A ZVS DC-side asymmetrical CDECS-RPFC has been proposed in [9] and standard-recovery diodes can be used as a bridge-rectifier. The major problem with this technique is the high current stresses in the power switches, which results in low efficiency. Recently, a zero-current-switching DC-side asymmetrical Class-D current-source driven rectifier for PFC (CDCS-RPFC) has been proposed in [17] and it has greatly reduced current stress. However, the main disadvantage of this topology is the use of a large electromagnetic interference (EMI) filter due to the large high frequency ripple current of the line current. Therefore, it is very attractive to explore a single-stage PFC converter for lighting applications that has low current stresses, high efficiency and low cost.

The objective of this paper is to introduce a new topology for a resonant rectifier for PFC, called a DC-side symmetrical ZCS Class-D current-source driven rectifier. The efficiency of this circuit is higher than that of the other single-stage topologies, because the zero value of the driving-current near the zero-crossing of the line voltage can be obtained. The line current in the proposed symmetrical Class-D ZCS rectifier has twice the switching frequency when compared to the asymmetrical Class-D ZCS rectifier [17], which allows the switching ripple current to be removed with a smaller EMI filter. In additional, standard-recovery diodes can be used as

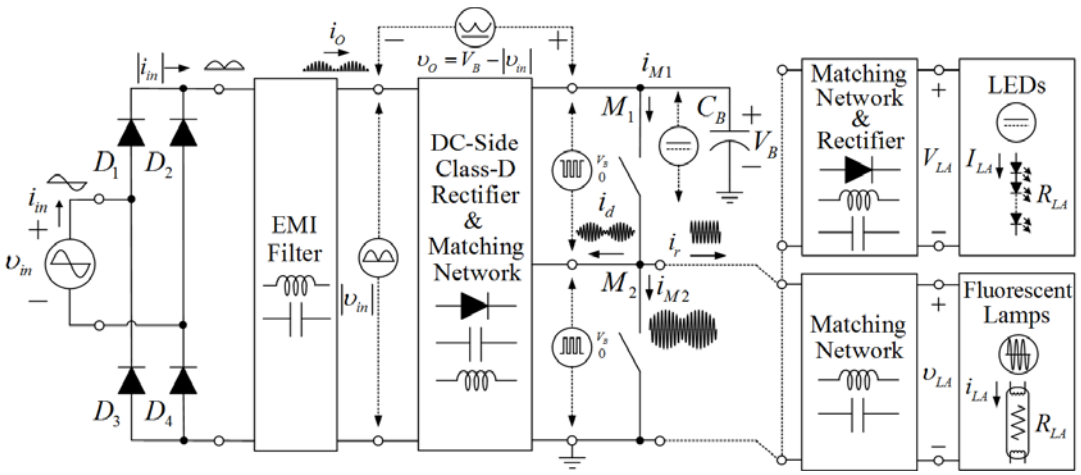


Fig. 3. Conceptual diagram of DC-side CDCS-RPFC for lighting applications.

the bridge rectifier. Thus, the cost can be reduced.

This paper is organized as follows. Section II presents the basic concepts of the proposed topology. In Section III, a circuit description is provided. The operating principle is reported in Section IV. A design example of the proposed topology is presented in Section V. Section VI gives a conduction loss analysis of the CDCS-RPFC. Simulation and experimental results to confirm the validity of the theoretical analysis and design procedure are presented in Section VII. Section VIII gives a discussion of the junction-capacitance effect of the CDCS-RPFC. Section IX gives some conclusions to summarize the merits of this paper.

II. Proposed Topology

Various configurations for the DC-side CDCS-RPFC are shown in Fig. 1. The high-frequency current-source to drive a symmetrical CDCS-RPFC is supplied by the square-wave output voltage of the power converter through a matching network. Symmetrical CDCS-RPFC networks can be inserted on the AC-side, both the AC and DC side, or the DC-side without any restrictions as depicted in Fig. 1(a)-1(c), respectively. However, the symmetrical CDCS-RPFC can employ low-cost standard-recovery diodes as a bridge-rectifier due to the fact that the EMI filter is connected in cascade with the front-end bridge-rectifier. Circuit diagrams of the symmetrical CDCS-RPFCs, without considering the EMI filter, are depicted in Fig. 2(a)-2(c). In order to simplify the analysis of the DC-side symmetrical CDCS-RPFC, the input voltage is considered only in a positive half-cycle and the following assumptions are made: Fundamental-component approximation is used in the analysis of the rectifier with adequate accuracy.

1. The operation is steady-state with a constant switching frequency, f_s, and two main switches are alternately ON and OFF with a duty cycle, D, that is nearly 0.5.
2. All of the switches and diodes are considered to be ideal.
3. The capacitance of the bulk-filter capacitor, C_B, is large enough. Thus, the DC-bus voltage, V_B, can be regarded as a voltage source.
4. The lamp is regarded as an open circuit before ignition and as a resistive load, R_{LA}, at the steady-state.

III. Circuit Description

Fig. 3 shows a conceptual diagram of a DC-side symmetrical Class-D ZCS rectifier and an EMI filter. They are inserted between the front-end bridge-rectifier and the bulk-filter capacitor to increase the conduction angle of the bridge-rectifier diode current for obtaining a near unity power-factor and low line current harmonics distortion. In addition, a part of the DC-side Class-D ZCS rectifier performs the function of a pass device, in which the voltage difference, $\upsilon_O = V_B - |\upsilon_{in}|$, is dropped. Furthermore, it roughly matches the required basic characteristics for power-factor correction.

The proposed ZCS CDCS-RPFC displayed in Fig. 2(c), consists of standard-recovery bridge-rectifier diodes, D_1–D_2–D_3–D_4, and fast-recovery diodes D_{D1} and D_{D2}, which are the DC-side symmetrical CDCS-RPFC. The inverter semi-state, composed of two switches, M_1 and M_2, is supplied by a bulk-filter capacitor, C_B, which is replaced by an ideal voltage source, since the DC-bus voltage, V_B, across this capacitor is nearly constant. This results in constant lamp current amplitudes. The inverter is a Class-D ZVS resonant inverter, which has been presented in many studies [1], [27]. A matching network, L_d–C_{d1}–C_{d2}, is fed by a high-frequency square-wave voltage source from the Class-D ZVS resonant inverter. The square-wave voltage is converted into a high-frequency current source to drive the DC-side symmetrical CDCS-RPFC by the matching network. Additionally, two capacitors, C_{d1} and C_{d2}, serve the functions of a filter capacitor and a coupling capacitor.

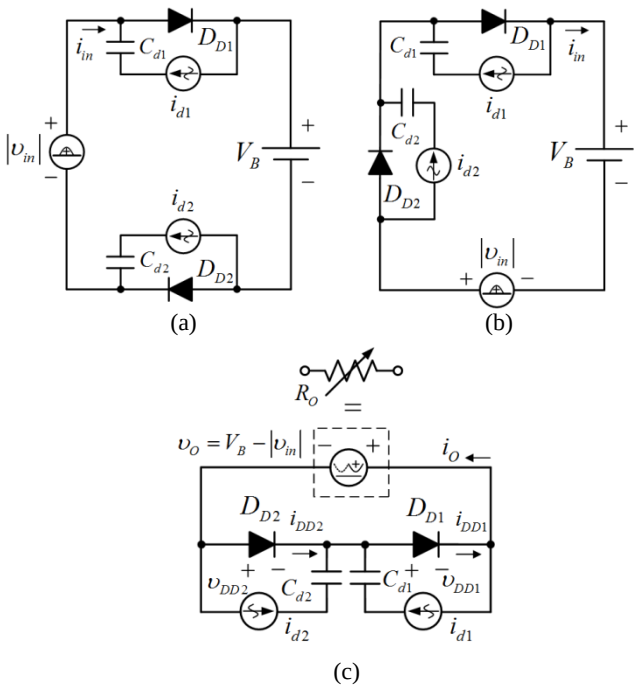
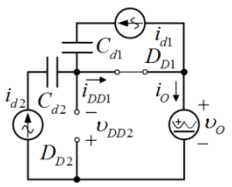
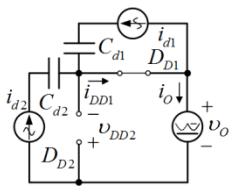
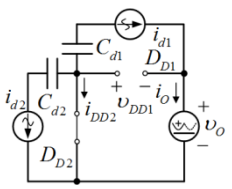
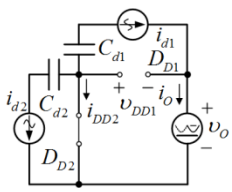


Fig. 4. Circuit derivation of PFC with DC-side symmetrical Class-D ZCS rectifier during positive half-cycle of line voltage.

TABLE I
EQUIVALENT CIRCUIT OPERATION MODES IN ONE SWITCHING CYCLE OF SYMMETRICAL CDCS-RPFC.

Mode	Positive Half-Cycle	Negative Half-Cycle
Mode 1		
Mode 2		

IV. PRINCIPLE OF THE TOPOLOGY

The operation principle of the DC-side symmetrical Class-D ZCS rectifier in the PFC semi-stage is displayed by the equivalent circuit shown in Fig. 4. The line voltage is represented as $\upsilon_{in} = V_{in} \sin \omega_L t$, where ω_L is the line angular frequency. The bridge-rectifier output is a full-wave rectified sinusoidal voltage source $|\upsilon_{in}| = V_{in} |\sin \omega_L t|$. The current waveform of the matching network that drives the DC-side symmetrical CDCS-RPFC is assumed to be a sine wave and is represented as $i_d = I_d \sin \omega_s t$, where ω_s is the switching angular frequency. The driving-current, $i_d = i_{d1} = i_{d2}$, is forced by the symmetrical matching network, L_d–C_{d1}–C_{d2}, which is illustrated in Fig. 2(c). It is assumed that the switching frequency, f_s, is much higher than the line frequency, f_L.

Therefore, during the positive half-cycle of the line voltage, the full-wave rectified sinusoidal voltage source, $|\upsilon_{in}|$, appears as a short circuit in the AC component. As shown in Fig. 4(a), the first driving current, i_{d1}, and the series capacitor, C_{d1}; and the second driving current, i_{d2}, and the series capacitor, C_{d2}, can be connected in parallel with the diode, D_{D1}, and the diode, D_{D2}, respectively. In addition, the parallel connection of D_{D1} with the series connection $C_{d1,}$ i_{d1}; and the parallel connection of D_{D2} with the series connection $C_{d2,}$ i_{d2} are connected in series with the voltage source, $|\upsilon_{in}|$. The sequence of these elements is interchangeable, as shown in Fig. 4(b). In this circuit, the DC-bus voltage source, V_B, and the full-wave rectified sinusoidal voltage source, $|\upsilon_{in}|$, are connected in series. Thus, these voltage sources can be combined into one voltage source, $\upsilon_O = V_B - |\upsilon_{in}|$, as shown in Fig. 4(c). However, the output voltage of the Class-D ZCS rectifier is forced by the voltage source υ_O. This leads to a varying load resistance, R_O, for the ZCS Class-D rectifier. The equivalent circuit of the DC-side symmetrical CDCS-RPFC during the negative half-cycle of the line voltage is similar to the equivalent circuit during the positive half-cycle of the line voltage. Thus, the explanations are omitted.

The current alternatively flows through diodes D_{D1} and D_{D2} when each diode is ON, as shown in Table I. The diodes begin to turn off when their current reaches zero to reduce the turn-off switching loss. The key waveforms of the current and voltage in one-switching cycle near the peak of the line voltage of the proposed circuit are illustrated in Fig. 5. Figure 6(a) shows a sinusoidal line voltage waveform in one line cycle. Fig. 6(b) show the full-wave rectified line voltage, $|\upsilon_{in}|$, and the DC-bus voltage, V_B, waveforms. Figure 6(c) shows the combined voltage, $V_B - |\upsilon_{in}|$, waveform. In these figures, if the instantaneous value of υ_{in} is positive and low, the output voltage of the Class-D ZCS rectifier, $V_B - |\upsilon_{in}|$, is high, and the rectifier-diode current is low. Thus, the average value of the rectifier diode current in one switching cycle is also low. Conversely, if the instantaneous value of υ_{in} is positive and high, the output of the Class-D ZCS rectifier, $V_B - |\upsilon_{in}|$, is low, and the rectifier-diode current is high.

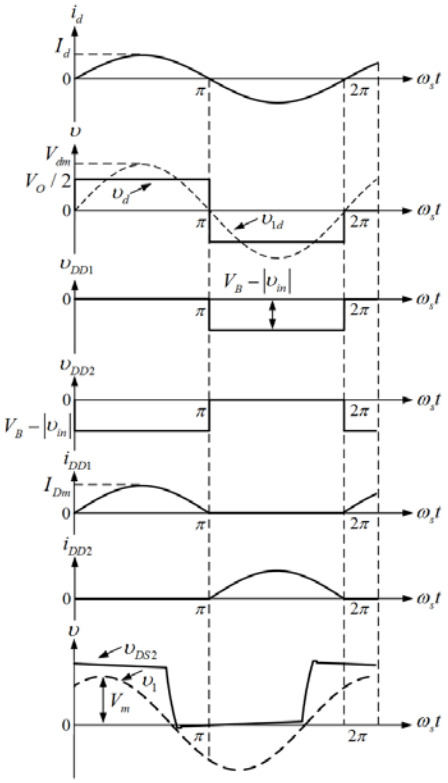


Fig. 5. Key waveforms in one switching cycle of the Class-D ZCS rectifier.

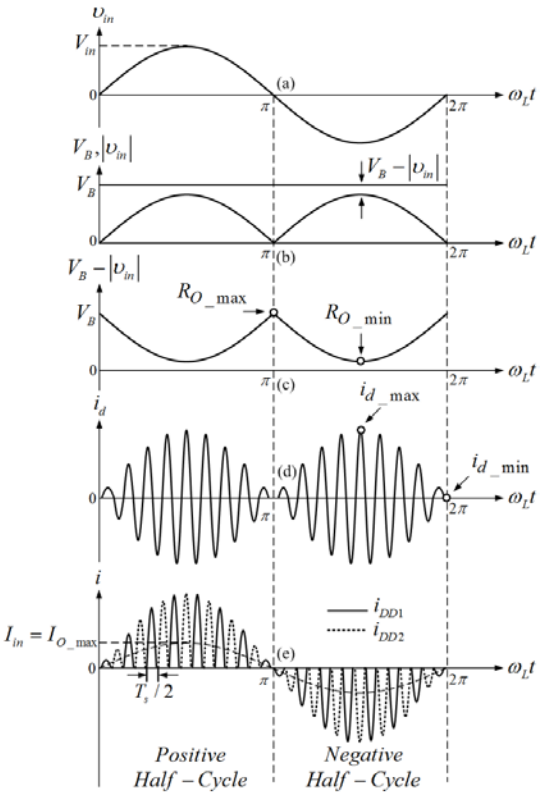


Fig. 6. Conceptual waveforms in one line cycle of CDCS-RPFC.

Thus, the average value of the diode current in one switching cycle is also high. Fig. 6(d) shows the driving-current, i_d, which is forced by the symmetrical matching network, L_d–C_{d1}–C_{d2}. The input-current waveform, i_{in}, which is the filtered average diode current of the symmetrical Class-D ZCS rectifier, is displayed in Fig. 6(e). This waveform shows that the line current in the symmetrical Class-D ZCS rectifier has twice the switching frequency, which allows the switching ripple current to be easily removed with a smaller EMI filter. For the negative half-cycle of the line voltage, one can be considered to be the same as with the positive half-cycle of the line voltage.

Fig. 7 shows the circuit configuration of the new proposed single-stage electronic ballast with the DC-side symmetrical ZCS CDCS-RPFC. The principle of operation of the proposed circuit is illustrated by the equivalent circuit shown in Fig. 8. The input impedance of the Class-D ZCS rectifier is represented by an input resistor, R_i. The voltage transfer function, M_V, [29] of this circuit, when the total conversion efficiency is assumed to be equal to 1, can be described by:

$$M_V = \frac{V_O}{V_B} = \frac{1}{\sqrt{1+Q^2\left(\frac{\omega_s}{\omega_r}-\frac{\omega_r}{\omega_s}\right)^2}}. \quad (1)$$

where ω_r is the resonant frequency, and Q is the loaded quality factor of the matching network in the PFC stage. The range of M_V is from zero to 1. The equivalent circuit in Fig. 8(a) can be divided into two parts. A simplified circuit of the CDCS-RPFC semi-stage and an equivalent circuit of the inverter semi-stage are illustrated in Figs. 8(b) and (c), respectively. The coupling capacitor, C_s, the resonant capacitor, C_r, and the lamp resistance, R_{LA}, of the Class-D ZVS resonant inverter are converted to a series R_s–C_{rs} circuit and the MOSFETs are modeled by switches with the on-resistances, r_{DS1} and r_{DS2}. The resistances r_{Ld} and r_{Lr} represent the equivalent resistances of the inductors L_d and L_r, respectively. From Fig. 8(b), the minimum value of the load resistance, $R_{O\_\min}$, occurs at the minimum output voltage, $\upsilon_{O\_\min}$, as does the maximum output current, $i_{O\_\max}$, of the Class-D ZCS rectifier.

V. Design of the Proposed Topology

A design example is shown is this section to demonstrate the validity of the theoretical analysis. The proposed DC-side symmetrical CDCS-RPFC for electronic ballast applications can be divided into three parts: the PFC semi-stage, the ballast semi-stage and the EMI filter.

A. Design of the PFC Semi-Stage

The electronic ballast was designed to handle a line rms voltage, V_{irms}, of 220 V and a line frequency, f_L, of 50 Hz. It was assumed that the total ballast efficiency, η, was equal to

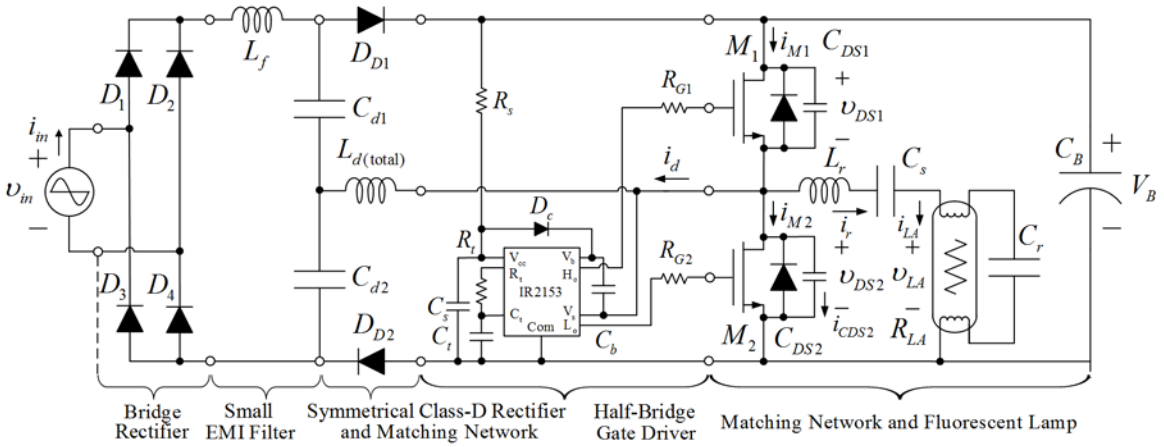


Fig. 7. Circuit configuration of proposed topology for electronic ballast application.

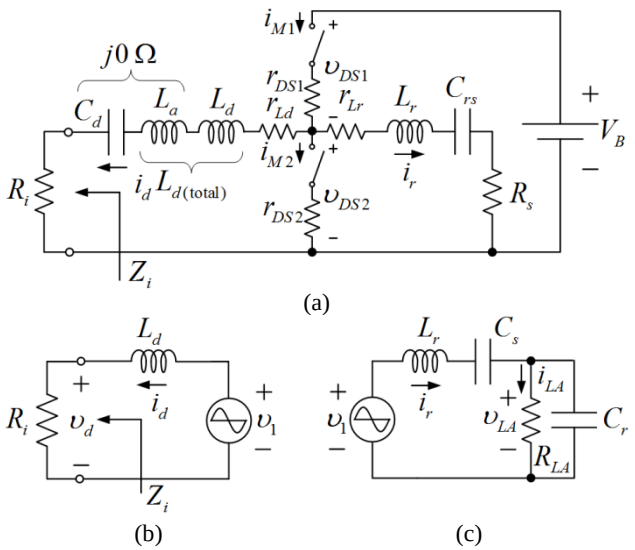


Fig. 8. Equivalent circuits of proposed high-power-factor single-stage electronic ballast.

0.93. The ballast drew the sine wave input line current. The input power of the proposed DC-side symmetrical CDCS-RPFC is determined by:

$$P_{in}=\frac{P_{out}}{\eta}=\frac{34}{0.93}=36.559\ \text{W}. \tag{2}$$

where P_{out} is the output power of the fluorescent lamp when operated at a high frequency. The amplitude of the ballast input line current is calculated from:

$$I_{in}=\frac{\sqrt{2}P_{in}}{V_{irms}}=\frac{\sqrt{2}\times 36.559}{220}=0.235\ \text{A}. \tag{3}$$

It is assumed that the Class-D ZCS rectifier is driven by an ideal high-frequency sinusoidal current-source. When $I_{in}=I_{Omax}$, the magnitude of the high-frequency driving-current at full load is:

$$I_{d\_\max}=\pi I_{O\_\max}=\pi\times 0.235=0.738\ \text{A}. \tag{4}$$

The voltage ratio V_B/V_{in} = 1.1 was chosen due to it providing a good tradeoff between an appropriate value of the harmonic distortion of line current, i_{in}, and the voltage stress of the main switches, υ_{DS} ; the amplitude of the line voltage $V_{in}=\sqrt{2}V_{irms}\approx 311$ V; and the DC-bus voltage $V_B\approx 342$ V. The input impedance of the Class-D ZCS rectifier at a full load, $R_{i\_\min}$, is obtained by:

$$\begin{aligned}R_{i\_\min}&=\frac{V_{in}^2}{\pi^2 P_{in}}\left(\frac{V_B}{V_{in}}-1\right)\\&=\left(\frac{311^2}{\pi^2\times 36.559}\right)\times\left(\frac{342}{311}-1\right)=26.719\ \Omega.\end{aligned} \tag{5}$$

From Fig. 8(b), the value of the inductance, L_d, is given from:

$$\begin{aligned}L_d&=\frac{\sqrt{\left(\frac{2V_B}{\pi I_{d\_\max}}\right)^2-R_{i\_\min}^2}}{2\pi f_s}\\&=\frac{\sqrt{\left(\frac{2\times 342}{\pi\times 0.738}\right)^2-26.719^2}}{2\times\pi\times 50\times 10^3}=935.215\ \mu\text{H}.\end{aligned} \tag{6}$$

The switching frequency, f_s, is 50 kHz. For a finite value of the capacitance C_d = C_{d1} = C_{d2}, an additional L_a can be added to L_d to compensate for the reactance of C_d = 100 nF. The value of the additional inductance is given by:

$$L_a=\frac{1}{4C_d\pi^2 f_s^2}=\frac{1}{4\times 100\times 10^{-9}\times\pi^2\times(50\times 10^3)^2}=101.321\ \mu\text{H}. \tag{7}$$

The total inductance, $L_{d(\text{total})}$, is expressed as:

$$L_{d(\text{total})}=L_d+L_a=935.215\times 10^{-6}+101.321\times 10^{-6}=1.036\ \text{mH}. \tag{8}$$

To achieve a ripple voltage of less than 1%, the value of the bulk-filter capacitor is determined by:

$$C_B\geq\frac{P_{in}}{0.04\pi f_L V_B^2}=\frac{36.559}{0.04\times\pi\times 50\times 342^2}=49.746\ \mu\text{F}. \tag{9}$$

The E6 standard value of 68 μF is selected for C_B.

B. Design of the Ballast Semi-Stage

The Class-D ZVS resonant inverter shown in Fig. 8(c),

was designed by using the design procedure defined elsewhere [1], [28]. The switching frequency should be selected to be above the resonant frequency to ensure the ZVS condition. A 36-W fluorescent lamp (TLD36W/856) from Philips is used in this design. At startup, the resonant circuit operates with a high-quality factor that generates a high ignition voltage to strike the lamp. Because the lamp is high frequency driven, the steady-state lamp resistance is:

$$R_{LA} = \frac{V_{LA(rms)}^2}{P_{out}} = \frac{103^2}{34} = 312.029\,\Omega.. \quad (10)$$

The relationship among the loaded-quality factor, Q_L, of the inverter semi-stage, the DC-bus voltage, V_B, and the rms lamp voltage, $V_{LA(rms)}$, is described by:

$$Q_L = \frac{\pi V_{LA(rms)}}{\sqrt{2}V_B} = \frac{\pi \times 103}{\sqrt{2} \times 342} = 0.669. \quad (11)$$

The resonant inductor, L_r, is expressed as:

$$L_r = \frac{R_{LA}}{Q_L \omega_r} = \frac{312.029}{0.669 \times 2 \times \pi \times 50 \times 10^3} = 1.484\,\text{mH}. \quad (12)$$

The resonant capacitor C_r is determined by:

$$C_r = \frac{Q_L}{R_{LA}\omega_r} = \frac{0.669}{312.029 \times 2 \times \pi \times 50 \times 10^3} = 6.824\,\text{nF}. \quad (13)$$

The E6 standard value of 6.8 nF is selected for C_r. In order to simplify the design procedure, a close to parallel resonance was assumed. Therefore, the DC-blocking capacitor, C_s, is selected to be a hundred times the resonant capacitor, C_r, so that C_s is 0.68 μF.

C. Design of the EMI Filter

The design of the EMI filter in Fig. 7 can be found elsewhere [30]. The line current of the CDCS-RPFC consists of the high-frequency current components of the switching frequency, f_s. Thus, a second order low-pass filter is employed at the DC-side of the bridge-rectifier to filter these high-frequency current harmonics. The upper limit capacitance of the filter capacitor, $C_{f\_\max}$, is calculated from:

$$C_{f\_\max} = \frac{I_{in}\tan\theta}{4\pi f_L V_{in}} = \frac{0.235 \times \tan 2.562^\circ}{4 \times \pi \times 50 \times 311} = 53.811\,\text{nF}. \quad (14)$$

where f_L is the line frequency. It was assumed that the displacement power-factor, $\cos\theta$, was equal to 0.999. However, the filter capacitor, C_f, should be lower than $C_{f\_\max}$. Thus, a value of 50 nF is selected for C_f and represented as $C_f = C_{d1}C_{d2} / (C_{d1} + C_{d2})$. Finally, the filter inductor, L_f, is determined by:

$$L_f = \frac{1}{(2\pi f_c)^2 C_f} = \frac{1}{\left(2 \times \pi \times 10 \times 10^3\right)^2 \times 50 \times 10^{-9}} \approx 5\,\text{mH}. \quad (15)$$

where f_c is the cut-off frequency, to ensure a low distortion, the cut-off frequency, f_c, should be at least ten times lower than the switching frequency, f_s.

VI. Conduction Loss Analysis

The losses are generally divided into two parts: the conduction losses and the switching losses. However, the switching losses can be neglected, because the fast-recovery diodes, D_{D1} and D_{D2}, are turn off under ZCS and the power MOSFETs, M_1 and M_2, are turned on under ZVS. Likewise, the conduction losses due to the parasitic resistance in the capacitors are very small. Therefore, their effects were neglected. The rms value of the resonant current in the ballast semi-stage, $I_{r,rms}$, is calculated from:

$$\begin{aligned} I_{r,rms} &= \frac{\sqrt{2}V_B Q_L \sqrt{Q_L^2 + 1}}{\pi R_L} \\ &= \frac{\sqrt{2} \times 342 \times 0.669 \times \sqrt{0.669^2 + 1}}{\pi \times 312.029} \\ &= 397.137\,\text{mA}. \end{aligned} \quad (16)$$

The power loss in each of the MOSFETs' forward resistance, r_{DS}, can be obtained as:

$$\begin{aligned} P_{rDS} &= \frac{\left(\left(\frac{1.57I_{in} + I_r}{\sqrt{2}}\right)\sqrt{\frac{2+m^2}{2}}\right)^2 \times r_{DS}}{2} \\ &= \frac{\left(\left(\frac{1.57 \times 0.235 + 397.137 \times 10^{-3}}{\sqrt{2}}\right)\sqrt{\frac{2+0.33^2}{2}}\right)^2 \times 0.48}{2} \\ &= 78.304\,\text{mW}. \end{aligned} \quad (17)$$

The converter uses MOSFETs (STMicroelectronics IRF740), with on-resistances, r_{DS}, of 0.48 Ω. In case of the ZCS-RPFC [17], the envelope of the driving-current is an AM waveform with a modulation index of m = 0.33. The result has shown that the current stresses of the power MOSFETs have been significantly reduced when compared to the previously reported CECS-RPFC and CDECS-RPFC topologies [4], [5], [8], [9]. The bridge rectifier was built using standard-recovery diodes (Fairchild Semiconductor 1N4006) with a forward voltage drop of V_D = 0.82 V. The power loss in each of the bridge rectifier diodes, D_1–D_4, due to the forward voltage, V_D, is obtained as:

$$P_{DB} = \frac{V_D I_{in}}{2} = \frac{0.82 \times 0.235}{2} = 96.35\,\text{mW}. \quad (18)$$

The DC-side symmetrical CDCS-RPFC was built using two fast-recovery diodes, D_{D1}–D_{D2}, (Fairchild Semiconductor UF4006) with a forward voltage drop of V_D = 1.08 V. The power loss in these fast-recovery diodes, due to the forward voltage, V_D, is:

$$P_{DD} = \frac{2V_D I_d}{\pi^2} = \frac{2 \times 1.08 \times 0.718}{\pi^2} = 157.136\,\text{mW}. \quad (19)$$

The equivalent series resistance (ESR) of the filter inductor, r_{Lf}, is 1.432 Ω. Thus, the conduction loss in the filter inductor, P_{rLf}, can be obtained as:

TABLE II
PARAMETERS OF POWER CIRCUIT

Parameter	Part Number and Value	Type
Bridge Rectifier and EMI Filter		
D_1–D_4	1N4006	Standard-Recovery Diode
C_f	50 nF	Polypropylene
L_f	5 mH	EE20/10/6 N87-EPCOS
PFC Stage		
D_{D1} and D_{D2}	UF4006	Fast-Recovery Diode
C_{d1} and C_{d2}	100 nF	Polypropylene
$L_{d(\text{total})}$	1.03 mH	EE25/13/7 N87-EPCOS
Inverter Stage		
M_1 and M_2	IRF740	N-Channel MOSFET
C_B	68 μF	Electrolytic E6 Series
C_r	6.8 nF	Polypropylene
C_s	0.68 μF	Polypropylene
L_r	1.48 mH	EE25/13/7 N87-EPCOS
Driver		
U_1	IR2153	Half-Bridge Gate Driver

$$P_{rLf} = \frac{I_{in}^2 r_{Lf}}{2} = \frac{0.235^2 \times 1.432}{2} = 39.541\,\text{mW}. \quad (20)$$

The ESR of the series inductor, r_{Ld}, is 0.093 Ω. Thus, the conduction loss in the inductor, P_{rLd}, is obtained from:

$$P_{rLd} = \left(\frac{3.14 I_{in}}{\sqrt{2}}\sqrt{\frac{m^2}{2}}\right)^2 r_{Ld} = \left(\frac{3.14 \times 0.235}{\sqrt{2}}\sqrt{\frac{1^2}{2}}\right)^2 \times 0.093 = 12.659\,\text{mW}. \quad (21)$$

The parasitic resistance of the resonant inductor, r_{Lr}, is 0.343 Ω. The conduction loss in the resonant inductor, P_{rLr}, is obtained by:

$$P_{rLr} = I_{r,rms}^2 r_{Lr} = \left(397.137 \times 10^{-3}\right)^2 \times 0.343 = 54.097\,\text{mW}. \quad (22)$$

VII. SIMULATION AND EXPERIMENTAL RESULTS

The proposed electronic ballast with the DC-side symmetrical CDCS-RPFC topology was constructed using the component values obtained from the above analysis. Summaries of the circuit parameters and components are presented in Table II. The switching frequency, f_s, was fixed at 50 kHz. The line voltage was set to 220 V_{rms}, and the line frequency, f_L, was 50 Hz.

A. Simulation Results

The proposed DC-side symmetrical CDCS-RPFC was simulated using PSpice to confirm the theoretical analysis. The simulation results of the input line current waveforms without the EMI filter of both the asymmetrical and the symmetrical CDCS-RPFCs are shown in Fig. 9. These waveforms show that the input line current in the DC-side symmetrical CDCS-RPFC has half the peak value and twice the switching frequency when compared to the DC-side asymmetrical CDCS-RPFC. Therefore, the ripple current of the DC-side symmetrical CDCS-RPFC can be removed by a smaller EMI filter. This large line input current is the main drawback of the DC-side asymmetrical CDCS-RPFC.

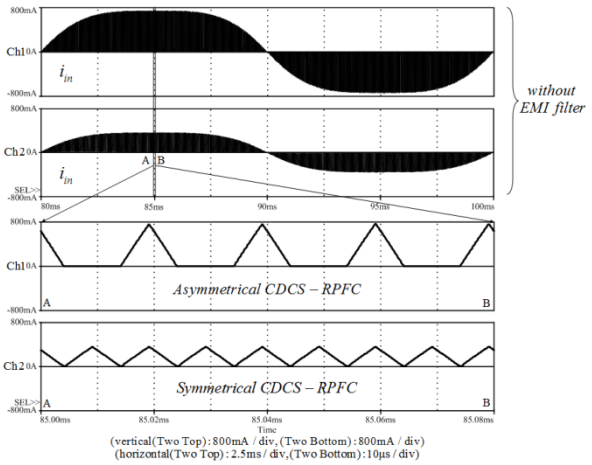


Fig. 9. Comparison of simulated waveforms of the input line current without EMI filter of asymmetrical and symmetrical CDCS-RPFCs; bottom two waveforms are zoomed-in views of top two waveforms.

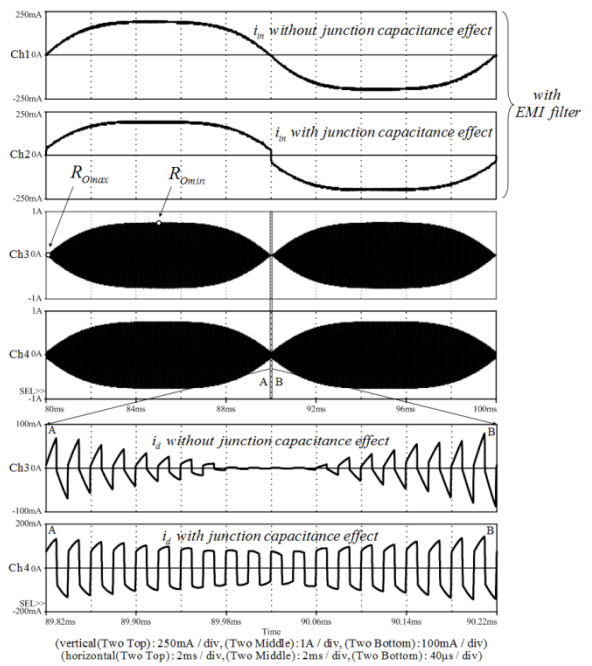


Fig. 10. Comparison of simulated waveforms of input line current and driving current with and without junction capacitance effect; bottom two waveforms are zoomed-in views of middle two waveforms.

Fig. 10 shows the simulated waveforms of the input line current and the driving current with and without the junction-capacitance effect. As can be seen, there is distortion

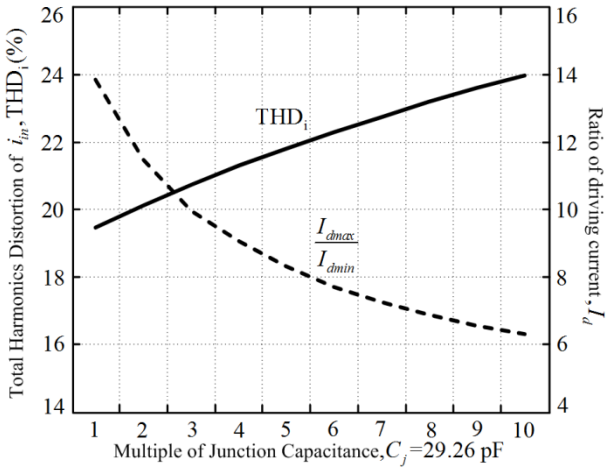


Fig. 11. Total harmonics distortion of i_{in} versus ratio of maximum and minimum of I_d and varied diode junction capacitance, C_j.

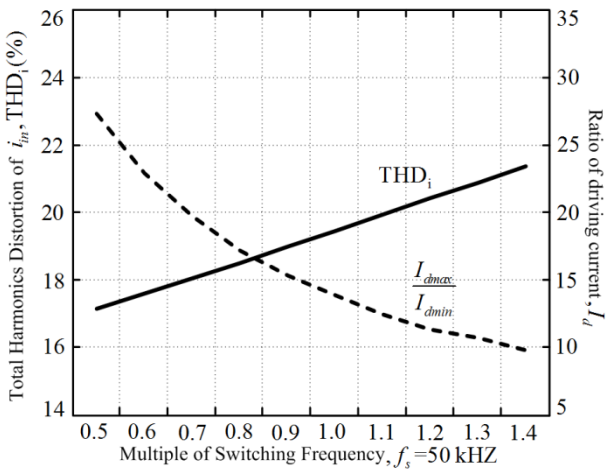


Fig. 12. Total harmonics distortion of i_{in} versus ratio of maximum and minimum of I_d and varied switching frequency.

in the line current waveform close to the zero crossing. This distortion occurs because the driving current, i_d, cannot reach zero due to the junction-capacitance effect of the Class-D ZCS rectifier diode. The waveform of the high frequency driving current, i_d, through the matching circuit is nearly a square-wave at the line's zero crossing. The total harmonics distortion of i_{in} versus the ratio of the maximum and minimum values of I_d with variations of both the diode junction capacitance, C_j, and the switching frequency, f_s, are shown in Fig. 11 and 12, respectively. It can be seen that the total harmonics distortion of i_{in} depends on both the junction capacitance of the fast-recovery diodes used in the CDCS-RPFC and the switching frequency. Therefore, the selections of the fast-recovery diode and switching frequency have a significant impact on the line current harmonic distortion. The analysis is given in Section VIII.

B. Experimental Results

The measured line power was 36.4 W, while the input

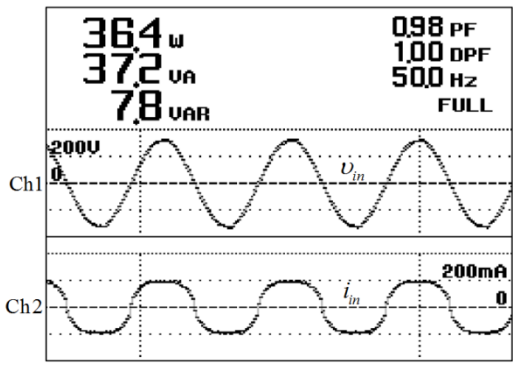


Fig. 13. Measured waveforms of input line voltage and current.

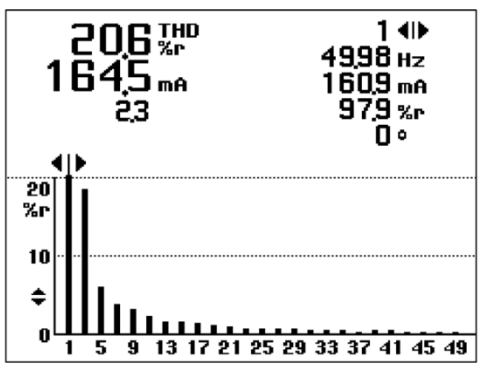


Fig. 14. Measured THD of i_{in} from power analyzer.

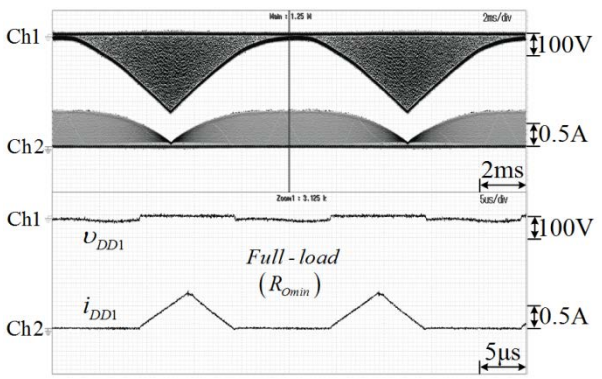


Fig. 15. Measured waveforms of v_{DD1} and i_{DD1} near peak of line voltage; bottom two waveforms are zoomed-in views of top two waveforms.

power-factor was approximately 0.98 as shown in Fig. 13. In this figure, there is distortion in the line current waveform close to the zero-crossing which is the same as in the simulation results.

The THD of the input line current THD$_i$ was 20.6% as depicted in Fig. 14. However, all of the measured harmonic components still satisfy the IEC 61000-3-2 Class-C standard. Fig. 15 and 16 display the experimental waveforms of the diode current, i_{DD1}, and the diode voltage, v_{DD1}, of the symmetrical CDCS-RPFC near the peak and the zero-crossing of the line voltage, respectively. As expected, the current peak of the diode current decreased as the

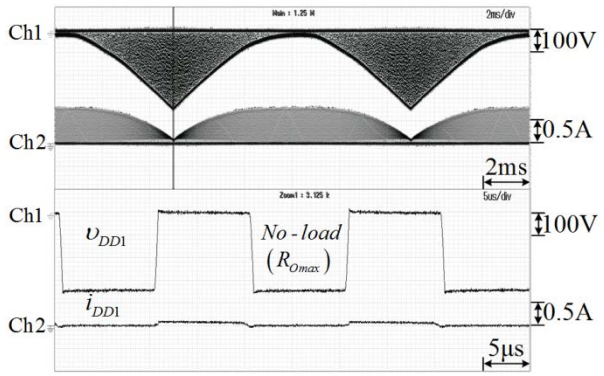


Fig. 16. Measured waveforms of υ_{DD1} and i_{DD1} near zero-crossing of the line voltage; bottom two waveforms are zoomed-in views of top two waveforms.

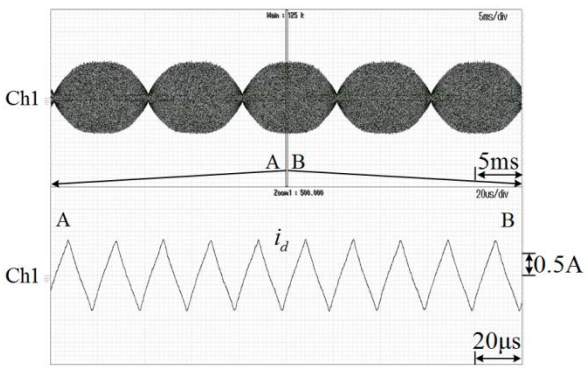


Fig. 17. Measured waveform of driving-current, i_d; lower waveform is a zoomed-in view of top waveform near peak of line voltage.

instantaneous line voltage decreased, which roughly matches the required waveforms shown in Fig. 6. The experimental waveforms of the driving-current, i_d, at the no-load condition near the zero crossing and at the full-load condition near the peak of the line voltage are illustrated Fig. 17. The zero value of the driving-current near the zero crossing is obtained. The measured waveforms of the line voltage (Ch1), line current (Ch2), line power (Math1), lamp voltage (Ch3), lamp current (Ch4) and output power (Math2) are displayed in Fig. 18. The line power, P_{in}, was 36.5 W and the output power, P_{out}, was 34.2 W. The efficiency of the ballast was about 93.5%, indicating that a good efficiency can be obtained by using the proposed topology.

VIII. Discussion of the Effect of the Parasitic Capacitance of the CDCS-RPFC

To obtain the low line-current harmonic distortion at the zero-crossing of the line voltage, υ_{in}, the line current, i_{in}, must equal to zero, which is the no-load condition of the CDCS-RPFC. In fact, the line current, i_{in}, and the driving current, i_d, cannot reach zero near the zero-crossing of υ_{in} because of the junction capacitance effect [31] of the

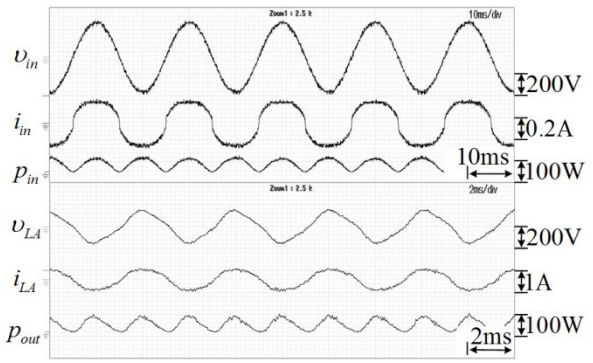


Fig. 18. Measured line voltage, line current, line power, lamp voltage, lamp current and lamp power waveforms.

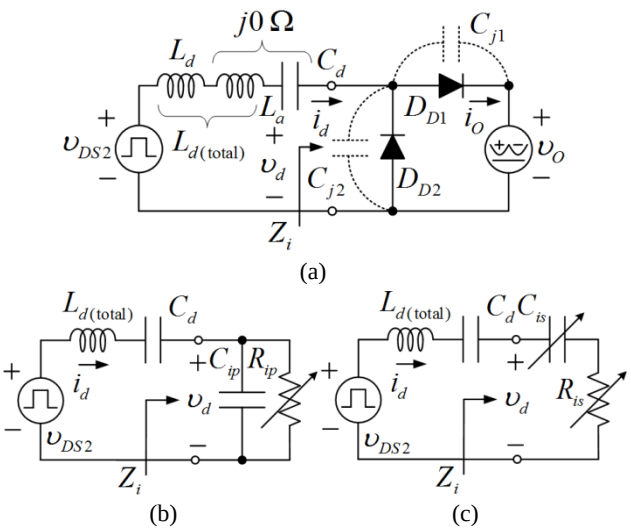


Fig. 19. Equivalent circuit of PFC semi-stage with parasitic capacitance effect of Class-D ZCS rectifier diode.

fast-recovery diodes, D_{D1} and D_{D2}, of the Class-D rectifier as shown in Fig. 19(a). The junction capacitance is present in all of the reverse biased diodes because of the depletion region.

Therefore, the junction capacitors, C_{j1} and C_{j2}, are modeled in parallel with the fast-recovery diodes, D_{D1} and D_{D2}. It can be seen that the input impedance of the CDCS-RPFC cannot be modeled by a single equivalent input resistor, R_i. In the first simplified approach, the input impedance, Z_i, of the CDCS-RPFC with the parasitic capacitance effect can be described by the parallel or series equivalent circuits [31] of the equivalent input resistor, R_i, with the equivalent input capacitor, C_i, and the input voltage is obtained from the square-wave output voltage of the Class-D inverter as shown in Fig. 19(b) and (c), respectively. From Fig. 19(b), it is well known that the voltage transfer function, M_V, of the Class-D LCC series resonant parallel load inverter is more than 1. The ratio V_d/V_{DS2} versus f_s/f_r at various values of the quality factor Q is shown in Fig. 20. Therefore, near the zero-crossing of the line voltage, υ_{in}, D_{D1} can conduct current due to the fact that the voltage at its anode is more positive than the voltage at its cathode. As a

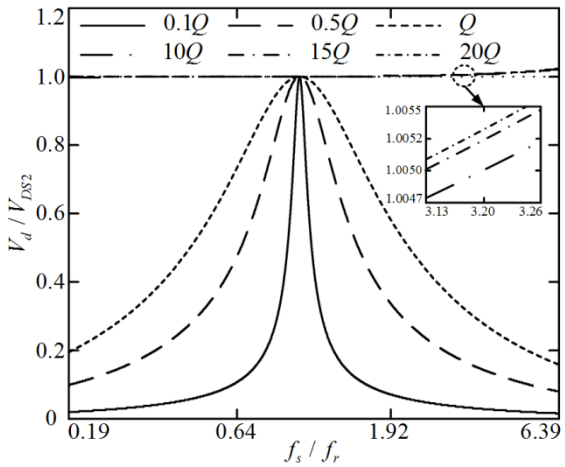


Fig. 20. V_d/V_{DS2} versus f_s/f_r at varied values of Q.

result, the driving current, i_d, cannot reach zero. Accordingly, the selection of the fast-recovery diode as the CDCS-RPFC has a significant impact on the line current harmonic distortion. Diodes with a small C_j are preferred.

IX. Conclusion

This paper has presented the analysis, design and implementation of the DC-side symmetrical ZCS-CDCS-RPFC to improve the low power-factor and the high line current harmonic distortion for single-stage electronic ballast applications. The proposed topology combines a PFC stage based on a Class-D ZCS rectifier and an inverter stage based on a Class-D ZVS inverter into a single-stage power converter, making this technique attractive for commercial applications. However, this topology is only suitable for low power applications.

The design procedure is based on the principle of the symmetrical Class-D ZCS rectifier. The analysis, design and experimental results show that the proposed DC-side symmetrical ZCS-CDCS-RPFC for electronic ballast applications has the following characteristics:

1. It is easy to design for automatic line current shaping, due to the fact that only the full-load condition is considered near the peak of the line voltage. The proposed scheme also provides a more systematic and feasible analysis methodology.
2. The conduction angle of the bridge-rectifier diode current was increased and a low line harmonic distortion and a power-factor near unity were achieved naturally
3. Standard-recovery diodes can be used as the bridge-rectifier and the cost can be reduced, since the EMI filter was connected in cascade with the front-end bridge-rectifier. Therefore, the cost is reduced when compared with the topologies using fast-recovery diodes in the bridge-rectifier.
4. The line current in the symmetrical CDCS-RPFC has twice the switching frequency, which allows for the use of a smaller EMI filter when compared with asymmetrical topologies.
5. The efficiency of the proposed scheme was increased, because the current stresses in the power switches near the zero-crossing of the line voltage have been reduced when compared with the ZVS rectifier topologies.
6. The junction capacitance C_j of the Class-D ZCS rectifier diode has a significant impact on the line current harmonic distortion. Fast-recovery diodes with a small C_j are preferred.

The circuit operation was described and design equations were derived. A prototype designed for a T8-36W fluorescent lamp was built and tested to verify the theoretical analysis. The experimental results show that the single-state electronic ballast with a DC-side symmetrical CDCS-RPFC had a 0.98 power-factor, a 20.6% THD_i, which is below the limit according to the IEC 61000-3-2 Class-C standard, and an efficiency of 93.5 %.

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