JPE 15-3-9

http://dx.doi.org/10.6113/JPE.2015.15.3.660
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

A PDPWM Based DC Capacitor Voltage Control Method for Modular Multilevel Converters

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Abstract

This paper presents a control scheme with a focus on the combination of phase disposition pulse width modulation (PDPWM) and DC capacitor voltage control for a chopper-cell based modular multilevel converter (MMC) for the purpose of eliminating the time-consuming voltage sorting algorithm and complex voltage balancing regulators. In this paper, the convergence of the DC capacitor voltages within one arm is realized by charging the minimum voltage module and discharging the maximum voltage module during each switching cycle with the assistances of MAX/MIN capacitor voltage detection and PDPWM signals exchanging. The process of voltage balancing control introduces no extra switching commutation, which is helpful in reducing power loss and improving system efficiency. Additionally, the proposed control scheme also possess the merit of a simple executing procedure in application. Simulation and experimental results indicates that the MMC circuit together with the proposed method functions very well in balancing the DC capacitor voltage and improving system efficiency even under transient states.

Key words: DC voltage control, MMC, PWM

I. INTRODUCTION

The modular multilevel converter (MMC) has attracted a great deal of research interest in recent years due to its capability of processing both active and reactive power with its terminals directly connected to high-voltage networks [1]. The double-star structure together with the modular characteristic enables the MMC circuit to act as high-voltage inverter, rectifier, or four-quadrant converter without bulky transformers in high-power application such as motor drives, static synchronous compensators (STATCOM) and high voltage dc transmission (HVDC) [2]-[4].

Recently, many studies have been published on the MMC concerning modeling, modulation, DC voltage balancing, digital control, low-frequency operation, simulation techniques, and so forth [1]. Among these, the modulation method is the key to determining the final performance of the MMC circuit and to affecting the charging and discharging of the module capacitor [5]. The studies relating to modulation can be generally divided into four types, namely, nearest voltage level (NVL) [6], look-up table [7], [8], carrier phase shifted pulse width modulation (CPSPWM) [9]-[11], and phase disposition pulse width modulation (PDPWM) [5], [12]. The NVL method is a widely used modulation approach for MMC circuits because of its simple executing process [6]. Usually, it works together with a sorting algorithm to keep the individual capacitor voltage balanced. However, this may lead to the drawback of a heavy computational burden on the digital controller and an increase in the average switching frequency for the semiconductor devices. Taking each arm with N series-connected modules as an example, the voltage sorting algorithm requires (N-1)N/2 times the number of subtraction operations and data movements to sort the DC voltage in descending or ascending order for one arm. A MMC circuit with six arms may have to face the challenge of a heavy computational burden to fulfill the voltage balancing control, especially when the module number is large. Additionally, the methods using a look-up table derive the switching angles through selective harmonic elimination (SHE) [7] or other approaches [8], and then stores them in the memory of the digital controller for on-line invoking. Generally, this method could realize a very low switching frequency. However, it is usually acompanied by the issues of modulation ratio

Manuscript received Jul. 17, 2014; accepted Oct. 13, 2014.
Recommended for publication by Associate Editor Sanjeet K. Dwivedi.
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discretization, controller hardware occupation, and difficulty in terms of DC capacitor voltage correction. Moreover, CPSPWM has been researched in depth and extended to MMC applications [9]-[11]. Specialized proportional and integral (PI) regulators are adopted to generate the AC voltage trimming part for DC voltage balancing [9], [10]. This means that the control becomes difficult and the system stability runs the risk of increasing the voltage levels [5]. In order to eliminate the voltage balancing regulator, a method based on executing a voltage sorting algorithm after each crossing of the reference and the carriers is presented in [11]. However, this method introduces another problem in terms of a heavy computational burden on the digital controller. Furthermore, PDPWM is also studied in the application of MMC modulation [5], [12]. The study in [12] demonstrates an approach utilizing carrier circular transposition every line cycle for balancing the capacitor voltage. The absorbed power of each module can be equally distributed during N line cycles (N is the number of modules in each arm), but the balance of the capacitor voltages cannot be achieved because of the different power losses and uncontrollable fluctuations. The study in [5] presents an innovative solution for exchanging switching signals based on the detection of MAX/MIN voltages. The switching-cycle control results in a high efficiency for voltage balancing control. However, it is acompanied by an issue of higher power loss caused by extra switching commutations.

In this paper, the modulation of PDPWM is chosen, because it can potentially reduce the carrier number to one. As to the capacitor voltage control, the replacement of the sorting algorithm with MAX/MIN voltage detection greatly lightens the computational burden on the digital controller. Meanwhile, it also eliminates the specialized voltage balancing regulators, which simplifies the system control [5]. This paper carries out further research and proposes a simplified voltage balancing principle without introducing any extra switching commutation. In addition, it achieves a very low average switching frequency for improving the system efficiency. The performance of proposed method is justified by both the simulation and experimental results.

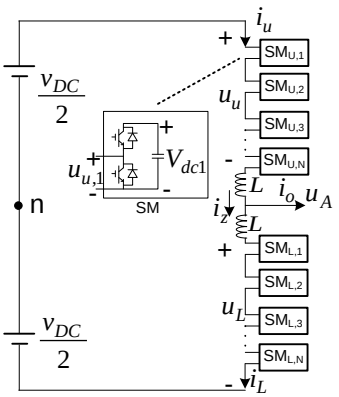


Fig. 1. Structure of MMC circuit, taking single-phase converter for an example.

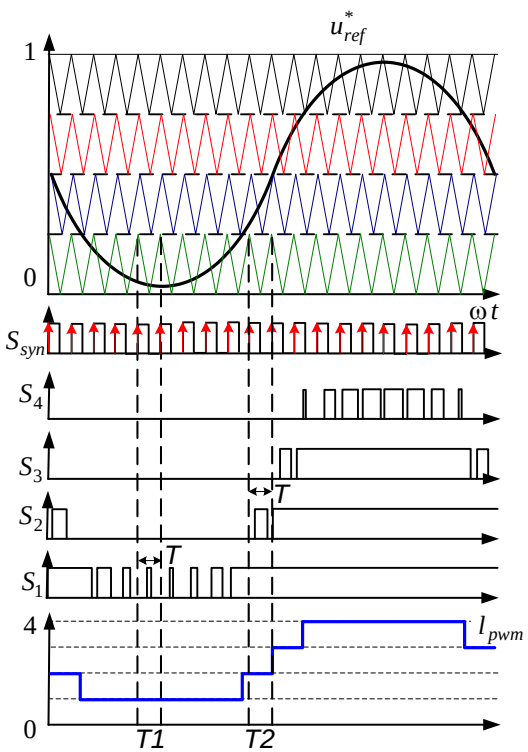


Fig. 2. Analysis of PDPWM, taking the series-connected number of N=4 for an example.

II. Operation Principle

This section presents the proposed method. Part A analyzes the switching signals modulated by the PDPWM. Part B demonstrates the principle of the signal assignment for the voltage balancing control.

A. The Analysis of the PDPWM

Fig. 1 shows the circuit configuration of the MMC. All of the positive directions are defined in Fig. 1. The chopper cells are connected in series to form one arm. A pair of upper and lower arms connect together through two interface inductors to build one phase converter. Three phases have a symmetric structure and parameters. The middle taps are considered as AC ports to supply power to a high-voltage load or they are directly hooked into an AC utility for active and reactive power processing. In practice, the working state of each module is determined by the switching signal, which is generated by the modulation strategy. This paper employs the modulation of PDPWM with the fundamentals shown in Fig. 2.

The reference voltage crosses with carriers to produce N switching signals for the modules in one arm. When the reference is larger than one carrier, the corresponding switching signal works in the on state, otherwise, it is in the off state. During one switching cycle, the reference just crosses with one carrier and the duty ratio of switching signal is always equal or larger than that located in the upper layers. In other

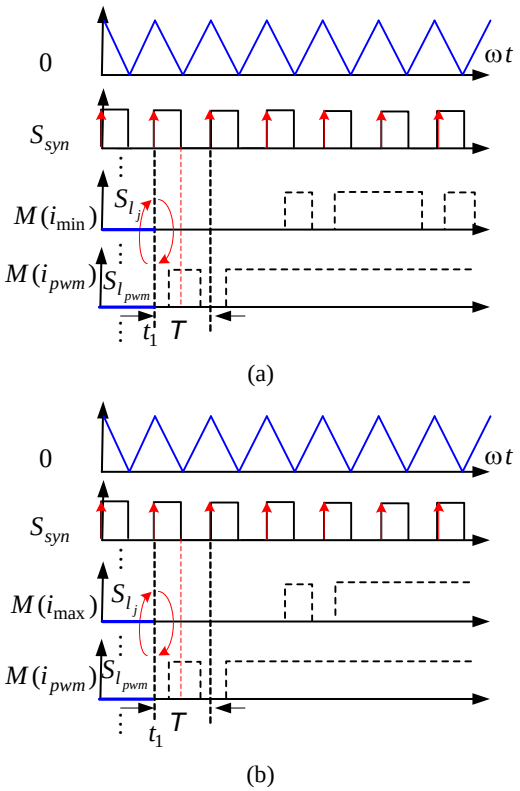


Fig. 3. Signal exchanging principles for first-half switching cycle. (a) charging state (i_{arm}>0). (b) discharging state (i_{arm}<0).

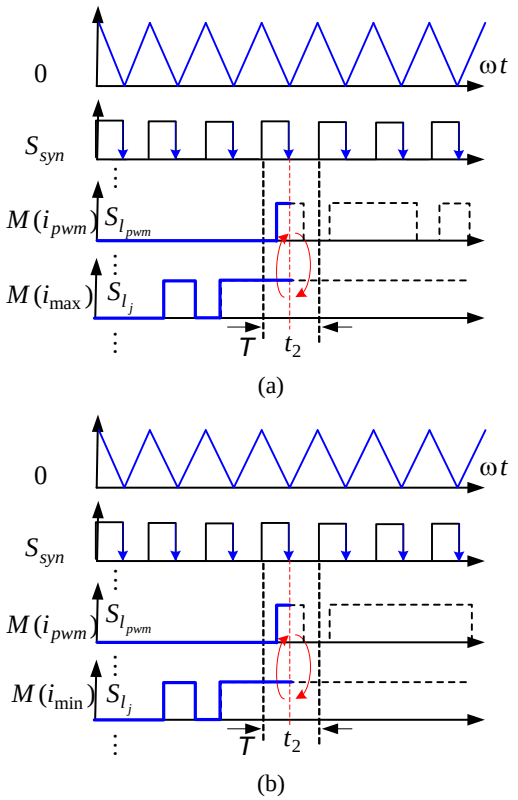


Fig. 4. Signal exchanging principles for second-half switching cycle. (a) charging state (i_{arm}>0). (b) discharging state (i_{arm}<0).

words, only one module switches in each switching cycle while the others keep the original working state. Therefore, only one of them is a PWM signal while others are non-PWM signals. Here, the PWM signal means that it has both on and off states in one switching cycle. Meanwhile, the non-PWM signals keep the working state constant during the whole cycle. For example, S_1 is the PWM signal at the switching period T1. Then S_2 becomes the PWM signal at the switching period T2. The indicator of the lpwm directly shows the index of the PWM signal. All of these properties are valuable for designing the capacitor voltage balancing control.

B. Proposed Principles for the Voltage Balancing Control

The DC voltage of each module is determined by the charge stored in the capacitor. Proper charging and discharging can correct the capacitor voltage and make it balanced. In order to achieve this goal, the signal of S_{syn} in Fig. 2 is introduced. It is synchronous to a triangle carrier with its leading edge at the peak value and its falling edge at the valley value. The leading edge of S_{syn} indicates that in the first-half switching cycle one more module must be turned on. When the current is positive (which flows for charging the modules, i_{arm}>0) and the minimum voltage module is in the off state (whose signal index is higher than that of the PWM signal, l_j>l_{pwm}), the minimum-voltage and PWM-assigned modules should exchange their switching signals to make the minimum-voltage module turn on and become charged within the first-half switching cycle. Otherwise, when the current is negative (which flows for discharging the modules, i_{arm}<0) and the maximum-voltage module is in the off state (whose signal index is higher than that of the PWM signal, l_j>l_{pwm}), the maximum-voltage module and PWM-assigned module should exchange their switching signals to make the maximum-voltage module turn on and become discharged within the first-half switching cycle. The details of these two situations are demonstrated in Fig. 3. The time instant for the signal exchanging is marked as t_1, leading to no extra switching commutation because both modules work in the off state.

The falling edge of S_{syn} reveals that in the second-half of the switching cycle one more module must be turned off. When the current is positive (i_{arm}>0) and the maximum-voltage module is in the on state (l_j<l_{pwm}), the maximum-voltage and PWM-assigned modules should exchange their switching signals to make the maximum-voltage module turn off within the second-half of the switching cycle for the purpose of preventing continuous charging. Otherwise, when the current is negative (i_{arm}<0) and the minimum-voltage module is in the on state (l_j<l_{pwm}), the minimum-voltage and PWM-assigned modules should exchange their switching signals to make the minimum-voltage module turn off within the second-half of

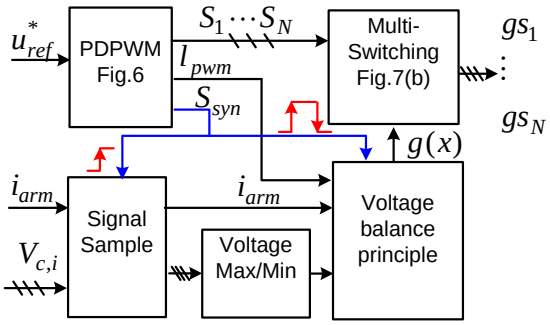


Fig. 5. Block diagram of the control implementation.

the switching cycle for the purpose of preventing continuous discharging. The details of these two situations are demonstrated in Fig. 4. The time instant for the signal exchanging is marked as t_2, resulting in no extra switching commutation because both of the modules work in the on state.

Note that this method only focuses on the maximum-voltage, minimum-voltage and PWM-assigned modules. It is not concerned with the series-connected number of modules in one arm. At each leading and falling edge of S_{syn}, the relative switching signals are exchanged according to the proposed philosophy without introducing any extra switching commutations. The DC voltage convergence of the maximum-voltage and minimum-voltage modules achieves voltage balancing among all of the modules within one arm.

III. Implementation of the Proposed Control Method

In order to implement the proposed voltage balancing principle, a digital controller based on both a DSP and a FPGA is composed and tested. Meanwhile, a control scheme is designed with the structure shown in Fig. 5. The switching signals are produced by applying PDPWM to the reference voltage. As is shown in Fig. 6, the reference voltage has a normalized value in the range from 0 to1 and the triangle carrier is designed with an amplitude of 1/N to guarantee normal modulation. According to the authors of [5], the generation of carrier signals can be realized by adding a proper dc bias to the triangle waveform, which brings the advantage of requiring only one triangle waveform. When the reference voltage crosses with the carrier signals, the switching signals are produced. In order to identify the PWM signal, one variable 'l_{pwm}' is introduced, which can be obtained by applying the 'ceil' function to the reference variable of Nu^*_{ref}. Meanwhile, the synchronous signal S_{syn} is also brought in for triggering the voltage and current sampling. It is also used for conducting the switching signal exchanging.

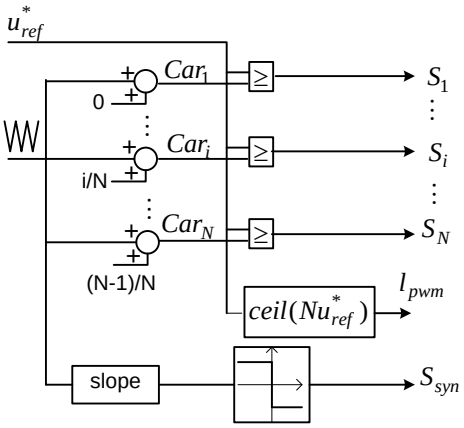


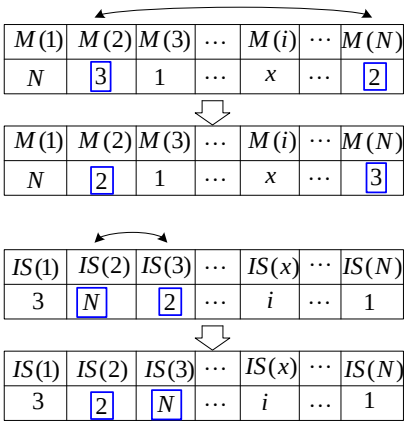
Fig. 6. Block diagram of PDPWM by using only one triangle carrier.

At the leading and falling edges of S_{syn}, the digital controller samples the arm current and all of the capacitor voltages. Then, the two modules with the highest and lowest voltages are selected by using the algorithm published in [5]. After deriving these signals, the condition judgment for the switching signal exchanging is conducted according to the voltage balancing principle described in Section II. If the condition is satisfied, the relative switching signals are exchanged and recorded in the arrays of *M(i)* and *IS(x)*. The valuation of *M(i)=x*, for example, means that module *i* uses the switching signal S_x. Similarly, the valuation of *IS(x)=i* means that switching signal S_x is assigned to module *i*. Based on the array of *M(i)*, the multi-switching reconstructs immediately to provide channels for forming the gating signals.

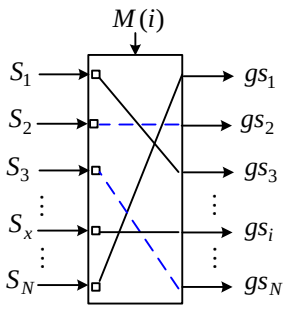
As shown in Fig. 7, if module 2 has the lowest voltage ($i_{min}=2$ *and* $l_j=3$), and the signal S_2 is the PWM signal ($l_{pwm}=2$) at the leading edge of S_{syn}, the situation of the voltage balancing principle demonstrated in Fig. 3(a) is satisfied. By using l_{pwm} as an index to the array of *IS(x)*, the number *N* is returned, which means that module *N* is adopts the PWM signal. Consequently, modules 2 and N should exchange their switching signals. Therefore, the stored values in *M(2)* and *M(N)* are exchanged. Similarly, the stored values in *IS(2)* and *IS(3)* should also be exchanged. According to the updated value in the array of *M(i)*, the reconnections of gs_2 to S_2 and from gs_N to S_3 would execute while the other connections remain the same.

IV. Simulation Verification

In order to verify the performance of proposed method, a simulation model based on the PSCAD platform was designed and tested. The circuit configuration is shown in Fig. 1 with 10 modules connected in series to form one arm. The upper and lower arms connect together through two interface



(a)



(b)

Fig. 7. Block diagram of multi-switching for signal assignment. Taking an example that the index of minimum voltage module is 2 (i_{min}=2 *and* l_j=3) and S_2 is the PWM signal (l_{pwm}=2). (a) Stored value exchanging in arrays. (b) Gating signal reconstruction.

TABLE I

CIRCUIT PARAMETERS IN FIG. 1

Nominal AC voltage		10kV
Power rating	P	5MVA
Common DC bus voltage	V_{DC}	20kV
Number of submodule for each arm	N	10
Nominal DC capacitor voltage of each submodule	V_C	2kV
Capacitance of each DC capacitor	C	3700uF
Inductance of interface inductor	L	10mH
Carrier frequency		1kHz
Load	R_{load} L_{load}	20Ω 20mH

inductors with an inductance of 10mH. The two terminals of the middle tap and neutral point work as an AC port to supply power to the RL load with a resistance of 20Ω and an inductance of 20mH. All of the other circuit parameters are summarized in Table I. In the simulation, the triangle carriers for the upper and lower arms are assigned with the same phase angle for increasing the voltage level and reducing the voltage step in the AC voltage waveform [1]. Based on the simulation model, the steady state performance, dynamic

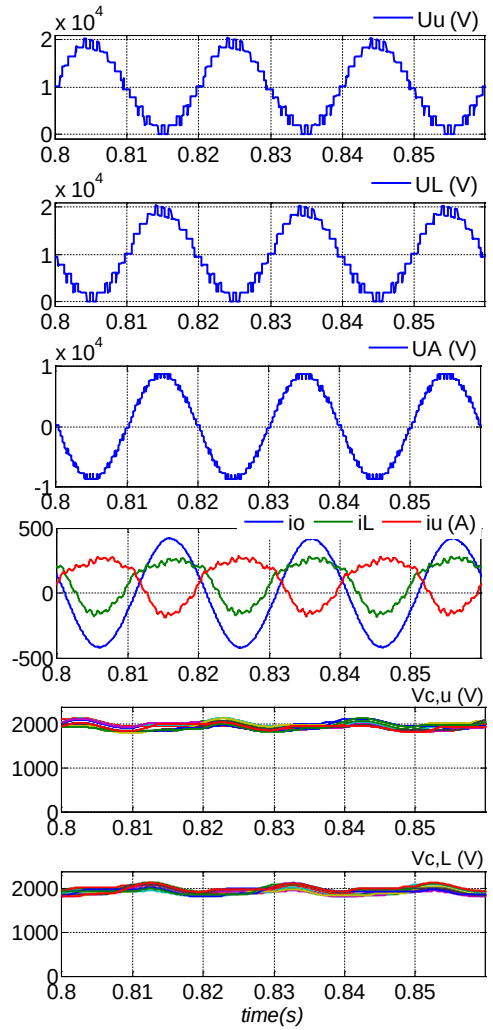


Fig. 8. Simulation results verifying the steady state performance.

response and switching commutations are tested separately. The simulation results are shown in Fig. 8, Fig. 9 and Fig. 10.

Fig. 8 verifies the steady state performance of the proposed method. In order to clearly show the waveforms, the results obtained from a model with a series-connected number of N=10 are presented. Both the upper and lower arms generate 11-level voltage waveforms due to the use of 10 modules for each of them. The output voltage u_A produces 21 levels where the height of voltage step is reduced by 50%. The optimized AC voltage waveform is very convenient in terms of the filter design. Meanwhile, the capacitor voltages are balanced very well with the voltage ripple limited to within 5%. The simulation results in Fig. 8 successfully confirm the excellence of the steady-state performance.

Fig. 9 presents the dynamic response of the proposed voltage balancing method. At the beginning of the simulation, the voltage balancing control is intentionally disabled and the capacitor voltages of the 10 modules exhibit noticeable deviations. Meanwhile, a large amount of circulating current is observed in the MMC circuit. This is due to the distortion

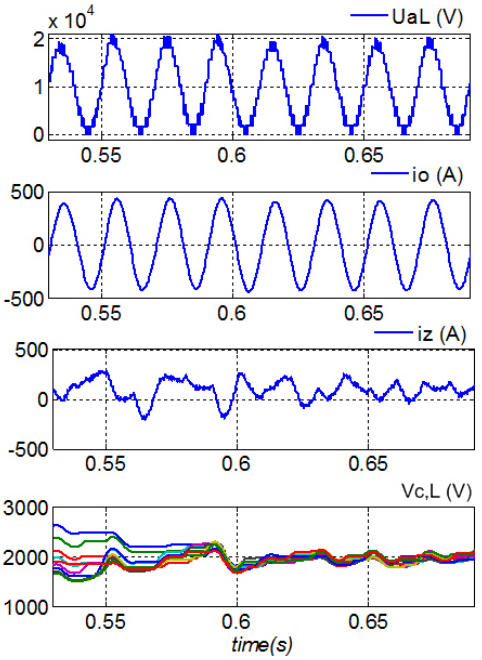


Fig. 9. Simulation results confirming the dynamic response.

of the AC voltage caused by an imbalance of the capacitor voltage. At the time instant of 0.54s, the proposed voltage balancing control is enabled. As is shown in Fig. 9, the capacitor voltages merge together quickly and are maintained at the nominal value of 2000V. During this process, the circulating current in the circuit is suppressed as expected. The simulation results in Fig. 9 agree with the theoretical analysis very well, which confirms the effectiveness of the proposed method.

Fig. 10 shows the switching commutation in one line period of 20ms by using the model with a series-connected number of N=10. The voltage waveform generated by the lower arm contains 34 switching commutations including 17 times of turning on and 17 times of turning off. This effectively steps up or steps down the arm voltage to make it follow the sinusoidal reference. Meanwhile, the 10 modules also have 34 switching commutations in total and each of them strictly corresponds with that in terms of arm voltage. This phenomenon indicates that the proposed method introduces no extra switching commutation at the time instants of the arm voltage stepping up or stepping down, or in the time period when the arm voltage keeps the voltage level. The switching position with a consideration of the capacitor voltage balancing control based on the proposed method is kept the same as that with the original PDPWM signals. This results in the advantage of no extra power loss being introduced. Additionally, the 34 commutations for the 10 modules in one line period of 20 ms result in an average switching frequency of 85Hz for each of the semiconductor devices. In practice, the reduced switching frequency can result in reduced power loss. Therefore, the consistency

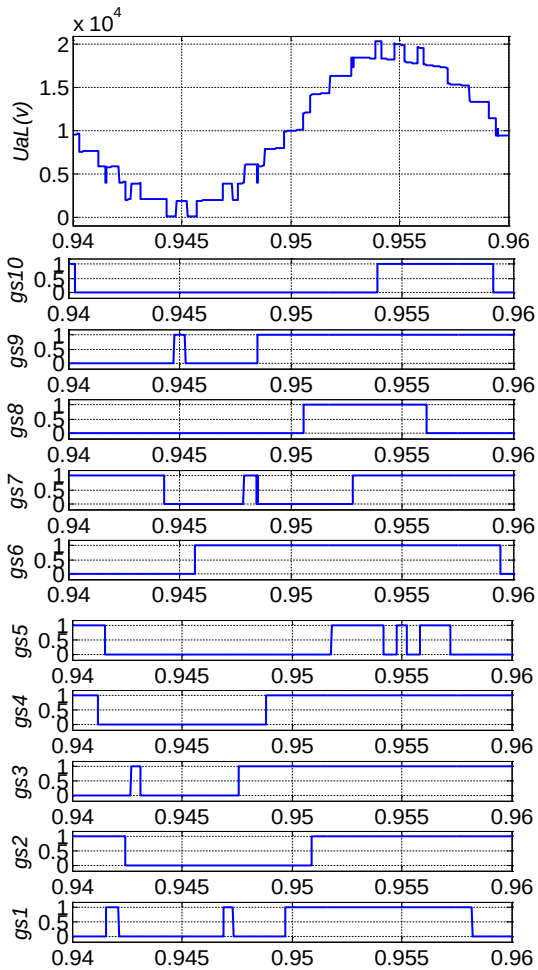


Fig. 10. Simulation results confirming the characteristic of introducing no extra switching commutation.

between the simulation result and the theoretical analysis confirms the control effect in terms of balancing the capacitor voltage and in improving the system efficiency.

V. Experimental Results

An experimental prototype of a MMC-based inverter is designed, constructed and tested for further verification. Due to the limitations of authors' lab, only one single-phase inverter is built with 4 series-connected half-bridge modules for each arm. The circuit configuration is kept the same as that in Fig. 1 and a view of the prototype is provided in Fig. 11. Although the experiments are carried out based on a single-phase MMC-based inverter, it is still reasonable to prove the validation of the proposed voltage balancing method because of its focus on the control strategy. The detailed parameters of the circuit are presented in Table II.

Note that the proposed method in this paper can also be easily extended to three-phase MMC circuits. When it is applied to a three-phase converter, the voltage balance control remains the same as that of a single-phase converter. The only

Fig. 11. Photo of the single-phase MMC-based inverter.

TABLE II
CIRCUIT PARAMETERS OF THE PROTOTYPE

DC bus voltage	V_{DC}	200V
Power rating	P	2000W
Modulation ration	m	0.8
Number of module for each arm	N	4
Nominal DC capacitor voltage of each module	V_C	50V
Capacitance of each DC capacitor	C	4700μF
Inductance of interface inductor	L	3.5mH
Carrier frequency		800Hz
Inductance of load	L_{load}	18mH
Resistance of load	R_{load}	8Ω

thing that needs to be done is replacing the single-phase current/voltage-loop control with the DQ-transformation-based current/voltage-loop control. The following experimental results are obtained from the single-phase MMC-based inverter.

Fig. 12 shows the experimental results for testing the proposed control scheme. Both the upper and lower arms generate 5-level voltage waveforms due to the cascaded number of N=4 for each arm. The output voltage of one phase produces 9 voltage levels with a reduced height of the voltage step due to the same phase angle assignment for the carriers in the upper and lower arms. A THD analysis for the converter currents shows that the DC and fundamental AC components in the arm current are the major parts for supporting power conversion between the DC and AC sides of the MMC circuit. Meanwhile the apparent even-order harmonics just flow as circulating current because they do not exist in the output current. Note that the 16-order harmonic in arm current results from a carrier frequency of 800Hz and the cancellation of them between the upper and lower arms make the THD value of the output current as low as 0.75%. The optimized waveform greatly improves the output spectrum, further reduces the ripple in the output current, and simplifies

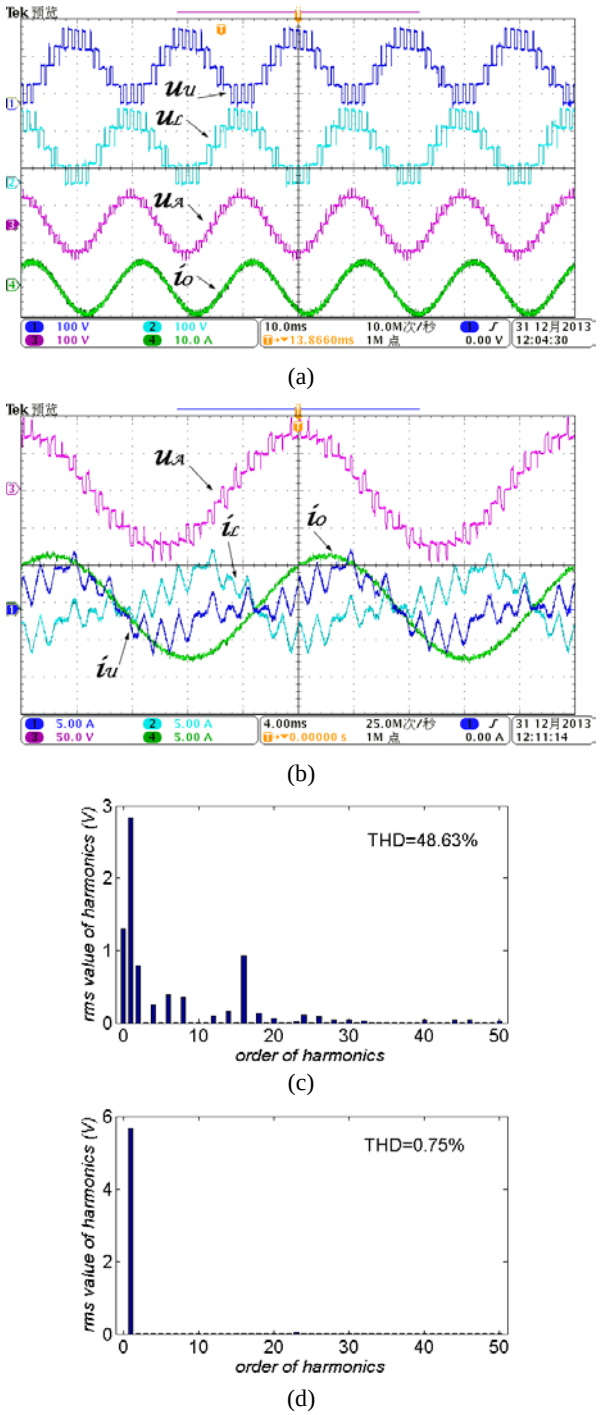
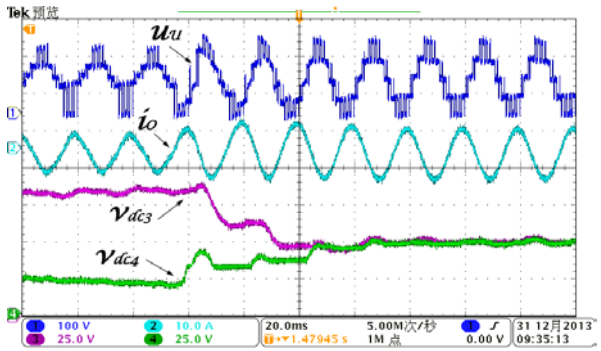


Fig. 12. Experimental result verifying the performance of control scheme. (a) Converter voltages and output current. (b) Output voltage and converter currents. (c) THD analysis for arm current i_u. (d) THD analysis for output current i_o.

the filter design. However, the assignment of the same carrier phase angle also brings the disadvantage of a doubled current ripple in the circulating current. A detailed analysis can be found in the study in [1]. Anyway, the circulating current just flows among converters and does not harm the utility or the AC load. The experiment results in Fig. 12 verify that the prototype along with the control scheme work smoothly.



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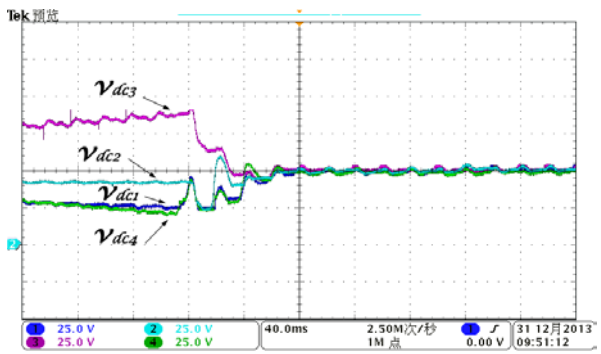


(b)

Fig. 13. Experimental result verifying the effect of proposed voltage balancing control. (a) The outputs of converter and DC capacitor voltages in upper arm. (b) All the DC capacitor voltages in upper arm.

Fig. 13 confirms the control effect of the proposed voltage balancing method. When the prototype starts up, the voltage balancing control is intentionally disabled for a short period of time. All of the DC capacitor voltages deviate from the nominal value of 50V quickly and the output voltage is seriously distorted. Then, the voltage balancing control is triggered and the trajectories of the capacitor voltages converge as one line with a fast speed and are maintained at the given value of 50V. The distortion in the output voltage and load current are noticeably suppressed. In steady state, the capacitor voltage difference among the modules and the voltage error between the reference value and the measured value are negligibly small. The experimental results in Fig. 13 verify the validation of the proposed method.

Fig. 14 and Fig. 15 show the dynamic response of the MMC circuit with the proposed control method. When the process of load is suddenly doubled and the modulation ration is sharply changing from 0.45 t0 0.9, the MMC-based inverter runs normally with the DC capacitor voltage maintained at the given value. The experimental results in Fig. 14 and Fig. 15 confirm that the proposed method functions very well in balancing the DC capacitor voltage even under the sudden changed in the working conditions.

Fig. 16 presents the switching commutations of the converters in upper arm within two line period of 40ms. It is clearly shown that the upper arm voltage generates 30 times

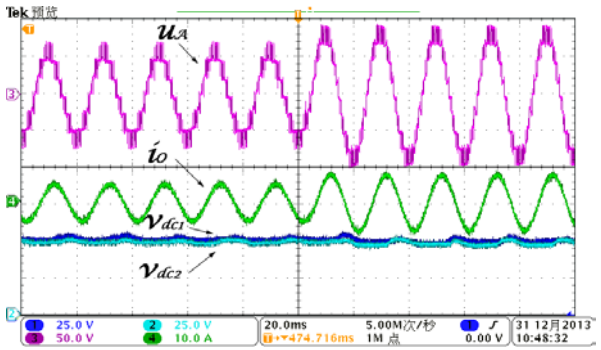


Fig. 14. Experimental result verifying the dynamic response with sudden change of modulation ratio from 0.45 to 0.9.

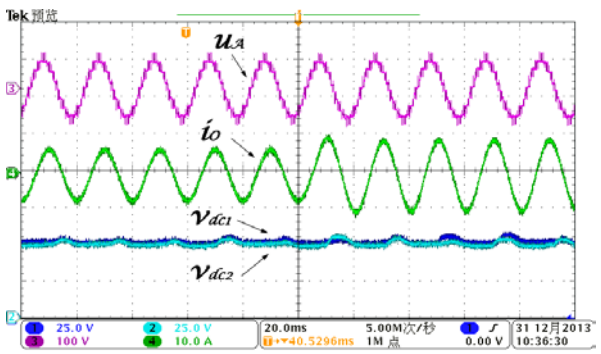
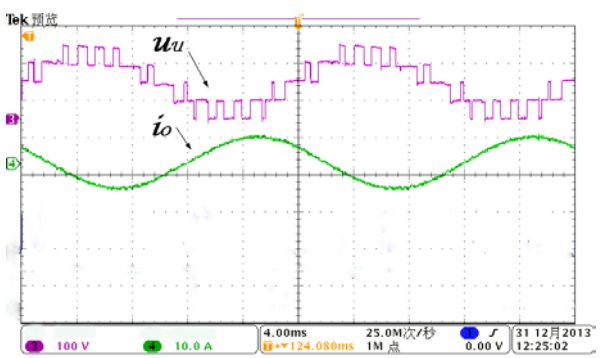


Fig. 15. Experimental result verifying the dynamic response with the load suddenly doubled.



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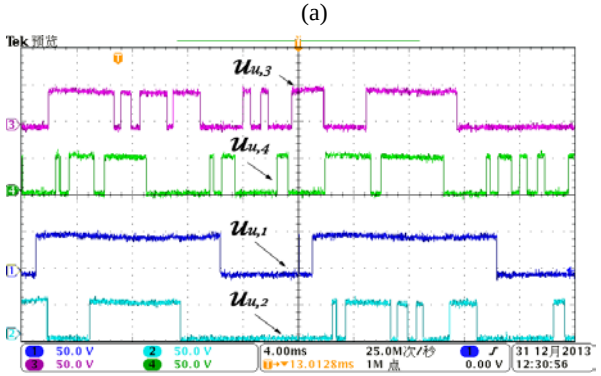

(b)

Fig. 16. Experimental result verifying the characteristic of no extra switching commutation introduction. (a) converter voltage and output current. (b) output voltages of the four modules in upper arm.

of turning on and turning off for each line cycle, which coincides with that of the voltages produced by the four modules in total. That means that no extra switching commutation is introduced when the arm voltage steps up and down, as well as during the time interval where the voltage level is maintained. The 30 switching commutations in each line cycle lead to an average switching frequency of 187.5Hz for each switching device. The difference between the simulation and experimental results can be attributed to the different carrier frequency and different cascaded number of the arms. As the number of series-connected modules increases, the average switching frequency decreases. The experimental results in Fig. 16 verify that the MMC circuit along with the proposed control method work smoothly in improving system efficiency because of the lower average switching frequency and the fact that it does not produce any extra switching commutations.

VI. CONCLUSIONS

This paper described a PDPWM-based voltage balancing method for MMC circuits without any extra switching commutation. The proposed method requires no voltage sorting algorithm or specialized voltage balancing regulators. The detection of the MAX/MIN capacitor voltage greatly simplifies the control process and lightens the computational burden on the digital controller. Both the steady state and dynamic responses are confirmed by simulation and experimental results. These results show that the MMC circuit along with the proposed method function satisfactory in processing power and balancing the capacitor voltage.

REFERENCES

[1] Z. Li, P. Wang, H. Zhu, Z. Chu, and Y. Li, "An improved pulse width modulation method for chopper-cell-based modular multilevel converters," *IEEE Trans. Power Electron.*, Vol. 27, No. 8, pp. 3472-3481, Aug. 2011.

[2] H. P. Mohammadi and M. T. Bina, "A transformerless medium-voltage STATCOM topology based on extended modular multilevel converters," *IEEE Trans. Power Electron.*, Vol. 26, No. 5, pp. 1534-1545, Jul. 2011.

[3] M. Saeedifard and R. Iravani, "Dynamic performance of a modular multilevel back-to-back HVDC system," *IEEE Trans. Power Del.*, Vol. 25, No. 4, pp. 2903-2912, Jul. 2010.

[4] A. Antonopoulos, K. Ilves, and L. Ängquist, "On interaction between internal converter dynamics and current control of high-performance highpower AC motor drives with modular multilevel converters," in *Proc. IEEE ECCE*, pp. 4293-4298, 2010.

[5] J. Mei, K. Shen, B. Xiao, L. M. Tolbert, and J. Zheng, "A new selective loop bias mapping phase disposition PWM with dynamic voltage balance capability for modular multilevel converter," *IEEE Trans. Ind. Electron.*, Vol. 61, No. 2, pp. 798-807, Feb. 2014.

[6] Q. Tu and Z. Xu. "Impact of sampling frequency on harmonic distortion for modular multilevel converter," *IEEE Trans. Power Del.*, Vol. 26, No. 1, pp. 298-306, Jul. 2011.

[7] K. Ilves, A. Antonopoulos, S. Norrga, and H.-P. Nee, "A new modulation method for the modular multilevel converter allowing fundamental switching frequency," *IEEE Trans. Power Electron.*, Vol. 27, No. 8, pp. 3482 -3494, Aug. 2012.

[8] S. Du, J. Liu, and T. Liu, "Modulation and close-loop based DC capacitor voltage control for MMC with fundamental switching frequency," *IEEE Trans. Power Electron.*, Vol. 30, No. 1, pp. 327-338, Jan. 2015.

[9] M. Hagiwara, K. Nishimura, and H. Akagi, "A medium-voltage motor drive with a modular multilevel PWM inverter," *IEEE Trans. Power Electron*, Vol. 25, No. 7, pp. 1786-1799, Jul. 2010.

[10] M. Hagiwara, R. Maeda, and H. Akagi, "Control and analysis of the modular multilevel cascade converter based on double-star chopper-cells (MMCC-DSCC)," *IEEE Trans. Power Electron.*, Vol. 26, No. 6, pp. 1649-1658, Jun. 2011.

[11] E. Solas, G. Abad, J. A. Barrena, S. Aurtenetxea, A. Cárcar, and L. Zajac., "Modular multilevel converter with different submodule concepts – Part I: capacitor voltage balancing method," *IEEE Trans. Ind. Electron.*, Vol. 60, No. 10, pp. 4525-4535, Oct. 2014.

[12] K. Shen, B. Xiao, J. Mei, L. M. Tolbert, J. Wang, X. Cai1, and Y. Ji, "A modulation reconfiguration based fault-tolerant control scheme for modular multilevel converters," *APEC2013, Twenty-Eighth Annual IEEE*, pp. 3251-3255, 2013.

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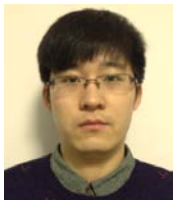

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