JPE 15-3-10

http://dx.doi.org/10.6113/JPE.2015.15.3.670
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

A Novel Quadrant Search Based Mitigation Technique for DC Voltage Fluctuations in Multilevel Inverters

Johnson Anitha Roseline[†], Subramanian Vijayenthiran[*], Rajini V[*], and Senthil Kumaran Mahadevan[*]

[†*]Department of Electrical and Electronics Engineering, SSN College of Engineering, Chennai, India

Abstract

The hybrid cascaded multilevel inverter (HCMLI) is a popular converter topology that is being increasingly used in high power medium voltage drives. The intricacy of the control technique for a HCMLI increases with the number of levels and due to fluctuating dc voltages. This paper presents a novel offline quadrant search based space vector modulation technique to synthesize a sinusoidal output from a dispersed pattern of voltage vectors due to different voltages in the auxiliary unit. Such an investigation has never been reported in the literature and it is being attempted for the first time. The method suggested distributes the voltage vectors for a reduced total harmonic distortion at minimal computation. In addition, the proposed algorithm determines the maximum modulation index in the linear modulation range in order to synthesize a sinusoidal output for both normal and abnormal vector patterns. It is better suited for a wide range of practical applications. It is particularly well suited for renewable source fed inverters which utilize large capacitor banks to maintain the dc link, which are prone to such slow fluctuations. The proposed quadrant search space vector modulation technique is simulated using MATLAB/SIMULINK and implemented using a Nexys-2 Spartan-3E FPGA for a developed prototype.

Key words: Fluctuating DC voltages, Hybrid cascaded MLI, Quadrant search, Space vector modulation

I. INTRODUCTION

Multilevel inverters (MLI) have emerged as a solution to construct medium and high power converters using low power semiconductor devices [1]-[3] with an increase in the quality of the output AC voltage [4]. This breed of inverters has a wide range of applications in energy conversion, transportation, mining, petrochemicals, etc. They are also employed as active power filters and static compensators in power systems. In recent years researchers have developed different MLI topologies. All of the topologies are either revisions or hybridizations of three basic topologies [5] viz. Diode Clamped (DC), Flying Capacitor (FC) and Cascaded H Bridge (CHB). Among these basic topologies, the FC and CHB are referred to as multi cell converters, since they are built using many smaller converters called power cells. Due to the increased redundancies and modularity of the CHB topology, it is more attractive since it can enable fault tolerant operation and increase the output levels by only adjusting the DC voltage ratios between the power cells. The major issue with the CHB MLI is that it requires large number of isolated DC sources [6]-[8].

A three phase CHB MLI can be realized using various structures. *Type 1*, Cascading CHBs to construct a single phase MLI and connecting three such single phase inverters in the phase shifting mode [9]. *Type 2*, By having a six pulse inverter as a central inverter unit and cascading a single phase CHB as an auxiliary unit with each phase [10].

Considering the number of realizable levels that can be achieved for a particular component count, the three phase inverters of type 2 seem to be superior since the output of six pulse inverter itself has five levels. Since number of required switches and DC voltage sources is lower for the six pulse inverter, it can be used as a high voltage cell in an asymmetric MLI to minimize the switching losses. The quality of the output voltage depends on the number of levels. Therefore, a larger number of levels in the output voltage can be achieved

Manuscript received Aug. 28, 2014; accepted Jan. 24, 2015
Recommended for publication by Associate Editor Trillion Q Zheng.
[†]Corresponding Author: anithar@ssn.edu.in
Tel: +91-044-27469700, Ext: 522, SSN College of Engineering
[*]Department of Electrical and Electronics Engineering, SSN College of Engineering, India

by setting the DC source voltage ratio to 3:1, which is called the maximal distension [11], [12]. For all of the integer voltage ratios up to the maximal distension, the voltage vectors are distributed over a hexagonal pattern. If the voltage ratio is a non-integer or exceeds the maximal distension, the voltage vector pattern becomes patched [13], and if the DC source voltages in the auxiliary units are unequal, the vector pattern becomes clustered.

There are studies on the control of MLIs for such unevenly distributed vector patterns obtained by setting different voltages between the main and auxiliary cells [14]. Based on the switching frequencies, low frequency approaches such as selective harmonic elimination [15]-[21]; nearest vector and nearest level methods; and high frequency methods such as Sinusoidal PWM (SPWM), sub harmonic PWM (SHPWM), space vector pulse width modulation (SVPWM), and carrier based PWM were developed for harmonic reduction. In SPWM and SHPWM control algorithms, the power cells in each phase have to be dealt individually. SVPWM is generally preferred since it deals with all of the three phases and power cells together. Several SVPWM control methods have been proposed for MLIs with equal DC voltage sources [22]-[26]. A dual SVM control strategy [23] has been proposed for asymmetric MLIs with a voltage ratio of the maximal distension for which the voltage vectors are uniformly distributed. For abnormally distributed voltage vectors due to non-integer voltage ratios and voltage ratios greater than the maximal distension the modulation can be achieved by using suitably selected non-integer ratios or by locating an equilateral triangle out of the unordered vectors [22]-[24]. In [27], [28], an offset voltage injection technique was studied to balance the output voltage of a multilevel cascaded inverter. However, the use of an integrator in the compensation method reduces the dynamic characteristics in drive applications. A multilevel multiphase feed forward space vector modulation technique was proposed to compensate the voltage imbalance in [29].

This paper makes two significant contributions. Primarily, the proposed novel algorithm can be applied to multilevel inverters irrespective of or their topology or level. Secondly, the proposed algorithm has the ability to produce a sinusoidal output irrespective of the distention ratio. The main objective of the proposed control algorithm is to provide a generalized solution for multilevel inverters when powered by isolated DC sources such as capacitors, fuel cells, and solar panels, which are easily exposed to voltage variations depending on their system dynamics.

This paper presents a generalized quadrant search based SVPWM algorithm considering three phase cascaded MLIs of type 2 powered by isolated DC voltage sources for both auxiliary and central units which results in dispersed vector patterns. Section II describes the topology of the HCMLI considered for this work. It also describes the switching states and vector patterns. In Section III, the algorithm is discussed in detail. The performance of the algorithm is validated by simulation and experimental results which are discussed in Section IV. Section V concludes this paper.

II. Power Circuit Configuration and Analysis of Voltage Vectors

Fig. 1 shows the topology of the 3-φ hybrid cascaded multilevel inverter considered for this work. It comprises of a six pulse inverter as a central unit and a single phase H Bridge inverter as an auxiliary unit connected in series with each phase of the central inverter. The number of levels can be increased by connecting additional H bridges in series. The central inverter and auxiliary units are powered by isolated DC voltage sources of V_{dc}, R_aV_{dc}, R_bV_{dc} and R_cV_{dc}, respectively. R_a, R_b and R_c are the voltage ratios of the auxiliary unit to the central unit of the respective phases. A maximum of four and six levels are attained when both the central and auxiliary units are equally powered and at the maximum distension, as shown in Fig. 2(a) and Fig. 2(b). Table I shows a comparison of the commercially available four level inverter MLI topologies. From this table it is evident that due to the capacitorless power circuit, the voltage balancing problem can be completely avoided. The number of isolated DC voltage sources is high, which is considered to be a drawback of the considered topology.

The switching states of a branch in the central unit are SA0, SB0 and SC0 and in the auxiliary unit they are SA1, SB1, and SC1. The state of the central unit can be assigned as 0 or 1 depending on whether the switches (Sp) are connected to a negative or positive terminal of the DC source and the state of the auxiliary unit can be -1, 0 or 1 as described in Table II. Among the 2^K (where K is the number of switches) available switching states only 2b (where b is the number of branches) of the states are valid for satisfying the following conditions.

1. The sources must not be short circuited.
2. The load must not be left open.

The output voltage vectors of a star connected load in terms of the switching state is given by Equation (1):

$$\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = \frac{V_{dc}}{3} \times \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \left\{ \begin{bmatrix} S_A \\ S_B \\ S_c \end{bmatrix} + \begin{bmatrix} R_a & 0 & 0 \\ 0 & R_b & 0 \\ 0 & 0 & R_c \end{bmatrix} \begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} \right\} \quad (1)$$

Where:

R_a, R_b, and R_c are the ratios of the auxiliary unit to the central unit DC source voltage of the respective phases.

By calculating the phase voltages using equation (1), the space vectors corresponding to any state of a MLI can be obtained using equation (2). The voltage vector patterns obtained for the considered topology for different ratios are shown in Fig. 2(a)-2(f).

$$V_s = V_{an} + V_{bn}.e^{j2\pi/3} + V_{cn}.e^{j4\pi/3} \quad (2)$$

Various space vector modulation schemes have been proposed for MLIs [14]-[17]. None of these methods have

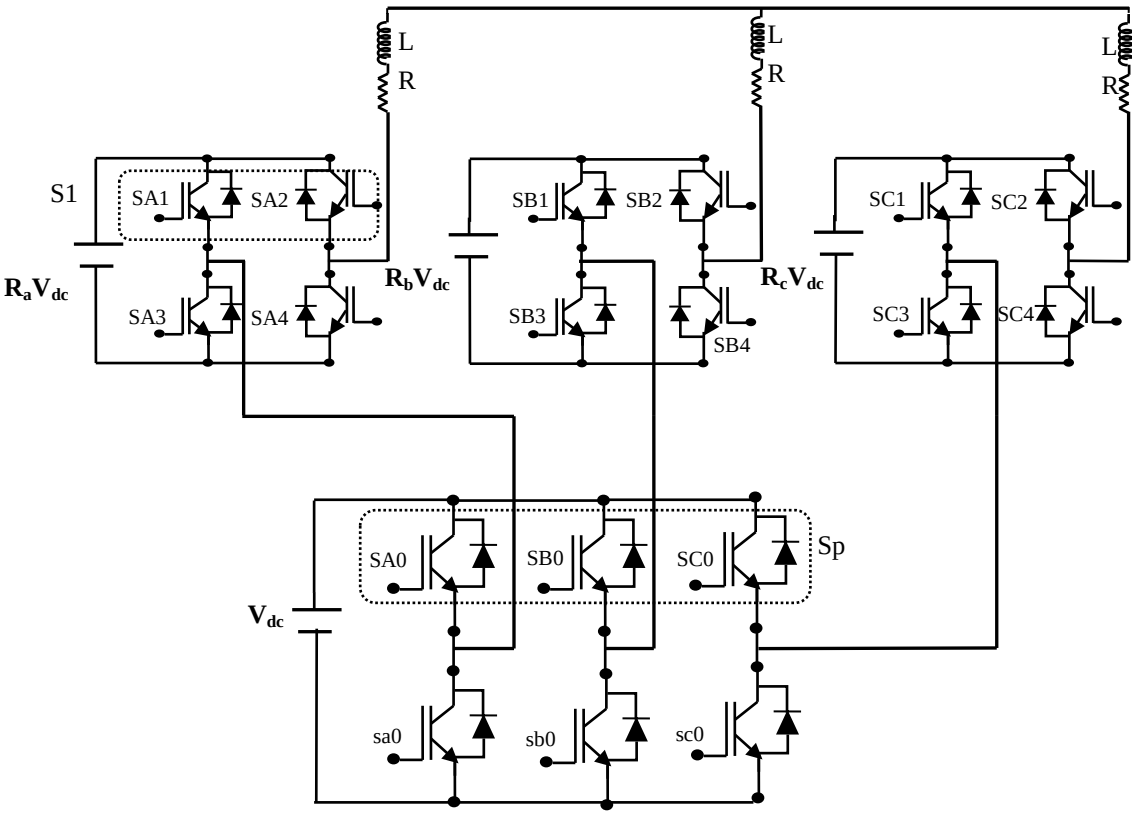


Fig. 1. Topology of 3-ϕ Hybrid cascaded Multilevel Inverter (HCMLI).

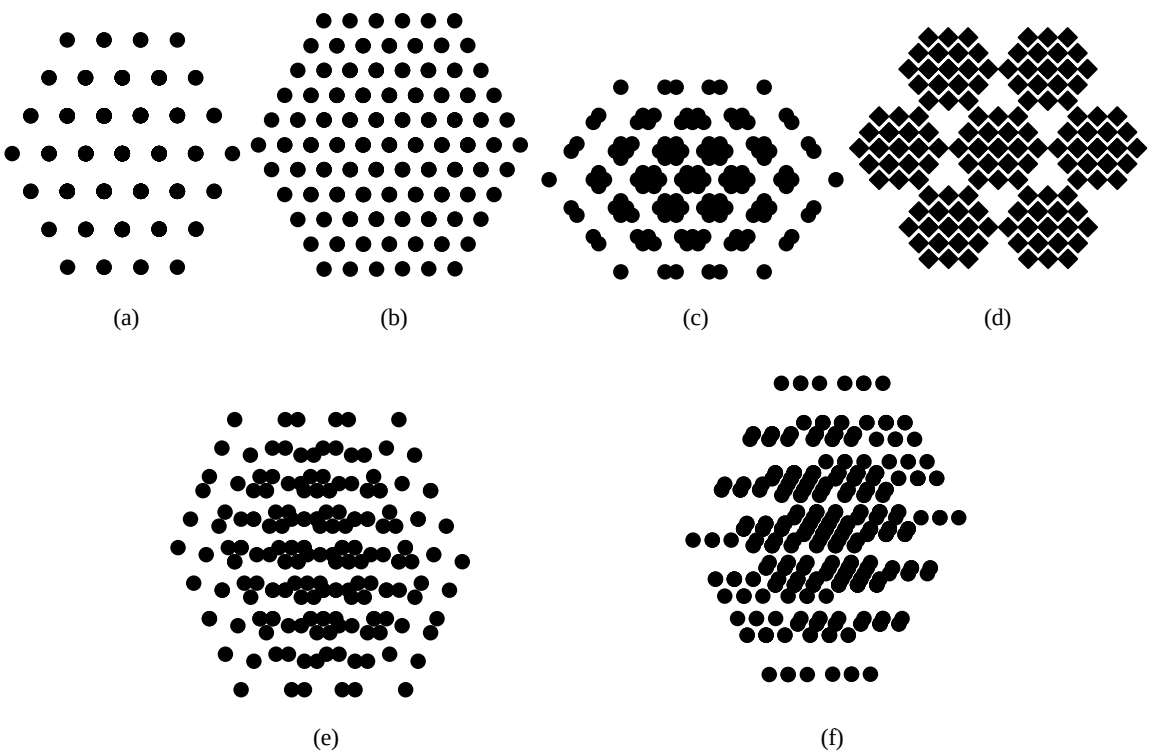


Fig. 2. (a) $R_a=R_b=R_c=1$. (b) $R_a=R_b=R_c=0.3$. (c) $R_a=R_b=R_c=0.8$. (d) $R_a=R_b=R_c=0.4$. (e) $R_a=0.8$, $R_b=0.5$ and $R_c=0.4$. (f) $R_a=0.3$, $R_b=0.7$ and $R_c=0.9$.

TABLE I
COMPARISON OF THE COMMERCIALLY AVAILABLE FOUR LEVEL MULTILEVEL TOPOLOGIES

Topology	No of Dc link Capacitor + auxiliary Capacitor	Clamping Diode	No of Switch-Diode pairs	No Of levels	No of DC Source
3-ϕ Diode Clamped (DC-MLI)	3 + 0	36	18	4	1
3-ϕ Flying Capacitor (FC-MLI)	3 + 18	-	18	4	1
3-ϕ HCMLI	-	-	**18**	**4**	**4**

TABLE II
SWITCHING STATES OF THE INVERTER UNITS

Central Unit		Auxiliary Unit		
Switch Sp	State	Switch S1		State
		SA1	SA2	
ON	1	OFF	OFF	0
		OFF	ON	1
OFF	0	ON	OFF	-1
		ON	ON	0

addressed the issue of different voltage sources ($R_a \neq R_b \neq R_c$) in the auxiliary cells. Fig. 2(e) and Fig. 2(f) portray the vector pattern for unequal voltage ratios ($R_a \neq R_b \neq R_c$) in the auxiliary units.

III. PROPOSED QUADRANT SEARCH SPACE VECTOR ALGORITHM

Fig. 3 shows a flowchart of the proposed algorithm. The major steps involved in this algorithm are as follows:

1. Determine the maximum output voltage that can be synthesized using the available voltage vectors.
2. Identification of the three nearest enclosing vectors using a quadrant search.
3. Calculation of the duty cycle for the identified vectors.

A. Determination of the Maximum Output Voltage

If the DC link voltages between the central unit and the auxiliary unit are equal, integers and less than or equal to the maximal distention then the vectors that can produce the maximum output voltage will form a hexagon, as shown in Fig. 4. The maximum synthesizable output voltage is given by Equation (3).

$$\frac{2}{3} *(V_{central} + V_{aux\_min} + V_{aux\_max}) *\cos 30^{\circ} \quad (3)$$

In the case of non-integer voltage ratios between the auxiliary and the central units, the vector distribution is dispersed as shown in Fig. 5

In which case, equation (3) is modified by a factor **X**:

$$\frac{2}{3} * (V_{central} + V_{aux\_min} + V_{aux\_max}) * \mathbf{X}$$

Where ***X*** is a factor by which the length of the maximum synthesizable output voltage reduces, as shown in Fig. 6, in order to obtain a sinusoidal output.

Hence, to obtain the maximum synthesizable voltage an algorithm is framed which is discussed below. The steps involved in this algorithm are shown in Fig. 7.

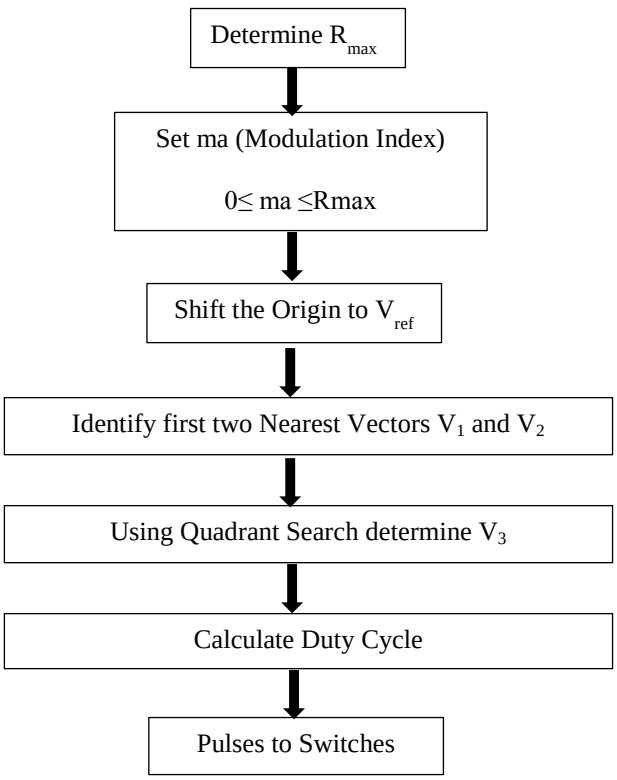


Fig. 3. Flowchart of the proposed Algorithm.

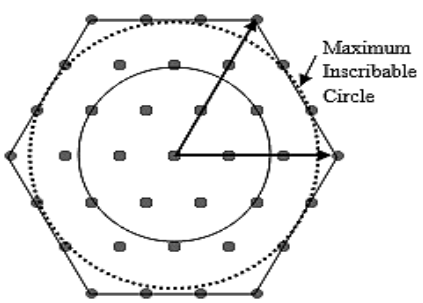


Fig. 4. Maximum synthesizable output voltage.

The angles between 0^o to 360^o are divided into M equal sectors. The maximum voltage vector in each sector (m_i where i = 1, 2, 3….. M) is identified. Three specific values of M are selected (72, 18 and 6) to illustrate how a circle of the minimum radius fits into a maximum, moderate and minimum number of points. If the scan angle is selected

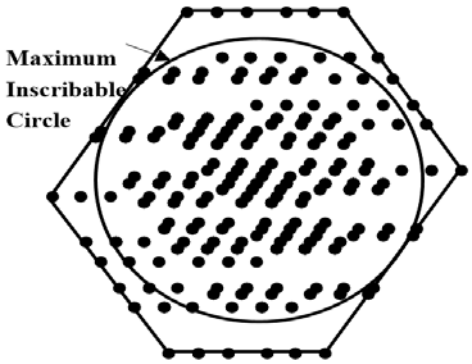


Fig. 5. Maximum output voltage – Unbalanced Condition.

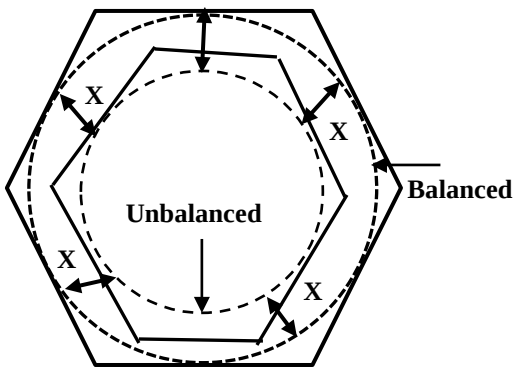


Fig. 6. Reduction in the maximum output voltage.

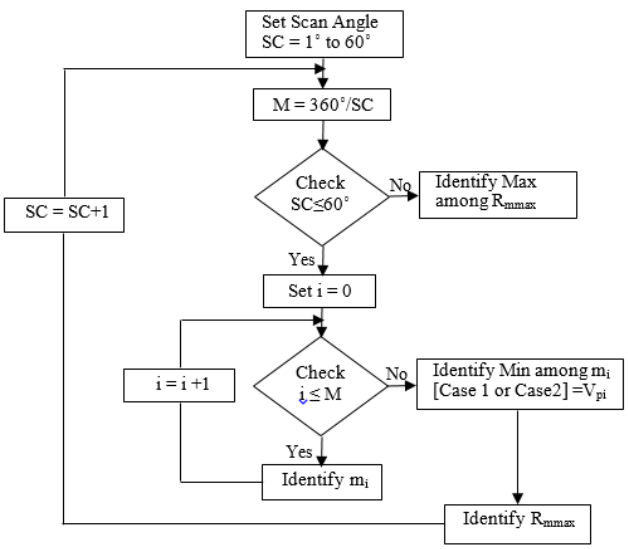


Fig. 7. Flow chart to determine R_{max}.

randomly there may be the possibility of choosing a minimum R_{max}. For the balanced case, R_{max} is obtained at M=6 as shown in Fig. 8. For the unbalanced case the maximum R_{max} is obtained when M=18 as shown in Fig. 9. To avoid such scenarios, the R_{max} values of various scan angles ranging from 1° to 60° are found and the maximum among them is selected. The above discussion is illustrated for balanced (R_a=R_b=R_c=1) and unbalanced voltage ratios (R_a=0.8, R_b=0.5, R_c=0.4) in Fig. 8 and Fig. 9, respectively.

The minimum voltage point (V_{pi}) on the line joining m_i and m_{i+1}, in adjacent sectors is determined. There are two cases for determining V_{pi}.

Let:

α = angle between the lines joining m_i, origin and m_i, m_{i+1}

β = angle between the lines joining m_{i+1}, origin and m_{i+1}, m_i

Φ = angle between m_i and the real axis

θ = angle between m_{i+1} and the real axis

V_i = vector length of m_i

V_{i+1} = vector length of m_{i+1}

***Case 1*:** If the lines joining the origin (zero vector) and the points m_i and m_{i+1} subtend an acute angle, then the length of the perpendicular distance of the line joining the vectors m_i and m_{i+1} to the origin is the minimum point, as shown in Fig. 10a. The distance ($V_{i,i+1}$) between the two vectors m_i *and* m_{i+1} can be calculated using equation (4).

$$V_{i,i+1} = \sqrt{V_i^2 + V_{i+1}^2 + 2 * V_i x V_{i+1} * \cos(\theta - \emptyset)} \quad (4)$$

If $V_{i,i+1} < \sqrt{V_i^2 + V_{i+1}^2}$ the angles α and β are acute.

V_{pi} is given by equation (5).

$$V_{pi} = V_i \times \sin\alpha \quad (5)$$

Where $\sin\alpha = \sin(\theta - \Phi) \times \frac{V_{i+1}}{V_{i,i+1}}$.

Case II: If $V_{i,i+1} > \sqrt{V_i^2 + V_{i+1}^2}$, then the minimum voltage point $V_{pi} = V_i$, as shown in Fig. 10(c).

If $V_i \leq V_{i+1}$, then $V_{pi} = V_{i+1}$, as shown in Fig. 10(b).

a. The above procedure is carried out for all of the M sectors and the values of V_{pi} in each sector are determined. The minimum among the values of V_{pi} in all of the sectors is the radius (R_{mmax}) of the maximum inscribable circle. R_{mmax} gives the maximum output voltage that can be synthesized for a particular value of M.

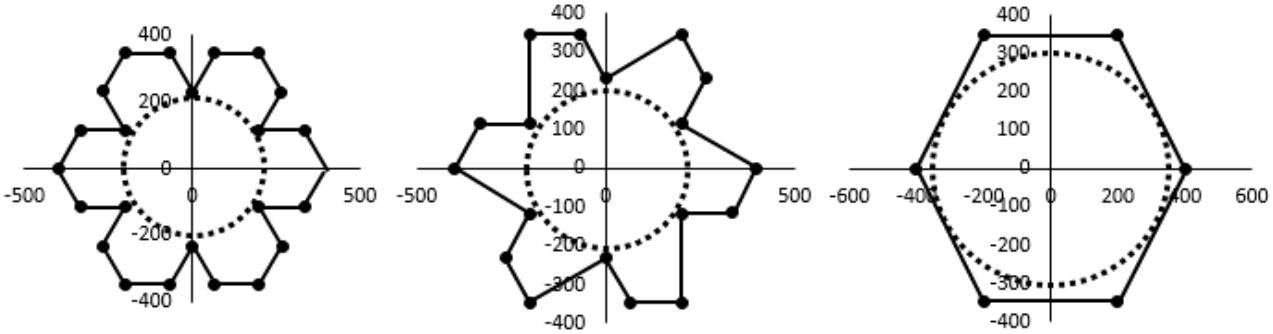
   The above procedure is repeated for different values of M as shown in Fig. 8(a)-(c) and Fig. 9(a)-(c), and the values of R_{mmax} that correspond to each of the values of M are determined.

b. To synthesize the maximum output voltage, R_{max}, which is maximum value among R_{mmax}, is selected. Fig. 11 and Fig. 12 show a plot between the different values of M and the corresponding values of R_{mmax}.

B. Quadrant Search for Vectors (V_1, V_2 and V_3)

The reference vector of a constant magnitude rotates at $2\pi f_r$ to achieve a three phase balanced output voltage with a frequency of f_r. At any instant, the reference voltage is synthesized using three switching vectors, V_1, V_2 and V_3, so that the three vectors enclose the reference vector with a lesser area. It is also used to locate the reference vector point in a way that is similar to a human eye trying to enclose a point within three points.

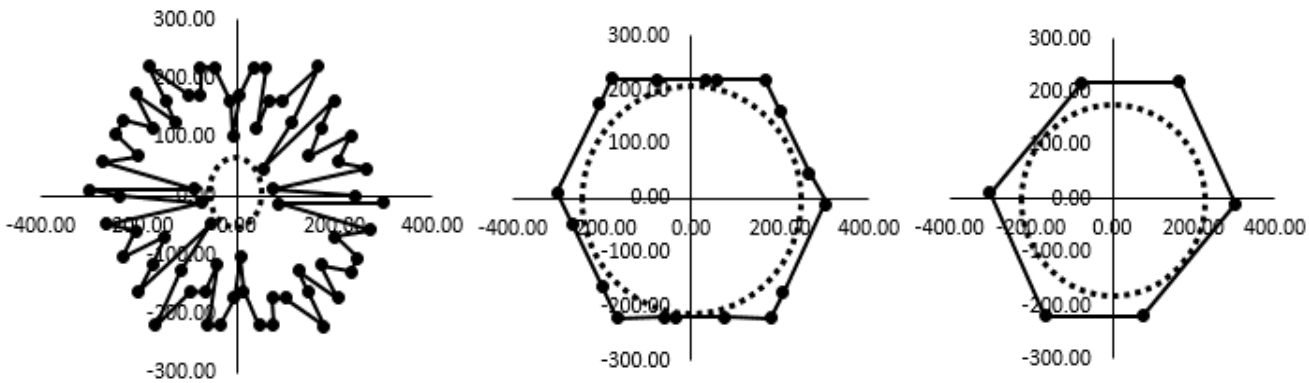
Balanced case ($R_a = R_b = R_c = 1$)



(a) i = 5 & M = 72. (b) i = 20 & M = 18. (c) i = 60 & M = 6.

Fig. 8. Maximum voltage vectors for different values of M under balance condition.

Unbalanced case ($R_a = 0.8$, $R_b = 0.5$ and $R_c = 0.4$)



(a) i = 5 & M = 72. (b) i = 20 & M = 18. (c) i = 60 & M = 6.

Fig. 9. Maximum voltage vectors for different values of M under Unbalance condition.

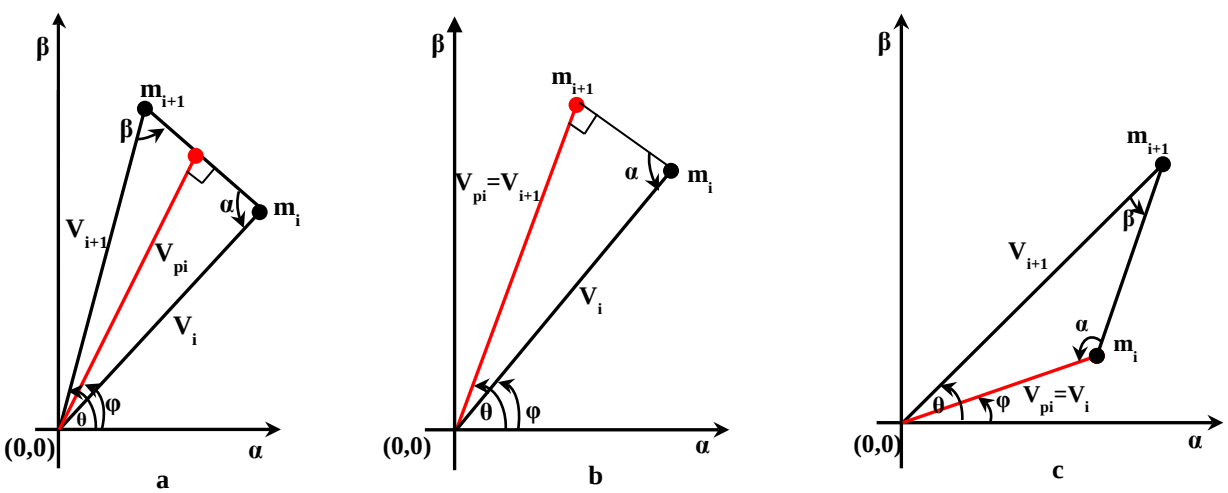


Fig. 10. Vector diagram to identify minimum point.

TABLE III
POSSIBLE POSITION OF VECTOR V3 FOR DIFFERENT LOCATIONS OF V1 AND V2

	POSSIBLE QUADRANT COMBINATIONS											
	1A	**1B**	**2A**	**2B**	**3A**	**3B**	**4A**	**4B**	**S1**	**S2**	**E1**	**E2**
POSSIBLE POSITION OF VECTORS	V_1	V_2							1	0	0	1
	V_2	V_1							0	1	1	0
			V_1	V_2					1	0	0	1
			V_2	V_1					0	1	1	0
					V_1	V_2			1	0	0	1
					V_2	V_1			0	1	1	0
							V_1	V_2	1	0	0	1
							V_2	V_1	0	1	1	0

For all Quadrant -A combinations if (S1) >(S2) and E1<= 0 and E2>=0 then all vectors covered in the shaded region can be V3
For all Quadrant -B combinations if (S1) <(S2) and E1>= 0 and E2<=0 then all vectors covered in the shaded region can be V3
1 = higher value, 0 = lesser value

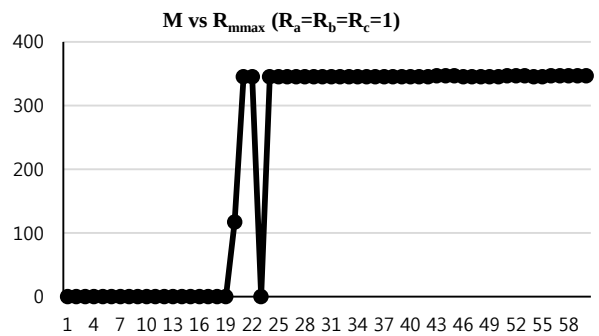


Fig. 11. Radius of Maximum Inscribable circle R_{max} = 346.4V.

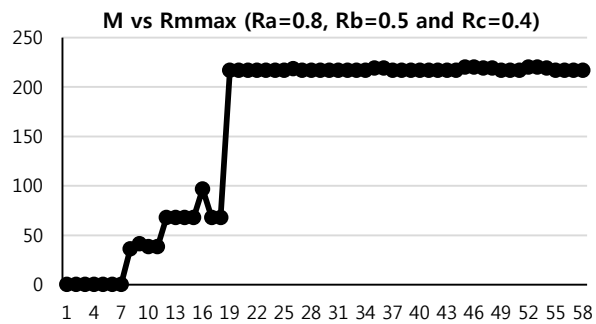


Fig. 12. Radius of Maximum Inscribable circle R_{max} = 220V.

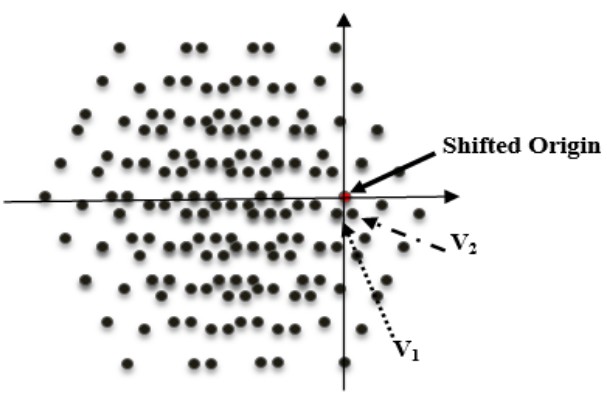


Fig. 13. Reference as shifted origin.

The whole plane is shifted with the reference point (vector) as the origin, as shown in Fig. 13. Now the nearest vectors are obtained by using simple coordinate geometry. The two nearest values are identified as the first vector (V_1) and the second vector (V_2). Then it is possible to locate V_3, the quadrant in which V_1 and V_2 lie with reference to the shifted origin, the equation of which ensures reduced voltage distortion in the output voltage. The mechanism line joining the shifted reference and the two vectors V_1 and V_2 has to be determined as E1 and E2 and their corresponding slopes S1 and S2. Based on the data, the quadrant in which the third point V_3 exist is determined, which results in ${}^4P_2=\frac{4!}{(4-2)!}$ combinations (four Quadrants with two point combinations = 12 possibilities), as shown in the Fig. 14(a)-(h).

Case A: The vectors V_1 and V_2 lie in the same quadrant as in Fig. 14(a), and the locations of V_1 and V_2 are interchanged as shown in Fig. 14(b). Possible Case A combinations are analyzed based on the line equations and their corresponding slopes when V1 and V2 lie in the same quadrant and are tabulated in Table III.

Case B: A graphical representation of vectors V_1 and V_2 in Quadrant 1 and 2 and vice versa are shown in Fig. 14(c).

Case C: A graphical representation of vectors V_1 and V_2 in Quadrant 1 and 3 and vice versa are shown in Fig. 14(d).

Case D: A graphical representation of vectors V_1 and V_2 in Quadrant 1 and 4 and vice versa are shown in Fig. 14(e).

Case E: A graphical representation of vectors V_1 and V_2 in Quadrant 2 and 3 and vice versa are shown in Fig. 14(f).

Case F: A graphical representation of vectors V_1 and V_2 in Quadrant 2 and 4 and vice versa are shown in Fig. 14(g).

Case G: A graphical representation of vectors V_1 and V_2 in Quadrant 3 and 4 and vice versa are shown in Fig. 14(h).

All of the possible quadrant combinations ***case (B–G)*** are analyzed based on the line equation and their corresponding slopes and are tabulated in Table IV.

In Fig. 14 (a)-(h), the shaded regions indicate the quadrant in which the third vectors V_3 are located**.** Having found the

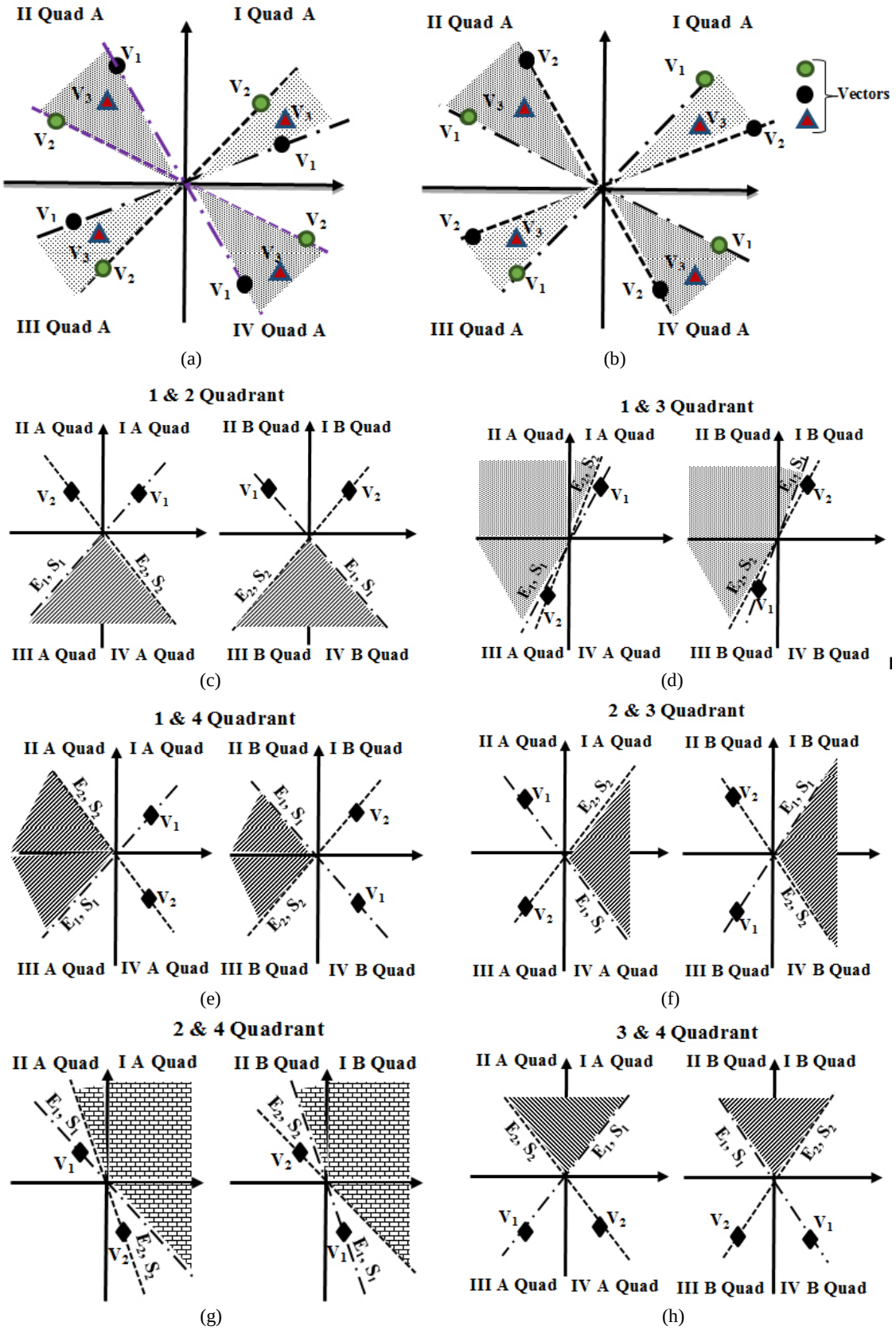


Fig. 14. Graphical representation of CASE A. (a) Quadrant A combination. (b) Quadrant B Combination. (c) Location of V_3 when V_1 and V_2 are in quadrant 1 and 2. (d) Location of V_3 when V_1 and V_2 are in quadrant 1 and 3. (e) Location of V3 when V1 and V2 are in quadrant 1 and 4. (f) Location of V3 when V1 and V2 are in quadrant 2 and 3. (g) Location of V3 when V1 and V2 are in quadrant 2 and 4. (h) Location of V_3 when V_1 and V_2 are in quadrant 3 and 4.

TABLE IV
POSSIBLE POSITION OF VECTOR V_3 FOR DIFFERENT LOCATIONS OF V_1 AND V_2

	POSSIBLE QUADRANT COMBINATIONS											
POSSIBLE LOCATION OF VECTORS	**1A**	**1B**	**2A**	**2B**	**3A**	**3B**	**4A**	**4B**	**S1**	**S2**	**E1**	**E2**
	V_1		V_2						1	0	1	0
		V_2		V_1					0	1	0	1
	V_1				V_2				1	0	1	0
		V_2				V_1			0	1	0	1
	V_1						V_2		1	0	0	1
		V_2						V_1	0	1	1	0
			V_1		V_2				1	0	0	1
				V_2		V_1			0	1	1	0
			V_1				V_2		1	0	1	0
				V_2				V_1	0	1	0	1
					V_1		V_2		1	0	1	0
						V_2		V_1	0	1	0	1

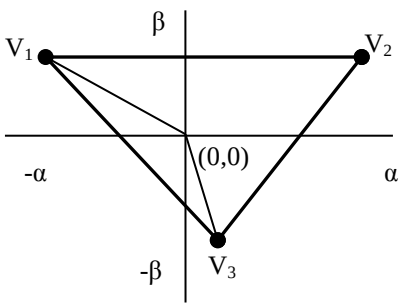


Fig. 15. Reference vector Synthesis.

quadrant, the nearest of the selected V_3 vectors is determined. The data obtained in Table III and Table IV are based on a geometric analysis of the distributed voltage vectors.

C. Calculation of the Duty Cycle for the Switching Vectors

The ON time of the switches depends on the duty cycles of the three switching vectors. From Fig. 15, by vector addition to synthesize the reference voltage (V_r), equation (6) must be satisfied. By solving equations (7), (8) and (9), D_1, D_2 and D_3 can be determined.

$$D_1V_1 + D_2V_2 + D_3V_3 = V_r \quad (6)$$

This implies that:

$$D_1X_1 + D_2X_2 + D_3X_3 = 0 \quad (7)$$

$$D_1Y_1 + D_2Y_2 + D_3Y_3 = 0 \quad (8)$$

Where Di is the duty cycle and Xi, Yi are the co-ordinates of Vi with reference to Vr (where i = 1, 2, 3) and since V1, V2 and V3 encloses Vr.

$$D_1 + D_2 + D_3 = 1 \quad (9)$$

Equations (6) and (7) suggest a way to use PWM to generate a three phase voltage of which the average value follows a given three phase reference by switching among the vectors V_1, V_2 and V_3 with the duty cycles of D_1, D_2 and D_3, respectively.

The modulation index (m_a) is given by:

$$m_a = \frac{V_{ref}}{V_d} \quad (10)$$

$$V_{ref(max)} = R_{max}$$

$$V_d = \frac{2}{3} * (V_{Central} + V_{Aux\_max} + V_{Aux\_min}) \quad (11)$$

$$m_{max} = \frac{V_{ref\_max}}{V_d} = 0.866$$

The range of m_a is $0 \le m_a \le 0.866$

IV. SIMULATION AND EXPERIMENTAL RESULTS

The performance of the proposed modulation technique has been validated by both simulation and experimental verification. A conventional test was conducted, as shown in Fig. 16, for the 3-φ squirrel cage induction motor to estimate its equivalent circuit parameters. The estimated motor parameters are shown in Table V. The same parameters are used for simulation in Matlab/Simulink. A Nexys-2 Spartan-3E FPGA was used to implement the algorithm.

A 3-ϕ hybrid cascaded multilevel inverter was built using four smart power IGBTs with built in gate driver (FSBB20CH60B) modules. The rating of any power device depends on the commutation voltage, which is defined by the DC voltage of the unit in which the device is connected. Since the maximum commutation voltage among all of the switches under all of the considered cases was found to be 200V in the simulation. Hence, power IGBTs (18) of 600V, 20A were selected. The modules were fixed with a suitable heat sink and snubber circuit for protection. A diode rectifier rated at 600V, 35A was provided at the converter input for AC voltage to DC bus voltage conversion. All of the PWM signals are isolated using an IC 6N137. Sensors are provided for current measurement. An Agilent Infinii vision oscilloscope was used to capture the waveforms.

The simulation and experimental verifications were done at no load, as shown in Fig. 17 and Fig. 18, for the four different cases listed in Table VI.

TABLE V
MOTOR SPECIFICATIONS

Rated Power	0.37kw (0.5Hp)
Rated Voltage	415 (rms)
Rated Current	1.2A (star)
No of Pole Pairs	2
Rated torque	2.54 Nm
Rated speed	1500 rpm
Frequency	50Hz
Duty	S1
Stator Resistance (R_s)	32.71Ω
Stator Inductance (LI_s)	0.1035H
Rotor Resistance (R_r')	20.47 Ω
Rotor Inductance (LI_r')	0.1028H
Mutual Inductance (L_m)	1.1H

TABLE VI
SIMULATION PARAMETERS

	Value
3φ Induction Motor (Star)	Refer Table. 5
Central Cell DC Voltage	200 V
Output Voltage frequency	50 Hz
Switching frequency	5 kHz
Auxiliary cell DC Voltage Source	
Case I – Balanced Condition	R_a=R_b=R_c =1
Case II-Above Maximum distention	R_a=R_b=R_c=0.8
Case III - Unequal Voltage ratio	R_a=0.8, R_b=0.5 and R_c=0.4
Case IV- Unequal Voltage ratio	R_a = 0.3, R_b = 0.7and R_c=0.9

Fig. 16. Conventional test to estimate the motor parameters.

Case I-Balanced Condition (R_a = R_b = R_c = 1)

Simulation and experimental verifications were carried out by setting V_{dc}=200V, R_aV_{dc}=R_bV_{dc}=R_cV_{dc} =200V and operating the machine at no load. R_{max} for this case was found to be 346.6V. At a modulation index of m_a = 0.66, $V_{L\ (peak)}$ = 578V,

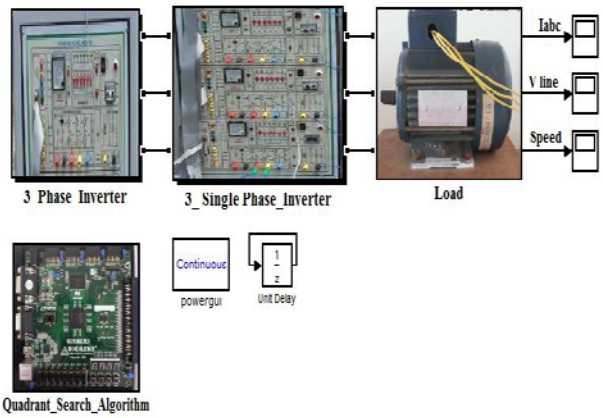


Fig. 17. Simulation of the Algorithm by MATLAB/Simulink.

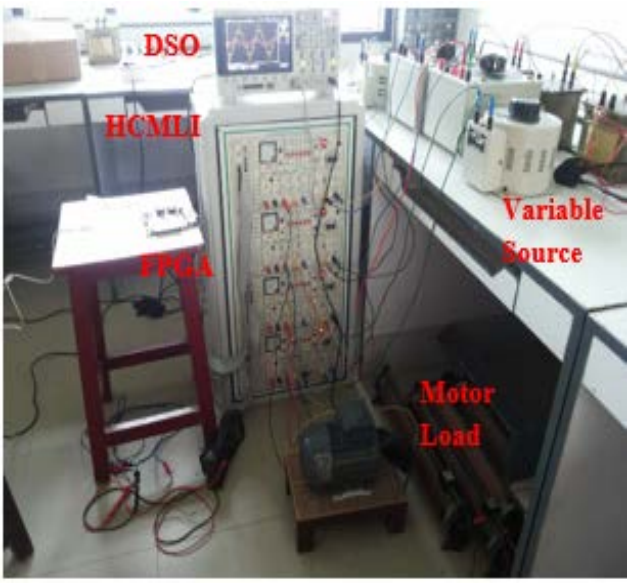


Fig. 18. Experimental setup for verification of the Algorithm.

$V_{L\ (rms)}$ = 408V. In addition, $I_{L\ (peak)}$ = 0.714A, $I_{L\ (rms)}$ = 0.505A and speed of the motor was 1473 rpm. As shown in Fig. 19 and Fig. 20 similar results were obtained in both the simulation and the experiment. The THD of the load current was found to be 0.82%.

Case II-Above the Maximum distention (R_a = R_b = R_c = 0.8)

Voltages of V_{DC} = 200V, R_AV_{DC}=RbV_{DC}=R_CV_{DC}=160V were applied for both the simulation and experimental setups and the machine was operated at no load. The Rmax for this case was found to be 300.5V. At a modulation index of ma = 0.77, VL (peak) = 266.9V, VL (rms) = 188.7V. In addition, IL (peak) = 0.72A, IL (rms) = 0.51A and speed of the motor was 1473 rpm. From Fig. 21 and Fig. 22 it is evident that similar results were obtained from both the simulation and the experiment. The THD of the load current was 1.60%.

Case III- Unbalance ratios Ra = 0.3, Rb = 0.7 and Rc = 0.9

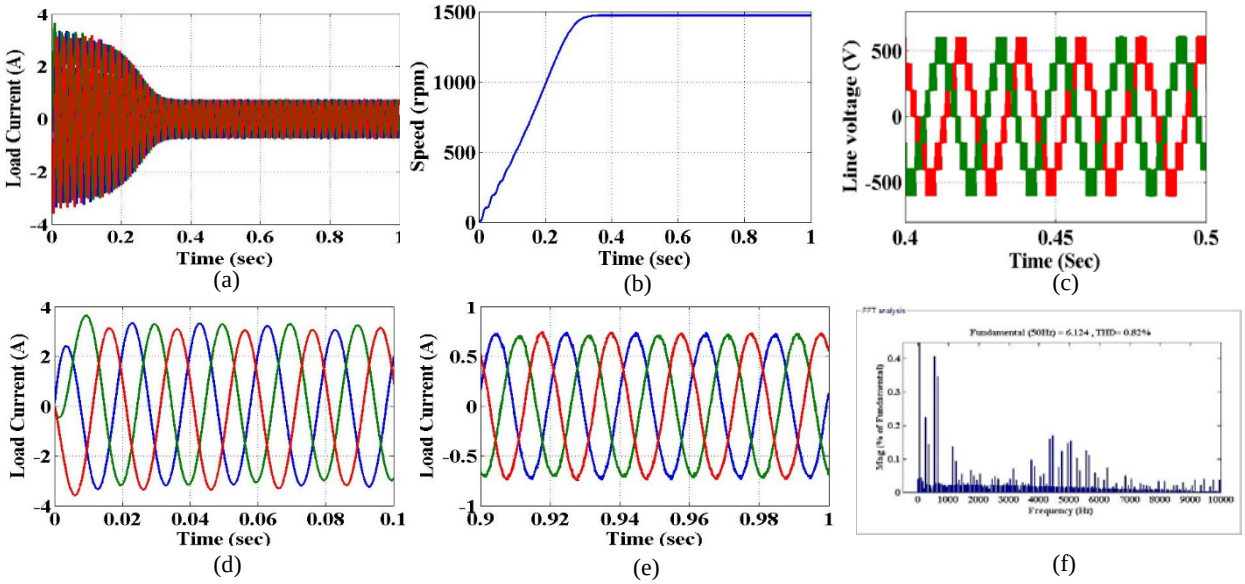


Fig. 19. Simulation results obtained for balanced voltage ratios (R_a=R_b=R_c=1) with motor load. (a) Load current. (b) Speed of the motor. (c) Line voltages. (d) and (e) Enlarged view of current at (0-0.1sec) and (0.9 -1 sec). (f) THD of load current (0.82%).

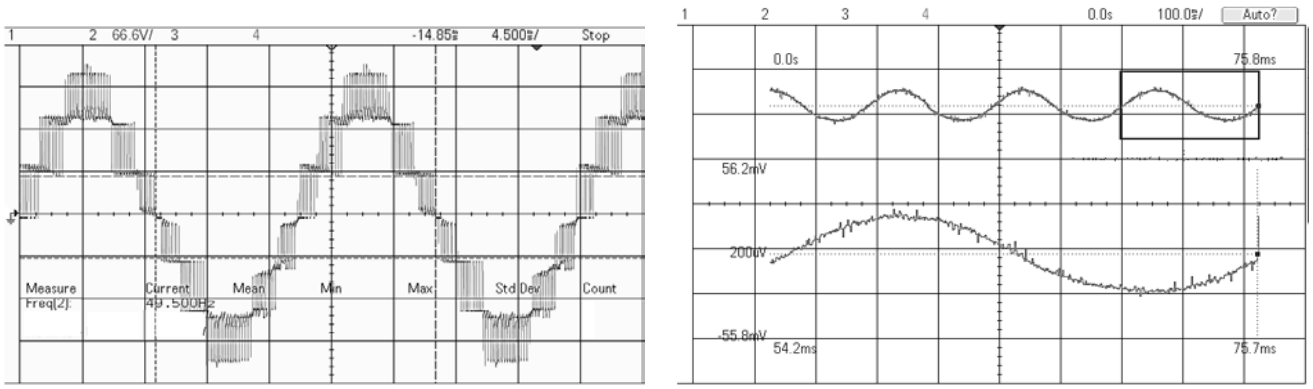


Fig. 20. Line voltage and Load current for (R_a=R_b=R_c= 1) at no load & ma = 0.66.

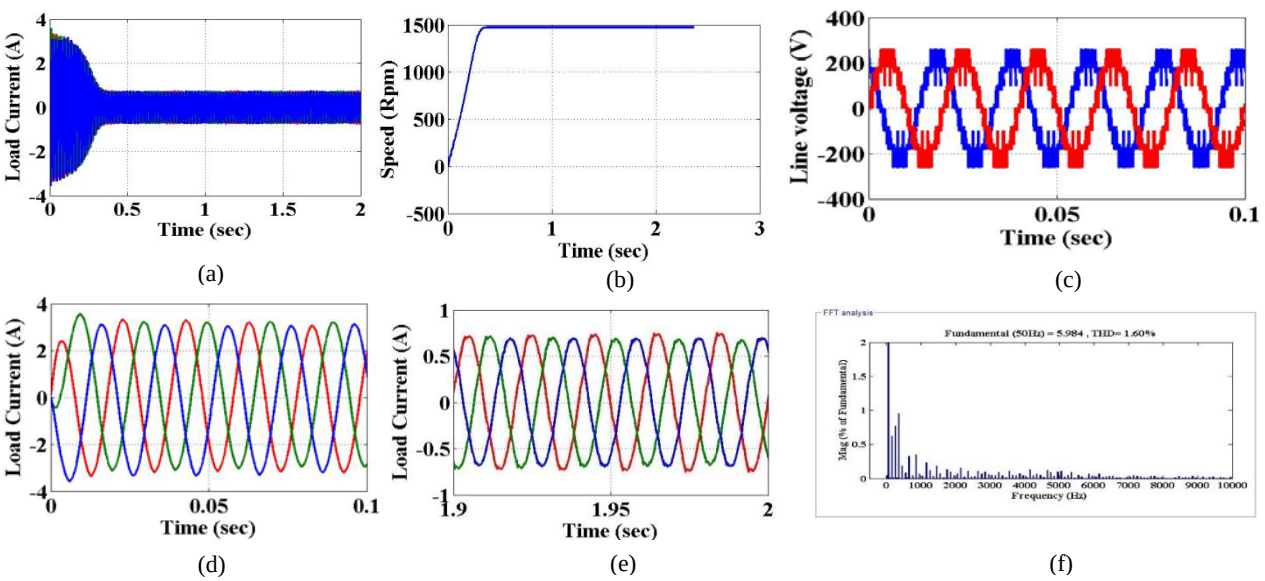


Fig. 21. Simulation results for voltage ratios (R_a=R_b=R_c=0.8) with motor load. a) Load current, b) Speed of the motor, c) line voltages d and e) Enlarged view of current at (0-0.1sec) and (1.9 -2 sec) (f) THD of load current (1.60%).

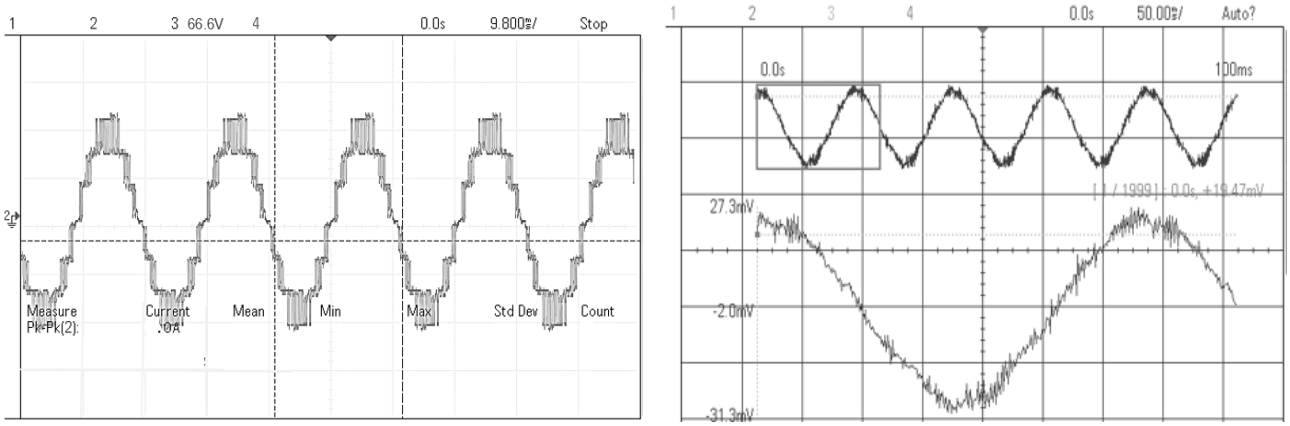


Fig. 22. Line voltage and Load current for (R_a=R_b=R_c=0.8) at no load & ma = 0.77.

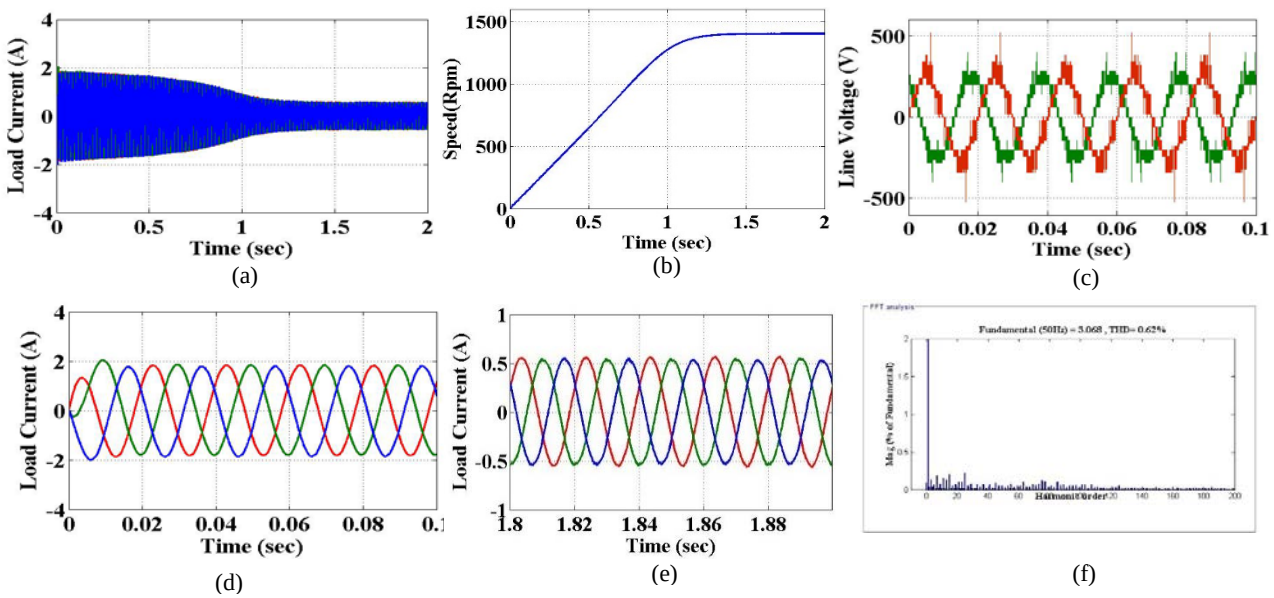


Fig. 23. Simulation results for voltage ratios (R_a=0.3, R_b=0.7 and R_c=0.9) with motor load. (a) Load current. (b) Speed of the motor. (c) line voltages. (d) and (e) Enlarged view of current at (0-0.1sec) and (1.8 – 1.9 sec). (f) THD of load current (0.62%).

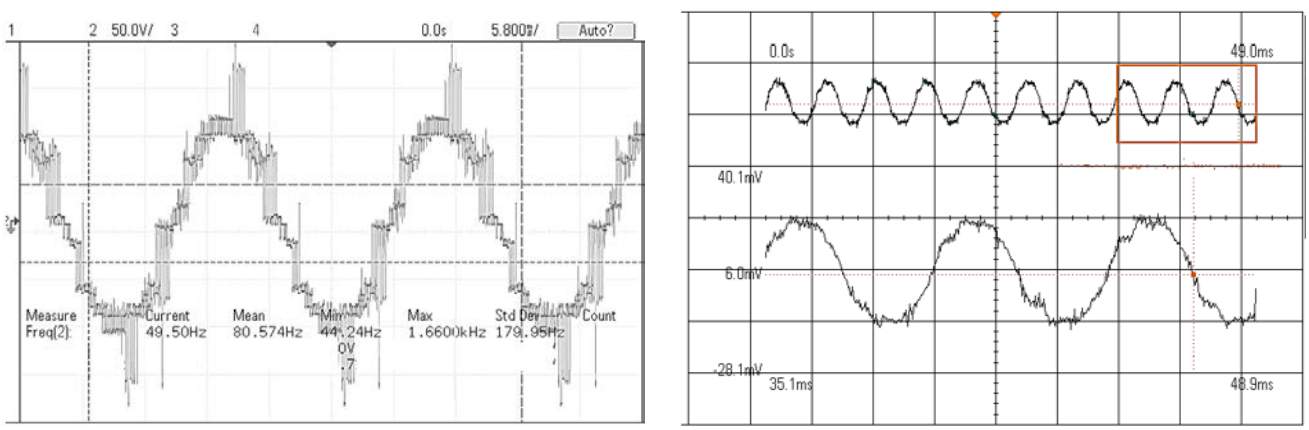


Fig. 24. Line voltage and Load current for (R_a=0.3, R_b=0.7 and R_c=0.9) at no load & ma = 0.5.

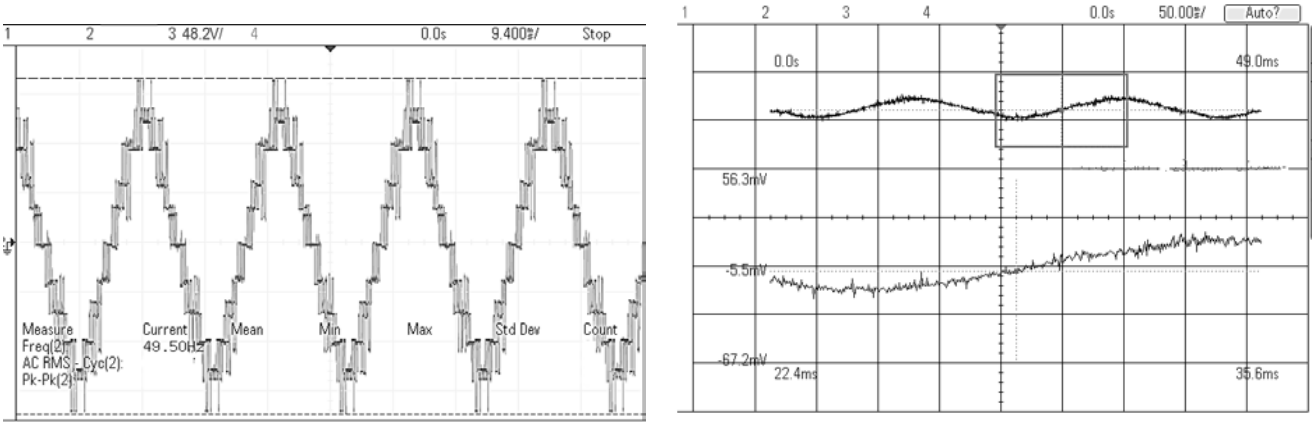


Fig. 25. Line voltage and Load current for (R_a=0.8, R_b=0.5 and R_c=0.4) at no load & ma = 0.5.

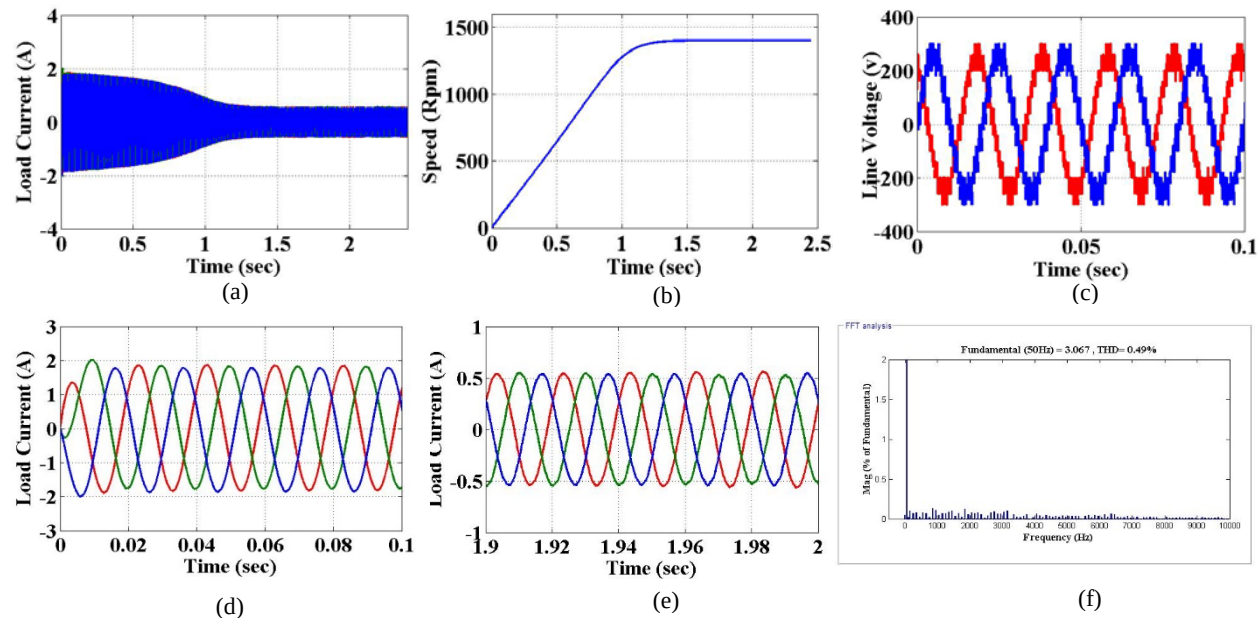


Fig. 26. Simulation results for voltage ratios (Ra=0.8, Rb=0.5 and Rc=0.4) with motor load. (a) Load current. (b) Speed of the motor. (c) line voltages. (d) and (e) Enlarged view of current at (0-0.1sec) and (1.9 -2 sec),(f) THD of load current (0.49%).

Assuming that a voltage fluctuation has occurred, an unbalance in the voltage among the auxiliary units was created by adjusting the isolated DC voltage sources to Vdc = 200V, RaVdc = 60V, RbVdc = 140V and RcVdc = 180V. The radius of the maximum inscribable circle Rmax for this case was found to be 230.6V. For ma = 0.5, VL (peak) = 254V, VL (rms) = 179.6. In addition, IL (peak) = 0.58A, IL (rms) = 0.41A and speed of the motor was 1400 rpm. From Fig. 23 and Fig. 24 it can be seen that due to DC voltage fluctuations the line voltage is distorted but the load current remains sinusoidal verifying the capability of the proposed algorithm. The THD of the load current was found to be 0.62% as shown in Fig. 23(f).

Case III- Unbalance ratios Ra = 0.8, Rb = 0.5 and Rc = 0.4

To demonstrate that a voltage fluctuation has occurred, an unbalance in voltage among the auxiliary units was created by setting the isolated DC voltage sources to different voltages, Vdc = 200V, RaVdc = 160V, RbVdc = 100V and RcVdc = 80V. The radius of the maximum inscribable circle Rmax for this case was found to be 220.V. For ma = 0.5, VL (peak) = 298V, VL (rms) = 210V. In addition, IL (peak) = 0.51A, IL (rms) = 0.36A and speed of the motor was 1400 rpm. From Fig. 25 and Fig. 26 it can be seen that the line voltage is distorted due to DC voltage fluctuations but the load current is still sinusoidal verifying the capability of the proposed algorithm. The THD of the load current was found to be 0.49% as shown in Fig. 26(f).

V. Conclusion

An offline quadrant search space vector algorithm has been investigated for a 3-ϕ Hybrid cascaded MLI. The MLI has two stages which are a central six pulse inverter cascaded with a 1-ϕ H Bridge inverter as an auxiliary unit in each phase. The process of space vector modulation is for the identification of the three nearest vectors. The proposed

algorithm can be extended to any three phase multilevel inverters irrespective of topology, number of levels and distention ratios. The difference between topologies is only the switching states corresponding to the vectors. The results show that the proposed technique generates an output with an improved quality when compared to other techniques proposed in the literature. In addition, this technique is also suitable for any voltage ratio which produces evenly, islanded and clustered voltage vectors. The voltage level in each step of the output voltage is not the same as in the case of clustered voltage vectors. An experimental investigation was carried out to validate the proposed algorithm and it yielded significant results.

REFERENCES

[1] J. S. Lai and F. Z. Peng, "Multilevel converters – A new breed of power converters," *IEEE Trans. Ind. Appl*., Vol. 32, No. 3, pp. 509-517, May/Jun. 1996.

[2] J. Rodriguez, L. G. Franquelo, S. Kouro, J. I. Leon, R. C. Portillo, M. A. M. Prats, and M. A. Perez, "Multilevel converters: An enabling technology for high-power applications," *Proc. IEEE*, Vol. 97, No. 11, pp.1786-1817, 2009.

[3] L. Maharjan, S. Inoue, and H. Akagi, "A transformerless energy storage system based on a cascade multilevel PWM converter with star configuration", *IEEE Trans. Ind. Appl*., Vol. 44, No. 5, pp.1621-1630, Sep./Oct. 2008.

[4] L. G. Franquelo, J. Rodriguez, J. I. Leon, Kouro, S.-R. Portillo, and M. A. M. Prats, "The age of multilevel converters arrives," *IEEE Ind. Electron. Mag.*, Vol. 2, No. 2, pp. 28-39, Jun. 2008.

[5] J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, Vol. 49, No. 4, pp. 724-738, Aug. 2002.

[6] R. Teodorescu, F. Blaabjerg, J. K. Pedersen, E. Cengelci, and P. N. Enjeti, "Multilevel inverter by cascading industrial VSI," *IEEE Trans. Ind. Electron*., Vol. 49, No. 4, pp.832-838, Aug. 2002.

[7] B. K. Bose, "Power electronics and motor drives recent progress and perspective", *IEEE Trans. Ind. Electron.*, Vol. 56, No. 2, pp. 581-588, Feb. 2009.

[8] Y. S. Lai and F. S. Shyu, "Topology for hybrid multilevel inverter," *Proc. Inst. Elect. Eng.—Elect. Power Appl.*, Vol. 149, No. 6, pp.449-458, 2002.

[9] R. Rabinovici, D. Baimel, J. Tomasik, and A. Zuckerberger, "Series space vector modulation for multi-level cascaded H-bridge inverters," *IET Power Electron.*, Vol. 3, No. 6, pp.843-857, Nov. 2010.

[10] H. Liu, L. M. Tolbert, S. Khomfoi, B. Ozpineci, and Z. Du, "Hybrid cascaded multilevel inverter with PWM control method," *Proc. IEEE 39th Power Electron. Spec. Conf.*, pp. 162-166, 2008.

[11] K. A. Corzine, S. D. Sudhoff, and C. A.Whitcomb, "Performance characteristics of a cascaded two-level converter," *IEEE Trans. Energy Convers*, Vol. 14, No. 5, pp. 433-439, Sep. 1999.

[12] X. Kou, K. A. Corzine, and M. W. Wielebski, "Over-distention operation of cascaded multilevel inverters," *Proc. IEEE Int. Elect. Mach. Drives Conf*., pp. 1535-1542, 2003.

[13] S. Lu, S. Mariethoz, and K. A. Corzine, "Asymmetrical cascade multilevel converters with non integer or dynamically changing DC voltage ratios: Concepts and modulation techniques," *IEEE Trans. Ind. Electron.*, Vol. 57, No. 7, pp. 2411-2418, Jul. 2010.

[14] Z. Du, L. M. Tolbert, and J. N. Chiasson, "Active harmonic elimination for multilevel converters," IEEE Transactions on Power Electronics, Vol. 21, No. 2, pp. 459-469, Mar. 2006.

[15] M. G. H. Aghdam, S. H. Fathi, and G. B. Gharehpetian, "Elimination of harmonics in a multi-level inverter with unequal DC sources using the homotopy algorithm," *IEEE International Symposium on Industrial Electronics*, pp. 578-583, 2007.

[16] T. Tang, J. Han, and X. Tan, "Selective harmonic elimination for a cascade multilevel inverter," *IEEE International Symposium on Industrial Electronics*, pp.977-981, 2006.

[17] J. R. Wells, B. M. Nee, and P. L. Chapman, "Selective harmonic control: A general problem formulation and selected solutions," *IEEE Trans. Power Electron*., Vol. 20, No. 6, pp. 1337-1345, Nov. 2005.

[18] M. S. A. Dahidah and V. G. Agelidis, "Selective harmonic elimination PWM control for cascaded multilevel voltage source converters: A generalized formula," *IEEE Trans. Power Electron*., Vol. 23, No. 4, pp. 1620-1630, Jul. 2008.

[19] D. W. Kang, H. C. Kim, T. J. Kim, and D. S. Hyun, "A simple method for acquiring the conducting angle in a multilevel cascaded inverter using step pulse waves," *IEE Proceedings on Electric Power Applications*, Vol. 152, pp. 103-111, 2005.

[20] Y. Liu, H. Hong, and A. Q. Huang, "Real-time calculation of switching angles minimizing THD for multilevel inverters with step modulation," *IEEE Trans. Ind. Electron*., Vol. 56, No. 2, pp. 285-293, Feb. 2009.

[21] T. Ishida, T. Miyamoto, T. Oota, K. Matsuse, K. Sasagawa, and L. Huang, "A control strategy for a five-level double converter with adjustable DC link voltage," *Industry Applications Conference*, pp. 530-536, 2002.

[22] S. K. Mondal, J. O. P. Pinto, and B. K. Bose, "A neural-network-based space vector pwm controller for a three-level voltage-fed inverter induction motor drive," *IEEE Trans. Power Electron.*, Vol. 38, No. 3, pp. 660-669, May/Jun. 2002.

[23] N. Celanovic and D. Boroyevich, "A fast space vector modulation algorithm for multilevel three phase converters," *IEEE Trans. Ind. Appl.*, Vol. 37, No. 2, pp. 637-641, Mar./Apr. 2001.

[24] S. Wei, B. Wu, F. Li, and C. Liu, "A general space vector pwm control algorithm for multilevel inverters," *Applied Power Electronics Conference and Exposition, Eighteenth Annual IEEE*, Vol. 1, pp. 562-568, 2003.

[25] S. Mekhilef, and M. N. A. Kadir, "Novel vector control method for three-stage hybrid cascaded multilevel inverter," *IEEE Trans. Ind. Electron.*, Vol. 58, No. 4, pp. 1339-1349, Apr. 2011.

[26] S. Vazquez, J. I. Leon, L. G. Franquelo, J. J. Padilla, and J. M. Carrasco, "DC voltage ratio control strategy for multilevel cascaded converters fed with a single dc source," *IEEE Trans. Ind. Electron.*, Vol. 56, No. 7, pp. 2513-2521, Jul. 2009.

[27] Y. Cho, T. Labella, J.-S. Lai, and M. K. Senesky, "A carrier-based neutral Voltage Modulation strategy for multilevel cascaded inverters under unbalanced DC sources," *IEEE Trans. Ind. Electron.*, Vol. 61, No. 2, pp.

625-636, Feb. 2014.
[28] Y. M. Park, H. S. Ryu, H. W. Lee, M. G. Jung, and S. H. Lee, " Design of a cascaded h-bridge multilevel inverter based on power electronics building blocks and control for high performance," *Journal of Power Electronics*, Vol. 10, No. 3, pp. 262-269, May 2010.
[29] F. Carnielutti, H. Pinheiro, and C. Rech, "Generalized Carrier-based modulation strategy for cascaded multilevel converters operating under fault conditions," *IEEE Trans. Ind. Electron*., Vol. 59, No. 2, pp. 679-689, Feb. 2012.

Johnson Anitha Roseline received her Bachelor degree in 2002 from the University of Madras, Chennai, India, in 2002. She received and Master degree in 2006 from Anna University. She is presently working as an Assistant Professor in the Department of Electrical and Electronics Engineering at the SSN College of Engineering, Chennai, India. She has 12 years of academic experience. Her current research interests include power electronics and control.

Subramanian Vijayenthiran received his Bachelor degrees in Electrical and Electronics Engineering from Anna University, Chennai, India, in 2013. He is presently working as Research Assistant in the Department of Electrical and Electronics Engineering at the SSN College of Engineering, Chennai, India. His current research interest include robotics and power electronics.

Rajini V received her B.E. and M.E. degrees from Annamalai University, Chidambaram, India, and her Ph.D. degree from Anna University, Chennai, India. She is presently a Professor at the SSN College of Engineering, Chennai, India. She has 22 years of academic experience. Her current research interests include power electronics and high voltage engineering.

Senthil Kumaran Mahadevan received his Bachelor and Master degrees in Electrical and Electronics Engineering from the University of Madras, Chennai, India, in 1999 and 2001, respectively, and his Ph.D. degree from Anna University, Chennai, India, in 2013. He is presently working as an Assistant Professor in the Department of Electrical and Electronics Engineering at the SSN College of Engineering, Chennai, India. His current research interests include electric drives, control and signal processing,