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A Bidirectional Single-Stage DC/AC Converter for Grid Connected Energy Storage Systems

Jianliang Chen*, Xiaozhong Liao*, and Deshang Sha†

*†School of Automation, Beijing Institute of Technology, Beijing, China

Abstract

In this paper, a unified control strategy using the current space vector modulation (CSVM) technique is proposed and applied to a bidirectional three-phase DC/AC converter. The operation of the converter changes with the direction of the power flow. In the charging mode, it works as a buck type rectifier; and during the discharging mode, it operates as a boost type inverter, which makes it suitable as an interface between high voltage AC grids and low voltage energy storage devices. This topology has the following advantages: high conversion efficiency, high power factor at the grid side, tight control of the charging current and fast transition between the charging and discharging modes. The operating principle of the mode analysis, the gate signal generation, the general control strategy and the transition from a constant current (CC) to a constant voltage (CV) in the charging mode are discussed. The proposed control strategy has been validated by simulations and experimental results obtained with a 1kW laboratory prototype using supercapacitors as an energy storage device.

Key words: Bidirectional power flow, Current source converter, Energy storage system

I. INTRODUCTION

Energy storage systems (ESSs) are widely used in many applications such as UPS, electrical vehicles and distributed power generation systems [1]-[3]. The voltage rating for each cell in an energy storage device (ESD) such as supercapacitors or batteries is relatively low. To allow for use in high voltage applications, many cells are series connected, which decreases the system reliability by adding a voltage equalizer to each cell [4], [5]. Therefore, it is desirable to keep the number of cells as low as possible to avoid complicated voltage equalizing circuits. This leads to the amplitude of the DC side voltage being lower than that of the AC side grid voltage.

The well-known voltage-source inverter (VSI) is a buck type inverter when power flows from DC to AC and a boost type PWM rectifier when it is the other way around [6], [7]. This means the amplitude of the DC side voltage must be greater than that of the AC side. In addition, the DC current cannot be regulated tightly due to the lack of a DC side inductor. This makes it unsuitable for ESSs with low voltage ESDs.

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†Corresponding Author: shadeshang@bit.edu.cn
Tel: +86-010-68918613, Beijing Institute of Technology
*School of Automation, Beijing Institute of Technology, China

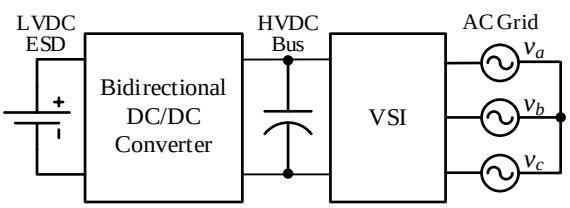


Fig. 1. Bidirectional DC/DC converter cascaded with VSI.

In order to overcome the shortcomings of the conventional VSI, a double-stage power conversion system typically involving a bidirectional DC/DC converter cascaded with the VSI, as shown in Fig. 1, can be used [8], [9]. The DC/DC converter stage is to boost the low DC voltage to a higher voltage DC bus, while the VSI connects to the AC grid. However, this topology requires two separate control strategies and bulky electrolytic capacitors at the DC bus, resulting in lower reliability and efficiency, as well as a more complicated control scheme.

In literature [10], [11], a high frequency AC link (HFACL) is used for isolation and to raise the low DC voltage. However, the front end switches may suffer from high voltage stress resulting from hard switching during current commutation. In addition, the high frequency transformer will decrease the

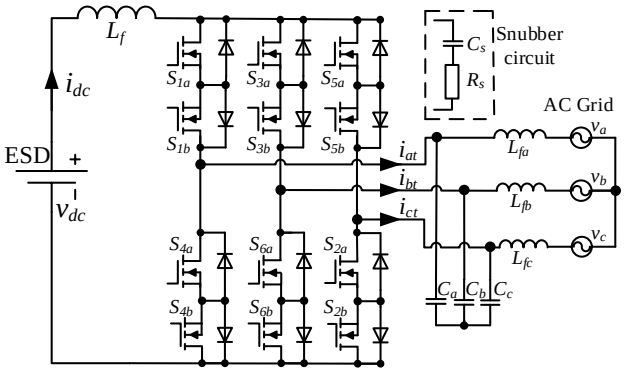


Fig. 2. Bidirectional Single-Stage DC/AC Converter.

conversion efficiency.

To achieve direct power conversion between a high voltage AC grid and a low voltage ESD and to eliminate the drawbacks of the previous solutions, a single-stage bidirectional current-source converter, as shown in Fig. 2, can be used. In the conventional current-source inverter (CSI) [12]-[16], each switch is composed of a MOSEFT in series with a diode. Then the power flow can only move from DC to AC, which makes it non-applicable for ESSs. By replacing the diode with another MOSFET, the power flow can be bidirectional. It can also operate as a step-down rectifier from AC to DC with tight control of the DC current. Owing to the DC inductor, the DC current ripple can be dramatically reduced, which is desirable for ESDs.

The power circuit and mode analysis are given and analyzed in section II. The control strategy implementation is provided in section III. The simulation results are illustrated in section IV. A 1kW experimental prototype is fabricated and tested in section V. Section VI presents some conclusions.

II. Circuit Topology and Mode Analysis

Fig. 2 shows the power circuit for the single-stage bidirectional three-phase DC/AC converter, where v_{dc} is the voltage of the ESD. v_a, v_b and v_c are three-phase line-to-neutral voltages. The converter connects to the DC side through a DC inductor L_f and to the AC side through a filter formed by L_{fa}, L_{fb}, L_{fc} and C_a, C_b, C_c. The converter is composed of six bidirectional switches, in which two MOSFETs are in anti-series connection with a common source. Therefore, an isolated power supply for the gate drivers of the two MOSFETs is not necessary. An RC snubber circuit can be connected to each bidirectional switch in parallel to avoid voltage spikes.

When it works during the discharging mode, all six of the bottom switches of each bidirectional switch (S_{xb}) are off, while the top switches (S_{xa}) conduct alternately. The current flows through the body diode of the bottom switches when the corresponding top switches are turned on. This is completely opposite to the charging mode. Therefore, only the discharging mode operation will be discussed in detail.

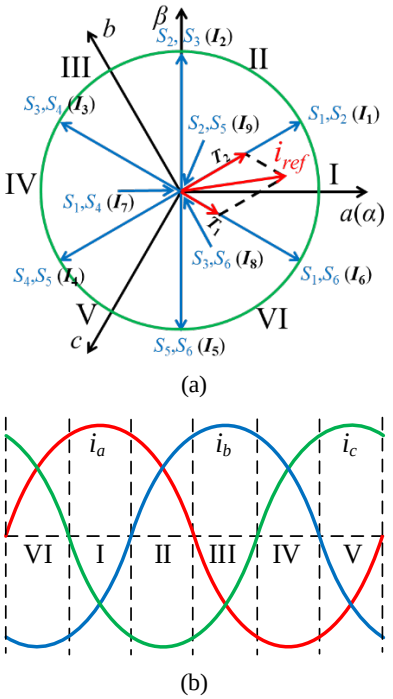


Fig. 3. (a) Current vector space. (b) Six sectors boundaries under three-phase current

Like the conventional CSI, the current in the DC side cannot be interrupted due to the existence of the DC inductor. Therefore, at least one bidirectional switch in the three upper bridges and another switch in the three lower bridges should conduct at the same time. However, if any two switches in the upper or lower bridges are turned on simultaneously, the voltage of one of the filtering capacitors may be clamped to that of another. Thus, only two bidirectional switches can conduct at the same time, one in the upper bridges, and the other in the lower bridges. This leads to nine combinations of switching patterns.

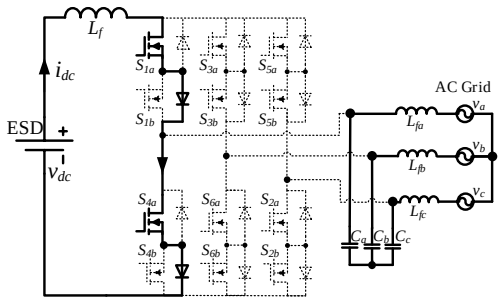
It can be readily determined that the DC current i_{dc} is the same as the current flowing through each switch. This indicates that the current i_{at}, i_{bt} and i_{ct} is either 0 or i_{dc}. Through a Clark transformation, the nine current vectors can be projected onto a phase plane.

As shown in Fig. 3(a), I_1 to I_6 are non-zero vectors, and I_7, I_8, I_9 are zero vectors. Therefore, the current vector space can be divided into six sectors separated by six non-zero vectors whose magnitudes are $2i_{dc}/\sqrt{3}$.

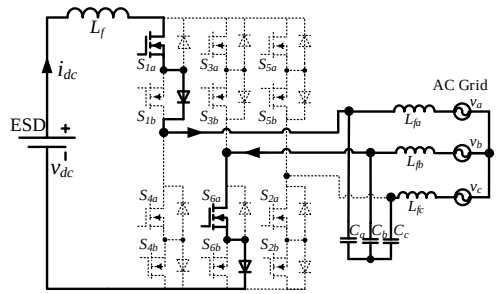
Fig. 3(b) shows the boundaries of the six sectors with respect to the three-phase reference current. In fact, the zero-crossing point of each phase current is right at the position where the sector changes. For a given reference vector in Fig. 3(a), two adjacent vectors can be chosen to compose it. Therefore, in one switching period, three switching modes are used. Two of them are adjacent vectors, and the third one is one of the three zero vectors that is used to occupy the remaining time. It should be

TABLE I
SELECTION OF CURRENT VECTORS IN EACH SECTOR

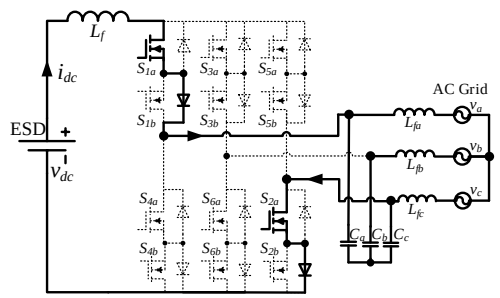
	I	II	III	IV	V	VI
Zero vector	I_7	I_9	I_8	I_7	I_9	I_8
Non-zero vector 1	I_6	I_1	I_2	I_3	I_4	I_5
Non-zero vector 2	I_1	I_2	I_3	I_4	I_5	I_6



(a) Mode 1.



(b) Mode 2.



(c) Mode 3.

Fig. 4. Operating modes in sector I.

noted that in a specific sector, two adjacent vectors have a common conducting switch. In order to reduce the switching times, the zero vector should be selected to have the same conducting switch. Hence, the selection of the vectors is fixed in each sector and can be shown in Table I.

According to the gate sequence for the converter, the operation can be classified into three modes in each sector. To simplify the analysis, only sector I is analyzed. The respective working modes are sketched in Fig. 4.

Mode 1: Zero vector I_7 is applied. S_{1a} and S_{4a} are turned on. The voltage of the DC inductor is equal to v_{dc}. In the discharging mode, the magnetic energy stored in the inductor increases with i_{dc}. During this period, no energy is transferred to the AC side. While in the charging mode, the other one of the same bidirectional switch (S_{xb}) is turned on. The DC current i_{dc} decreases in the opposite direction.

Mode 2: Non-zero current vector I_6 is used. S_{4b} is turned off, and S_{6b} is turned on. Regardless of the voltage of the filtering inductors, the voltage of the DC inductor is v_{dc}-v_{ab}. Since the DC voltage is lower than the AC voltage in the discharging mode, v_{dc}-v_{ab} is negative. Therefore, the DC current i_{dc} decreases and is injected to the AC gird.

Mode 3: Non-zero vector I_1 is used. S_{6b} is turned off, and S_{2b} is turned on. Similar to Mode 2, the voltage of the DC inductor is v_{dc}-v_{ac}. The DC current i_{dc} continues to decrease during this period.

The time duration calculation of each mode can be expressed as follows. Supposing the reference vector lies in sector I, the two adjacent vectors are I_6 and I_1. The time durations of the two non-zero vectors are T_1 and T_2, and T_0 is the time duration of the zero vector.

$$\begin{cases} I_1T_2\cos 30^\circ + I_6T_1\cos 30^\circ = T_s i_\alpha \\ I_1T_2\sin 30^\circ - I_6T_1\sin 30^\circ = T_s i_\beta \end{cases} \tag{1}$$

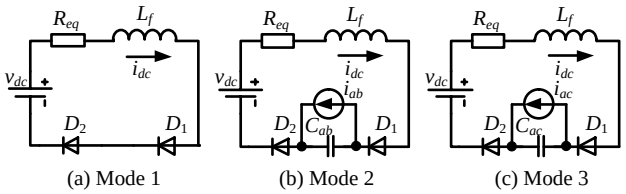
Where i_α and i_β are the projection of the reference vector into α, β axis. T_s is the switching period. Then the following can be obtained:

$$\begin{cases} T_1 = \dfrac{T_s}{2i_{dc}}\left(I_\alpha - \sqrt{3}i_\beta\right) \\ T_2 = \dfrac{T_s}{2i_{dc}}\left(I_\alpha + \sqrt{3}i_\beta\right) \\ T_0 = T_s - T_1 - T_2 \end{cases} \tag{2}$$

The time duration in other sectors can be calculated in the same way.

As mentioned previously, only one of the switches in the upper bridge and the other switch in the lower bridges should be on at any time. However, to avoid high-voltage spikes across the switches of the converter during the current commutation between two adjacent switching modes, the gate signals for the two consecutive switches should be overlapped. This implies that the consecutive mode switch has to be turned on before the current mode switch is turned off. For example, in sector I, when mode 1 switches to mode 2, the switch S_{6a} is turned on before S_{4a} is turned off by Δt. Although both of the switches are gated on during the overlapping time duration, the three-phase AC side line-to-line voltage v_{ab} cannot be short-circuited for the reverse blocking capability of the body diodes of the switches S_{6b} and S_{4b}. The current does not shift to S_{4a} until S_{6a} is completely turned off.

It should be noted that the voltage of the ESD cannot be too low or too high. In the discharging process, the simplified equivalent circuits in sector I are shown in Fig. 5, where R_{eq} is the sum of the inductor ESR, the MOSFET $R_{ds(on)}$ and the inner resistor of the ESD. The maximum voltage gain can be



(a) Mode 1 (b) Mode 2 (c) Mode 3

Fig. 5. Equivalent circuit of three operating modes in sector I.

obtained when the sector changes. At the beginning of sector I, the time duration of Mode 3 is quite short compared with Mode 1 and Mode 2. Therefore, Mode 3 is neglected. The voltage of the inductor is given by

$$\begin{cases} v_L = v_{dc} - i_{dc}R_{eq} - 2v_D & \text{Mode 1} \\ v_L = v_{dc} - i_{dc}R_{eq} - 2v_D - v_C & \text{Mode 2} \end{cases} \quad (3)$$

Where v_D is the diode voltage drop when it conducts, and v_C is the voltage of the filtering capacitor. The current of the capacitor is given by

$$\begin{cases} i_c = -i_o & \text{Mode 1} \\ i_c = i_{dc} - i_o & \text{Mode 2} \end{cases} \quad (4)$$

Where i_c is the current flowing into the filtering capacitor and i_o is the current flowing into the grid.

Assume that the time duration of Mode 1 is DT_s and that Mode 2 is (1-D)T_s. According to the volt-second balance and charge balance, v_c=(v_{dc}-$i_{dc}R_{eq}$-2v_d)/(1-D) and i_o=(1-D)i_{dc}. Therefore

$$v_c = \left(v_{dc} - i_o R_{eq} / (1-D) - 2v_d\right) / (1-D) \quad (5)$$

$$\text{or} \quad v_{dc} = (1-D)v_c + R_{eq} i_o / (1-D) + 2v_D \quad (6)$$

For example, the peak line to line voltage is 200V. The power flowing into the grid is 1kW. Therefore, the output current i_o is 5A. Assume that R_{eq} is equal to 1Ω, and that v_D is 1V. As a result, v_{dc}=200 (1-D)+5/(1-D)+2. The DC voltage v_{dc} and the current i_{dc} versus duty cycle D are shown in Fig. 6. As can be seen, the minimum DC voltage is 65V when D is 0.84. Therefore, the maximum gain is about 3. However, the gain increases if the output current and ESR of the circuit decrease.

On the other hand, the DC voltage must be lower than v_c at all times. Fig. 7 shows that in each sector the minimum voltage of the capacitor is half of the peak line to line voltage. Therefore, the ESD voltage must be satisfied as follows

$$(1-D)v_c + R_{eq} i_o / (1-D) + 2v_D < v_{dc} < v_{line,peak}/2 \quad (7)$$

While in the charging process, this system works as a buck type rectifier. The DC voltage can be as low as 0V, and the maximum DC voltage can approach the peak line to line voltage when it acts as an uncontrolled rectifier. However, in this situation, the three-phase AC current cannot be sinusoidal. If a unity power factor is required, the DC voltage cannot exceed the minimum voltage of the capacitors in each sector. This is similar to the discharging process. Therefore, during the charging process, the DC voltage can range from 0V to $V_{line,peak}$/2.

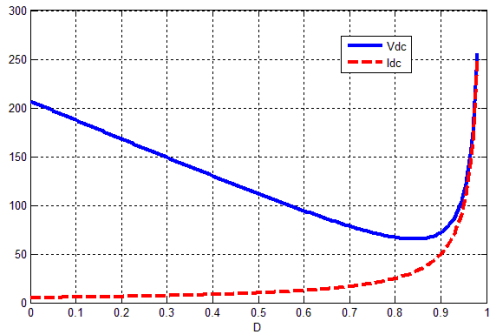


Fig. 6. DC voltage v_{dc} and current i_{dc} vs duty cycle D.

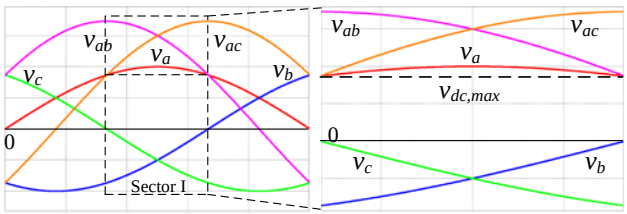


Fig. 7. Line to line voltage and phase voltage in sector I.

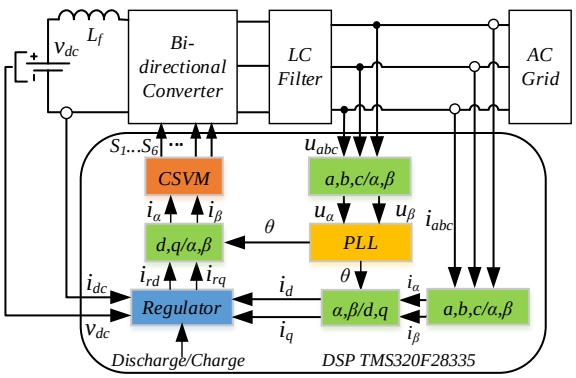


Fig. 8. General control strategy.

III. CONTROL STRATEGY

A. General Control Strategy

Fig. 8 shows the general control strategy for an ESS. The three-phase AC side voltage and current are sampled and transformed by the Clark and Park transformations. This leads to two phases being decoupled and time invariant outputs i_d in the d-axis and i_q in the q-axis. Both of them along with the charging/discharging function signal, i_{dc} and v_{dc} work as the inputs for the regulator whose specific design will be discussed later in Fig. 9 and Fig. 10.

Through the regulator, two independent outputs i_{rd} and i_{rq} can be obtained. These two values along with the value of θ achieved from phase lock loop (PLL) of the AC grid work as the inputs for the inverse Park transformation. Then the outputs $i_{r\alpha}$ and $i_{r\beta}$ can be obtained. These are the two components in the α/β stationary orthogonal reference frame. They are also the inputs of the current space vector modulation unit whose outputs are the gate signals S_1, S_2 … S_6 for the converter.

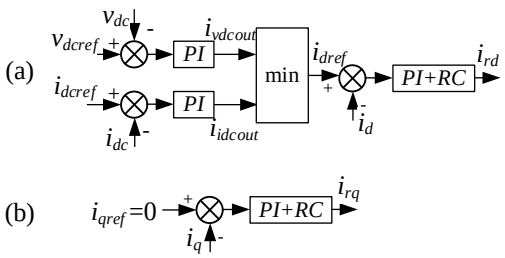


Fig. 9. Regulator design in the charging mode. (a) *d*-axis design. (b) *q*-axis design.

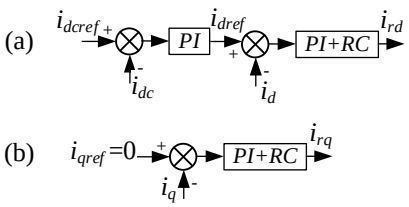


Fig. 10. Regulator design in the discharging mode. (a) *d*-axis design. (b) *q*-axis design.

The detailed regulator design can be explained as follows. Fig. 9 shows the design of the *d*-axis and *q*-axis in the charging mode. In this mode, the charging process needs to be switched from constant current (CC) to constant voltage (CV) to prevent overcharging. In the conventional charger design, the transfer moment is usually determined by the instantaneous value of the DC voltage v_{dc}. However, it is difficult to define a suitable set point for the voltage over the ESD since it varies with the charging currents due to the existence of a parasitical resistance. To achieve a smooth transfer from CC to CV, a transfer-logic is proposed and illustrated in Fig. 9(a). For the *d*-axis design, i_{dcref} is the current reference for the current compensator. Meanwhile, v_{dcref} works as the voltage reference for the voltage compensator. This is determined by the maximum charging voltage for the ESD. i_{dcout} and v_{dcout} are the outputs of the current compensator and the voltage compensator, respectively. At any instant, the actual outer loop regulator output for the *d*-axis is the minimum value between i_{dcout} and v_{dcout}. This can be explained as follows. At the initial state of the charging mode, the voltage v_{dc} is lower than the voltage reference v_{dcref}. Therefore, the voltage compensator becomes saturated and the charging process works in CC state. When the voltage of the ESD becomes larger than v_{dcref}, the voltage compensator comes out of saturation and v_{dcout} becomes lower. When v_{dcout} is lower than i_{dcout}, the charging current becomes lower than the current reference i_{dcref} and the current compensator become saturated. Then, the charging process works in the CV state and the transfer is very smooth.

The minimum value can be regard as the reference for the *d*-axis. Fig. 9(b) shows the regulator of the *q*-axis in the charging mode. Since a unity power factor from the AC side is required, the reference for the *q*-axis i_{qref} is set to zero.

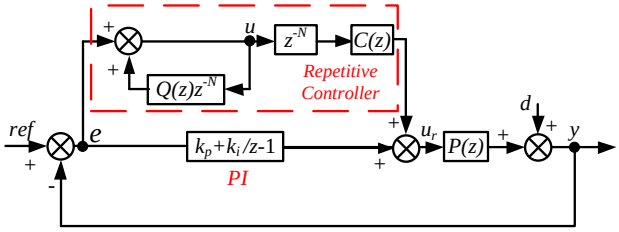


Fig. 11. Discrete block diagram of the control system.

In the discharging mode, the control strategy to achieve a fixed DC current is provided in Fig. 10. As shown in Fig. 10(a), the *d*-axis compensator is also composed of two loops. The outer loop is the DC side current tracking loop whose output works as the current reference for the *d*-axis component. To achieve a unit power factor, the current reference for the *q*-axis is also set to zero, as shown in Fig. 10(b). It should be noted that in the discharging mode, the regulator output is actually the magnitude of the reference vector projected to the *d*/*q* axis. The larger the magnitude becomes, the shorter the time duration of the zero vector becomes, which results in less energy being transferred to the AC side. Therefore, the output of the regulator should be inverted before the continued inverse Park transformation.

B. Regulator Design

In the synchronous reference frame (SRF), the sinusoidal variables are transformed into DC variables. Theoretically, PI controllers have a good dynamic response and can track DC signals with zero steady-state error. However, the steady state error does not become zero by using PI controller due to an unbalanced grid voltage and some nonlinear factors. Using a repetitive controller (RC) can deal with the issue of a periodic disturbances. It has a good steady-state performance but poor dynamic response. Therefore, both controllers are used together.

Fig. 11 shows the structure of the control system, where $P(z)$ is the model of the converter, and d represents a periodic disturbance. ref denotes i_{dref} or i_{qref}. u_r represents the controller output, and the currents in the *d*/*q* axis are the output y. In fact, the RC is only a complement to the PI controller. Therefore, the PI controller should be designed and verified before the RC is applied to the system. Due to the fact that many publications have discussed PI controller design methods for current source inverter and rectifier [13], [14], only the design of the RC is discussed here in detail.

Since the switching frequency is 10kHz and the line frequency is 50Hz, the value of N is chosen as 200. The loop in the RC can be written as $u(z)/e(z)=1/(1-Q(z)z^{-200})$ or $u(k)=Q(z)u(k\text{-}200)+ e(k)$. In practice, $Q(z)$ is generally a constant that is slightly less than 1, typically 0.95, otherwise the system tends to become unstable. Although there is a small steady state tracking error, it is acceptable.

$C(z)$ is a compensator and it can be equal to $P^{-1}(z)$ if the

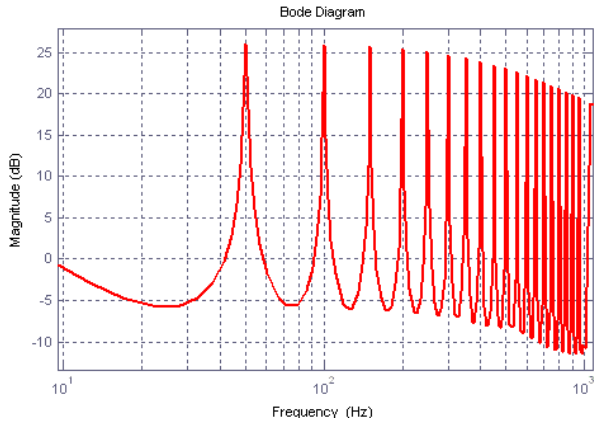


Fig. 12. Bode diagram of repetitive controller.

TABLE II
SIMULATION PARAMETERS

v_{dcinit}	95V	i_{dcref}	20A
v_{dcref}	100V	AC $v_{l\text{-}lrms}$	200V
$C_{a,b,c}$	30μF	Supercapacitor	0.3F
L_f	2mH	Inner Resistor	0.1Ω
$L_{fa,b,c}$	1mH	Switching Freq	10kHz
$R_{lfa,b,c}$	0.1Ω	Grid Freq	50Hz

modeling of the converter is acquired accurately. However, this is so difficult that $C(z)$ is usually given by $C(z)=K_r z^k S(z)$, where K_r is a constant, in order to adjust the gain. z^k is a phase-lead compensator and $S(z)$ is a low pass filter. In the experiment, the gain of the RC is set to be 10% of the PI controller. Since three-phase current mainly contains low order harmonics, $S(z)$ is chosen as a first order low pass filter whose cutoff frequency is 500Hz and phase-lag is 5.8 degree at 50Hz. Allow for one step delay of the digital controller and some other tiny factors, k=1+5.8/360*200=5. A Bode diagram of the repetitive controller is shown in Fig. 12. It can be determined that the errors at the integral times of the fundamental frequency of 50Hz can be mitigated dramatically.

IV. SIMULATION VERIFICATION

Simulations of the converter and the control strategy are carried out in PSIM. The specific parameters of the system are shown in Table II.

Fig. 13 shows simulation results of the three working states: charging from CC to CV and discharging consecutively. The initial voltage is set to 95V. At first, the system works in the charging mode with the constant charging current set as 20A. As can be sees, the three-phase current is in phase with the corresponding phase voltage indicating that a unity power factor is achieved. When the voltage of the supercapacitor increases to 100V, the voltage compensator of the outer loop comes out of saturation and becomes lower than the DC current compensator. Then it changes to the CV state when the DC current becomes lower and lower, and finally becomes

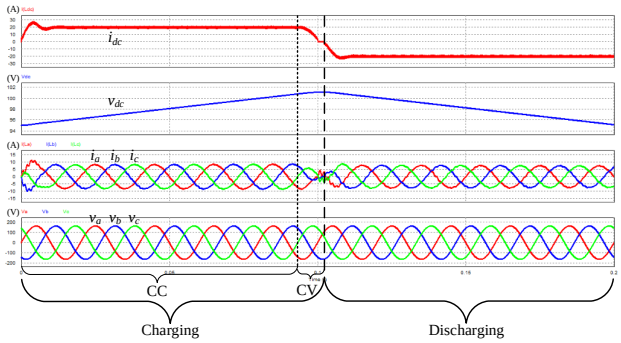


Fig. 13. Simulation results of three working states.

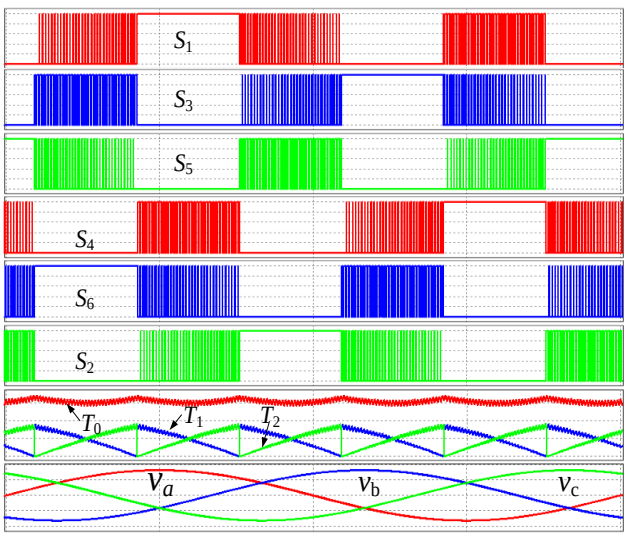


Fig. 14. Simulation results of gate signals and time duration.

zero. The DC voltage becomes stable and a little more than 100V. When a discharging signal occurs, it changes to the discharging mode, which is opposite to the charging mode in the CC state. The three-phase AC current is out of phase with each phase voltage.

The first six waveforms in Fig. 14 illustrates the gate signals for all of the working switches in a line cycle, in which six sectors can be readily figured out. The seventh waveform shows the time duration of the three current vectors, which are almost the same in each sector, although the current vectors are not.

V. EXPERIMENTAL VERIFICATION

A prototype rated at 1kW was built in the laboratory. The main parameters of the system are chosen as follows: L_f=2mH, L_{fa}=L_{fb}=L_{fc}=1mH, C_a=C_b=C_c=30μF. The twelve power MOSFETs of the converter are IXFH44N50P (500V/44A) whose on-resistance $R_{DS(on)}$ is 0.14Ω. A supercapacitor bank consisting of three modules connected in series is chosen as the ESD. Each module is composed of twelve supercapacitor cells connected in series and each cell is 120F/2.7V. With this setup, the total capacitance of the bank is 3.3F and its maximum

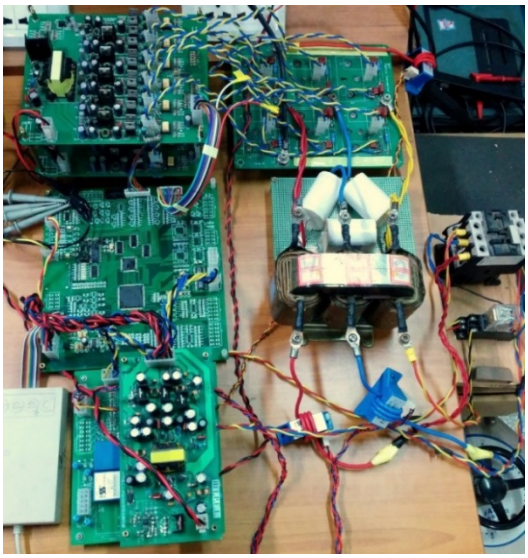


Fig. 15. Photo of the experimental prototype.

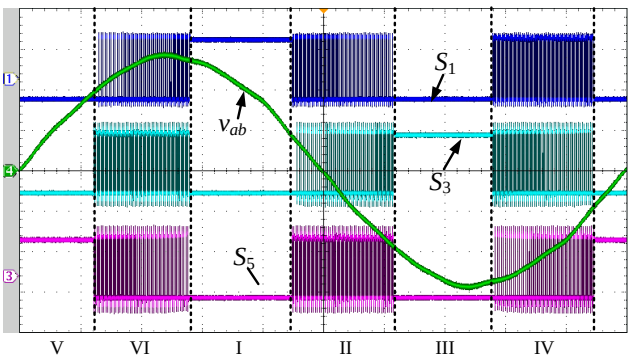


Fig. 16. Gate signals for a complete line cycle.

voltage rating is 97.2V. The rated RMS value of the line-to-line AC voltage is 150V with 50Hz. The digital control strategy was implemented on a DSP (TMS320F28335), with which 12 channel PWM signals are generated. To guarantee the sensing accuracy, an external 14-bit A/D AD7657 is used to measure the DC and three-phase AC current and voltage.

Fig. 15 shows a photo of the experimental prototype. The three circuit boards on the left from top to bottom are the driving circuit, the DSP control board and the auxiliary power supply. The elements on the right are the main circuit, three filtering capacitors and inductors. The supercapacitor and DC inductor are not shown in the photo.

Fig. 16 shows the actual gate signals for the switches in the upper bridge S_1, S_3 and S_5. These are the same as the simulation results. Taking S_1 as an example, due to the requirement of a unity power factor, the phase current i_a should be in phase with the phase voltage v_a or 30 degrees ahead of v_{ab}. Therefore, sector I starts 30 degrees after v_{ab} reaches its maximum. S_1 remains on, and S_3 and S_5 remain off during the whole sector.

On the other hand, the lower switches S_2, S_4 and S_6 are turned on and off alternately. This is shown in Fig. 17. The

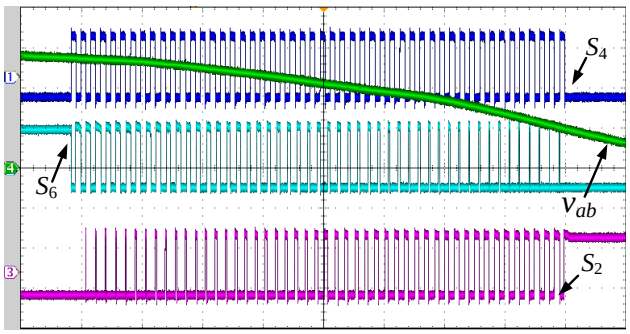


Fig. 17. Gate signals of S2, S4 and S6 in sector I.

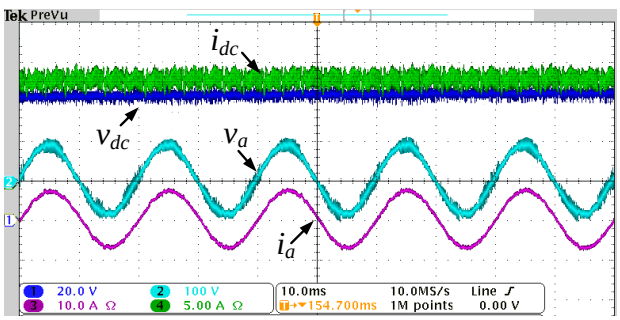


Fig. 18. Charging process.

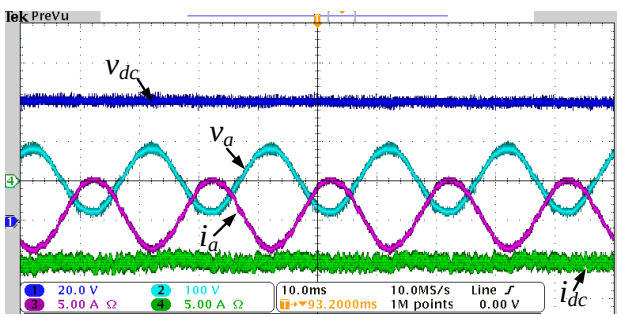


Fig. 19. Discharging process.

zero vector time duration T_0 is actually the modulation ratio of S_4, while the non-zero vector time durations T_1 and T_2 are the modulation ratios of S_6 and S_2, respectively. As can be sees, T_1 decreases gradually from being constantly on in sector III to being constantly off in sector V, and T_2 is on the opposite of this, which also correspond simulation results.

Fig. 18 and 19 show the charging and discharging process respectively with a constant DC current set as 13A. The phase current i_a is almost sinusoidal and has little distortion.

Fig. 20 shows the transition from the charging mode to the discharging mode with an almost constant DC side current. Before the transition, the phase current i_a is almost sinusoidal and in phase with its phase voltage v_a, indicating a high power factor for the AC side. After the transition, i_a is out of phase with v_a, which also leads to a high power factor. The transition is smooth and fast. Fig. 21 shows the transition from the discharging mode to the charging mode. The sharp increase and decrease of the DC voltage v_{dc} at the transition moment result from the inner resistance of the supercapacitor, which is

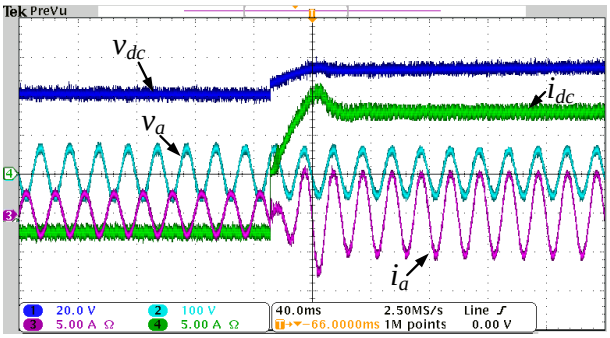


Fig. 20. Transition from discharging mode to charging mode.

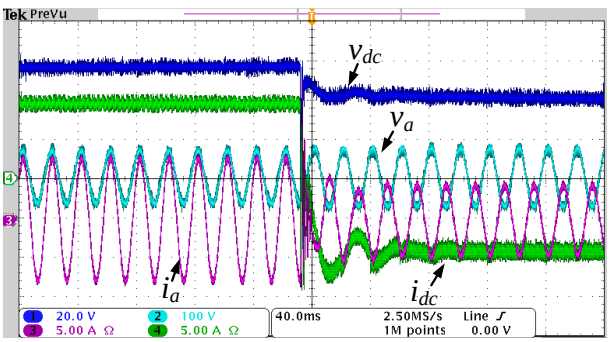


Fig. 21. Transition from charging mode to discharging mode.

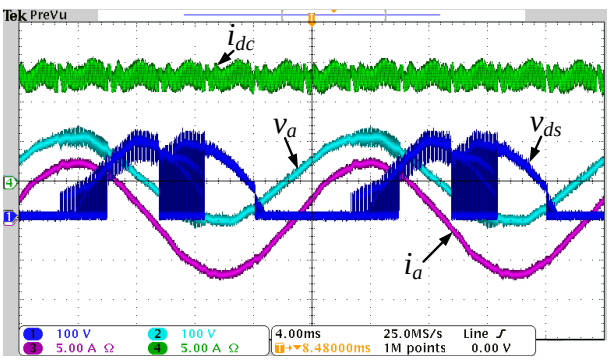


Fig. 22. Drain-to-source voltage of MOSFET working as switch.

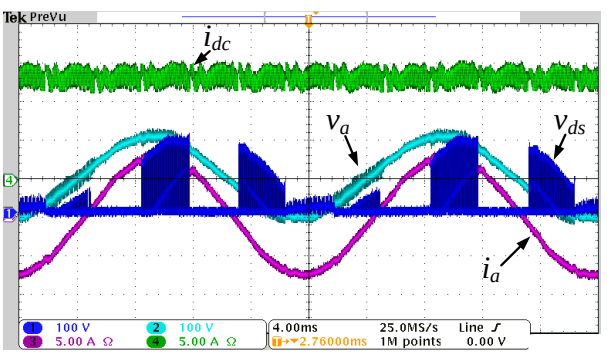


Fig. 23. Drain-to-source voltage of MOSFET working as diode.

determined to be nearly 1Ω.

Fig. 22 and 23 show the drain-to-source voltage of the two MOSFETs in a bidirectional switch when the converter operates in the charging mode. In Fig. 22, the MOSFET works as a switch which turns on and off according to the gate signal. In Fig. 23, the MOSFET only works as a diode. All of the other bidirectional switches share the same waveforms except for a phase delay. During the discharging mode, the situations of the two kinds of switches only interchange with each other. The maximum voltage is the peak value of the line-to-line voltage regardless of the voltage spike. As can be seen, the voltage spike can be suppressed significantly by adding an 1μs overlapping time for the switches when they commutate.

Due to the desire to achieve a constant DC current, the power of the DC side and the AC side is always changing. Therefore, it is difficult to obtain the instantaneous power of both sides simultaneously. In order to get the efficiency, an oscilloscope is used to measure the power. The efficiency at the maximum charging power, rated at 1kW, is 95.7%. In addition, a unity power factor is achieved according to the power quality analyzer.

VI. CONCLUSIONS

In this paper, a unified control strategy using the CSVM technique for a single stage bidirectional three-phase grid connected DC/AC converter is proposed. In the charging mode, the converter works as a buck type AC/DC rectifier. While in the discharging mode, it operates as a boost type DC/AC inverter. The operating principle, mode analysis, gate signals generation, control strategy and transfer logic from CC to CV in the charging mode are also given.

When compared with the conventional two-stage topology typically composed of a Buck/Boost DC-DC converter cascaded with a VSI, the proposed topology requires twelve power switches rather than eight and has more power loss due to the conduction of the diodes. However, it still has many advantages over the conventional topology. First, the conventional two-stage units need two separate control systems, making them a bit more complicated. Second, the voltage rating of all of the eight switches in the conventional topology are equal to the high voltage DC bus regardless of the voltage spike. Meanwhile, in the proposed topology, it is only the peak line to line voltage of the AC grid, which is much lower. Third, bulky electrolytic capacitors are necessary to stabilize the high voltage DC bus when the transient power between the two stages is not matched. This results in lower reliability and efficiency. In addition, the boost ratio of the first stage must be higher so that the high voltage DC bus can be inverted by the VSI. Furthermore, the AC side filtering inductance of the proposed topology can be smaller because of the existence of the DC inductor. Therefore, this topology is a good alternative to the conventional two-stage topology.

In addition to these advantages over the conventional topology, it also has many benefits including high conversion efficiency, a high power factor and tight control of the DC current. Furthermore, a fast transition can be achieved from the charging mode to the discharging mode and vice versa. A 1kW

ESS prototype using supercapacitors is fabricated and evaluated. The simulation and experimental results validate the advantages and effectiveness of the proposed control strategy.

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+REFERENCES

[1] Sang-Hyup Han, Heung-Geun Kim, Honnyong Cha, Tae-Won Chun, and Eui-Cheol Nho, "Bi-directional multi-level converter for an energy storage system," *Journal of Power Electronics*, Vol. 14, No. 3, pp. 499-506, May 2014.

[2] D.-H. Jang and S.-K. Han, "Low cost high power density photovoltaic power conditioning system with an energy storage system," *Journal of Power Electronics*, Vol. 12, No. 3, pp. 487-494, May 2010

[3] B.-Y. Chen and Y.-S. Lai, "New digital-controlled technique for battery charger with constant current and voltage control without current feedback," *IEEE Trans. Ind. Electron*., Vol. 59, No. 3, pp. 1545,1553, Mar. 2012.

[4] P. A. Cassani and S. S. Williamson, "Design, testing, and validation of a simplified control scheme for a novel plug-in hybrid electric vehicle battery cell equalizer," *IEEE Trans. Ind. Electron*., Vol. 57, No. 12, pp. 3956-3962, Dec. 2010.

[5] Y.-S. Lee and D. Jiun-Yi, "Fuzzy-controlled individual-cell equaliser using discontinuous inductor current-mode Cuk convertor for lithium-ion chemistries," *IEE Proceedings Electric Power Applications*, Vol. 152, No. 5, pp. 1271-1282, Sep. 2005.

[6] C. Y. Inaba, E. Hiraki, and M. Nakaoka, "Three phase voltage source soft switching inverter with high frequency pulse current transformers," *Journal of Power Electronics*, Vol. 2, No. 4, pp. 288-296, Oct. 2002.

[7] X. H. Wu, S. K. Panda, and J. X. Xu, "Design of a plug-in repetitive control scheme for eliminating supply-side current harmonics of three-phase PWM boost rectifiers under generalized supply voltage conditions," *IEEE Trans. Power Electron*., Vol. 25, No. 7, pp. 1800-1810, Jul. 2010.

[8] B.-D. Min, J.-P. Lee, J.-H. Kim, T.-J. Kim, D.-W. Yoo, K.-R. Ryu, J.-J. Kim, and E.-H. Song, "A novel grid-connected PV PCS with new high efficiency converter," *Journal of Power Electronics*, Vol. 8, No. 4, pp. 309-316. Oct. 2008.

[9] Y. Zhang; J. Liu, and C. Zhang, "Comparison of traditional two-stage buck-boost voltage source inverter and diode-assisted buck-boost voltage source inverter," *Applied Power Electronics Conference and Exposition (APEC), 2012 Twenty-Seventh Annual IEEE*, pp.141,148, 2012.

[10] D. Sha and Z. Qin, "A digitally controlled three-phase cycloconverter type high frequency ac link inverter using space vector modulation," *Journal of Power Electronics*, Vol. 11, No. 1, pp. 28-36, Jan. 2011.

[11] D. Sha, G. Xu, and X. Liao, "Control strategy for input-series-output-series high-frequency AC-link inverters," *IEEE Trans. Power Electron*., Vol. 28, No. 11, pp. 5283-5292, Nov. 2013.

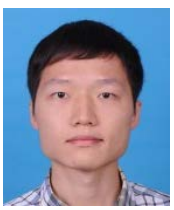
[12] S. M. Dehghan, M. Mohamadian, and A. Yazdian "Current-type nine-switch inverters," *Journal of Power Electronics*, Vol. 10, No. 2, pp. 146-154, Mar. 2010.

[13] B. Mirafzal, M. Saghaleini, and A. K. Kaviani, "An SVPWM-Based switching pattern for stand-alone and grid-connected three-phase single-stage boost inverters," IEEE Trans. Power Electron., Vol. 26, No. 4, pp. 1102-1111, Apr. 2011.

[14] Z. Qin, D. Sha, and X. Liao, "A three-phase boost-type grid-connected inverter based on synchronous reference frame control," *Applied Power Electronics Conference and Exposition (APEC), 2012 Twenty- Seventh Annual IEEE*, pp. 384,388, 2012.

[15] B. Sahan, A. N. Vergara, N. Henze, A. Engler, and P. Zacharias, "A single-stage PV module integrated converter based on a low-power current-source inverter," *IEEE Trans. Ind. Electron*., Vol. 55, No. 7, pp. 2602-2609, Jul. 2008.

[16] Y. Chen and K. Smedley, "Three-phase boost-type grid-connected inverter," IEEE Trans. Power Electron., Vol. 23, No. 5, pp. 2301-2309, Sep. 2008.



Jianliang Chen was born in 1990. He received his B.S. degree from the Beijing Institute of Technology (BIT), Beijing, China, in 2013. He is currently working toward his Ph.D. degree in the School of Automation, BIT. His current research interests include power electronics converters, renewable energy power conversion and micro-grid applications.

Xiaozhong Liao was born in China, in 1962. She received her B.S. and M.S. degrees in Electrical Engineering from Tianjin University, Tianjin, China, in 1982 and 1984, respectively, and her Ph.D. degree in Control Sciences and Engineering from the Beijing Institute of Technology (BIT), Beijing China, in 2004. She was a Visitor Researcher in the Department of Electrical and Electronic Engineering, University of Central Lancashire, Preston, U.K., form 1995 to 1996. She is presently an Associate Dean and Full Professor in the School of Automation, Beijing Institute of Technology. Her current research interests include power electronics, motor drives and renewable energy power conversion.

Deshang Sha was born in 1977. He received his B.S. degree from the Luoyang Institute of Technology, Luoyang, China, in 1998, his M.S. degree from the Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2001, and his Ph.D. degree from the Institute of Electrical Engineering, Chinese Academy of Sciences, Beijing, China, in 2005, all in Electrical Engineering. From 2005 to 2007, he worked as the Head and Chief Engineer of the Fully-digitalized Welding Machine Research Department of Time Group Inc., Beijing, China. Since 2008, he has been with the School of Automation, Beijing Institute of Technology (BIT), Beijing, China, where he is presently an Associate Professor. From 2012 to 2013, he was a Visiting Scholar with the Future Energy Electronics Center (FEEC), Virginia Polytechnic Institute and State University, Blacksburg, VA, USA. His current research interests include the modeling and control of power converters, high-efficiency power conversion, power electronics applications in renewable energy power generation systems and micro-grid systems. Dr. Sha received an Excellent Yong Scholar Award from BIT, in 2010.