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Elimination of the State-of-Charge Errors for Distributed Battery Energy Storage Devices in Islanded Droop-controlled Microgrids

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Abstract

Battery energy storage devices (ESDs) have become more and more commonplace to maintain the stability of islanded power systems. Considering the limitation in inverter capacity and the requirement of flexibility in the ESD, the droop control was implemented in paralleled ESDs for higher capacity and autonomous operation. Under the conventional droop control, state-of-charge (SoC) errors between paralleled ESDs is inevitable in the discharging operation. Thus, some ESDs cease operation earlier than expected. This paper proposes an adaptive accelerating parameter to improve the performance of the SoC error eliminating droop controller under the constraints of a microgrid. The SoC of a battery ESD is employed in the active power droop coefficient, which could eliminate the SoC error during the discharging process. In addition, to expedite the process of SoC error elimination, an adaptive accelerating parameter is dedicated to weaken the adverse effect of the constraints due to the requirement of the system running. Moreover, the stability and feasibility of the proposed control strategy are confirmed by small-signal analysis. The effectiveness of the control scheme is validated by simulation and experiment results.

Key words: Adaptive accelerating parameter, Droop control, Energy storage device, Small-signal analysis, SoC error elimination

I. INTRODUCTION

In recent years, environmental concerns and the ongoing depletion of fossil fuel reserves have spurred significant interest in renewable energy sources (RESs). Since RESs have different characteristics than the conventional power generators fired by fossil fuel, novel control techniques and topologies have developed quickly [1]-[6]. By harvesting energy from nearby RESs, an islanded microgrid can be established as an effective solution to cope with power supply problems, especially in remote areas or islands.

The inherent intermittency of RESs such as photovoltaic or wind power produces a fluctuating power, which will greatly reduce the stability of islanded microgrids. Therefore, ESDs are usually installed in the vicinity of RESs to deal with the power quality issue of islanded microgrids. As one of the major static energy storage components with a higher energy density, a battery is utilized to compensate the fluctuation introduced by RESs, especially in long time span, large-scale capacity and high RES penetration [3]-[5]. Lots of efforts have been carried out on the integration and coordination of RESs and battery ESDs [6]-[8]. Furthermore, distributed parallel ESDs have been implemented to deal with the demand for increased capacity in islanded microgrids [9]-[12]. When compared with centralized ESDs, distributed ESDs provide an easier way to replace or retrofit batteries with small capacity ESD modules.

As a mature control strategy, droop control has been utilized to operate distributed ESDs, thus constituting truly distributed and redundant systems [13], [14]. Many control methods have been proposed to improve the performance of droop control in the transient and steady-state [15], [16]. To achieve accurate power sharing, the affection of the line impendence parameter was discussed separately in terms of capacitive [17], inductive [18] and resistive [19].

It is well known that the SoCs of paralleled battery ESDs are affected by a number of factors, such as the characteristic of the ESD, parameters of the controller, and uncertain disturbances. If a targeted scheme is not utilized, a SoC error between paralleled battery ESDs is inevitable in the

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discharging process. The SoC error will result in over-discharging in a battery ESD with a low SoC among paralleled ESDs. Furthermore, in the scenario of a long-time RES interval, some ESDs will cease operation earlier than expectation due to a too-low SoC value. This reduces the capacity of paralleled ESDs. Meanwhile, due to the sudden running out of energy in a ESD, an extremely rapid change in the power flow will be caused which impairs the power quality and stability of the power system. Therefore, an extra SoC error elimination scheme, based on a conventional controller, is needed to extend the running time of paralleled ESDs.

Several scholars have worked on the above issue and some efforts have been carried out on power management in microgrids to eliminate the SoC error in paralleled battery ESDs [20]-[23]. However, it is worth noting that the former schemes were designed based on the communication function, including wire communication or low bandwidth wireless communication (e.g. EMS). The case with communication is usually viewed as less reliable since any communication malfunction failure will likely lead to instability. In addition, wire communication is hard to carry out when the ESDs are located in a large area. Meanwhile, low bandwidth wireless communication is unable to control ESDs in real-time. Furthermore, as the number of ESDs increases, there is a challenge to get all of the ESDs to cooperate by low bandwidth communication.

To overcome the adverse effects from communication malfunctions, droop control based solely on the locally measured information of the inverter is preferred. Although ESDs with a droop controller have been widely utilized in microgrids, literatures focusing on SoC balancing to improve performance are rare.

In [24], a novel droop controller was proposed to balance the SoC in the discharging process of a battery ESD. However, it is worth noting that a significant value of the voltage deviation is created when ESDs are running under low SoC conditions. Although voltage deviations reduce the performance and stability of islanded microgrids, the author did not discuss above issue in greater detail. Further, to avoid the negative impact from constraints, the operation conditions of islanded microgrids are planned in detail. Thus, the SoC-balancing strategy works under ideal conditions. It is well know that the operation conditions of microgrids exist in uncertainty and randomness. The analysis of the adverse effects from constraints is ignored, which limits its application in practice.

In [25], a virtual output impedance control strategy based on fuzzy control was proposed to achieve SoC balancing among paralleled ESDs. In order to restrain voltage deviation, the variation range of the virtual output impedance is calculated based on the equivalent impedance of the microgrid. However, the 'plug and play' feature of RESs is one of the most significant merits of a microgrid. Any new connection or disconnection of a RES will change the equivalent model of the microgrid and hence degrades the proposed scheme in [25] in terms of reaching its designed performance.

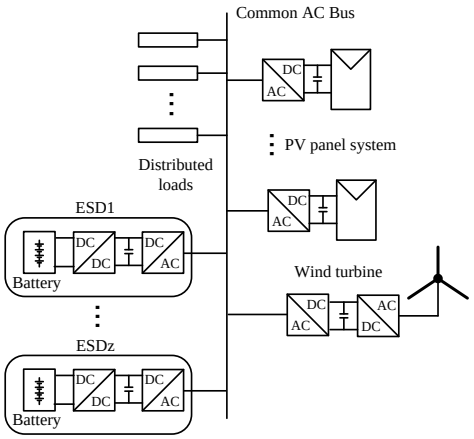

Fig.1. Diagram of an islanded microgrid.

To deal with the aforementioned issues, in this paper, an adaptive accelerating parameter SoC error eliminating droop controller is proposed to balance the SoC of paralleled battery ESDs in the discharging process. A logarithm function, comprising the SoC, is employed in the active power droop coefficient to adjust the power sharing between paralleled battery ESDs. In addition, an exponent item, working as an accelerating parameter, is utilized to expedite the process of SoC error elimination. In addition, an offset item is utilized to prevent over-discharging by limiting the running range of the battery ESD. Further, to realize autonomous operation in islanded microgrids and "plug and play" in ESDs, variations in the range of the active power droop coefficient and the max output power of the inverter are integrated in the analysis to reveal the adverse effects from constraints. Therefore, an adaptive accelerating parameter, which is generated by the locally measured information of the ESD, is derived to improve the performance of SoC error elimination under constraints.

II. Principle of the SoC Error Eliminating Droop Controller

Fig. 1 shows a general scheme of an islanded droop controlled microgrid which consists of inherent intermittency RESs, ESDs, distributed loads, and electric power interfaces to transfer energy to the common ac bus. When sufficient power is harvested from the RESs, the ESDs charge the battery with the dual-loop control strategy until fully charged. While the RESs suffer due to intrinsic intermittency, the battery ESDs should be able to cover the total power demanded from loads. Under this scenario, an uninterrupted power should be supplied from the ESDs to maintain the stability of an islanded power system, by adjusting its output-voltage references as a function of the dispatched power.

In order to extend the running time of paralleled ESDs, the paralleled ESDs should deplete energy simultaneously.

Therefore, to effectively eliminate the SoC error between the paralleled battery ESDs, the output power of the ESDs need to be adjusted according to their SoCs. *LCL* filters are placed in the inverters to suppress the harmonic component. Therefore, the reactance is greater than the resistance in the output line impedance. Based on a conventional droop controller [13]-[19], the SoC error eliminating droop controller is designed as:

$$\begin{cases} \omega_{iref} = \omega^* - m_{Pi} p_i \\ V_{iref} = V^* - m_Q q_i \end{cases} \tag{1}$$

$$m_{Pi}=m_{P0} / \{n_i \times [-\ln(SoD_i)]^{n_i}\} \tag{2}$$

$$SoD_i = 1 - SoC_i \tag{3}$$

where ω^* and V^* are the nominal frequency and voltage set points; p and q are the active and reactive powers passed through a low pass filter (LPF); m_{Pi} and m_Q are the active and reactive power droop coefficients; m_{P0} is the common active power droop coefficient; *SoD* is the state-of-discharge in the battery; and n is the accelerating parameter, $n>1$.

According to the principle of the droop control strategy [13]-[19], the expression of the frequency deviation can be written as:

$$\omega^* - \omega_{1ref} \approx \omega^* - \omega_{2ref} \approx \cdots \approx \omega^* - \omega_{iref} \tag{4}$$

Using (1)-(4), the relationship between the output active power and the active power coefficient yields:

$$m_{P1} p_1 \approx m_{P2} p_2 \approx \cdots \approx m_{Pi} p_i \tag{5}$$

The SoC error between any two paralleled ESDs can be expressed as:

$$e_{SoC} = SoC_{upper} - SoC_{lower} \qquad (SoC_{upper} > SoC_{lower}) \tag{6}$$

where e_{SoC} is the SoC error between the paralleled battery ESDs; SoC_{upper} and SoC_{lower} are the SoC values of ESDs with more SoC and less SoC, respectively.

Based on (5) and (6), the ratio of the output active power between paralleled ESDs can be approximately derived as:

$$\begin{aligned} \frac{P_{upper}}{P_{lower}} &= \frac{m_{Plower}}{m_{Pupper}} = \frac{n_i \times [-\ln(SoD_{upper})]^{n_i}}{n_i \times [-\ln(SoD_{lower})]^{n_i}} \\ &= [\log_{1-SoC_{lower}} (1 - SoC_{lower} - e_{SoC})]^{n_i} > 1 \end{aligned} \tag{7}$$

where P_{upper} and P_{lower} are the output active powers for ESDs with SoC_{upper} and SoC_{lower}, respectively.

It can be seen from equation (7) that more active power is extracted from the ESD with SoC_{upper}, until e_{SoC} is reduced to zero during the discharging process. Furthermore, it is clear that the ratio of output active power between paralleled ESDs is increased by enlarging the accelerating parameter n_i. Thus, expediting the speed on the SoC error elimination.

To demonstrate the effectiveness of the proposed droop controller, the process of e_{SoC} elimination is analyzed under the minimum value of the accelerating parameter which is n_i=1. Furthermore, since the initial states of the paralleled battery ESDs are uncertain, the process of e_{SoC} elimination can be divided into two stages: 1)$e_{SoC} \geqslant SoC_{lower}$; 2)$e_{SoC} < SoC_{lower}$.

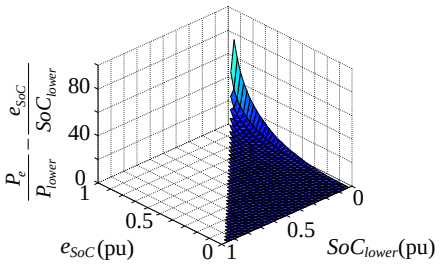

Fig. 2. 3D picture of the numerical solutions of equation (14).

1) $e_{SoC} \geqslant SoC_{lower}$: In the discharging process, the voltage of the battery can be approximately seen as a constant value. Hence, the time domain expression of e_{SoC} and SoC_{lower} are:

$$\begin{cases} e_{SoC}(t) = e_{SoC\_ini} - \int \frac{P_e(t)}{Bat} dt \\ SoC_{lower}(t) = SoC_{lower\_ini} - \int \frac{P_{lower}(t)}{Bat} dt \end{cases} \tag{8}$$

where e_{SoC_ini} and SoC_{lower_ini} are the initial values of e_{SoC} and SoC_{lower} at t=0, and *Bat* is the capacity of the battery ESD.

Assume that the relationship between P_{e_assum} and P_{lower_assum} is expressed as:

$$\frac{P_{e\_assum}(t)}{P_{lower\_assum}(t)} = \frac{e_{SoC}(t) P_k(t)}{SoC_{lower}(t) P_k(t)} \tag{9}$$

where P_{lower_assum} is the hypothetical value of the output active power of the ESD with SoC_{lower}; P_{e_assum} is the hypothetical difference value of the output active power between two paralleled ESDs; and P_k is the time-varying factor.

By substituting (9) into (8), equation (8) can be rewritten as:

$$\begin{cases} \frac{e_{SoC}(t)}{e_{SoC\_ini}} = 1 - \int \frac{e_{SoC}(t) \times P_k(t)}{e_{SoC\_ini} \times Bat} dt & \text{(a)} \\ \frac{SoC_{lower}(t)}{SoC_{lower\_ini}} = 1 - \int \frac{SoC_{lower}(t) \times P_k(t)}{SoC_{lower\_ini} \times Bat} dt & \text{(b)} \end{cases} \tag{10}$$

By subtracting (10.b) from (10.a), a differential equation is derived as:

$$\dot{x}(t) = -x(t) y(t) \tag{11}$$

where $x(t) = \frac{e_{SoC}(t)}{e_{SoC\_ini}} - \frac{SoC_{lower}(t)}{SoC_{lower\_ini}}$; $y(t) = \frac{P_k(t)}{Bat}$.

The solution of (11) is:

$$x(t) = x|_{t=0} \, e^{-y(t)t} \tag{12}$$

where $x|_{t=0} = \frac{e_{SoC}|_{t=0}}{e_{SoC\_ini}} - \frac{SoC_{lower}|_{t=0}}{SoC_{lower\_ini}} = 0$.

Equation (12) reveals that e_{SoC} and SoC_{lower} will be reduced to zero at the same time in the discharging process by using (9). Therefore, equation (9) can be seen as a boundary condition for making e_{SoC} reach zero before SoC_{lower}.

As a comparison, the time domain ratio of P_e to P_{lower} can be derived from (7), and this yields :

$$\frac{P_e(t)}{P_{lower}(t)} = \log_{1-SoC_{lower}(t)} \left(1 - \frac{e_{SoC}(t)}{1 - SoC_{lower}(t)}\right) \tag{13}$$

where P_e is the difference value of the output active power

between two paralleled ESDs.

By subtracting (9) from (13), the difference value can be expressed as:

$$\frac{P_e(t)}{P_{lower}(t)}-\frac{P_{e\_assum}(t)}{P_{lower\_assum}(t)} = \log_{1-SoC_{lower}(t)}\left[\frac{1-\frac{e_{SoC}(t)}{1-SoC_{lower}(t)}}{(1-SoC_{lower}(t))^{\frac{e_{SoC}(t)}{SoC_{lower}(t)}}}\right] \quad (14)$$

Fig.2 demonstrates the numerical solutions of equation (14). The 3D picture shows that all of the numerical solutions are positive. Therefore, it can be concluded the SoC error eliminating droop controller can force e_{SoC} to be equal with SoC_{lower} before SoC_{lower} is reduced to zero in the stage of $e_{SoC} \geqslant SoC_{lower}$.

2) $e_{SoC}<SoC_{lower}$: Equation (13) shows that $P_e>P_{lower}$ is satisfied when $e_{SoC}=SoC_{lower}$. Therefore, e_{SoC} will ultimately move into the range of $e_{SoC}<SoC_{lower}$.

In the stage of $e_{SoC}<SoC_{lower}$, the derivatives of e_{SoC} and SoC_{lower} are:

$$\begin{cases}\dot{e}_{SoC}(t)=P_e(t)/[e_{SoC}(t)\times Bat]\\ \dot{SoC}_{lower}(t)=P_{lower}(t)/[SoC_{lower}(t)\times Bat]\end{cases} \quad (15)$$

where $\dot{e}_{SoC}$ and $\dot{SoC}_{lower}$ are the derivatives of e_{SoC} and SoC_{lower}, respectively.

Using (13) and (15), the relationship between $\dot{e}_{SoC}(t)$ and $\dot{SoC}_{lower}(t)$ is derived as:

$$\frac{\dot{e}_{SoC}(t)}{\dot{SoC}_{lower}(t)}=\frac{P_e(t)/e_{SoC}(t)}{P_{lower}(t)/SoC_{lower}(t)} = \frac{SoC_{lower}(t)}{e_{SoC}(t)}[\log_{1-SoC_{lower}(t)}(1-SoC_{lower}(t)-e_{SoC}(t))-1] \quad (16)$$

The numerical solutions of equation (16) at all of the operation points of two paralleled battery ESDs are depicted in Fig.3. According to Fig.3, it can be seen that all of the numerical solutions are larger than 1. Therefore, the integration values of (16) can be written as:

$$\int \dot{e}_{SoC}(t)dt > \int \dot{SoC}_{lower}(t)dt \quad (17)$$

According to (17), it is clear that, over the same period, more e_{SoC} can be eliminated than SoC_{lower}, which is consumed. Therefore, in the stage of $e_{SoC}<SoC_{lower}$, the SoC error can be reduced to zero earlier than SoC_{lower}.

Using (14) and (17), it can be concluded that e_{SoC} can be eliminated before either of the ESDs ceases operation, which extends the running time of paralleled ESDs.

Fig.4 is depicted to demonstrate the discharging process of the paralleled battery ESDs. The operation conditions of the paralleled battery ESDs are SoC_{upper}=0.9, SoC_{lower}=0.7 and e_{SoC}=0.2, as n_i=1,3,6.

It can be seen from the curves in Fig.4 that e_{SoC} is eliminated earlier as n_i increases. Moreover, e_{SoC} plunges remarkably with an obvious exponential appearance. It declines steeply at the beginning, then becomes steadier and finally reaches zero

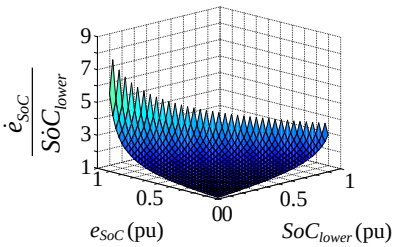

Fig. 3. 3D picture of the numerical solutions of equation (16).

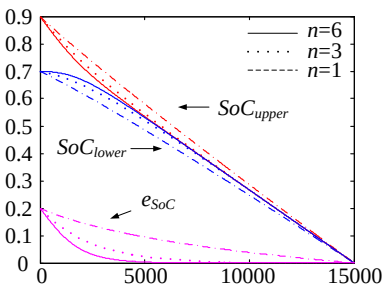

Fig. 4. Discharging process of droop-controlled paralleled ESDs as n=1, 3, 6.

smoothly. Therefore, the accelerating parameter n_i has a noticeable effect on expediting the speed of e_{SoC}.

In summary, an individual ESD can automatically generate the active power droop coefficient according to its remaining energy, and the power sharing between paralleled ESDs is adjusted to achieve e_{SoC} elimination by the SoC error eliminating droop controller, while preserving the basic function of the conventional droop controller. Moreover, as the accelerating parameter increases, the difference value of the output active power between paralleled ESDs is enlarged. Thus, e_{SoC} can be eliminated more efficiently.

III. Proposed Adaptive Accelerating Parameter

A. The Constraints of the System

As mentioned in Section Ⅱ, the proposed droop controller can effectively eliminate e_{SoC} under ideal conditions. However, the running process of an islanded microgrid exists in uncertainty and randomness. Thus, the constraints on the droop controlled inverters are indispensable to ensure the stability of the system.

Firstly, based on the analyses in Section Ⅱ, when e_{SoC} is eliminated, there is the possibility of a SoC_{lower} that is close to zero, which results in over-discharging in the battery ESD. This results in a detrimental effect on battery lifetime.

To prevent over-discharging in a battery, an extra offset item is employed in the active power droop coefficient. Thus, equation (2) is updated as:

$$m_{Pi}=m_{P0}/\{n_i\times[-\ln(SoD_i+C)]^{n_i}\} \quad (18)$$

where C is the value of the offset item.

Comparing (2) and (18), the characteristics of the droop

controller are moved along the *SoD* axis. This ensures that e_{SoC} is eliminated before $SoC_{lower}=C$. Furthermore, according to the characteristic of the logarithmic function, a negative value is calculated as $SoC_i<C$, which disables the droop controller. Therefore, C=0.1 is chosen in this paper to protect the battery.

Secondly, as one of the crucial issues in islanded microgrids, the variation range of the frequency deviation should be restrained. With the active power droop coefficient in (18), the value of the frequency deviation is derived as:

$$\omega^* - \omega = \frac{m_{P0}}{\sum_{j=1}^{z} n_j \times [-\ln(SoD_j + C)]^{n_j}} P_{load} \tag{19}$$

where ω is the frequency of the islanded microgrid, and P_{load} is the active power of the load in the islanded microgrid.

According to (18) and (19), when the *SoD*s of paralleled battery ESDs are close to 1-*C*, the value of the active power droop coefficient will be relatively large and a remarkable frequency deviation is caused. As a result, the frequency of the islanded microgrid will exceed the standard. Furthermore, in [15], according to the root locus of the small-signal model of the droop control, the poles will both move away from an imaginary axis and towards the right half plane with a large active power droop coefficient. This will degrade the stability of the system. Therefore, the variation range of the active power droop coefficient in (18) should be restrained, and the expression is written as:

$$m_{pi} = \begin{cases} m_{p0} / m & (n_i \times [-\ln(SoD_i + C)]^{n_i} \le m) \\ \dfrac{m_{p0}}{n_i \times [-\ln(SoD_i + C)]^{n_i}} & (n_i \times [-\ln(SoD_i + C)]^{n_i} > m) \end{cases} \tag{20}$$

where m is the threshold value of $n_i \times [-\ln(SoD+C)]^{ni}$.

It is clear that when the constraint in (20) is involved in the active power droop coefficient, the active power sharing among paralleled ESDs is restrained. If a large value is set for m, most of the operation points of the ESD will trigger the constraint of (20), and a more apparent influence on the e_{SoC} elimination will be observed. On the other hand, although a small value of m will relieve the adverse effect of the constraint on the e_{SoC} elimination, the value of m_{p0} has to be reduced at the same time to ensure that the variation range of the frequency deviation is limited to 2% under the full-loading condition, which yields:

$$\frac{m_{p0}}{m} \le \frac{2\% \times \omega^*}{P_{\max}} \tag{21}$$

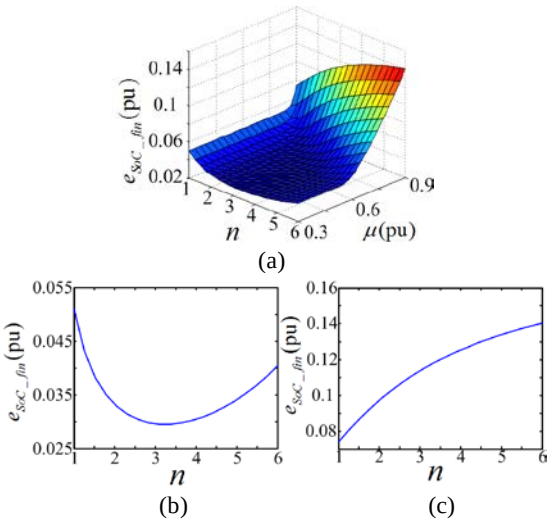

Fig. 5. Relation of n, μ and e_{SoC_fin}. (a) 3-D picture. (b) Sectional drawing of μ=0.3. (c) Sectional drawing ofμ=0.9.

where $P_{\max}$ is the maximum output active power of the inverter. Therefore, the compromised value of m is selected as 0.2.

Thirdly, the capacity of the paralleled ESDs should meet the active power of load in the islanded microgrid, which yields:

$$P_{load} = \mu \times (z \times P_{\max}) \tag{22}$$

where z is the number of battery ESDs in the islanded microgrid; μ is the loading condition factor of the islanded microgrid, and $\mu \in [0,1]$. Therefore, the loading condition of the islanded microgrid varies from no-loading to full-loading. As a result, μ increases from 0 to 1.

Further, the output active power of each ESD is restrained by the maximum output active power limitation of the inverter. Based on the principle of the droop controller [13]-[19], the output active power constraint of each ESD is derived and located at the bottom of this page.

If the constraint of equation (23) is triggered, the output active power of the ESD cannot cover the requirement from the droop controller, which weakens the performance of the e_{SoC} elimination.

In summary, all of the above constraints impair the effect of the proposed droop controller on e_{SoC} elimination, which enhances the stability and quality of the islanded microgrid. Therefore, the performance analysis of e_{SoC} elimination should be established on the constraints.

B. Performance of e_{SoC} Elimination under Constraints

To investigate the performance of e_{SoC} elimination by the

$$P_i = \begin{cases} \dfrac{n_i \times [-\ln(SoD_i + C)]^{n_i}}{\sum_{j=1}^{z} n_j \times [-\ln(SoD_j + C)]^{n_j}} P_{load} & \left(\dfrac{n_i \times [-\ln(SoD_i + C)]^{n_i}}{\sum_{j=1}^{z} n_j \times [-\ln(SoD_j + C)]^{n_j}} P_{load} < P_{\max}\right) \\ P_{\max} & \left(\dfrac{n_i \times [-\ln(SoD_i + C)]^{n_i}}{\sum_{j=1}^{z} n_j \times [-\ln(SoD_j + C)]^{n_j}} P_{load} \ge P_{\max}\right) \end{cases} \tag{23}$$

proposed droop controller, both the former mentioned constraints and the operation conditions of the paralleled battery ESDs should be considered. Firstly, the value of the accelerating parameter n is a important factor affecting the performance of the e_{SoC} elimination in the discharging process. In addition, considering the uncertainty and randomness in islanded microgrids, the different loading conditions and initial rest energy in paralleled battery ESDs should be taken into account.

To figure out the influence of the above scenarios on e_{SoC} elimination under constraints, a paralleled system comprising two ESDs is analyzed. This is done to show the effects of the proposed droop controller on the final result of e_{SoC}, which is defined as e_{SoC_fin}. In this study, both of the paralleled battery ESDs start-up simultaneously, and they cease operation when the SoC of either of the ESDs is reduced to 0.1. Therefore, a smaller value for e_{SoC_fin} means better performance in terms of e_{SoC} elimination.

First, the effect of the loading condition factor μ and the value of the accelerating parameter n on the e_{SoC} of the paralleled battery ESDs is illustrated, where the initial values of the two battery ESDs are SoC_{upper}=0.75 and SoC_{lower}=0.55, and the variation ranges of μ and n are 0.3-0.9 and 1-6, respectively. Therefore, Fig. 5 can be drawn to show the relationship between μ, n and e_{SoC_fin}. Fig. 5(a) shows the characteristics of e_{SoC_fin} for each combination of μ and n, with the initial value and various ranges listed above. In addition, Fig. 5(b) and Fig. 5(c) illustrate sectional drawings of Fig. 5(a) at μ=0.3 and 0.9, respectively.

Fig. 5(a) shows that e_{SoC_fin} increases as μ increases or as n decreases. Specifically, according to Fig. 5(b) and 5(c), e_{SoC_fin} first decreases and then increases like an arc under the low-loading condition with n increasing. This means an appropriate value of n is beneficial to balance the SoC of the batteries in different ESDs. On the other hand, e_{SoC_fin} increases rapidly under the high-load condition with n increasing. In addition, by comparing Fig. 5(b) and 5(c), it can be seen that a smaller e_{SoC_fin} can be obtained under the low-loading condition. This occurs because the elimination effect of n on the e_{SoC} forces the inverter of the ESD with a higher SoC to operate with the maximum output active power limitation in the high-loading condition, which weakens the ability of n to balance the SoC in paralleled ESDs. Furthermore, it can be seen that as both of the SoCs of the paralleled ESDs decrease continuously, a large n introduces the restriction shown in (20) in advance to force both of the ESDs to run under the same active power droop coefficient, which weakens the ability of the scheme to eliminate the e_{SoC}.

Second, the effects of the value of the accelerating parameter n and the initial value of the SoCs on e_{SoC_fin} are analyzed as follows, where μ=0.6, the initial e_{SoC} of the parallel battery ESDs e_{SoC_ini}=0.2, and SoC_{lower_ini}=SoC_{upper_ini}-e_{SoC_ini}. Therefore, Fig. 6 is obtained with Fig. 6(a) indicating the variations of

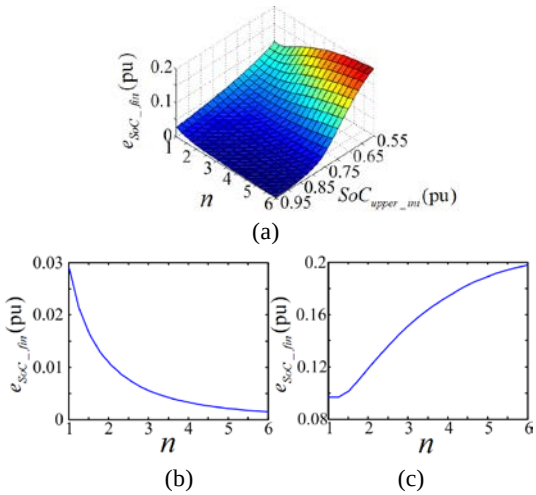

Fig. 6. Relation of n, SoC_{upper_ini} and e_{SoC_fin}. (a) 3-D picture. (b) Sectional drawing of SoC_{upper_ini} =0.95. (c) Sectional drawing of SoC_{upper_ini} =0.55.

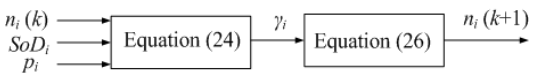

Fig. 7. The flowchart of adaptive accelerating parameter.

e_{SoC_fin} for each combination of SoC_{upper_ini} from 0.95 to 0.55, and n from 1 to 6. Fig. 6(b) and 6(c) display sectional drawings of Fig. 6(a) at SoC_{upper_ini}=0.95 and 0.55, respectively.

Fig. 6(a) show that a large n is more effective in reducing e_{SoC_fin} when the initial SoCs of both of the paralleled ESDs are relatively high. Further, when the initial SoCs are relatively low, the larger the value of n, the earlier the droop controller is involved in equation (20). Therefore, both of the paralleled ESDs will operate with m_{pi}= m_{p0}/m for a long time, which impedes the e_{SoC} from decreasing further. As a result, the value of e_{SoC_fin} in Fig. 6(c) is much higher than that in Fig. 6(b).

It can be concluded from the above analyses that the ability to eliminate the e_{SoC} of paralleled battery ESDs is restrained with a fixed accelerating parameter n under different operation scenarios. Furthermore, as μ increases and/or SoC decreases in paralleled battery ESDs, a large accelerating parameter n has negative impacts on the e_{SoC} suppression. This implies that the accelerating parameter n should be adjustable online with the ESD operation condition.

C. The Design of the Adaptive Accelerating Parameter

Based on the former conclusion, the value of the accelerating parameter n should be established on the information of the loading condition factor μ and the rest energy in paralleled battery ESDs to improve the performance of the e_{SoC} elimination. However, without a communication malfunction, only the locally measured information which includes P_i and $n_i \times[-\ln(SoD_i+C)]^{ni}$ can be sampled from the inverter.

In order to construct the information of an islanded microgrid, based on principle of the droop controller, the

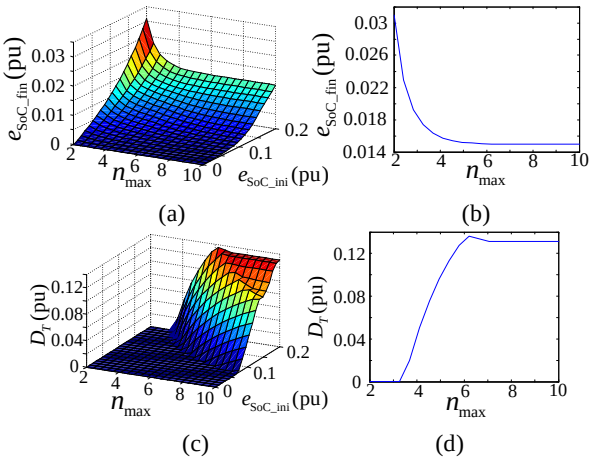

Fig. 8. Relation of $n_{\max}$, e_{SoC_ini}, e_{SoC_fin} and D_T. (a) 3D-picture of $n_{\max}$, e_{SoC_ini} and e_{SoC_fin}. (b) Sectional drawing of e_{SoC_ini}=0.2. (c) 3D-picture of $n_{\max}$, e_{SoC_ini} and D_T. (d) Sectional drawing of e_{SoC_ini}=0.2.

parameter γ is defined as:

$$\begin{aligned}\gamma_i &= P_i / \{n_i \times [-\ln(SoD_i + C)]^{n_i}\} \\ &= P_{load} / \{\sum_{j=1}^{z} n_j \times [-\ln(SoD_j + C)]^{n_j}\} \\ &= \frac{\mu \times z \times P_{\max}}{\sum_{j=1}^{z} \{n_j \times [-\ln(SoD_j + C)]^{n_j}\}}\end{aligned} \tag{24}$$

It is worth noting that equation (24) indicates that γ_i increases as μ increases and/or as the SoC decreases, which means that γ_i has the same characteristic as e_{SoC_fin}. More importantly, γ_i can be generated by locally measured information. Therefore, γ_i is utilized to approximately reveal the islanded microgrid state for constructing an adaptive accelerating parameter n.

To obtain the adaptive accelerating parameter n, the variation range of γ_i needs to be defined. Due to the constraints of (20) and (23), the maximum value of γ_i is expressed as:

$$\gamma_{\max} = \frac{P_{\max}}{m} \tag{25}$$

The expression and constraint of n_i are given by:

$$n_i = \begin{cases} \gamma_{\max} / \gamma_i & (1 \le \gamma_{\max} / \gamma_i < n_{\max}) \\ n_{\max} & (\gamma_{\max} / \gamma_i \ge n_{\max}) \end{cases} \tag{26}$$

where $n_{\max}$ denotes the maximum value of n.

In summary, the adaptive accelerating parameter n is obtained based on the above analyses. Specifically, according to (24)-(26), the adaptive accelerating parameter n is generated online based on the operation condition of each ESD, and the flowchart is shown in Fig. 7. When the discharging process is over, the output active power of each inverter is zero. Thus, the value of $\gamma_{\max}/\gamma_i$ is close to infinity. Therefore, the constraint in (26) will reset the value of n_i to $n_{\max}$ to wait for the next discharging process.

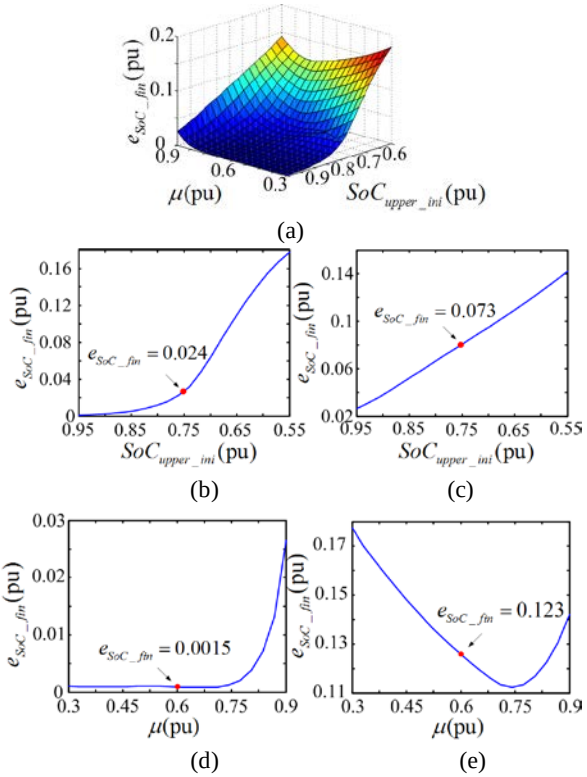

Fig. 9. Relation ofμ, SoC_{upper_ini} and e_{SoC_fin}. (a) 3-D picture. (b) Sectional drawing of μ=0.3. (c) Sectional drawing ofμ=0.9. (d) Sectional drawing of SoC_{upper_ini} =0.95. (e) Sectional drawing of SoC_{upper_ini} =0.55.

To select an appropriate $n_{\max}$, Fig.8 is utilized to analyze the effects of $n_{\max}$ on e_{SoC_fin} from the views of the e_{SoC_fin} value and the inverter operation time under the maximum output active power. The system is set to operate with SoC_{upper_ini} =0.75, SoC_{lower_ini}= SoC_{upper_ini} - e_{SoC_ini} and μ=0.6.

Fig. 8(a) shows that e_{SoC_fin} increases as $n_{\max}$ decreases or as e_{SoC_ini} increases. On the other hand, Fig. 8 (b) indicates that e_{SoC_fin} is a monotonic decreasing function when $n_{\max}$<6. If $n_{\max}$ is too small, it has a very limited effect on suppressing the e_{SoC_fin} value of the paralleled battery ESDs. D_T in Fig. 8(c) denotes the ratio between the time of the inverter running under the maximum output active power condition and the total operation time from start-up to the end. The expression of D_T is given by:

$$D_T = \frac{maximum\ output\ power\ operation\ time}{total\ operation\ time} \times 100\% \tag{27}$$

It can be seen from Fig. 8(c) that D_T increases as e_{SoC_ini} and $n_{\max}$ increase. Moreover, according to Fig. 8(d), D_T increases in a straight line when the inverter operates under the maximum output active power condition with a $n_{\max}$ that is larger than 6. This indicates that even a large $n_{\max}$ cannot expedite the process of balancing each of the SoCs of the paralleled battery ESDs. Meanwhile, as $n_{\max}$ increases, the active power droop coefficient m_{pi} changes rapidly in a large range, which undermines the stability of paralleled battery

ESDs. Therefore, n_{max}=6 is chosen to be the optimized factor for the adaptive accelerating parameter.

To analyze the effects of the proposed adaptive accelerating parameter scheme, Fig. 9(a) is pictured for contrast with the fixed accelerating parameter scheme, where μ and SoC_{upper_ini} are variables and the initial values are e_{SoC_ini} =0.2 and SoC_{lower_ini}= SoC_{upper_ini} - e_{SoC_ini}. Moreover, Fig. 9(b)-(e) are sectional drawings when μ=0.2, μ=0.6, SoC_{upper_ini} =0.95 and SoC_{upper_ini} =0.55, respectively.

According to Fig. 9(a), e_{SoC_fin} can stay at less than 0.05 under most operation conditions. Although e_{SoC_fin} increases slightly with a high-loading and low initial value of the SoC, the range of movement is remarkably compressed in comparison to the cases in Fig. 5(a) and Fig. 6(a).

It should be noted that a red dot is marked on both of the curves in Fig. 9(b) and 9(c) at SoC_{upper_ini}=0.75. This signifies the same external simulation environment as that shown in Fig. 5(b) and 5(c), respectively. It is obvious that the e_{SoC_fin} of the two red dots are both smaller than those of the corresponding cases with a fixed accelerating parameter n_i. Likewise, a red dot is marked on both of the curves in Fig. 9(d) and 9(e) at μ=0.4. This is the same as the external simulation environment of Fig. 6(b) and 6(c). It is obvious that the e_{SoC_fin} of the two red dots are smaller than or close to those of the corresponding cases with a fixed accelerating parameter n_i.

According to the above analyses, the proposed adaptive accelerating parameter n_i can effectively improve the performance of e_{SoC} elimination under constraints without communication.

IV. Small-Signal Modeling and Stability Analysis

Based on the analyses in section III, the structure of the proposed adaptive accelerating parameter SoC error eliminating droop controller is displayed in Fig. 10.

To investigate the stability of the system, a small signal model is presented by imposing a subtle disturbance on the proposed droop controller. Then, the active power and reactive power can be obtained as:

$$\begin{cases} \hat{P}_i = \dfrac{\partial P_i}{\partial \theta_i}\hat{\theta}_i + \dfrac{\partial P_i}{\partial V_i}\hat{v}_i \\ \hat{Q}_i = \dfrac{\partial Q_i}{\partial \theta_i}\hat{\theta}_i + \dfrac{\partial Q_i}{\partial V_i}\hat{v}_i \end{cases} \tag{28}$$

By employing a LPF, the active and reactive power of the ESD can be obtained as:

$$\begin{cases} \hat{p}_i = \dfrac{\omega_c}{s+\omega_c}\left(\dfrac{\partial P_i}{\partial \theta_i}\hat{\theta}_i + \dfrac{\partial P_i}{\partial V_i}\hat{v}_i\right) \\ \hat{q}_i = \dfrac{\omega_c}{s+\omega_c}\left(\dfrac{\partial Q_i}{\partial \theta_i}\hat{\theta}_i + \dfrac{\partial Q_i}{\partial V_i}\hat{v}_i\right) \end{cases} \tag{29}$$

Considering a small disturbance added to (1), it can be expressed as:

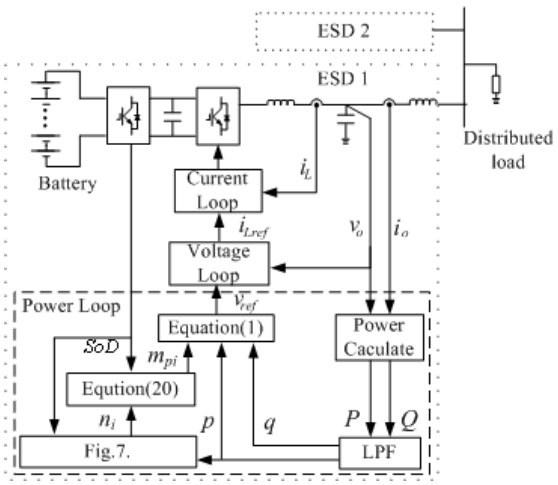

Fig. 10. Control structure of ESD by proposed droop controller.

$$\begin{cases} \hat{\omega}_i = -m_{pi}\hat{p}_i - \hat{m}_{pi}p_i \\ \hat{v}_i = -m_q\hat{q}_i \end{cases} \tag{30}$$

where the small disturbance of m_{pi} is considered as:

$$\hat{m}_{pi} = \frac{\partial m_{pi}}{\partial SoC_i}\hat{SoC}_i + \frac{\partial m_{pi}}{\partial n_i}\hat{n}_i \tag{31}$$

From equation (11) and (26), the perturbation equations of n_i and the SoC are achieved as:

$$\hat{n}_i = \frac{\partial n_i}{\partial SoC_i}\hat{SoC}_i + \frac{\partial n_i}{\partial n_i}\hat{n}_i + \frac{\partial n_i}{\partial p_i}\hat{p}_i \tag{32}$$

$$\hat{SoC} = -\frac{\hat{P}}{s \times Bat} \tag{33}$$

Considering that $\theta=\omega/s$, the characteristic equation of the system can be derived as follows according to (28)-(33).

$$A_0 s^5 + B_0 s^4 + C_0 s^3 + D_0 s^2 + E_0 s^1 + F_0 = 0 \tag{34}$$

Based on the analyses in section III, the restriction on n_i in equation (26), which makes n_i equal to n_{max} and the disturbance become zero when $n_i \geqslant n_{max}$, can reduce the order of (34) from 5 to 4. The modified characteristic equation is expressed as:

$$B_1 s^4 + C_1 s^3 + D_1 s^2 + E_1 s^1 + F_1 = 0 \tag{36}$$

Likewise, the disturbance of m_p is zero under the limitation shown in (20), which reduces the order to 3. The further modified characteristic equation is given by:

$$C_2 s^3 + D_2 s^2 + E_2 s^1 + F_2 = 0 \tag{37}$$

where the coefficients above can be calculated in Matlab.

It can be seen from Fig. 11(a) that with a fixed SoC value and an increasing output active power, the restrictions of (20) and (26) on the adaptive accelerating parameter n_i disappear. This turns the characteristic equation of the proposed droop controller from 3rd order to 5th order. In this case, there are 3 poles of the 5th order eigenvalue in the real axis, one of which is the same as that of the 3rd order eigenvalue. In addition, the conjugate poles of the 5th order eigenvalue move towards the real and imaginary axis simultaneously, thus degrading the dynamic performance of the droop controller while increasing

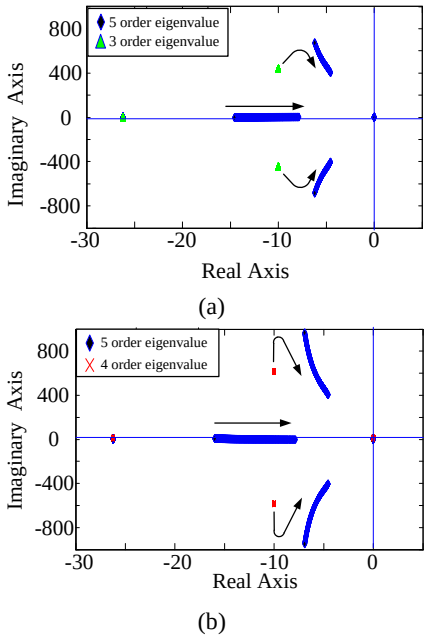

Fig. 11. Eigenvalue of proposed droop controller at SoC=0.5, P_{load}=3kW-18kW. (a) With constraint of (20). (b) Without constraint of (20)

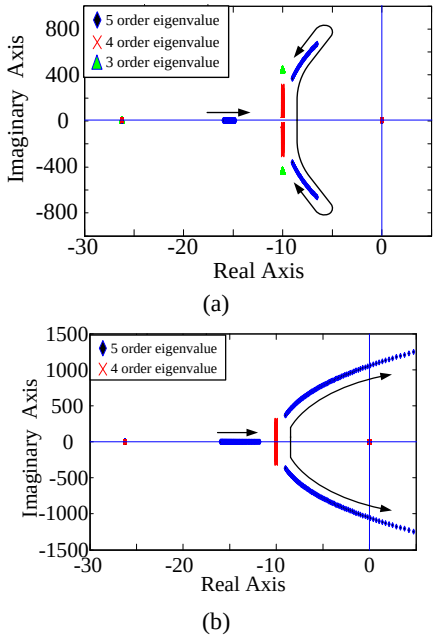

Fig. 12. Eigenvalue of proposed droop controller at P_{load}=10kW, SoC=0.8-0.2.(a) With constraint of (20). (b) Without constraint of (20).

the damping of the controller.

Fig. 11(b) illustrates the movement trajectory of the eigenvalues without the constraint of (20). The 4th order characteristic equation is shown, where the system is running under the low-loading condition. With the increasing output active power, the restriction of (26) on the adaptive accelerating parameter n disappeared. This turns the characteristic equation of the proposed droop controller from 4th order to 5th order. Although a better dynamic performance is achieve under the low-loading condition, a larger value of frequency deviation is generated, because the constraint of (20) is removed.

Fig. 12(a) analyzes the droop controller eigenvalue with a fixed output active power and different SoC values. It can be concluded that the droop controller characteristic equation transfers to the 5th order from the 4th order and finally to the 3rd order with decreasing values of the SoC. With a relatively large SoC value, the restriction of (26) forces n to be $n_{\max}$, which make the droop control to work under the 4th order characteristic equation. As the SoC value decreases, n varies in the range from 6 to 1 according to the operating condition of the ESD. As the SoC decreases further, the restriction of (20) on the droop controller appears and forces the system to work under a 3rd-order characteristic equation. It can be seen from the movement trajectory of the eigenvalue in Fig. 12(a) that the conjugate poles move far away from the imaginary axis with decreases in the SoC value. This improves the dynamic performance of the system.

Fig. 12(b) shows that without the constraint of (20), the conjugate poles of the 5th order eigenvalues shift towards the imaginary axis and away from the real axis. With decreases in the SoC, the conjugate poles pass over the imaginary axis and eventually move into the right half of the s-plane. As a result, the droop controller becomes unstable. Therefore, the constraint of (20) is necessary to ensure the stability of the droop controller.

In summary, the constraints of (20) and (26) ensure that all of the eigenvalues are in the left half of the s-plane thereby proving the stability of the proposed droop controller. In addition, Fig. 11 and 12 indicate that one pole is located near the origin in the case of both the 4th-order and 5th-order eigenvalue. Therefore, the sensitivity of this pole with respect to the other parameters of the system is analyzed as follows.

Table I indicates that the sensitivity of this pole with respect to the capacity of the battery is much higher than that of the other parameters. It is worth noting that the capacity can be adjusted in a wide range according to the requirements of the system while the active and reactive power droop coefficient should not be changed randomly since they can affect both the steady-state character and the transient performance of the whole system. Therefore, two operating statuses with the properties of the 4th-order and 5th-order characteristic equations are chosen to observe the root locus near the origin considering variations of the battery capacity.

Fig. 13 shows that the corresponding pole moves towards the origin along the real axis with a smaller step as the capacity of the battery is augmented. Furthermore, the poles are still located in the left half plane and the droop controller is still stable even when the capacity becomes ten times bigger.

In conclusion, the adaptive accelerate parameter SoC error eliminating droop controller presented in this paper will change the order of the characteristic equation under different

TABLE I
SENSITIVITY OF POLE WITH MP0, N AND BAT

order	m_{p0}	n	Bat
5 order eigenvalue	3.9643	3.9643	5.5159
4 order eigenvalue	1.3062	1.3062	2.5625

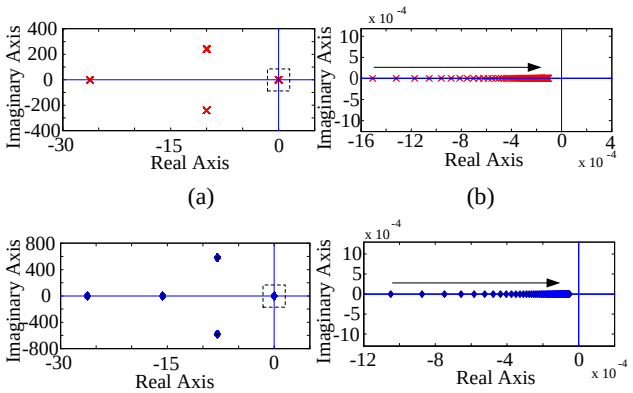

Fig. 13. Eigenvalue with 1.4×10^{8}J<Bat<2.88×10^{9}J. (a) 4-order eigenvalue. (b) Enlarged drawing of dashed-line. (c) 5-order eigenvalue. (d) Enlarged drawing of dashed-line.

operation conditions. In addition, the restrictions of equations (20) and (26) improve the stability of the control loop and guarantee that the proposed droop controller is applicable in paralleled battery ESDs.

V. SIMULATION AND EXPERIMENT RESULTS

The performance of the e_{SoC} elimination using the proposed adaptive accelerating parameter n has been tested in Matlab/Simulink. Its performance is also compared with the fixed accelerating parameter n and the strategy in [24]. The loading power factor μ of the paralleled ESDs is selected as 0.2, 0.5 and 0.8 for simulating low-loading to high-loading of the system. The SoC_{upper_ini} is changed from 0.95 to 0.55, and 0.2 for e_{SoC_ini} has been established. The rest of the parameters are listed in the Appendix.

The first comparison of the performance of e_{SoC} elimination is shown in Fig. 14 with the adaptive accelerating parameter n, the fixed accelerating parameter n=6, and the strategy in [24] n=6.

As a result of the comparison, it can be seen from Fig. 14 that the proposed adaptive accelerating parameter n achieves a smaller e_{SoC_fin} when compared with the fixed accelerating parameter n=6 and the strategy in [24] n=6. Under the low-loading condition, the curves of the fixed accelerating parameter and the adaptive accelerating parameter appear to overlap, which means that the adaptive accelerating parameter n is close to 6. Under the medium-loading and high-loading conditions, the difference in the values between the e_{SoC_fin}s, which are generated by the adaptive accelerating parameter and the fixed accelerating parameter, rises gradually as the

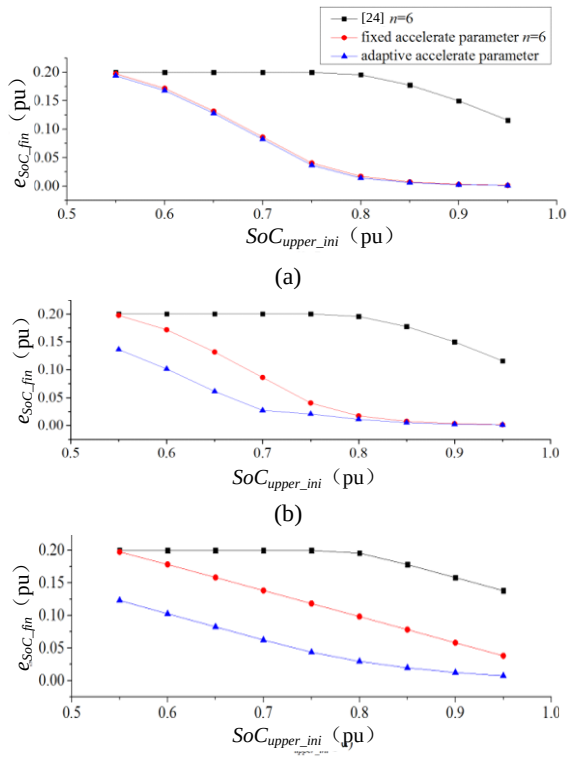

Fig. 14. The comparison of simulation result with adaptive accelerating parameter n, fixed accelerating parameter n=6 and [24] n=6. (a) μ=0.2. (b) μ=0.5. (c) μ=0.8.

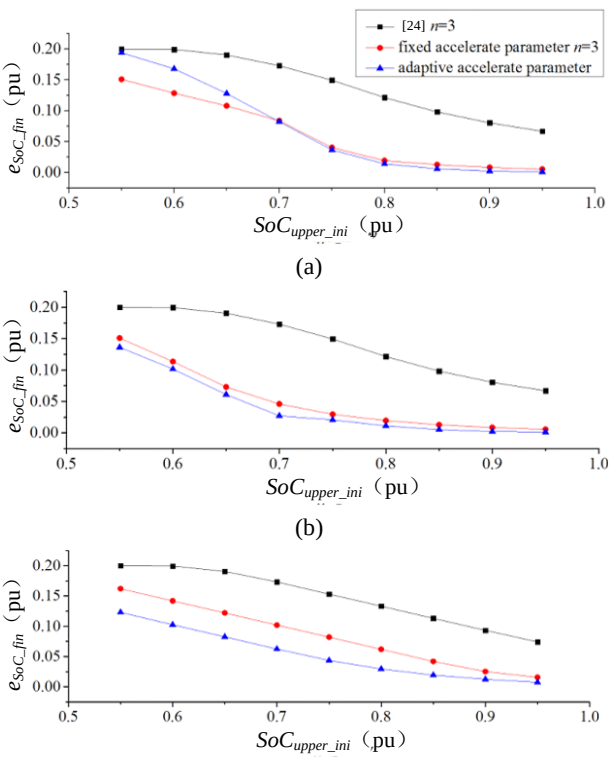

Fig. 15. The comparison of simulation result with adaptive accelerating parameter n, fixed accelerating parameter n=3 and [24] n=3. (a) μ=0.2. (b) μ=0.5. (c) μ=0.8.

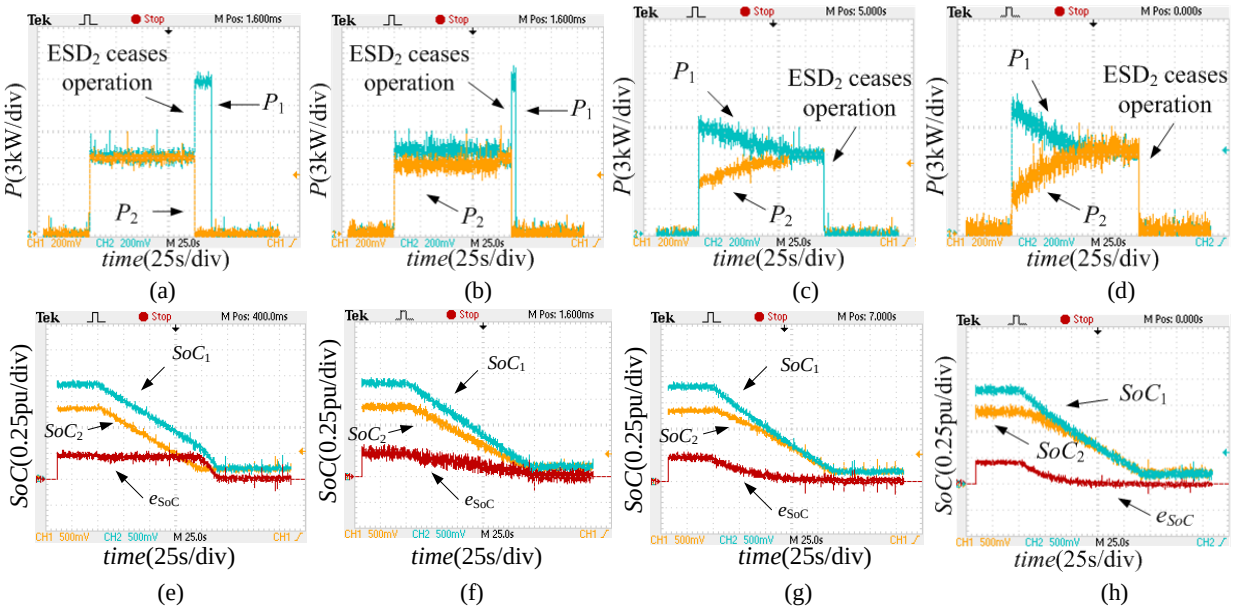

Fig. 16. Experiment results of output active power and *SoC* in paralleled battery ESDs. (a) Output power under conventional droop control. (b) Output power under fixed accelerating parameter n=1. (c) Output power under fixed accelerating parameter n=3. (d) Output power under adaptive accelerating parameter n. (e) *SoC* under conventional droop control. (f) *SoC* under fixed accelerating parameter n=1. (g) *SoC* under fixed accelerating parameter n=3. (h) *SoC* under adaptive accelerating parameter.

SoC_{upper_ini} decreases. That is due to the fact that the constraint of (20) is triggered early to impede the e_{SoC} elimination, when n is fixed as 6. The active power droop coefficients of the paralleled ESDs operate under the same value. Thus, the active power of the load is shared equally. By comparison, the curves of the strategy in [24] lay on top of all the pictures. Due to the remarkable frequency deviation, the constraint of (20) is involved too early. With the decrease in the SoC_{upper_ini}, the active power droop coefficients of the paralleled ESDs are running in the same value most of the operation time or even from the beginning. Therefore, using the strategy in [24], e_{SoC} can only be reduced slightly under a high value of the SoC_{upper_ini}.

The second comparison in the performance of the e_{SoC} elimination is shown in Fig. 15 with the adaptive accelerating parameter n, the fixed accelerating parameter n=3 and the strategy in [24] n=3.

Under medium-loading and high-loading conditions, a smaller e_{SoC_fin} is obtained by the adaptive accelerating parameter n. However, under the low-loading condition, the fixed accelerating parameter is able to achieve better performance in terms of e_{SoC} elimination, since the SoC_{upper_ini} is lower than 0.7. Under the low-loading condition, a relatively small value of γ_i is calculated by (24), even when the constraint of (20) is involved in the droop controller. Further, the adaptive accelerating parameter, which is close to 6, is derived from (26) and it triggers the constraint of (20) again. Therefore, the value of the adaptive accelerating parameter traps into an endless repetition and the performance of the e_{SoC} elimination is deteriorated. The curves by the strategy in [24] still lay on the top of the simulation results due to its limited ability in terms of e_{SoC} elimination under the restraint of (20).

In conclusion, when compared with the strategy in [24], the proposed fixed accelerating parameter and adaptive accelerating parameter have better performance in terms of e_{SoC} elimination under the restraint of (20). Further, the adaptive accelerating parameter has better performance fdespite the low range span of the SoC_{upper_ini} at the low-loading condition.

Two ESDs with 30kVA three-phase inverter units were built and tested to verity the performance of the proposed droop controller. Each inverter comprised an *LCL* output filter with the following parameters: L=3mH, L_g=0.8mH, C=20uF, and v_o=220Vrms/50Hz. The impendence of the load is 5+3.15jΩ. The proposed droop controller is implemented in an inverter with parameters shown in the Appendix.

It should be noted that the respective initial SoC values in the paralleled ESDs in Fig. 16 are 0.9 and 0.7. Specifically, (a), (b), (c), and (d) describe the output active power of the paralleled ESDs in one completed operation period. It can be seen that since the same active power droop coefficient is applied in the conventional droop controller, the output active power value of different ESDs will have no difference until one of the ESDs ceases operation due to an excessively low SoC. When compared with the conventional droop controller, the e_{SoC} eliminating droop controller brings a larger difference in the output active power of paralleled ESDs as the fixed accelerating parameter n increases. Further, according to the operation conditions of the paralleled ESDs, the adaptive accelerating parameter can generate a relatively large value of n and remarkably accelerate the process of e_{SoC} elimination. Therefore, the paralleled ESDs can then automatically adjust the output active power based on the current SoC condition and

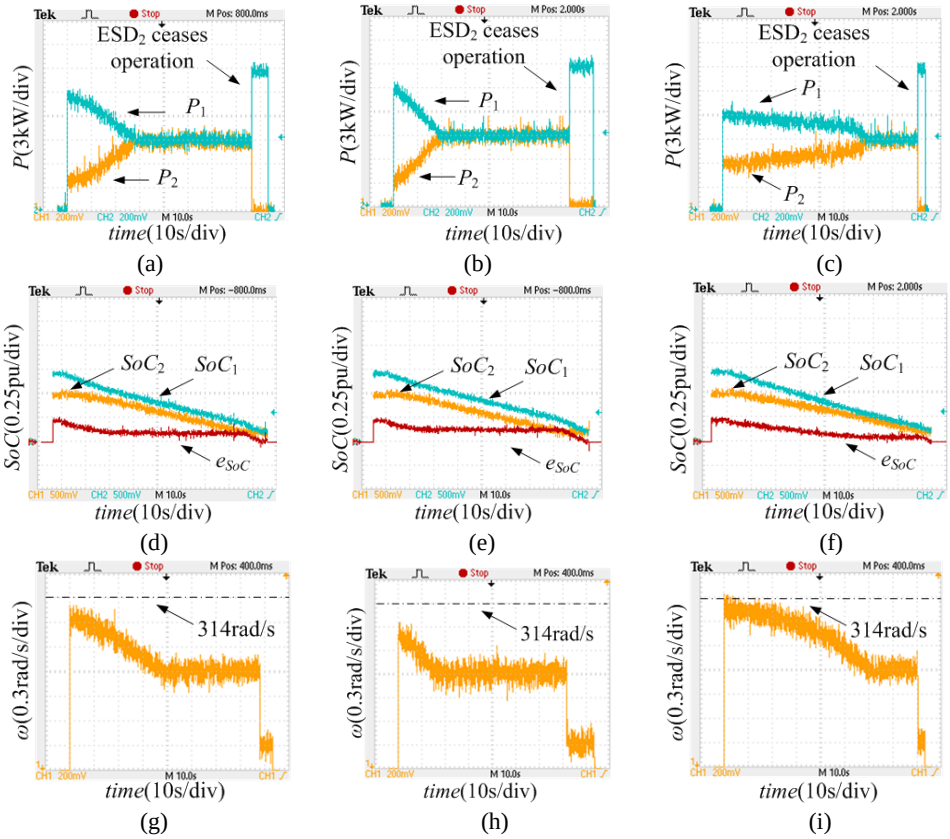

Fig. 17. Experiment results of output active power, *SoC* and frequency. (a) Output power under fixed accelerating parameter n=3. (b) Output power under fixed accelerating parameter n=6. (c) Output power under adaptive accelerating parameter n. (d) *SoC* under fixed accelerating parameter n=3. (e) *SoC* under fixed accelerating parameter n=6. (f) *SoC* under adaptive accelerating parameter n. (g) The frequency of islanded microgrid under fixed accelerating parameter n=3. (h) The frequency of islanded microgrid under fixed accelerating parameter n=6. (i) The frequency of islanded microgrid under adaptive accelerating parameter n.

make sure that both of the ESDs cease operation simultaneously. In addition, the paralleled ESDs which employ the accelerating parameter n display an obvious initial difference in the output active power, which diminishes smoothly as the discharging process goes on. Besides, (e), (f), (g), and (h) show the trajectories of the SoCs in the paralleled ESDs during operation. On the one hand, since the output active power is the same in the paralleled ESDs with the conventional droop controller, the SoC decreases with the same slope. On the other hand, in the case of the paralleled ESDs with a fixed accelerating parameter n, the situation differs according to the value of n. First, the e_{SoC} is reduced slowly when n=1 and because of the restriction of (20), the e_{SoC} cannot decrease any further. Second, the rate of the e_{SoC} elimination increases remarkably when n=3 and the e_{SoC} reaches zero smoothly in the end. Furthermore, the adaptive accelerating parameter scheme significantly reduces the time of the process of e_{SoC} elimination. In conclusion, a zero e_{SoC} can be achieved with paralleled ESDs employing the e_{SoC} eliminating droop controller. The adaptive accelerating parameter n will dramatically raise the rate of the e_{SoC} elimination.

Fig. 17 shows a contrast test between the fixed accelerating parameter n scenario, (n=3, n=6) and paralleled ESDs employing the adaptive accelerating parameter n with initial SoC values of 0.7 and 0.5. It can be seen from (a) and (b) that although a larger difference in the output power of the paralleled ESDs is achieve at the star-up time by n=6, the two ESDs are operated with the same active power droop coefficient too early because of the restriction of (20), which prevents the e_{SoC} from decreasing further and makes a smaller accelerating parameter (n=3) to achieve better performance. In contrast, it can be seen from (c) that the paralleled ESDs can adjust the accelerating parameter n according to the output active power and their SoC condition in real-time. A relatively small value of the accelerating parameter is calculated by (26) to improve the performance of e_{SoC} elimination under the low SoC scenario. Therefore, the restriction of (20) is prevented from being introduced too early, which helped to achieve a better suppression of e_{SoC}. In addition, (d), (e), and (f) show the trajectories of the SoC in the paralleled ESDs during operation. Although the e_{SoC}s are reduced at the start-up time, the constraint of (20) is triggered as the SoC decreases. As a result, the process of e_{SoC} elimination is ceased. When compared with (d) and (e), due to the fact that a relatively small value of n is generated by the adaptive accelerating parameter scheme in (f), the intervention time of (20) is postponed. Therefore, the

running time of the ESD_2 is extended. Thus, a better performance in terms of the e_{SoC} elimination is achieved by the adaptive accelerating parameter scheme. (g), (h), and (i) illustrate the frequency of an islanded microgrid, during the discharging process of paralleled battery ESDs. When compared with (g) and (h), a larger frequency deviation can be observed at the beginning of operation as the fixed accelerating parameter n increases. Further, since the constraint of (20) is involved earlier, both of the paralleled battery ESDs operate as a conventional droop controlled for long time, thus preventing the e_{SoC} from being reduced. Therefore, the frequency of the islanded microgrid is a fixed value for most of the operation time, until the energy of ESD_2 is depleted. As a result, the frequency sags again. Moreover, according to (21), the frequency deviation is limited to 2%, which satisfies the standards of islanded microgrids. (i) shows the frequency waveform under the adaptive accelerating parameter n. It is clear that a smaller frequency deviation is achieved at the beginning, and that the frequency drops slowly. Therefore, during most of the running time, the output active powers of the various paralleled battery ESDs are different, then the e_{SoC} can be reduced more effectively.

VI. CONCLUSION

In this paper, an adaptive accelerating parameter SoC error eliminating droop control scheme for paralleled ESDs in an islanded microgrid has been presented. The SoC is employed in the active power droop coefficient. Thus, the output active power of the ESDs can be adjusted in real-time, which could force the SoC error to decrease while preserving the basic function of the conventional droop controller. Furthermore, considering the restrictions in terms of protection and stability as well as the limitations of inverter power, an adaptive acceleration parameter n is generated without communication. It is then implemented in a droop controller to improve the performance of SoC error elimination under constraints. With the proposed scheme, paralleled ESDs can suppress the SoC error between any two devices in the battery discharging process.

A series of simulation and experiment were carried out to verify the performance of the proposed droop controller. The obtained results have demonstrated that the proposed control scheme can effectively suppress the SoC error, and that the adaptive accelerating parameter can effectively relieve the adverse effect from constraints to improve the performance of SoC error elimination.

APPENDIX

The parameters of the small-single model and the proposed droop controller are shown below:
220Vrms/50Hz, x = 1.8mH, r = 0.01Ω, Q = 483Var, m_{p0} = 2×10^{-5}rad/s/W, m_q = 1×10^{-5}V/Var, $n_{\max}$ = 6, ω_c = 20rad/s, Bat = 2.882×10^{8}J, C=0.1, m=0.2.

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