JPE 15-5-6

http://dx.doi.org/10.6113/JPE.2015.15.5.1200
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

Actively Clamped Two-Switch Flyback Converter with High Efficiency

Min-Kwon Yang* and Woo-Young Choi†

*,†Division of Electronic Engineering, Chonbuk National University, Jeonju, Korea

Abstract

This paper proposes an actively clamped two-switch flyback converter. Compared to the conventional two-switch flyback converter, the proposed two-switch flyback converter operates with a wide duty cycle range. By using an active-clamp circuit, the proposed converter achieves zero-voltage switching for all of the power switches. Zero-current switching of an output diode is also achieved. Thus, compared with the conventional converter, the proposed converter realizes a higher efficiency with an extended duty cycle. The performance of the proposed converter is verified by the experimental results with use of a 1.0 kW prototype circuit.

Key words: Active-clamp, Two-switch flyback converter, Zero-current switching, Zero-voltage switching

I. INTRODUCTION

High switching frequency pulse-width modulated DC-DC converters have been widely used for switch-mode power supplies [1]-[8]. Among these converters, the flyback converter is most popularly used because of its simple power circuit structure [9], [10]. However, the conventional flyback converter is limited by high switch voltage stress [11], [12]. The two-switch flyback converter shown in Fig. 1 uses an additional switch and two clamping diodes to overcome the drawback of the conventional flyback converter [13]. The two switches S_1 and S_2 are turned on and off simultaneously. The two clamping diodes D_{C1} and D_{C2} clamp the voltage across S_1 and S_2 by the input voltage V_{in}. The energy stored in the transformer T is recycled to the input side through the clamping diodes D_{C1} and D_{C2} [14]. However, the conventional two-switch flyback converter operates under a hard-switching condition [15], [16]. The energy stored in the leakage inductor L_{lk} causes voltage spikes when S_1 and S_2 are turned off. The voltage spikes increase the switching losses and consequently decrease the power efficiency. Moreover, the duty cycle of the conventional two-switch flyback converter is limited to 0.5 because the demagnetization of the transformer should be guaranteed [17]. The narrow duty cycle range limits the practical use of the two-switch flyback converter.

To address these problems, this paper proposes an actively clamped two-switch flyback converter. Fig. 2 shows the circuit diagram of the proposed converter. The proposed converter has auxiliary switches S_3 and S_4 and one clamping capacitor C_c. By using an active-clamp circuit, the proposed converter extends the duty cycle of the converter. With the help of the clamping capacitor voltage V_c, the transformer can be demagnetized for the duty cycle from 0 to 1. Furthermore, zero-voltage switching (ZVS) of all of the power switches is achieved. Zero-current switching (ZCS) of an output diode is also achieved. Given that the proposed converter operates under soft-switching conditions, this converter can better improve the power efficiency compared with the conventional converter. The operation principle and converter features are described with simulation verifications. The performance of the proposed converter is verified by the experimental results with the use of a 1.0 kW prototype circuit. Compared with the conventional converter, the proposed converter improves the efficiency by 1.5 % at the rated output power.

Manuscript received Jan. 30, 2015; accepted Apr. 24, 2015
Recommended for publication by Associate Editor Dehong Xu.
†Corresponding Author: wychoi@jbnu.ac.kr
Tel: +82-63-270-2409, Fax: +82-63-270-2394, Chonbuk Nat'l University
*Division of Electronic Eng., Chonbuk National University, Korea

II. PROPOSED CONVERTER

A. Operation Principle

Fig. 2 shows the circuit diagram of the proposed converter. The primary-side circuit consists of power switches (S_1, S_2, S_3,

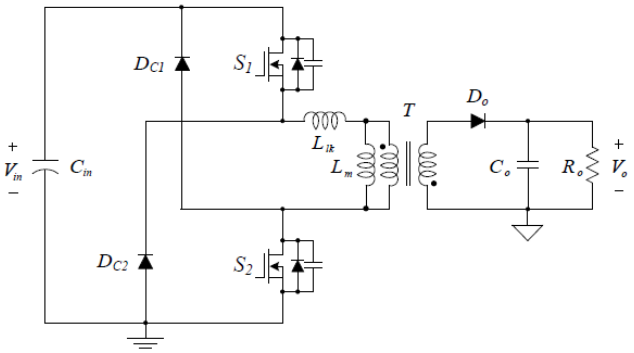


Fig. 1. Circuit diagram of the conventional two-switch flyback converter.

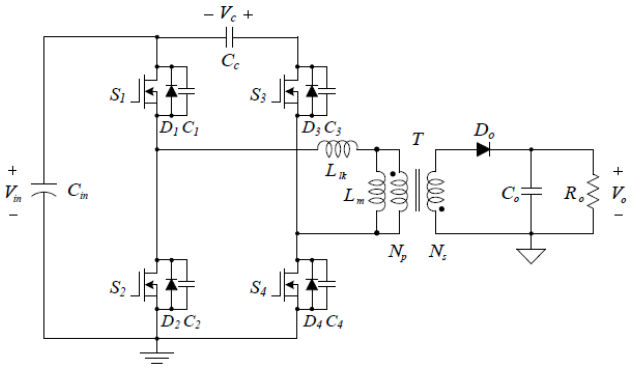


Fig. 2. Circuit diagram of the active-clamped two-switch flyback converter.

S_4), a clamping capacitor (C_c), and a transformer (T). Power switches have body diodes (D_1, D_2, D_3, D_4) and output capacitors (C_1, C_2, C_3, C_4). The transformer T has a magnetizing inductor (L_m) and leakage inductor (L_{lk}) with the turns ratio of 1:N, where $N = N_s/N_p$. The secondary-side circuit consists of an output diode (D_o) and an output capacitor (C_o). V_{in} is the input voltage. V_c is the clamping capacitor voltage. V_o is the output voltage.

Fig. 3 shows the operation modes of the proposed converter during one switching period T_s. The converter has five operation modes during T_s. Fig. 4 shows the switching waveforms of the proposed converter during T_s. Fig. 4(a) shows the switch voltages V_{S1} ,V_{S2}, V_{S3}, and V_{S4} and switch currents i_{S1}, i_{S2}, i_{S3}, and i_{S4}. Fig. 4(b) shows the output diode voltage V_{Do}, diode current i_{Do}, and primary current i_p. When S_1 and S_4 are turned on, S_2 and S_3 are turned off. When S_2 and S_3 are turned on, S_1 and S_4 are turned off. Power switches operate complementarily with a short dead time T_d. The duty cycle D is based on the on-time of S_1 and S_4. Then, the duty cycle of S_2 and S_3 is $1 - D$. Before $t = t_0$, S_2 and S_3 have been turned off. The voltages V_{S1} and V_{S4} have been zero when the primary current i_p flows through D_1 and D_4.

Mode 1 [t_0, t_1]: At $t = t_0$, S_1 and S_4 are turned on at zero voltage. L_m and L_{lk} stores energy from V_{in}. The magnetizing inductor current i_{Lm} increases linearly as follows:

$$i_{Lm}(t) = i_{Lm}(t_0) + \frac{V_{in}}{L_m + L_{lk}}(t - t_0). \tag{1}$$

Mode 2 [t_1, t_2]: At $t = t_1$, S_1 and S_4 are turned off. The primary current i_p charges C_1 and C_4 and discharges C_2 and C_3. V_{S1} increases from zero to V_{in}. V_{S4} increases from zero to $V_{in} + V_c$. V_{S3} decreases from $V_{in} + V_c$ to zero. V_{S2} decreases from V_{in} to zero. Given that the switch output capacitor C_s (= $C_1 = C_2 = C_3 = C_4$) is very small, the time interval during this mode is considered negligible compared with T_s. i_{Lm} is considered to be constant. The leakage inductor L_{lk} starts discharging its energy by the primary current i_p. D_2 and D_3 conduct the primary current i_p.

Mode 3 [t_2, t_3]: At $t = t_2$, S_2 and S_3 are turned on at zero voltage. i_{Lm} decreases linearly as follows:

$$i_{Lm}(t) = i_p(t_2) - \frac{(V_{in} + V_c)}{L_m + L_{lk}}(t - t_2). \tag{2}$$

When the output diode D_o is turned on, the energy stored in L_m is transferred to the output. A series-resonance between L_{lk} and C_c occurs. As the energy stored in L_{lk} is fully discharged by the series-resonance, the output voltage V_o at the secondary side is reflected to the primary side. The primary current i_p flows as follows:

$$\begin{aligned} i_p(t) &= i_p(t_2)\cos\omega_r(t - t_2) + \frac{(V_{in} + V_c) - V_o/N}{Z_r}\sin\omega_r(t - t_2) \\ &= \left(i_{Lm}(t) + \frac{(V_{in} + V_c)}{L_m + L_{lk}}(t - t_2)\right)\cos\omega_r(t - t_2) \\ &\quad + \frac{(V_{in} + V_c) - V_o/N}{Z_r}\sin\omega_r(t - t_2) \end{aligned}. \tag{3}$$

Z_r is the impedance of the series-resonant circuit. ω_r is the angular resonant frequency as follows:

$$Z_r = \sqrt{\frac{L_{lk}}{C_c}}, \tag{4}$$

$$\omega_r = \frac{1}{\sqrt{L_{lk} C_c}}. \tag{5}$$

Mode 4 [t_3, t_4]: At $t = t_3$, the series-resonance is finished when the output diode current i_{Do} is zero. D_o is turned off at zero current. ZCS of D_o is achieved. The leakage inductor L_{lk} has no energy in this mode.

Mode 5 [t_4, t_5]: At $t = t_4$, S_2 and S_3 are turned off. The primary current i_p charges C_2 and C_3 and discharges C_1 and C_4. V_{S1} decreases from V_{in} to zero. V_{S4} decreases from $V_{in} + V_c$ to zero. V_{S3} increases from zero to $V_{in} + V_c$. V_{S2} increases from zero to V_{in}. The leakage inductor L_{lk} starts charging its energy by the primary current i_p. D_1 and D_4 conduct the primary current i_p. The next switching cycle repeats when S_1 and S_4 are turned on at zero voltage.

B. Converter Features

By the volt-second balance law on L_m during T_s, the following relation between V_{in} and V_c is obtained as follows:

$$V_{in} D T_s - (V_{in} + V_c)(1 - D) T_s = 0. \tag{6}$$

From (6), the clamping capacitor voltage V_c is obtained as follows:

$$V_c = \frac{2D - 1}{1 - D} V_{in}. \tag{7}$$

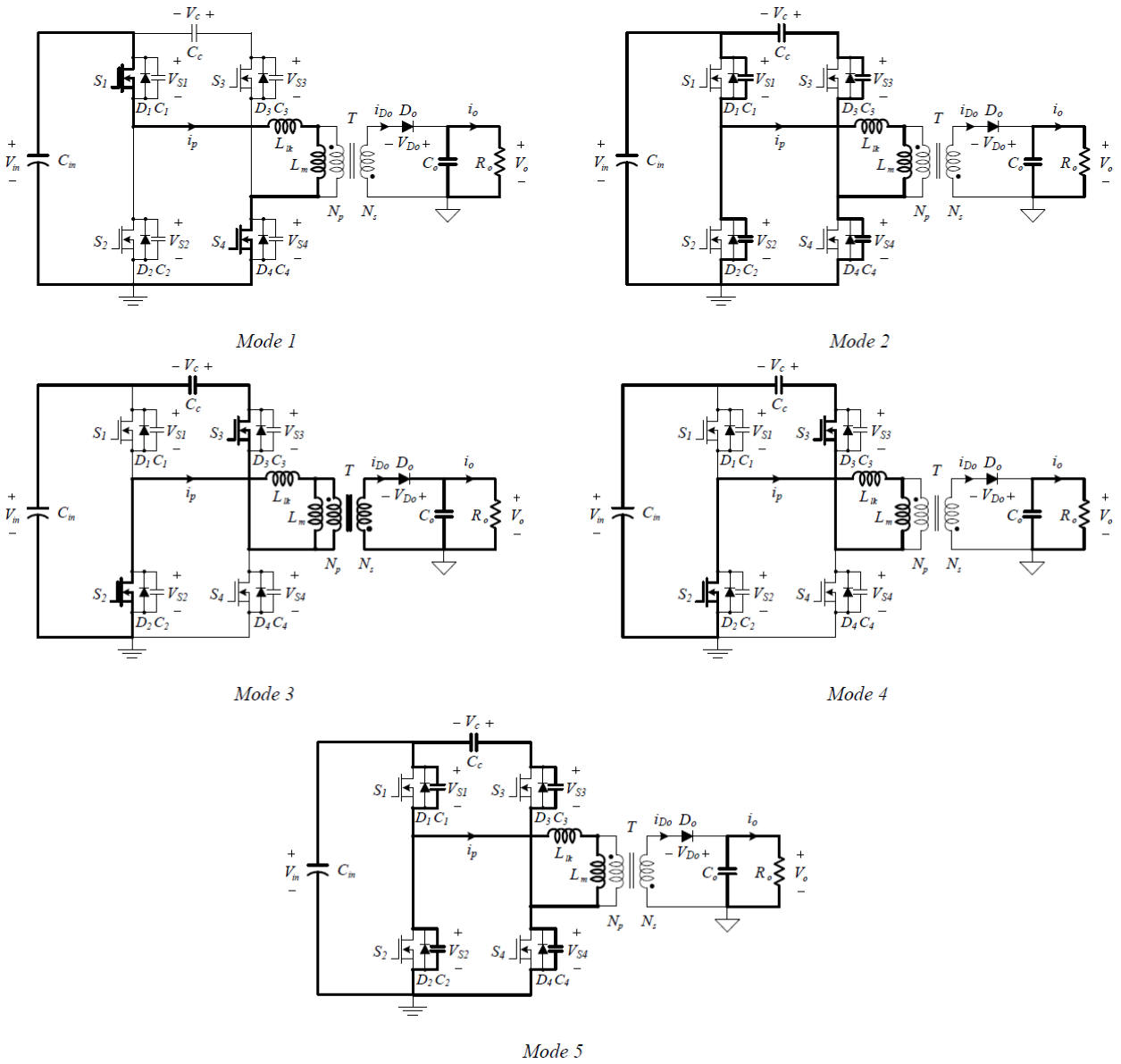


Fig. 3. Operation modes of the proposed converter during T_s.

By the volt-second balance law on the secondary winding of T during T_s, the following relation between V_{in} and V_o is obtained:

$$\frac{V_o}{V_{in}} = \frac{ND}{1-D}. \quad (8)$$

Fig. 5 shows the graph between the normalized voltage gain and the duty cycle D. The duty cycle ranges from 0 to 1. As shown in (7), the clamping capacitor voltage V_c is changed by the duty cycle D. This clamping capacitor voltage affects the transformer in the form of demagnetizing voltage when S_2 and S_3 are turned off. The proposed converter has a wider duty cycle compared with that of the conventional two-switch flyback converter.

At $t = t_0$, to achieve ZVS of S_1 and S_4, the energy stored in L_m is larger than the energy stored in C_s. The following condition should be satisfied to achieve ZVS of S_1 and S_4:

$$\frac{L_m i_{Lm}^2(t_o)}{2} > \frac{(C_1+C_2)}{2}V_{in}^2 + \frac{(C_3+C_4)}{2}(V_{in}+V_c)^2. \quad (9)$$

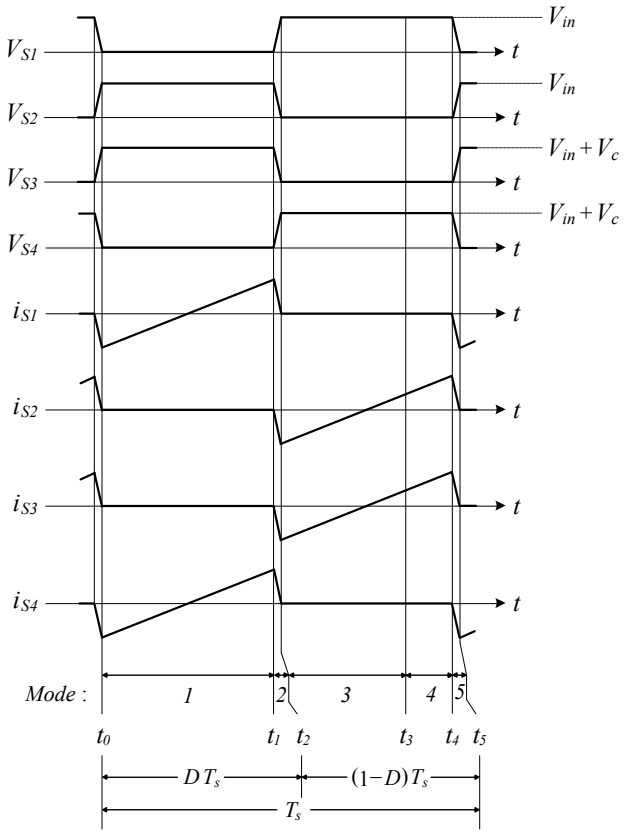
At $t = t_2$, to achieve ZVS of S_2 and S_3, the energy stored in L_m is larger than the energy stored in C_s. The following condition should be satisfied to achieve ZVS of S_2 and S_3:

$$\frac{L_m i_{Lm}^2(t_2)}{2} > \frac{(C_1+C_2)}{2}V_{in}^2 + \frac{(C_3+C_4)}{2}(V_{in}+V_c)^2. \quad (10)$$

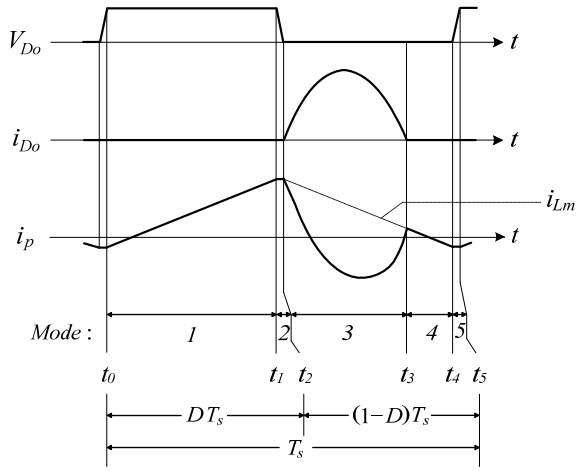
At $t = t_3$, to achieve ZCS of D_o, the diode current i_{Do} becomes zero before D_o is turned off. The time interval from t_3 to t_4 should be ensured to achieve ZCS of D_o. This time duration can be changed by the angular resonant frequency ω_r. The critical condition is $i_p(T_s) = i_{Lm}(T_s)$. Then, the angular resonant frequency must satisfy the following condition: as

$$\omega_r = \frac{1}{\sqrt{L_{lk}C_c}} > \omega_{rc}, \quad (11)$$

where the critical angular resonant frequency $\omega_{rc} = 2\pi f_{rc}$ is



(a)



(b)

Fig. 4. Switching waveforms of the proposed converter during T_s: (a) switch voltages V_{S1} ,V_{S2}, V_{S3}, and V_{S4} and switch currents i_{S1}, i_{S2}, i_{S3}, and i_{S4} and (b) output diode voltage V_{Do}, diode current i_{Do}, and primary current i_p.

decided by

$$\left[\frac{N^2(L_m+L_{lk})}{R_{o,\min}}+0.5(1-D)T_s\right]\cos\omega_{rc}(1-D)T_s$$

$$+\frac{D(L_m+L_{lk})}{L_{lk}\omega_{rc}}\sin\omega_{rc}(1-D)T_s=\frac{N^2(L_m+L_{lk})}{R_{o,\min}}-0.5(1-D)T_s, \quad (12)$$

where $R_{o,min}$ is the minimum output resistance.

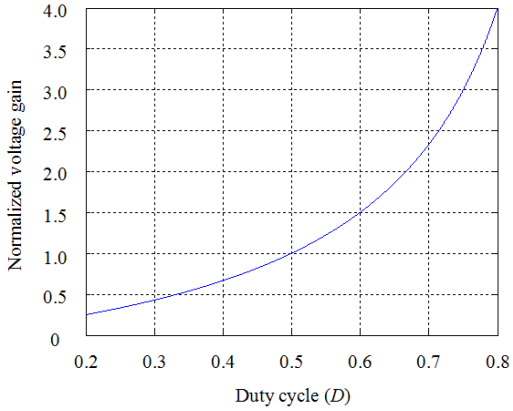
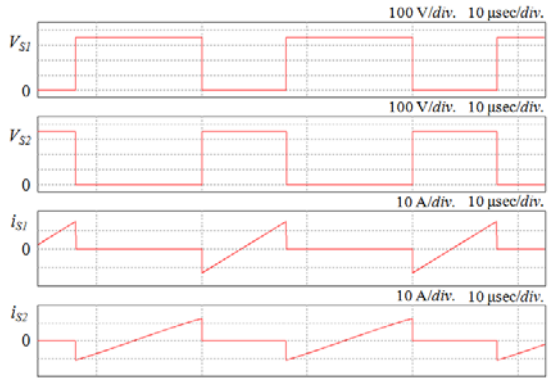
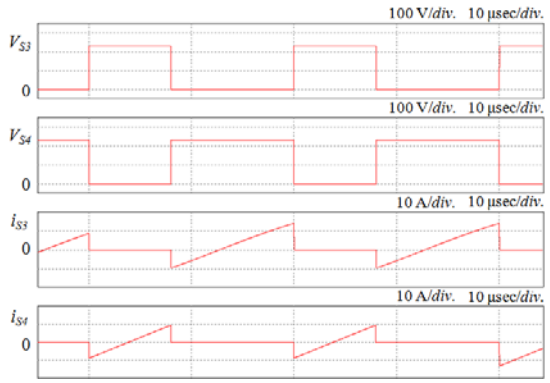


Fig. 5. Graph between the normalized voltage gain and the duty cycle D.



(a)



(b)

Fig. 6. Simulation results for D = 0.4: (a) switch voltages V_{S1} and V_{S2} and switch currents i_{S1} and i_{S2} and (b) switch voltages V_{S3} and V_{S4} and switch currents i_{S3} and i_{S4}.

III. SIMULATION VERIFICATIONS

Fig. 6 shows the simulation results of the proposed converter when V_{in} is 350 V, V_o is 200 V, and D is 0.4. Fig. 6(a) shows the switch voltages V_{S1} and V_{S2} and switch currents i_{S1} and i_{S2} for a 1.0 kW output power. Fig. 6(b) shows the switch voltages V_{S3} and V_{S4} and switch currents i_{S3} and i_{S4} for a 1.0 kW output power. Switch currents are negative before the power switches are turned on. Switch currents flow through the body diodes of the power switches before the power switches are turned on. Thus, ZVS of power

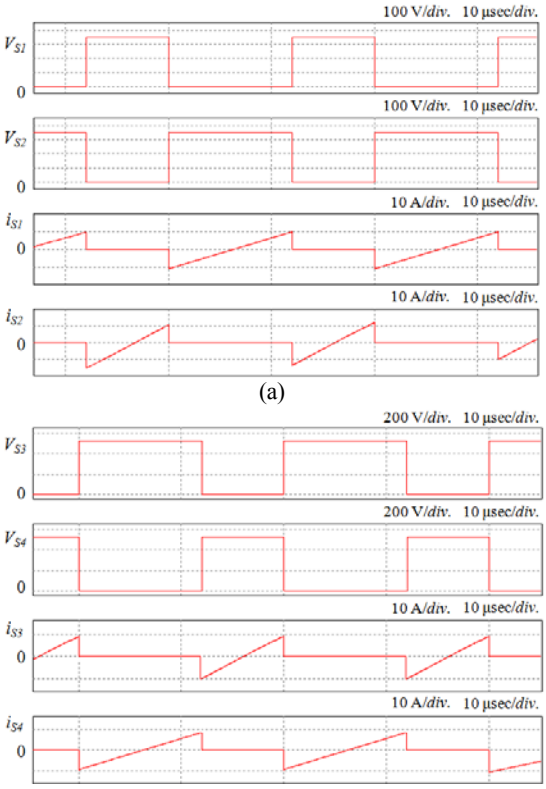


Fig. 7. Simulation results for D = 0.6: (a) switch voltages V_{S1} and V_{S2} and switch currents i_{S1} and i_{S2} and (b) switch voltages V_{S3} and V_{S4} and switch currents i_{S3} and i_{S4}.

switches is achieved. Fig. 7 shows the simulation results of the proposed converter when V_{in} is 350 V, V_o is 450 V, and D is 0.6. Fig. 7(a) shows the switch voltages V_{S1} and V_{S2} and switch currents i_{S1} and i_{S2} for a 1.0 kW output power. Fig. 7(b) shows the switch voltages V_{S3} and V_{S4} and switch currents i_{S3} and i_{S4} for a 1.0 kW output power. As shown in Fig. 7, ZVS of power switches is achieved. Moreover, the duty cycle of the converter can be extended to 0.6. The proposed converter operates with a wide duty cycle and reduced switching losses. Fig. 8 shows the simulated waveforms of the diode voltage V_{Do}, diode current i_{Do}, and primary current i_p when V_{in} is 350 V, V_o is 200 V, and D is 0.4 for a 1.0 kW output power. For the series-resonance between L_{lk} and C_c, L_{lk} = 7.0 μH and C_c = 1.0 μF are selected. The resonant frequency f_r (= $\omega_r/2\pi$) is decided as f_r = 60.1 kHz. Before the output diode is turned off, the diode current becomes zero. ZCS of an output diode is achieved, which reduces the switching power losses of the converter.

IV. Experimental Results

A 1.0 kW prototype circuit has been developed to verify the operation principles and performance of the proposed converter. Table I shows the electrical specification of the proposed converter. Table II shows the parameters of the power circuit components.

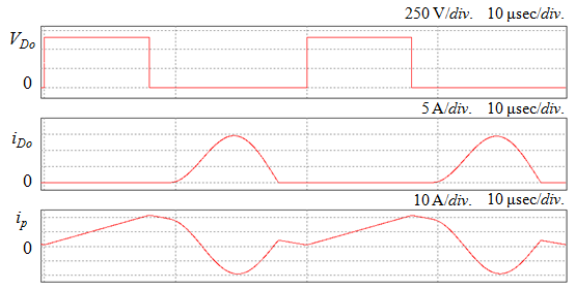


Fig. 8. Simulated waveforms of the diode voltage V_{Do}, diode current i_{Do}, and primary current i_p for D = 0.4.

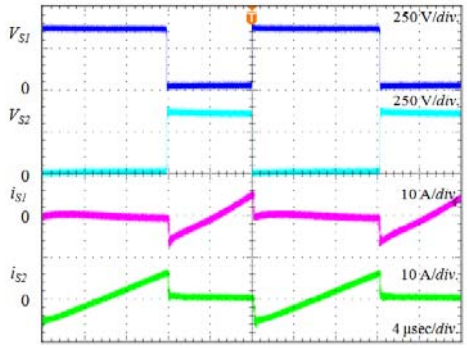
TABLE I
Electrical Specification of the Proposed Converter

Component	Parameter
Input voltage V_{in}	350 V
Output voltage V_o	200 V
Switching frequency f_s	50 kHz
Output power P_o	1.0 kW

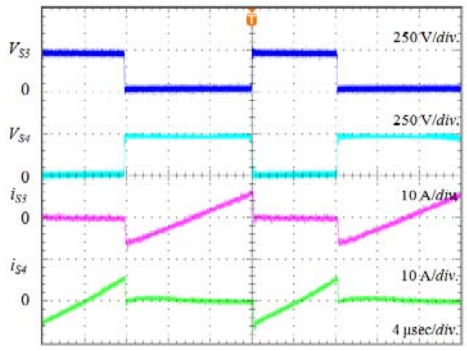
TABLE II
Parameters of the Power Circuit Components

Component	Parameter
Clamping capacitor C_c	1.0 μF
Power switches $S_1 \sim S_4$	FCH76N60NF
Switch output capacitor C_S	192.0 pF
Transformer turns ratio N	N_p : 14, N_s : 12
Magnetizing inductor L_m	80.0 μH
Leakage inductor L_{lk}	7.0 μH
Output diode D_o	RHRP15120
Output capacitor C_o	1.0 mF

Fig. 9 shows the experimental results of the proposed converter for an open-loop test. When D is 0.4, V_o is 200 V for V_{in} = 350 V. Fig. 9(a) shows the switch voltages V_{S1} and V_{S2} and switch currents i_{S1} and i_{S2} for a 1.0 kW output power. Fig. 9(b) shows the switch voltages V_{S3} and V_{S4} and switch currents i_{S3} and i_{S4} for a 1.0 kW output power. ZVS of power switches is achieved, which reduces the switching losses at the primary side. Fig. 10 shows the experimental results of the proposed converter for an open-loop test. When D is 0.6, V_o is 450 V for V_{in} = 350 V. Fig. 10(a) shows the switch voltages V_{S1} and V_{S2} and switch currents i_{S1} and i_{S2} for a 1.0 kW output power. Fig. 10(b) shows the switch voltages V_{S3} and V_{S4} and switch currents i_{S3} and i_{S4} for a 1.0 kW output power. The proposed converter can operate when the duty cycle is over 0.5. Fig. 11 shows the experimental waveforms of the diode voltage V_{Do}, diode current i_{Do}, and primary current i_p when V_o is 200 V with D = 0.4 for a 1.0 kW output power. The resonant frequency f_r is around f_r = 60 kHz, which is above the switching frequency f_r = 50 kHz. ZCS of output diode is also achieved, which reduces the switching power losses at the secondary side. Fig. 12 shows the experimental waveforms of the proposed converter for a closed-loop test. This figure also shows the

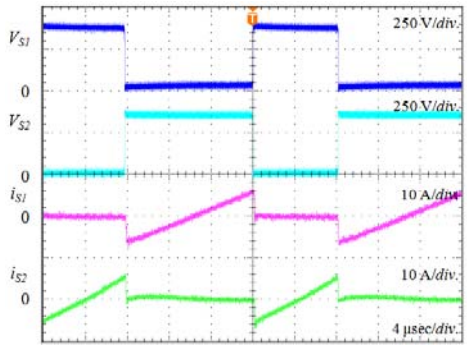


(a)

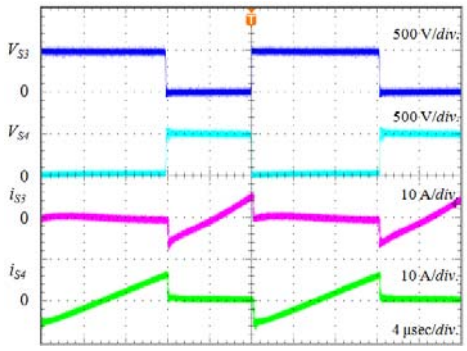


(b)

Fig. 9. Experimental results for D = 0.4: (a) switch voltages V_{S1} and V_{S2} and switch currents i_{S1} and i_{S2} and (b) switch voltages V_{S3} and V_{S4} and switch currents i_{S3} and i_{S4}.



(a)



(b)

Fig. 10. Experimental results for D = 0.6: (a) switch voltages V_{S1} and V_{S2} and switch currents i_{S1} and i_{S2} and (b) switch voltages V_{S3} and V_{S4} and switch currents i_{S3} and i_{S4}.

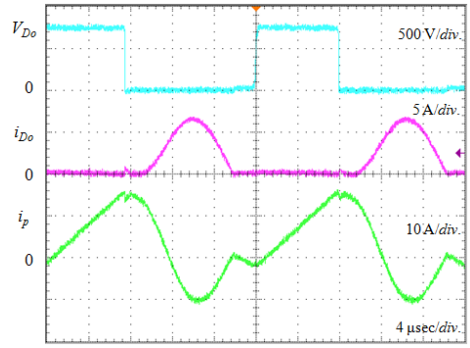


Fig. 11. Experimental waveforms of the diode voltage V_{Do}, diode current i_{Do}, and primary current i_p for D = 0.4.

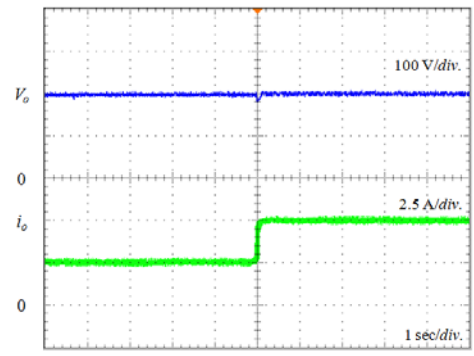


Fig. 12. Experimental waveforms of the output voltage V_o and output current i_o when the output power is changed abruptly.

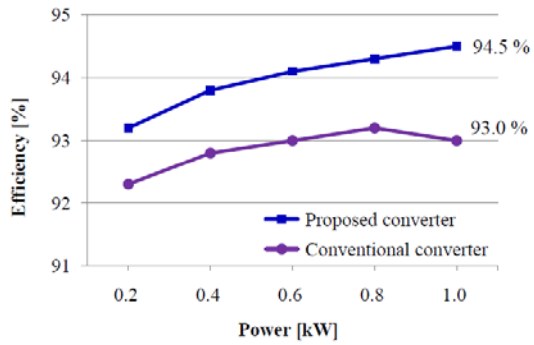


Fig. 13. Measured power efficiency curves of the different power levels.

output voltage V_o and output current i_o when the output power is changed abruptly. The output voltage V_o is regulated when the output power changes from 0.5 kW to 1.0 kW. Fig. 13 shows the measured power efficiency curves of the different power levels. The conventional two-switch flyback converter achieves the efficiency of 93.0 % for a 1.0 kW output power. On the contrary, the proposed converter realizes the efficiency of 94.5 % for a 1.0 kW output power. The proposed converter improves the converter efficiency by 1.5 %. The main factor for the efficiency improvement is the reduced switching losses. Given that the proposed converter is developed for high input voltage applications, the switching losses are more dominant than the conduction losses. The input voltage of the proposed

converter is 350 V. For such a high input voltage, the switching losses are more significant than the conduction losses. This significance is because the average current of the switching devices is reduced as the input voltage of the converter is increased. The duty cycle range is also extended from 0 to 1 for the practical use of the proposed converter for a wide input voltage range.

V. CONCLUSION

This paper has proposed an actively clamped two-switch flyback converter. Operation principle and converter features of the proposed converter are described. The duty cycle range is extended by using an active-clamp circuit. ZVS of all power switches is achieved. ZCS of an output diode is also achieved. The proposed converter reduces switching power losses with an extended duty cycle range. Simulation verifications and experimental results are presented to verify the performance of the proposed converter. The proposed converter realizes the efficiency of 94.5 % for a 1.0 kW output power. This converter improves power efficiency by 1.5 % for a 1.0 kW output power compared with the conventional converter. The proposed converter is suitable for a high-efficiency isolated power supplies for a wide input voltage range.

ACKNOWLEDGMENT

This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MISP) (2010-0028509).

REFERENCES

[1] B. R. Lin, H. K. Chiang, and S. L. Wang, "Interleaved ZVS DC/DC converter with balanced input capacitor voltages for high-voltage applications," *Journal of Power Electronics*, Vol. 14, No. 4, pp. 661-670, Jul. 2014.

[2] Z. Chen, Q. Zhou, J. Xu, and X. Zhou, "Asymmetrical pulse-width-modulated full-bridge secondary dual resonance DC-DC converter," *Journal of Power Electronics*, Vol. 14, No. 6 pp. 1224-1232, Nov. 2014.

[3] J. Zhang, S. Wang, Z. Wang, and L. Tian, "Design and realization of a digital PV simulator with a push-pull forward circuit," *Journal of Power Electronics*, Vol. 14, No. 3. pp. 444-457, May 2014.

[4] B. R. Lin, and Y. B. Nian, "Analysis and implementation of a new three-level converter," *Journal of Power Electronics*, Vol. 14, No. 3. pp. 478-487, May 2014.

[5] D. K. Jeong, M. H. Ryu, H. G. Kim, and H. J. Kim, "Optimized design of bi-directional dual active bridge converter for low-voltage battery charter," *Journal of Power Electronics*, Vol. 14, No. 3. pp. 468-477, May 2014.

[6] M. Baei, M. Narimani, and G. Moschopoulos, "A new ZVS-PWM full-bridge boost converter," *Journal of Power Electronics*, Vol. 14, No. 2. pp. 237-248, Mar. 2014.

[7] C. H. Park, S. H. Cho, J. H. Jang, S. K. Pidaparthy, and T. Y. Ahn, "Average current mode control for LLC series resonant DC-to-DC converters," *Journal of Power Electronics*, Vol. 14, No. 1. pp. 40-47, Jan. 2014.

[8] B. R. Lin, "Analysis, design and implementation of a soft switching DC/DC converter," *Journal of Power Electronics*, Vol. 13, No. 1. pp. 20-30, Jan. 2013.

[9] W. Hu, F. Zhang, Y. Xu, and X. Chen, "Output voltage ripple analysis and design considerations of intrinsic safety flyback converter based on energy transmission modes," *Journal of Power Electronics*, Vol. 14, No. 5. pp. 908-917, Sep. 2014.

[10] D. H. Kim, and J. H. Park, "High efficiency step-down flyback converter using coaxial cable coupled-inductor," *Journal of Power Electronics*, Vol. 13, No. 2. pp. 214-222, Mar. 2013.

[11] J. K. Kim and G. W. Moon, "Derivation, analysis, comparison of nonisolated single-switch high step-up converters with low voltage stress," *IEEE Trans. Power Electron*., Vol. 30, No. 3, pp. 1336-1344, Mar. 2015.

[12] Q. Vartak, A. Abramovitz, and K. M. Smedley, "Analysis and design of energy regenerative snubber for transformer isolated converters," *IEEE Trans. Power Electron*., Vol. 29, No. 11, pp. 6030-6040, Nov. 2014.

[13] M. G. Kim and Y. S. Jung, "A novel soft-switching two-switch flyback converter with a wide operating range and regenerative clamping," *Journal of Power Electronics*, Vol. 9, No. 5, pp. 772-780, Sep. 2009.

[14] M. R. Yazdani and S. Rahmani, "A new zero-current-transition two-switch flyback converter," in *Proc. PEDSTC*, pp. 390-395, 2014

[15] D. Murthy-Bellur and M. K. Kazimierczuk, "Zero-current-transition two-switch flyback pulse-width modulated DC-DC converter," *IET Power Electron*., Vol. 4, No. 3, pp. 288-295, Mar. 2011.

[16] C. Y. inaba, Y. Konishi, and M. Nakaoka, "High-frequency flyback-type soft-switching PWM DC-DC power converter with energy recovery transformer and auxiliary passive lossless snubbers," *IET Electric Power Applications*, Vol. 151, No. 1, pp. 32-37, Jan. 2004.

[17] J. Zhao and F. Dai, "Soft-switching two-switch flyback converter with wide range," in *Proc. ICIEA*, pp. 250-254, 2008.

Min-Kwon Yang was born in 1987 in Jeonju, South Korea, in 1987. He received his B.S. in Electronic Engineering from Chonbuk National University, Jeonju, South Korea, in 2012. He is currently working toward his Ph.D. in Electronic Engineering at Chonbuk Nation University. His current research interest is designing of switching power converters including the circuit design and control.

Woo-Young Choi was born in 1979 in Gwangju, South Korea. He received his B.S. in Electrical Engineering from Chonnam National University, Gwangju, South Korea, in 2004; and his Ph.D. in Electronic and Electrical Engineering from the Pohang University of Science and Technology, Pohang, South Korea, in 2009. Since 2010, he has been with the Division of Electronic Engineering at Chonbuk National University, Jeonju, South Korea, where is currently working as an Associate Professor. His research interest is power electronics system design for high-efficiency switching power converters.